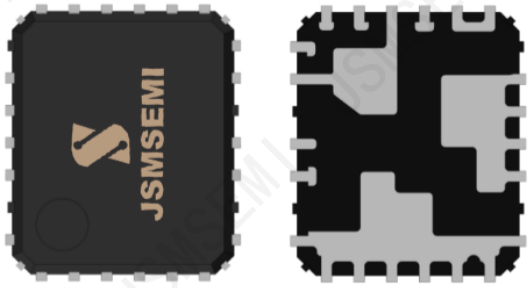
General Description

JSM07S65HQ is a highly integrated and highly reliable half-bridge brushless DC motor drive circuit, primarily

used for driving low-power motors such as fans. It incorporates Silicon Carbide power MOSFETs and half-bridge high-voltage gate drive circuits.

The JSM07S65HQ integrates an undervoltage protection function internally, providing excellent protection and fail-safe operation.

JSM07S65HQ features a design that is highly insulated, easily thermally conductive, and low in electromagnetic interference. It offers a very compact package, making it highly convenient to use, especially suitable for applications built into motors and situations requiring compact installation.JSM07S65HQ is packaged in ESOP13, can operate within the temperature range of -40 to 150°C.



Features

- 650 V $R_{DS(on)}$ = 0.5Ω(Typ) Silicon Carbide MOSFET Inverter with Gate Drivers and Protection
- Built-In Bootstrap Diodes Simplify PCB Layout
- High-Side Under-Voltage Protection
  -Trigger level : 8.2V
  -Reset level : 8.9V
- High-level effective, supported 3.3V, 5V and 15V input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500 V_{rms} / min.
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

Applications

- BLDC Motor control
- Indoor/outdoor air conditioning
- Refrigerator compressor
- Exhaust fan
- Fan
- Air purifier
- Dishwasher water pump

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
JSM07S65HQ	DFN5060-26L	JSM07S65HQ	-40 to 150°C	3	T&R,5000	Rohs

Pin descriptions

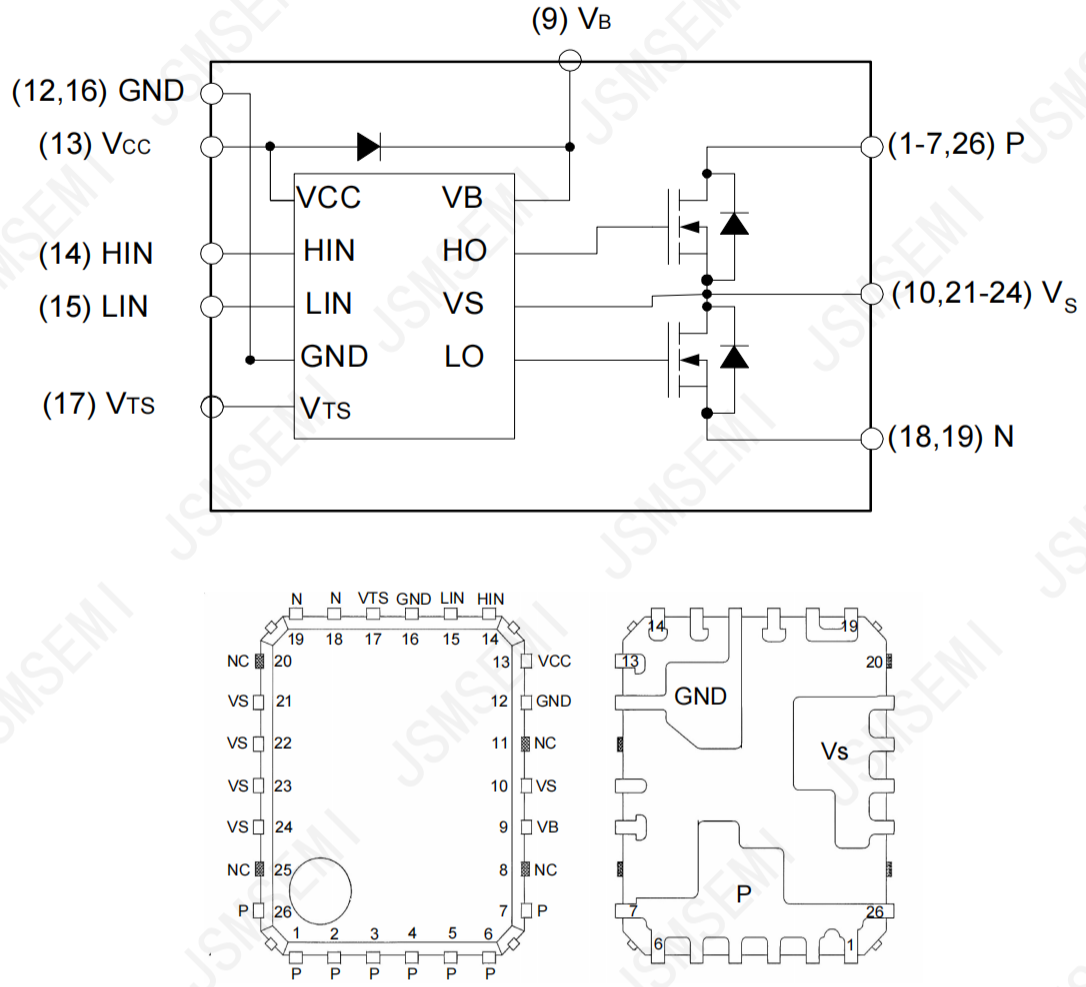


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Pin Number	Pin Name	Pin Description
1-7	P	Positive DC-Link Input
8	NC	No Connection
9	V_B	Bias Voltage for High-Side MOSFET Driving
10	V_S	Output for Bias Voltage Ground for High-Side MOSFET Driving
11	NC	No Connection
12	GND	IC Common Supply Ground
13	V_{CC}	Bias Voltage for Low Side MOSFET Driving
14	HIN	Signal Input for High-Side
15	LIN	Signal Input for Low-Side
16	GND	IC Common Supply Ground
17	V_{TS}	Output for HVIC Temperature Sensing
18-19	N	Negative DC-Link Input
20	NC	No Connection
21-24	V_S	Output for Bias Voltage Ground for High-Side MOSFET Driving
25	NC	No Connection
26	P	Positive DC-Link Input

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Inverter Part (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DSS}	Drain-Source Voltage of Each MOSFET	T_C = 25°C	650	V
I_D	Each MOSFET Current, Continuous	T_C = 25°C	7.0	A
		T_C=75°C	5.0	A
I_{DM}	Each MOSFET Pulse Current, Peak	T_C = 25°C, less than 100us	30	A
		T_C=75°C	21	A
I_{Drms}	Each MOSFET Current, Rms	T_C = 25°C, F_{PWM} <20KHz	2.8	Arms
P_D	Maximum Power Dissipation	T_C = 25°C， For Each MOSFET	75	W

Control Part (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between VB and VS	20	V
V_{IN}	Input Signal Voltage	Applied between V_{IN} and COM	-0.3~V_{CC}+0.3	V

Bootstrap Diode Part (each bootstrap diode unless otherwise specified.)

Symbol	Description	Conditions	Rating	Unit
V_{RRMB}	Maximum Repetitive Reverse Voltage	Tc = 25°C	650	V
I_{FB}	Forward Current	Tc = 25°C	0.25	A
I_{FPB}	Forward Peak Current, Peak	Tc = 25°C，Less than 1mS	0.5	A

Total System

Symbol	Parameter	Conditions	Ratings	Unit
Tj	Operating Junction Temperature		-40~150	℃
TSTG	Storage Temperature	Tc = 25°C	-40~150	℃
VISO	Isolation Voltage	60Hz, Sinusoidal， AC 1 min， between pins and heat-sink plate	1500	Vrms

NOTE1：To insure safe operation of the IPM, the average junction temperature should be limited to TJ ≤ 150°C (@Tc ≤ 100°C).

Thermal Resistance

Symbol	Parameter	Conditions	Ratings	Unit
Rth(J-B)	Thermal resistance, junction to mounting pad, each MOSFET	For Each MOSFET	1.0	°C/W
Rth(J-A)	Thermal resistance, junction to ambient, each MOSFET	For Each MOSFET	40	°C/W

Recommended Operating Condition

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P and N	-	300	400	V
V_{CC}	Control Supply Voltage	Applied between VCC and COM	13.5	-	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between VB and VS	13.5	-	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between VIN and COM	3.0	-	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	Blanking Time for Preventing Arm-Shor	V_{CC} = V_{BS} = 13.5 ~ 16.5 V, Tj <150°C	1.0	-	-	μs
F_{PWM}	PWM Switching Frequency	Tj <150°C	-	-	20	kHz

Electrical Characteristics (T_J = 25°C, V_{CC} = V_{BS} = 15 V unless otherwise specified.)

Inverter Part (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain - Source Breakdown Voltage	V_{IN} = 0 V, I_D = 250uA （NOTE 2）	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN} = 0 V, V_{DS} = 650 V	-	-	1.0	μA
V_{SD}	Drain - Source Diode Forward Voltage	V_{CC} = V_{BS} = 15V, V_{IN} = 0 V, I_D =-1 A	-	-	1.2	V
$R_{DS(on)}$	Drain-Source Turn-On Resistance	V_{CC} = V_{BS} = 15 V, V_{IN} = 5 V, I_D =1 A	-	0.5	-	ohm
t_{ON}	Switching Times	V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_D = 0.5 A V_{IN} = 0/5 V, Inductive Load L = 3 mH （NOTE 3）	-	850	-	ns
t_{OFF}			-	450	-	ns
t_{rr}			-	150	-	ns
E_{ON}			-	40	-	μJ
E_{OFF}			-	10	-	μJ
R_{BSOA}	Reverse Bias Safe Operating Area	V_{PN} = 400 V, V_{CC} = V_{BS} = 15 V, I_D = I_{DP}, V_{DS} = BV_{DSS}, T = 150°C	Full Square			

NOTE 2：BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside IPM. VPN should be sufficiently less than this value considering the effect of the stray inductance so that VDS should not exceed BV_{DSS} in any case.

NOTE 3: t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Fig 2 for the switching time definition.

Control Part (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QCC}	Quiescent VCC Supply Current	V_{CC} = 15V V_{IN} = 5V	Applied between VCC and COM	-	300	500	μA
I_{QB}	Quiescent VBS Supply Current	V_{DB} = 15V V_{IN} = 5V	Applied between VB -VS	-	50	200	μA
UV_{CCD}	Low-Side Under-Voltage Protection	VCC Under-Voltage Protection Detection Level		-	7.7	-	V
UV_{CCR}		VCC Under-Voltage Protection Reset Level		-	8.7	-	V
UV_{BSD}	High-Side Under-Voltage Protection	VBS Under-Voltage Protection Detection Level		-	7.7	-	V
UV_{BSR}		VBS Under-Voltage Protection Reset Level		-	8.7	-	V
V_{IH}	ON Threshold Voltage	Logic HIGH Level, Applied between VIN and COM		2.5	-	-	V
V_{IL}	OFF Threshold Voltage	Logic Low Level, Applied between VIN and COM		-	-	0.8	V
DT	Dead Time	Tc = 25°C ,VCC=15V		400	550	700	ns

Function Description

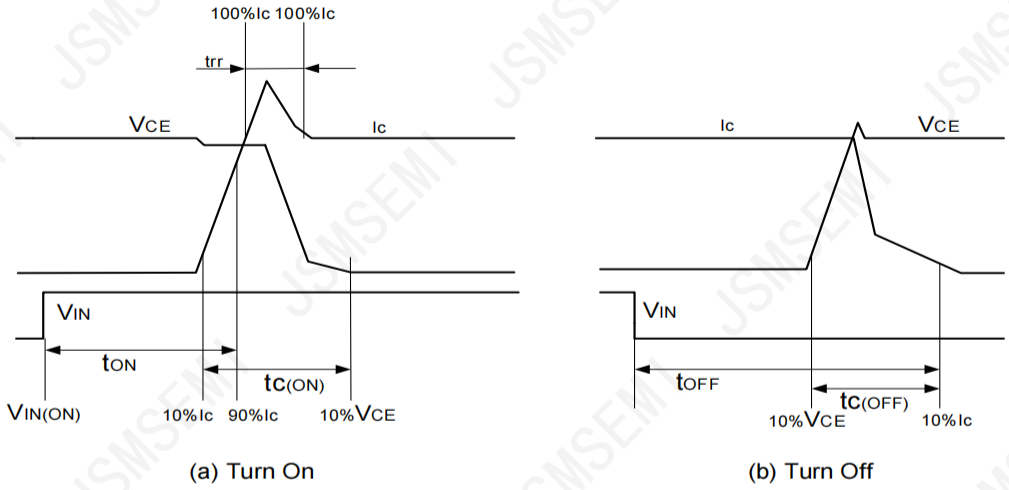


Figure 2. Switching Time Definitions

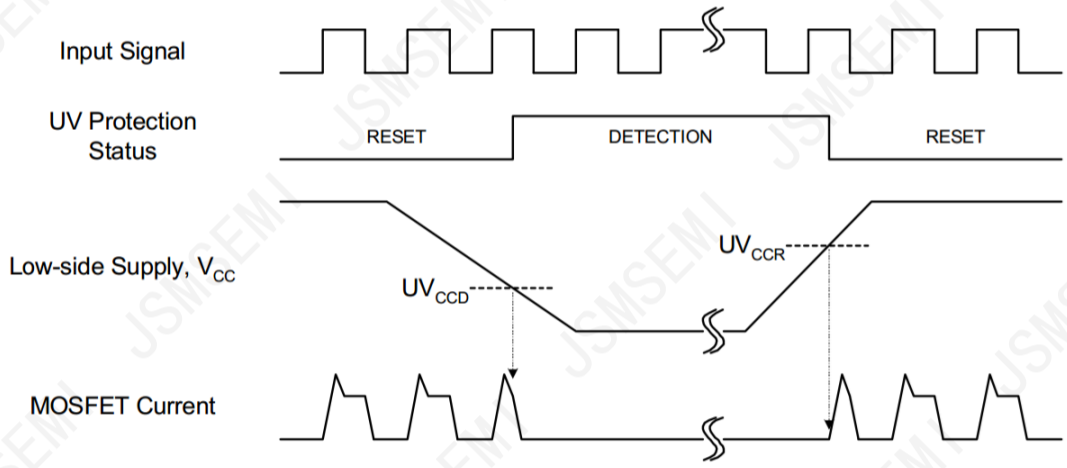


Figure 3. Under voltage Protection (Low-side)

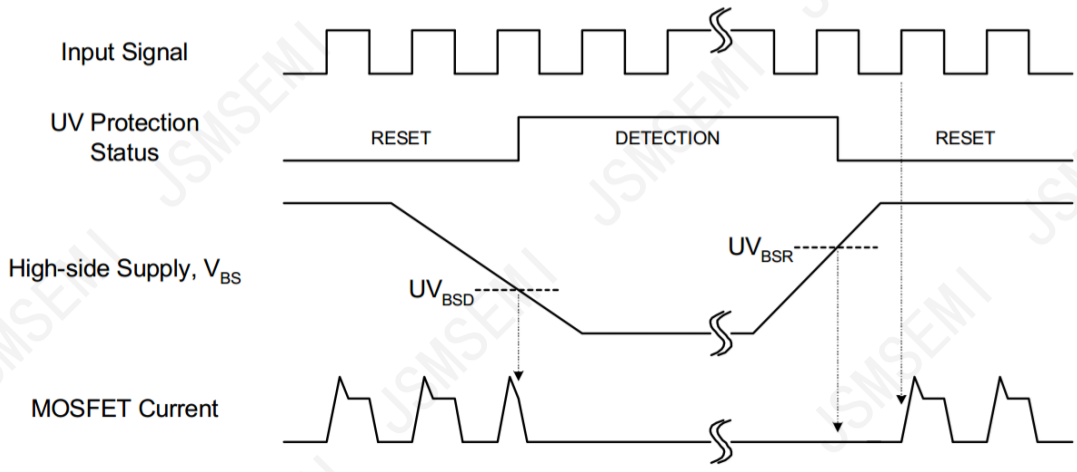


Figure 4. Under voltage Protection (High-side)

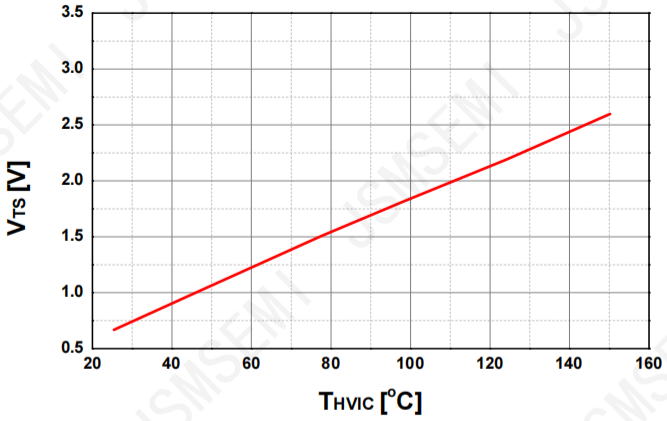


Figure 5. Temperature Profile of V_{TS} (Typical)

TypicalApplication Circuit

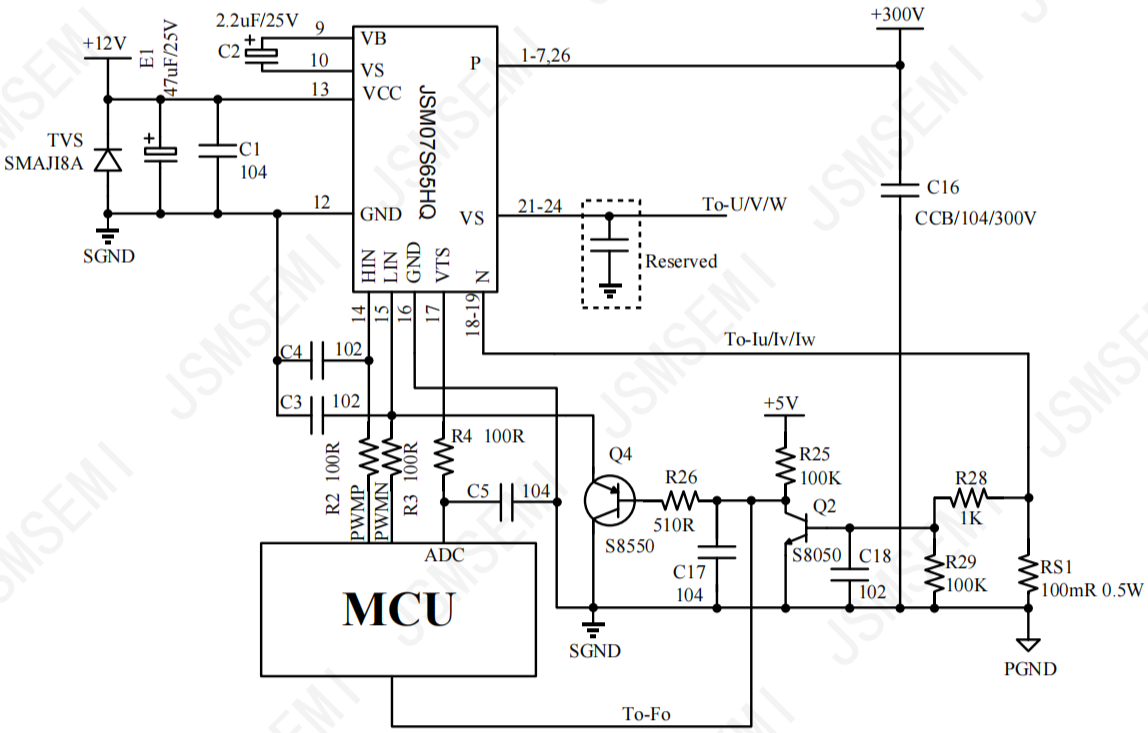


Figure 6. Typical Application Connection JSM07S65HQ

HIN	LIN	Output	Note
0	0	High Resistance	Both MOSFET Off
0	1	0	Low side MOSFET On
1	0	VDC	High side MOSFET On
1	1	Forbidden	Both MOSFET Off
open	open	High Resistance	Both MOSFET Off

Layout

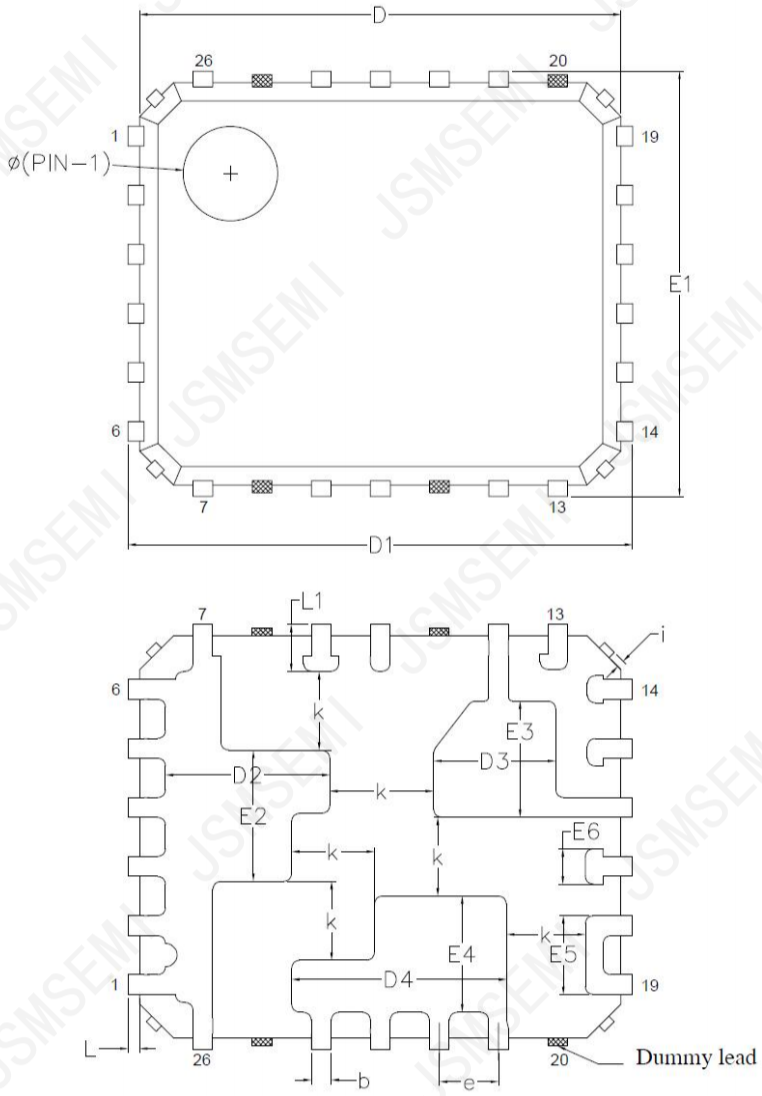
Layout Guidelines

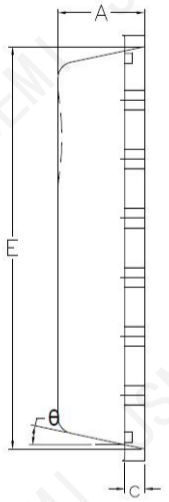
In the process of circuit board layout, the following points should be noted:

1. Due to the high-speed switching characteristics of SiC, in order to avoid dv/dt coupling interference, it is recommended that the PCBA reserve a VS-GND capacitor to absorb voltage spikes to compensate for insufficient EMC margin and improve the system's anti-interference capability.
2. RC-coupling at each input of JSMSEMI IPM and MCU are useful to prevent improper input signal caused by surge-noise.
3. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
4. All the filter capacitors should be connected close to JSMSEMI IPM, and they should have good characteristics for rejecting highfrequency ripple current.
5. For JSMSEMI IPMs, proper moisture protection is essential. It is recommended to apply conformal coating or external insulating adhesive.
6. It is recommended to monitor the VTS pin temperature signal of the JSMSEMI IPM and add over-temperature protection or reduce power consumption. The maximum protection temperature is 120℃ (VOT=2.5V).
7. Ensure adequate heat dissipation. For JSMSEMI IPMs, consider adding insulating pads or ceramic plates and attaching them to the heatsink.

Package Information

PQFN5060-26L





Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	0.950	1.100	1.250	E3	1.325	1.475	1.625
b	0.150	0.250	0.380	E4	1.325	1.475	1.625
c	0.154	0.254	0.354	E5	0.850	1.000	1.150
D	5.958	6.108	6.258	E6	0.300	0.450	0.600
D1	6.250	6.400	6.550	e	0.650	0.750	0.850
D2	1.935	2.085	2.325	i	/	/	0.200
D3	1.400	1.550	1.700	k	1.000	/	/
D4	2.575	2.725	2.875	L	0.050	0.200	0.350
E	4.958	5.108	5.258	L1	0.450	0.600	0.750
E1	5.250	5.400	5.550	θ	9°	12°	15°
E2	1.515	1.665	1.815	ϕ	1.000	1.200	1.400

Revision History

Rev.	Change	Date
V1.0	Initial version	2/27/2023

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