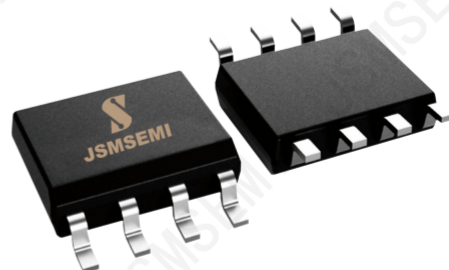


1 Description

The JSM2006SG is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 650V.

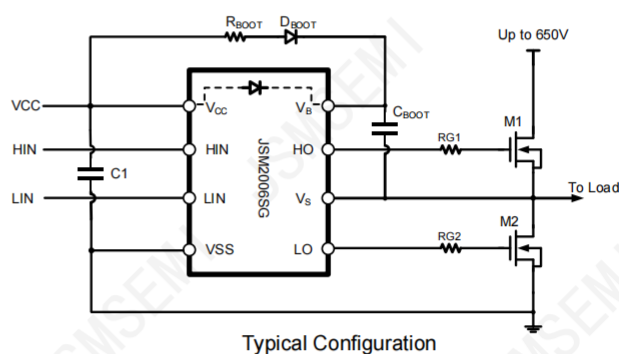


3 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives
- Home Appliance

2 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +650V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ± 50 V/nsec
- Allowable negative V_s capability: -9V
- Gate drive supply range from 10V to 20V
- Integrated VCC, VBS undervoltage lockout circuit
 - VCC UVLO 8.8V / 8.0V
 - VBS UVLO 8.2V / 7.5V
- Propagation delay
 - Ton/Toff = 250ns/150ns
 - Matching delay time 50ns
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 600mA/1000mA
- Prevent direct-through protection
 - Dead time 130ns
- Integrated Bootstrap diode
- RoSH compatible



4 Function Pin Description

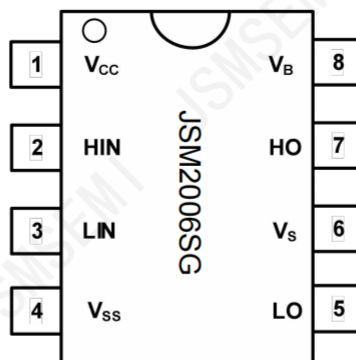


Table4-1 Lead Definitions

Number	Symbol	Description
1	V _{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	LIN	Logic input for low side gate driver output (LO), in phase
4	V _{SS}	Low side return
5	LO	Low side gate drive output
6	V _S	High side floating supply return
7	HO	High side gate drive output
8	V _B	High side floating supply

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
JSM2006SG	SOP-8	JSM2006SG	-40 to 125°C	3	T&R,4000	RoHS

5 Product specifications

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	-0.3	650	V
V _S	High side floating supply return	V _B - 25	V _B + 0.3	
V _{HO}	High side gate drive output	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and main power supply	-0.3	25	
V _{LO}	Low side gate drive output	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input of HIN & LIN	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	2000	—	V
	Machine Model	1000	—	V

Rated power

Symbol	Definition	MIN.	MAX.	Units
P _D	Package Power Dissipation @ TA ≤ 25°C	—	625	mW

Thermal information

Symbol	Definition	MIN.	MAX.	Units
R _{thJA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	V _S + 10	V _S + 20	V
V _S	High side floating supply return	-9	600	
V _{HO}	High side gate drive output	V _S	V _B	
V _{CC}	Low side and main power supply	10	20	
V _{LO}	Low side gate drive output	0	V _{CC}	
V _{IN}	Logic input of HIN & LIN	0	V _{CC}	
T _A	Ambient temperature	-40	125	°C

Note1: Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

Note2: When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

Electrical Characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC} = V_B = 15\text{V}$, $C_L = 1\text{nF}$, unless otherwise specified

Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	250	500	ns	$V_S = 0\text{V}$
t_{OFF}	Turn-off propagation delay	—	150	300	ns	$V_S = 600\text{V}$
t_R	Turn-on rise time	—	50	100	ns	
t_F	Turn-off fall time	—	35	90	ns	
DT	Dead time	—	130	260	ns	
MT	Matching delay ON and OFF	—	—	50	ns	

Static electrical characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC} = V_B = 15\text{V}$, $C_L = 1\text{nF}$, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	7.8	8.8	9.8	V	
V_{CCUV-}		6.5	8.0	9.5		
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	1.0	—		
V_{BSUV+}	VBS supply UVLO threshold	7.2	8.2	9.2		
V_{BSUV-}		6.5	7.5	8.5		
$V_{BSUVHYS}$	hysteresis of V_{BS} UVLO	—	0.9	—		
I_{LK}	High-side floating supply leakage current	—	—	50	μA	$V_B = V_S = 600\text{V}$
I_{QBS}	Quiescent VB supply current	—	35	100		$V_{IN} = 0\text{V}$ or 5V
I_{QCC}	Quiescent VCC supply current	—	60	150		
V_{IH}	Logic "1" input voltage	2.5	—	—	V	$V_{CC} = 10 \sim 20\text{V}$
V_{IL}	Logic "0" input voltage	—	—	0.8		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	0.2		$I_O = 0\text{A}$
V_{OL}	Low level output voltage, V_O	—	—	0.2		$I_O = 0\text{A}$
I_{IN+}	Logic "1" Input bias current	—	25	60	μA	$V_O = 0\text{V}$, $PW \leq 10\mu\text{s}$
I_{IN-}	Logic "0" Input bias current	—	—	5		$V_O = 15\text{V}$, $PW \leq 10\mu\text{s}$
I_{O+}	Output high short circuit pulsed current	—	0.6	—	A	$V_O = 0\text{V}$, $PW \leq 10\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	—	1.0	—		$V_O = 15\text{V}$, $PW \leq 10\mu\text{s}$

6 Function Description

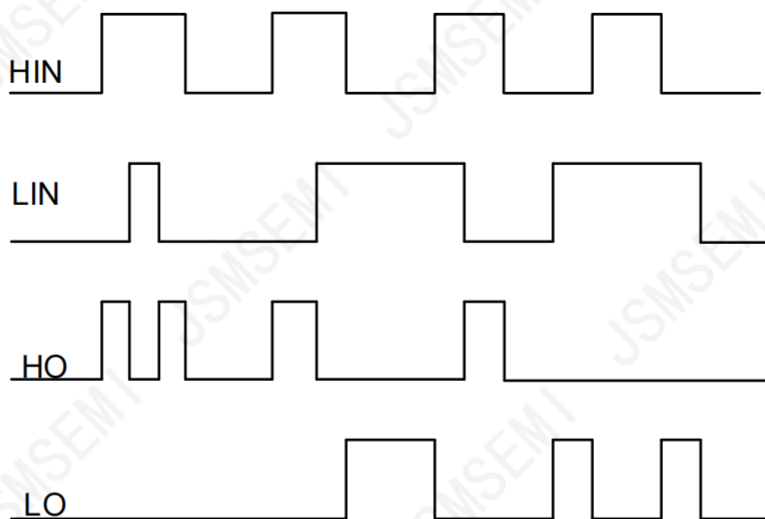


Figure 6-1. JSM2006SG Input and output timing waveform

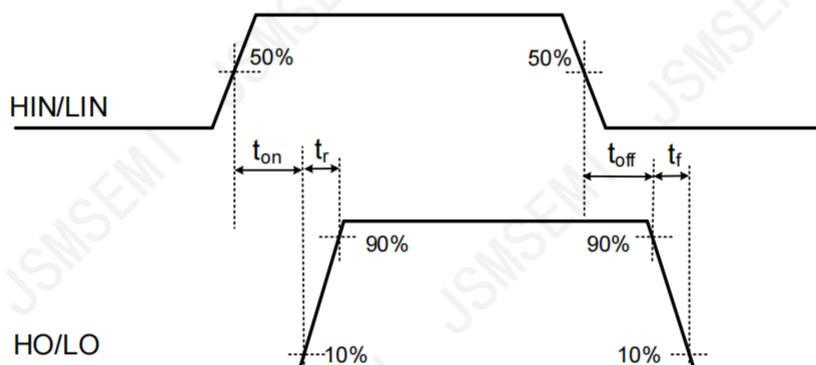


Figure 6-2. Propagation Time Waveform Definition

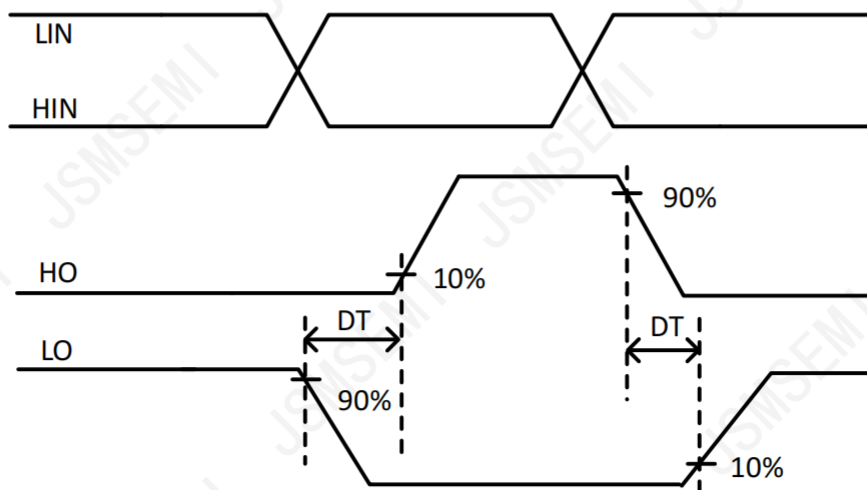


Figure 6-3. Definition of anti-pass-through delay waveform

7 JSM2006SG Description

Function Block Diagram

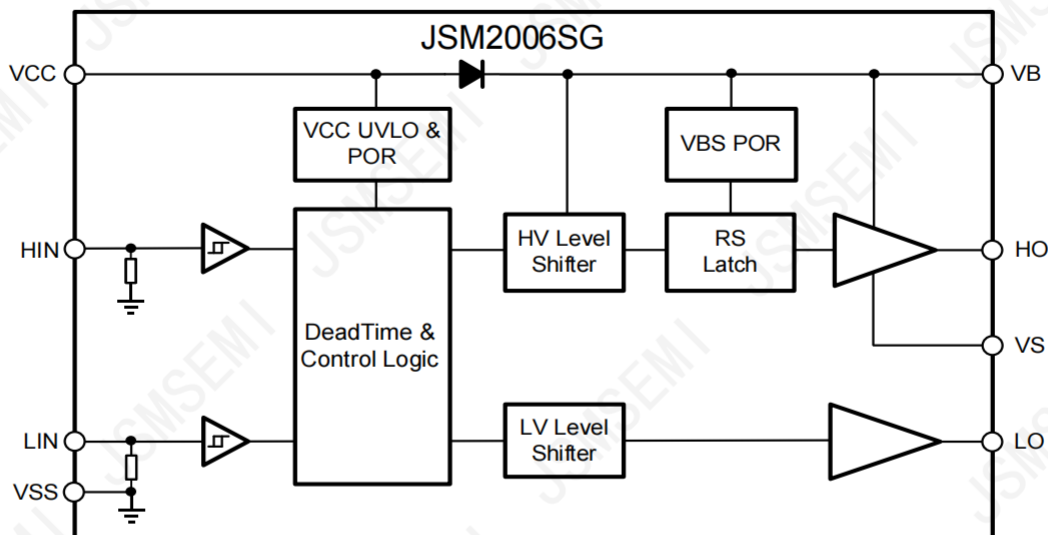


Figure7-1 Function Block Diagram of JSM2006SG

Application message

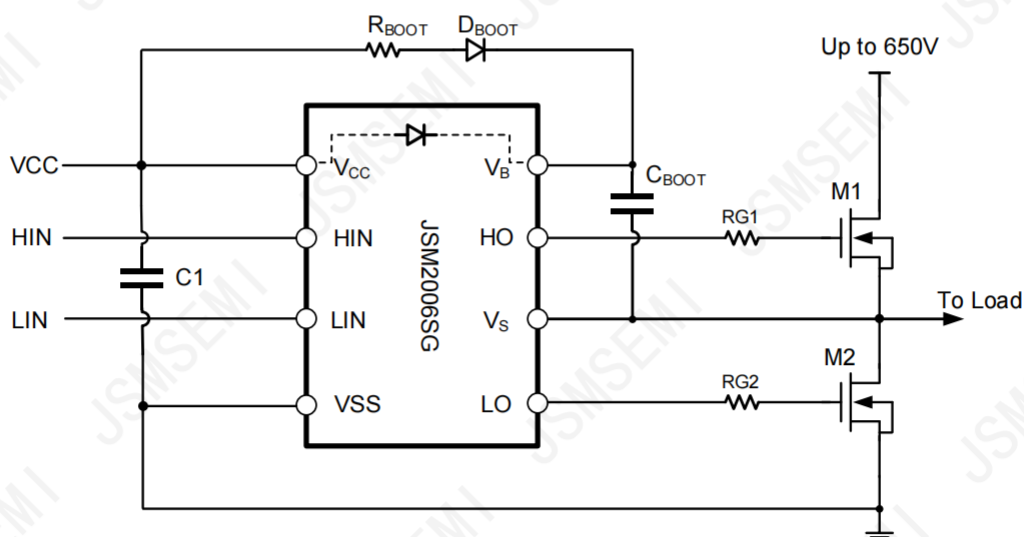


Figure7-2 Typical application circuit of JSM2006SG

Note: JSM2006SG has a built-in bootstrap diode. When the switching frequency $\geq 250\text{kHz}$ or when working in high temperature environments, peripheral bootstrap diodes and resistors should be used to ensure that the chip works properly. It is recommended to use fast recovery diodes for bootstrap diodes. (It is recommended to keep the footprint and routing for RBOOT and DBOOT on the (PCBA for optional population.)

Guide for bootstrap circuit design

The structure in the general half-bridge circuit is shown in Figure Figure 7-2, including three parts: bootstrapping resistance, bootstrap diode and bootstrap capacitance. This scheme is the most commonly used and the most cost-effective scheme in the current motor drive.

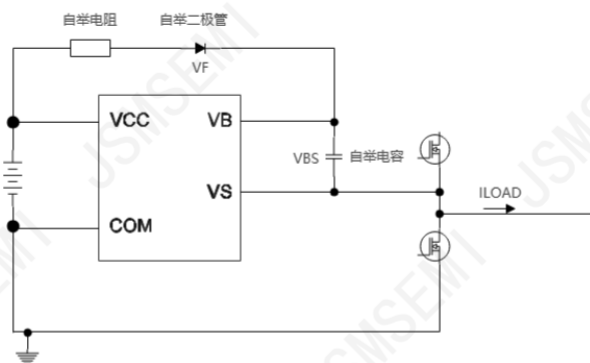


Figure 7-2 Basic structure of the bootstrap circuit

Selection of capacitance for bootstrap circuits

To determine the size of the bootstrap capacitor, we first need to evaluate the following points:

- The gate charge Q_g required for MOS activation;
- GS leakage I_{LK_GS} of MOS;
- The static working current I_{QBS} of the drive;
- Leakage I_{LK_DIODE} of bootstrap diode;
- Self bootstrap capacitor leakage I_{LK_CAP} ;
- Upper bridge setting high time T_{HON}

When the bootstrap capacitor uses an electrolytic capacitor, I_{LK_CAP} will be included in the calculation value, and other types of capacitors do not need to be considered. It is recommended to use at least one low ESR ceramic capacitor here. Parallel electrolytic capacitors and low ESR ceramic capacitors can achieve better circuit operating characteristics.

By calculation, we can obtain the capacitance value required for a single opening:

$$Q_{TOT} = Q_g + (I_{LK_GS} + I_{QBS} + I_{LK_DIODE} + I_{LK_CAP}) \times T_{HON}$$

During the bootstrapping process, the range of VBS descent ΔV_{BS}

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GSmin} - V_{DSon}$$

During this process, it is necessary to ensure that:

$$V_{GSmin} > V_{BSUV-}$$

V_F Reverse diode voltage drop of MOS

V_{GEmin} maintains the minimum gate voltage for MOSFET conduction

V_{DSon} Conduction voltage drop of V_{DSon} bridge MOS

Based on the above results, it can be calculated that:

$$C_{BOOTmin} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

Note: In the process of calculating the bootstrap capacitor here, only the amount of charge required for one pulse process was calculated, without considering issues such as PWM duty cycle and frequency. If the signal is

bootstrap capacitance size through a certain equivalent conversion.

Precautions for bootstrap circuits

A. Bootstrap resistor

Bootstrap resistors are used in some bootstrap circuits and are not mandatory components.

During startup, HO and LO may experience abnormal jumps. Increasing the bootstrap resistor will limit the current passing through the bootstrap diode during the bootstrap circuit startup, effectively suppressing some adverse signals and protecting the circuit.

B. Bootstrap capacitor

In the circuit design where the upper bridge arm is opened for a long time, the use of electrolytic capacitors as bootstrap capacitors must consider ESR. Long term opening of the upper bridge arm requires a bootstrap capacitor with a larger capacitance value, and electrolytic capacitors are generally used more often. However, electrolytic capacitors have a certain internal resistance, which can reduce the voltage division of the bootstrap resistor and prevent them from achieving their functions. Parallel connection of a low ESR ceramic capacitor can effectively prevent this situation from occurring.

C. Bootstrap diode

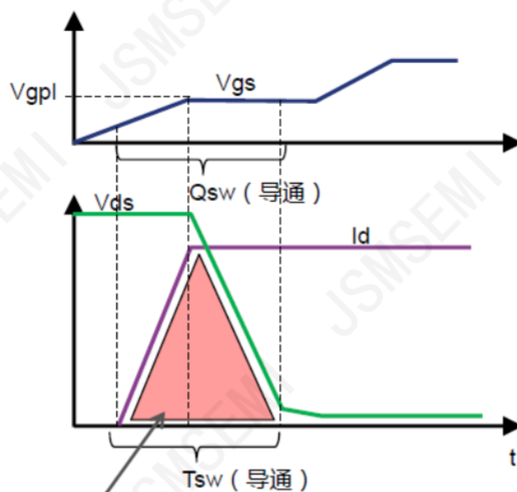
Bootstrap diodes are used to maintain voltage stability in bootstrap circuits. It is necessary to ensure that the reverse withstand voltage of the diode is greater than the driving power voltage, and on this basis, fast recovery diodes such as Schottky diodes should be selected as much as possible.

Bootstrap Circuit Design Guidelines

The gate resistor is used to control the switching speed and the slope of the rising and falling edges of the driven MOS, which can affect multiple performance factors in applications such as loss and reliability. This section will describe how to choose a driving resistor and discuss the impact it brings. The selection of gate resistance is closely related to the driving chip, MOSFET, and even circuit design used, and needs to be re selected according to the actual situation in different environments.

The common operating frequency of industrial brushless motors is about 2kHz -10kHz. Based on this, gate resistors with a resistance value of 20 Ω -120 Ω are usually chosen. This is determined by the following two points:

(1) The switching loss of MOS. The loss of MOS is partly due to switching loss and partly due to conduction loss. The gate resistance mainly affects the loss of the switching process. The larger the resistance value, the slower the switching process, and the larger the overlap area of voltage and current, the greater the loss. The most direct impact of excessive loss is that it will cause the chip temperature to rapidly rise, and under conditions above 150 , it will put the device at risk of failure.



$$P_{sw(on)} = \frac{1}{2} \times I_d \times V_{ds} \times T_{sw(on)}$$

Figure 7-3 MOS switch losses under resistive load conditions

(2) Reliability. Contrary to losses, the smaller the resistance of the gate resistance, the faster the switching speed of MOSFETs. In practical applications, the power terminal current is relatively large and sensitive to parasitic parameters. Excessive switching speed can increase signal instability, ranging from excessive EMI of the motor to circuit damage. The most common ones are:

- 1) The gate signal rings, causing MOS damage (as shown in Figure 7-4);
- 2) The dv/dt is too fast, causing the VS port to withstand high or low voltage signals, resulting in drive damage.

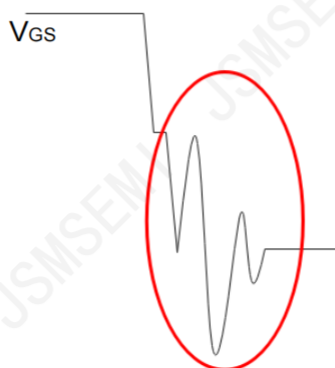


Figure 7-4 Gate Ringing Phenomenon

PCB Layout Guidelines

To achieve excellent performance of the half bridge gate driver chip, the following printed circuit board (PCB) layout and wiring guidelines should be followed.

- Low ESR/ESL capacitors should be placed between the VCC and COM pins near the driver chip, as well as between the VB and VS pins, to provide the peak current of the VCC and VB pins.

- To prevent large voltage transients in the high side MOSFET drain, it is necessary to connect a low ESR electrolytic capacitor and a ceramic capacitor between the high side MOSFET drain and ground (COM).

- To avoid excessive voltage negative transients on the switch node (VS) pins, it is necessary to minimize the parasitic inductance between the high side MOSFET source and the low side MOSFET (synchronous rectifier) source as much as possible.

- Efforts should be made to avoid overlapping between the VS layer and the ground (COM) layer, in order to minimize the coupling of switch noise from the VS layer to the ground layer to a greater extent.

- The heat dissipation pads of the driver chip should be connected to a large area of thick copper layer to improve the heat dissipation performance of the driver chip. Heat dissipation pads are usually connected to a ground plane that is equipotential with the chip COM. It is recommended to only connect this heat dissipation pad to the COM pins.

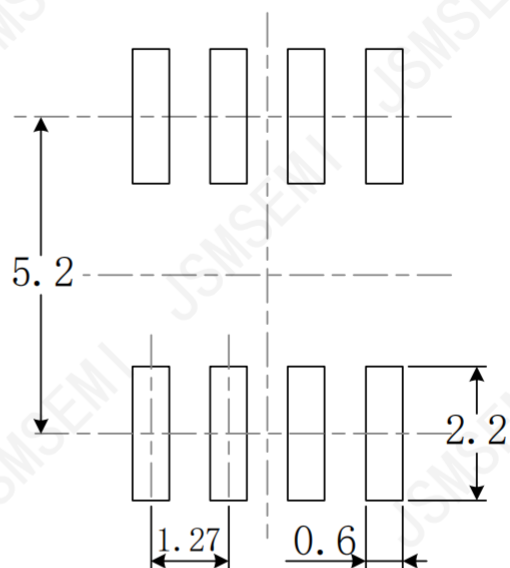
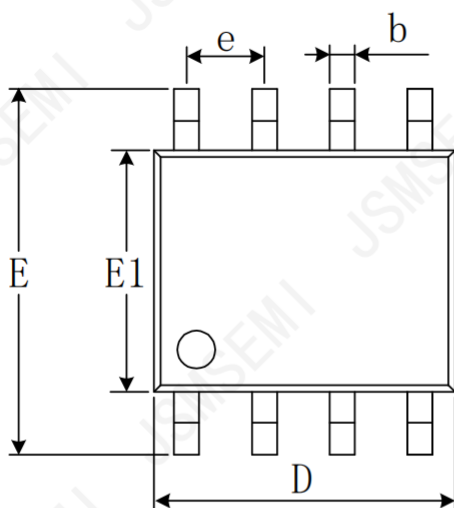
- Grounding precautions:

The primary goal of designing grounding connections is to limit the MOSFET gate charge discharge circuit to the smallest possible loop area. This method reduces the loop inductance and effectively avoids noise issues on the MOSFET gate. Meanwhile, the gate driver chip should be as close as possible to the MOSFET.

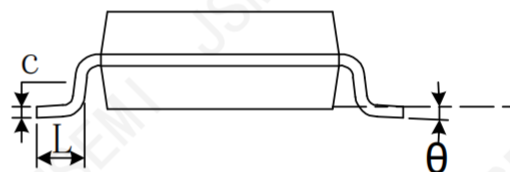
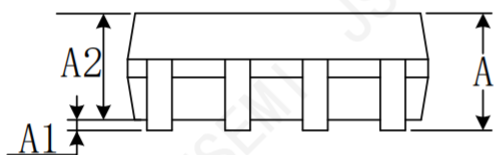
The second consideration is to ensure the rationality of the charging path for the bootstrap capacitor, which includes VCC bypass capacitors based on ground (COM), bootstrap diodes, bootstrap capacitors, and low side MOSFET body diodes. Due to the VCC bypass capacitor charging the bootstrap capacitor cycle by cycle through the bootstrap diode, and each charging occurs in a very short time, the charging path will pass through the peak current. Minimizing the loop length and area of the bootstrap circuit on the PCB as much as possible can ensure that the bootstrap circuit operates in a stable state, which is crucial for ensuring the reliable operation of the driver chip.

Package Information

SOP-8



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/17/2022

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER' S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

JSMSEMI All Rights Reserved. Information and data in this document are owned by JSMSEMI wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from JSMSEMI.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com