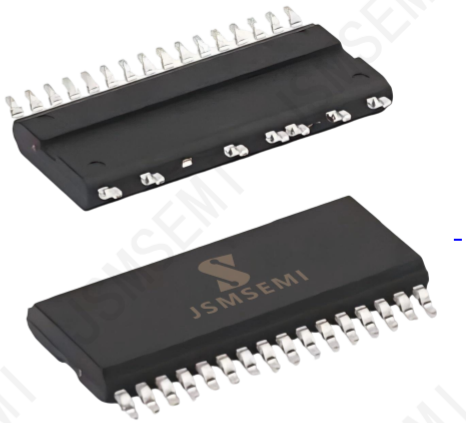
General Description

JSM10S65TAS is a highly integrated and highly reliable three-phase brushless DC motor drive circuit, primarily used for driving low-power motors such as fans. It incorporates six Silicon Carbide power MOSFETs and three half-bridge high-voltage gate drive circuits.

The JSM10S65TAS integrates an undervoltage protection function internally, providing excellent protection and fail-safe operation. Since each phase has an independent negative DC terminal, its current can be detected separately.

JSM10S65TAS features a design that is highly insulated, easily thermally conductive, and low in electromagnetic interference. It offers a very compact package, making it highly convenient to use, especially suitable for applications built into motors and situations requiring compact installation.



- Isolation Rating: 1500 V_{rms} / min.
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

Features

- 650 V $R_{DS(on)}$ = 0.52Ω(Max) Silicon Carbide MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Built-In Bootstrap Diodes Simplify PCB Layout
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3/5V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- HVIC for Gate Driving and Under-Voltage Protection

Applications

- 3-Phase Inverter Driver for Small Power AC Motor Drives
- Indoor/outdoor air conditioning
- Refrigerator compressor
- Exhaust fan
- Fan
- Air purifier
- Dishwasher water pump

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
JSM10S65TAS	SOP-23H	JSM10S65TAS	-40 to 150°C	1	T&R,500	Rohs

Pin descriptions

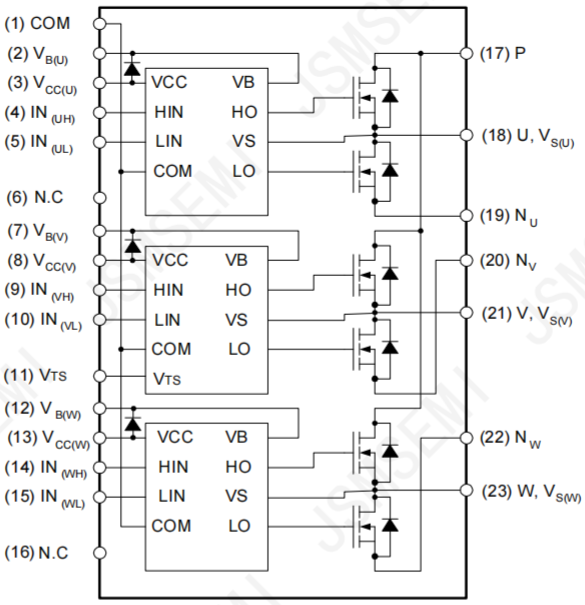


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U-Phase High-Side MOSFET Driving
3	$V_{CC(U)}$	Bias Voltage for U-Phase IC and Low-Side MOSFET Driving
4	$IN_{(UH)}$	Signal Input for U-Phase High-Side
5	$IN_{(UL)}$	Signal Input for U-Phase Low-Side
6	N.C	No Connection
7	$V_{B(V)}$	Bias Voltage for V-Phase High Side MOSFET Driving
8	$V_{CC(V)}$	Bias Voltage for V-Phase IC and Low Side MOSFET Driving
9	$IN_{(VH)}$	Signal Input for V-Phase High-Side
10	$IN_{(VL)}$	Signal Input for V-Phase Low-Side
11	V_{TS}	Output for HVIC Temperature Sensing
12	$V_{B(W)}$	Bias Voltage for W-Phase High-Side MOSFET Driving
13	$V_{CC(W)}$	Bias Voltage for W-Phase IC and Low-Side MOSFET Driving
14	$IN_{(WH)}$	Signal Input for W-Phase High-Side
15	$IN_{(WL)}$	Signal Input for W-Phase Low-Side
16	N.C	No Connection
17	P	Positive DC-Link Input
18	U, $V_{S(U)}$	Output for U-Phase & Bias Voltage Ground for High-Side MOSFET Driving
19	N_U	Negative DC-Link Input for U-Phase
20	N_V	Negative DC-Link Input for V-Phase
21	V, $V_{S(V)}$	Output for V-Phase & Bias Voltage Ground for High-Side MOSFET Driving
22	N_W	Negative DC-Link Input for W-Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High-Side MOSFET Driving

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Inverter Part (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
V_{DSS}	Drain-Source Voltage of Each MOSFET		650	V
*$I_{D\ 25}$	Each MOSFET Drain Current, Continuous	T_C = 25°C	10.0	A
*$I_{D\ 80}$	Each MOSFET Drain Current, Continuous	T_C = 80°C	7.0	A
*I_{DP}	Each MOSFET Drain Current, Peak	T_C = 25°C, PW < 100 μs	20.0	A
*I_{DRMS}	Each MOSFET Drain Current, Rms	T_C = 80°C, F_{PWM} < 20 kHz	2.5	Arms
*P_D	Maximum Power Dissipation	T_C = 25°C, For Each MOSFET	120	W

Control Part (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between V_B and V_S	20	V
V_{IN}	Input Signal Voltage	Applied between V_{IN} and COM	-0.3 ~ V_{CC} + 0.3	V

Bootstrap Diode Part (each bootstrap diode unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
V_{RRMB}	Maximum Repetitive Reverse Voltage		650	V
* I_{FB}	Forward Current	T_C = 25°C	0.25	A
* I_{FPB}	Forward Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	0.5	A

Thermal Resistance

Symbol	Parameter	Conditions	Rating	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each MOSFET under Inverter Operating Condition	7.0	°C/W

Total System

Symbol	Parameter	Conditions	Rating	Unit
T_J	Operating Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-40 ~ 150	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 Minute, Connect Pins to Heat Sink Plate	1500	V_{rms}

Recommended Operating Condition

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P and N	-	300	400	V
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	12.0		18.0	V
V_{BS}	High-Side Bias Voltage	Applied between V_B and V_S	12.0		18.0	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between V_{IN} and COM	3.0	-	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	Blanking Time for Preventing Arm-Short	V_{CC} = V_{BS} = 13.5 ~ 16.5 V, T_J ≤ 150°C	1.0	-	-	μs
f_{PWM}	PWM Switching Frequency	T_J ≤ 150°C	-	15	20	kHz

Electrical Characteristics (T_J = 25°C, V_{CC} = V_{BS} = 15 V unless otherwise specified.)

Inverter Part (each MOSFET unless otherwise specified.)

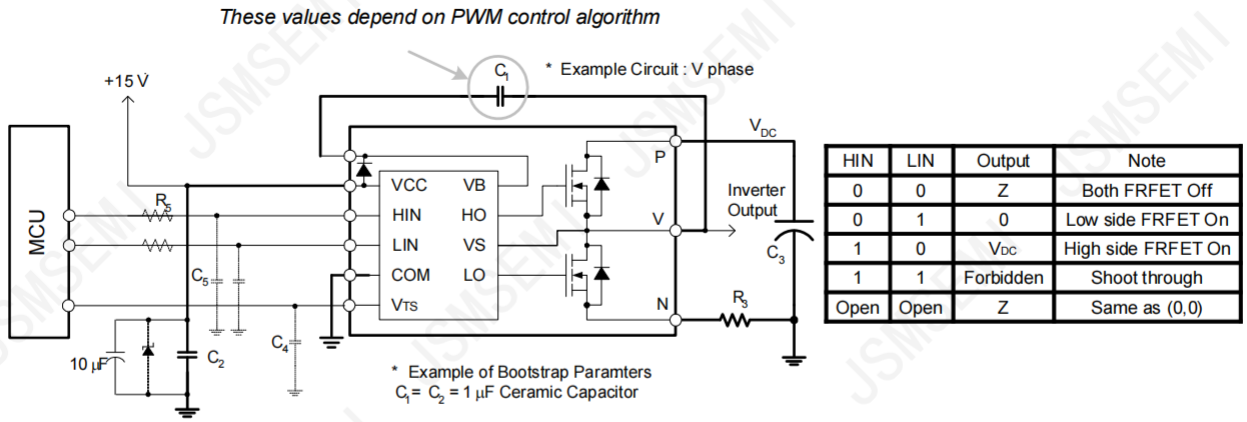
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain - Source Breakdown Voltage	V_{IN} = 0 V, I_D = 1 mA (2nd Note 1)	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN} = 0 V, V_{DS} = 650 V	-	-	1	mA
$R_{DS(on)}$	Static Drain - Source Turn-On Resistance	V_{CC} = V_{BS} = 10 V, V_{IN} = 5 V, I_D = 4.5 A	-	0.4	0.52	Ω
V_{SD}	Drain - Source Diode Forward Voltage	V_{CC} = V_{BS} = 10 V, V_{IN} = 0 V, I_D = -2.5 A	-	-	4.0	V
t_{ON}	Switching Times	V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_D = 0.5 A V_{IN} = 0 V ↔ 5 V, Inductive Load L = 3 mH High- and Low-Side MOSFET Switching	-	860	-	ns
t_{OFF}			-	460	-	ns
t_{rr}			-	70	-	ns
E_{ON}			-	45	-	μJ
E_{OFF}			-	15	-	μJ
RBSOA	Reverse Bias Safe Operating Area	V_{PN} = 400 V, V_{CC} = V_{BS} = 15 V, I_D = I_{DP}, V_{DS} = BV_{DSS}, T_J = 150°C High- and Low-Side MOSFET Switching	Full Square			

Control Part (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{QCC}	Quiescent V_{CC} Current	V_{CC} = 15 V, V_{IN} = 0 V	Applied between V_{CC} and COM	-	80	-	μA
I_{QBS}	Quiescent V_{BS} Current	V_{BS} = 15 V, V_{IN} = 0 V	Applied between $V_{B(U)}$ - U, $V_{B(V)}$ - V, $V_{B(W)}$ - W	-	30	-	μA
UV_{CCD}	Low-Side Under-Voltage Protection	V_{CC} Under-Voltage Protection Detection Level		-	11.5	-	V
UV_{CCR}		V_{CC} Under-Voltage Protection Reset Level		-	10.5	-	V
UV_{BSD}	High-Side Under-Voltage Protection	V_{BS} Under-Voltage Protection Detection Level		-	11.5	-	V
UV_{BSR}		V_{BS} Under-Voltage Protection Reset Level		-	10.5	-	V
V_{TS}	HVIC Temperature Sensing Voltage Output	V_{CC} = 15 V, T_{HVIC} = 25°C		300	600	900	mV
V_{IH}	ON Threshold Voltage	Logic HIGH Level	Applied between V_{IN} and COM	-	-	2.5	V
V_{IL}	OFF Threshold Voltage	Logic LOW Level		0.8	-	-	V

Bootstrap Diode Part (each bootstrap diode unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FB}	Forward Voltage	I_F = 0.1 A, T_C = 25°C	-	2.7	-	V
t_{rrB}	Reverse Recovery Time	I_F = 0.1 A, T_C = 25°C	-	80	-	ns
RBSD	BSD Current Limiting Resistor		-	15	-	ohm



HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low side FRFET On
1	0	V_{DC}	High side FRFET On
1	1	Forbidden	Shoot through
Open	Open	Z	Same as (0,0)

Figure 2. Recommended MCU Interface and Bootstrap Circuit with Parameters

Notes:

1. Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
2. RC-coupling (R_5 and C_5) and C_4 at each input of JSMSEMI IPM product and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge-noise.
3. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge-voltage. Bypass capacitors such as C_1, C_2 and C_3 should have good high-frequency characteristics to absorb high-frequency ripple-current.

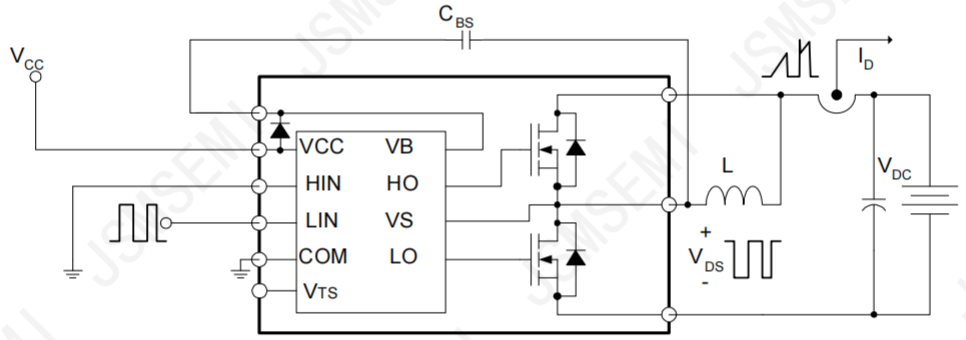


Figure 3. Switching and RBSOA (Single-Pulse) Test Circuit (Low-side)

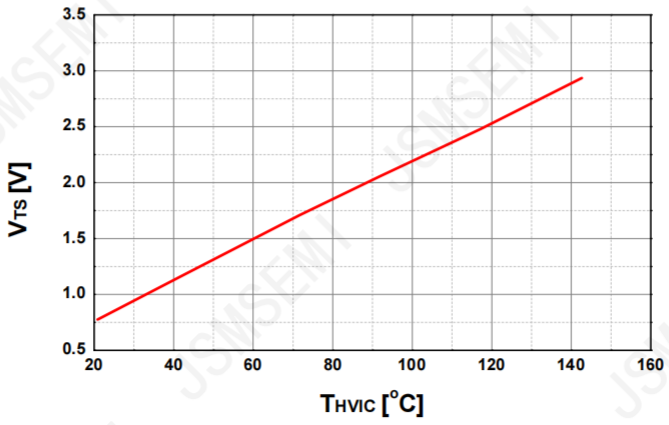


Figure 4. Temperature Profile of V_{TS}(Typical)

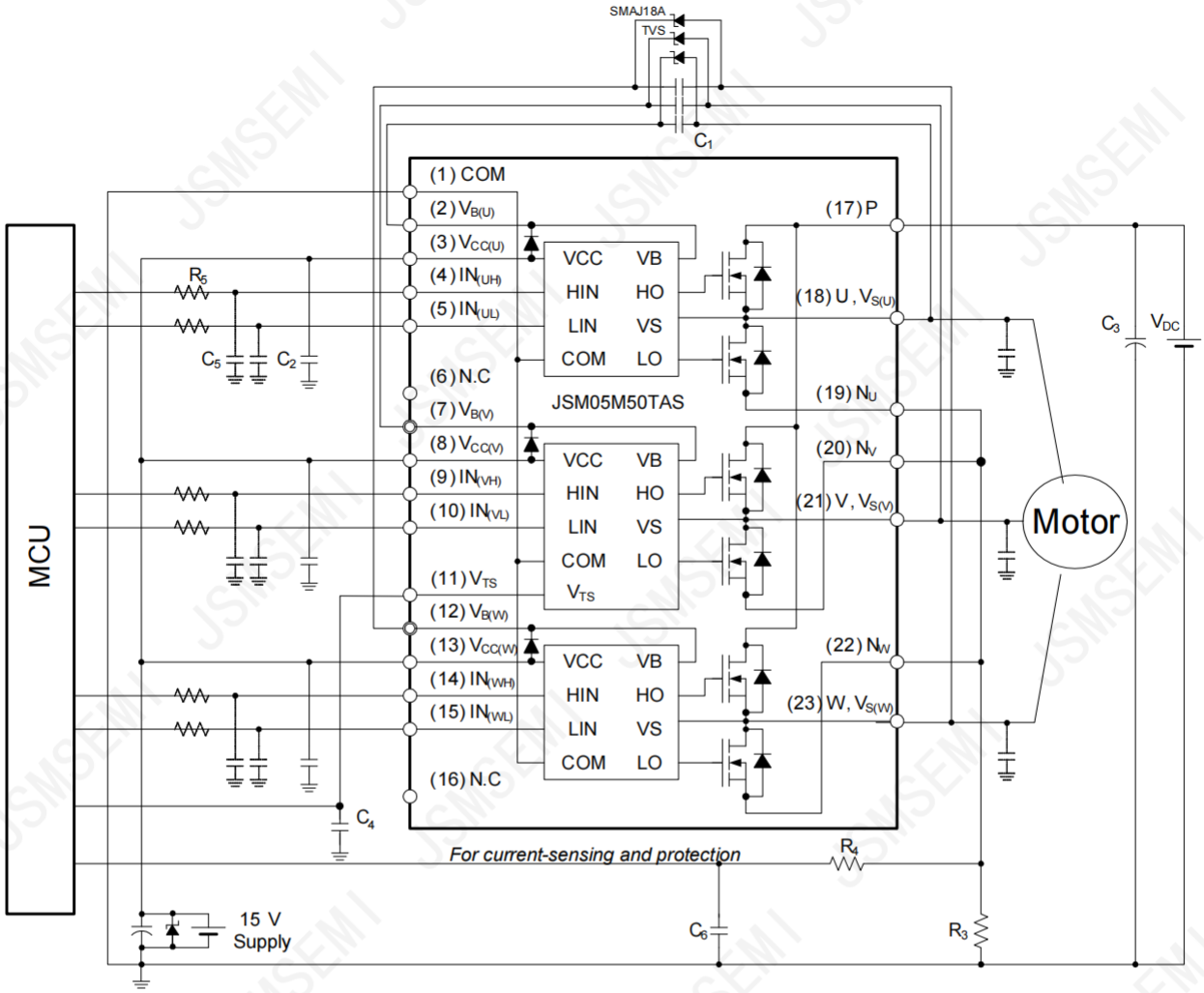


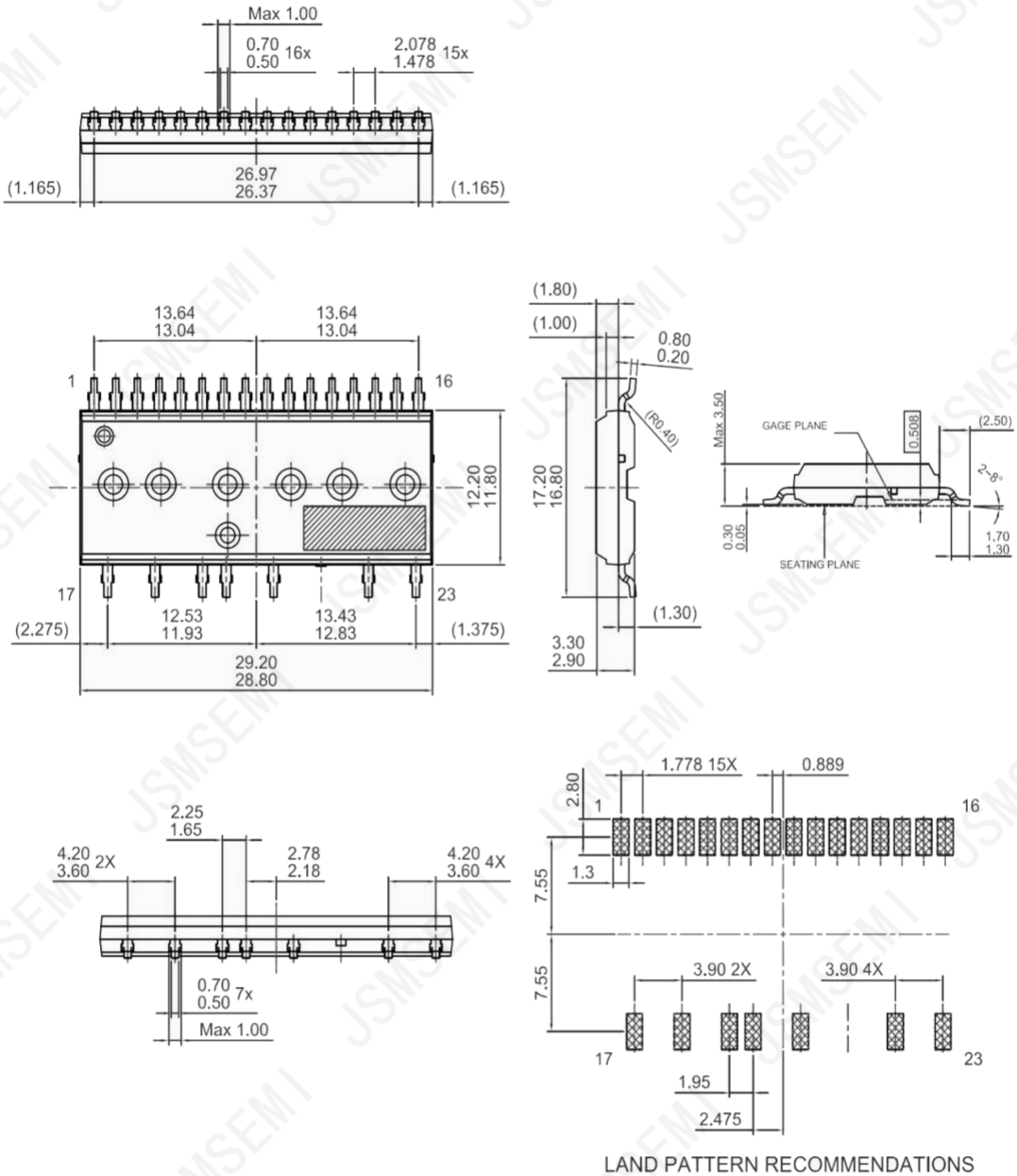
Figure 5. Example of Application Circuit

Notes:

1. About pin position, refer to Figure 1.
2. RC-coupling (R5 and C5, R4 and C6) and C4 at each input of JSMSEMI IPM and MCU are useful to prevent improper input signal caused by surge-noise.
3. The voltage-drop across R3 affects the lowside switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low-side MOSFET. For this reason, the voltage -drop across R3 should be less than 1 V in the steady-state.
4. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
5. All the filter capacitors should be connected close to JSMSEMI IPM, and they should have good characteristics for rejecting highfrequency ripple current.
6. Due to the high-speed switching characteristics of SiC, in order to avoid dv/dt coupling interference, it is recommended that the PCBA reserve a VS-GND capacitor to absorb voltage spikes to compensate for insufficient EMC margin and improve the system's anti-interference capability.
7. For JSMSEMI IPMs, proper moisture protection is essential. It is recommended to apply conformal coating or external insulating adhesive.
8. Ensure adequate heat dissipation. For JSMSEMI IPMs, consider adding insulating pads or ceramic plates and attaching them to the heatsink.

Package Information

SOP-23H



LAND PATTERN RECOMMENDATIONS

Revision History

Rev.	Change	Date
V1.0	Initial version	9/12/2021

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