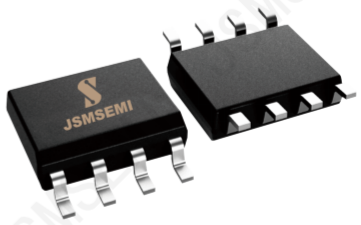
Description

The NCP5183 is a High Voltage High Current Power MOSFET Driver providing two outputs for direct drive of two N−channel power MOSFETs arranged in a half-bridge (or any other high-side +low-side) configuration.

It uses the bootstrap technique to insure a proper drive of the High-side power switch. The driver works with two indep endent inputs to accommodate any topology (including half-bridge,asymmetrical half-bridge, active clamp and full-bridge …).

The NCP5183 package can operate in the temperature range from -40℃ to 125℃.



Features

- Floating channel designed for bootstrap operation
- Voltage Range:up to 700V
- dV/dt Immunity ±50 V/ns
- Gate Drive Supply Range from 9 V to 18 V
- Output Source / Sink Current Capability 4.3 A / 4.3 A
- 3.3 V and 5 V Input Logic Compatible
- Extended Allowable Negative Bridge Pin Voltage Swing to –10V

  -Matched Propagation Delays between Both Channels

  -Propagation Delay 120 ns typically
- Undervoltage lockout for bothchannels

  -VCC UVLO 8.8V

  -VBS UVLO 8.3V
- Pin to Pin Compatible with Industry Standards
- Wide operating temperature range -40°C ~125°C
- These are Pb-free Devices

  SOP-8

Typical Application

. Power Supplies for Telecom and Datacom
. Half-Bridge and Full-Bridge Converters
. Push-Pull Converters
. High Voltage Synchronous-Buck Converters
. Motor Controls
. Electric Power Steering
. Class-D Audio Amplifiers

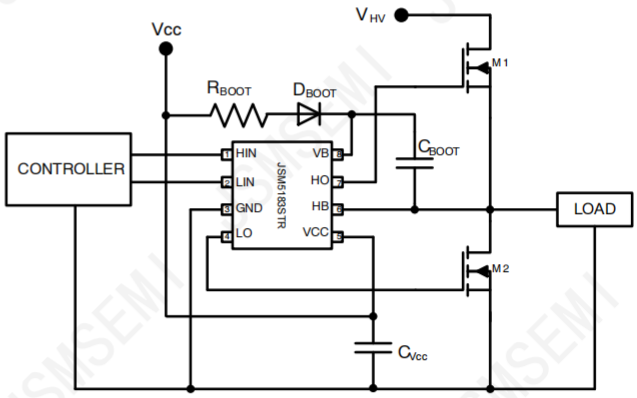
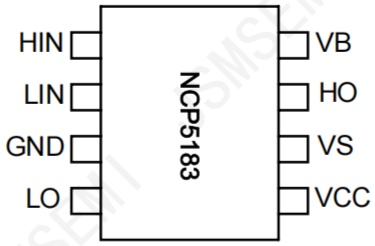


Figure 1. Application Schematic

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
NCP5183DR2G-JSM	SOP-8	JSM5183S	-40 to 125°C	3	T&R,4000	Rohs

PIN CONNECTIONS



PIN FUNCTION DESCRIPTION

Pin No. (SOP-8)	Pin Name	Description
1	HIN	High Side Logic Input
2	LIN	Low Side Logic Input
3	GND	Ground
4	LO	Low Side Gate Drive Output
5	Vcc	Main Power Supply
6	VS	Bootstrap Return or High Side Floating Supply Return
7	HO	High Side Gate Drive Output
8	VB	Bootstrap Power Supply

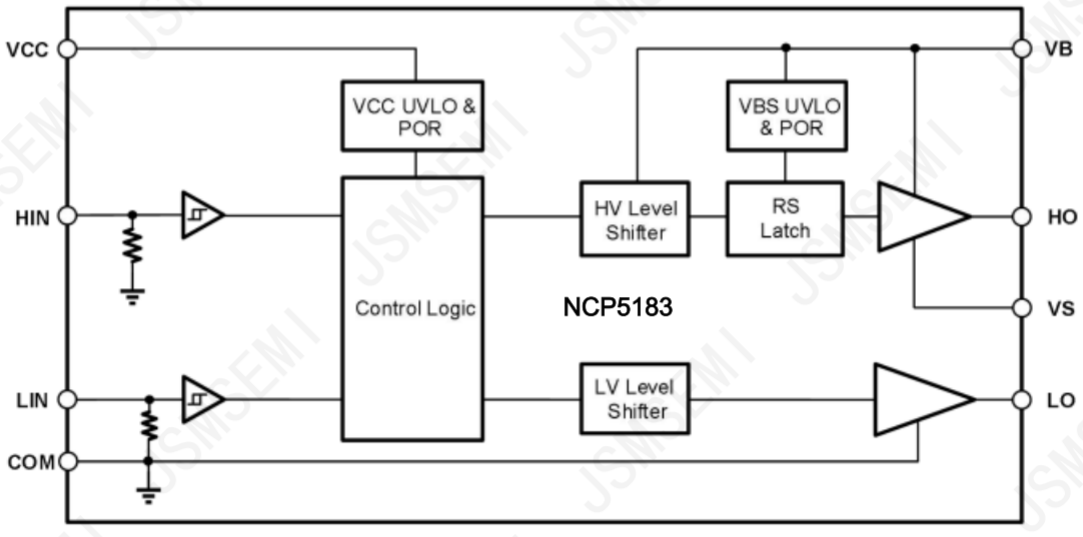


Figure 2. Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

All voltages are referenced to GND pin

Rating	Symbol	Value	Unit
Input Voltage Range	V_{CC}	-0.3 to 18	V
Input Voltage on LIN and HIN pins	V_{LIN}, V_{HIN}	-0.3 to 18	V
High Side Boot pin Voltage	V_B	(higher of {-0.3 ; V_{CC} – 1.5}) to 700	V
High Side Bridge pin Voltage	V_S	V_B - 18 to V_B + 0.3	V
High Side Floating Voltage	V_B – V_S	-0.3 to 18	V
High Side Output Voltage	V_{HO}	V_S – 0.3 to V_B + 0.3	V
		V_S – 2.0 to V_B + 0.3 (Note 3)	
Low Side Output Voltage	V_{LO}	-0.3 to V_{CC} + 0.3	V
		-2.0 to V_{CC} + 0.3 (Note 3)	
Allowable output slew rate	dV/dt	50	V/ns
Maximum Operating Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	-55 to 150	°C
ESD Capability, Human Body Model	ESDHBM	3	kV
ESD Capability, Charged Device Model	ESDCDM	1	kV
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

All voltages are referenced to GND pin

Rating	Symbol	Min	Max	Unit
Input Voltage Range	V_{CC}	10	17	V
High Side Floating Voltage	V_B – V_S	10	17	V
High Side Bridge pin Voltage	V_S	-1	650	V
High Side Output Voltage	V_{HO}	V_S	V_B	V
Low Side Output Voltage	V_{LO}	GND	V_{CC}	V
Input Voltage on LIN and HIN pins	V_{LIN}, V_{HIN}	GND	V_{CC} - 2	V
Operating Junction Temperature Range	T_J	-40	125	°C

Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ELECTRICAL CHARACTERISTICS

-40。C ≤ T_J ≤ 125。C, V_{CC} = V_B = 15 V, V_S = GND, outputs are not loaded, all voltages are referenced to GND; unless otherwise noted. Typical values are at T_J = +25。C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Supply Section						
V_{CC} UVLO	V_{CC} rising	V_{CCon}	7.8	8.8	9.8	V
	V_{CC} falling	V_{CCoff}	7.2	8.3	9.1	V
	V_{CC} hysteresis	V_{CChyst}		0.5		V
V_B UVLO	V_B rising	V_{Bon}	7.8	8.8	9.8	V
	V_B falling	V_{Boff}	7.2	8.3	9.1	V
	V_B hysteresis	V_{Bhyst}		0.5		V
V_{CC} pin operating current	f = 20 kHz, C_L = 1 nF	I_{CC1}		520	700	μA
V_B pin operating current	f = 20 kHz, C_L = 1 nF	I_{B1}		700	800	μA
V_{CC} pin quiescent current	V_{LIN} = V_{HIN} = 0 V	I_{CC2}		95	160	μA
V_B pin quiescent current	V_{LIN} = V_{HIN} = 0 V	I_{B2}		65	100	μA
V_B to GND quiescent current	V_B = V_S = 700 V	I_{HSleak}			50	μA
Input Section						
Logic High Input Voltage		V_{INH}	2.5			V
Logic Low Input Voltage		V_{INL}			1.2	V
Logic High Input Current	V_{xIN} = 5 V	I_{xIN+}		25	50	μA
Logic Low Input Current	V_{xIN} = 0 V	I_{xIN-}			1	μA
Input Pull Down Resistance	V_{xIN} = 5 V	R_{xIN}		250		kΩ
Output Section						
Low Level Output Voltage	I_{LO} = 0 A	V_{LOL}			35	mV
Low Level Output Voltage (HS Driver)	I_{HO} = 0 A	V_{HOL}			35	mV
High Level Output Voltage	I_{LO} = 0 A, V_{LOH} = V_{CC} - V_{LO}	V_{LOH}			35	mV
High Level Output Voltage (HS Driver)	I_{HO} = 0 A, V_{HOH} = V_B – V_{HO}	V_{HOH}			35	mV
Output Positive Peak current	V_{LO} = 0 V, PW = 10 μs	I_{LOH}		4.3		A
Output Negative Peak current	V_{LO} = 15 V, PW = 10 μs	I_{LOL}		4.3		A
Output Positive Peak current (HS Driver)	V_{HO} = 0 V, PW = 10 μs	I_{HOH}		4.3		A
Output Negative Peak current (HS Driver)	V_{HO} = 15 V, PW = 10 μs	I_{HOL}		4.3		A
Output Resistance		R_{OH}		1.7		Ω
Output Resistance		R_{OL}		1.1		Ω
Dynamic Section						
Turn On Propagation Delay		t_{ON}		120	200	ns
Turn Off Propagation Delay		t_{OFF}		120	200	ns
Delay Matching	Pulse width = 1 μs	t_{MT}		0	50	ns
Minimum Positive Pulse Width	V_{xIN} = 0 V to 5 V	t_{minH}			150	ns
Minimum Negative Pulse Width	V_{xIN} = 5 V to 0 V	t_{minL}			100	ns
Switching Parameters						
Output Voltage Rise Time	10% to 90%, C_L = 1 nF	t_r		12	40	ns
Output Voltage Fall Time	90% to 10%, C_L = 1 nF	tf		12	40	ns
Negative VS pin Voltage	PW ≤ t_{ON}, V_{CC} = V_B = 10 V	V_{Sneg}		-8	-7	V

- Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area
- Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25。C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible

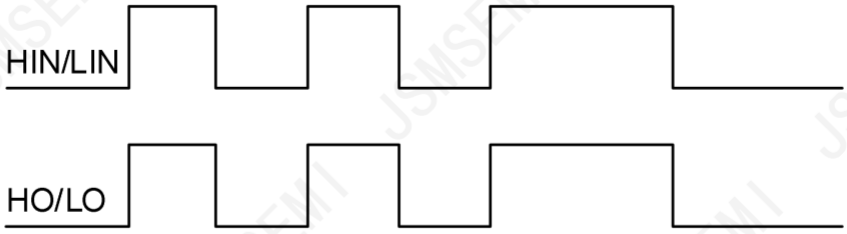


Figure 3. Input and output timing waveform

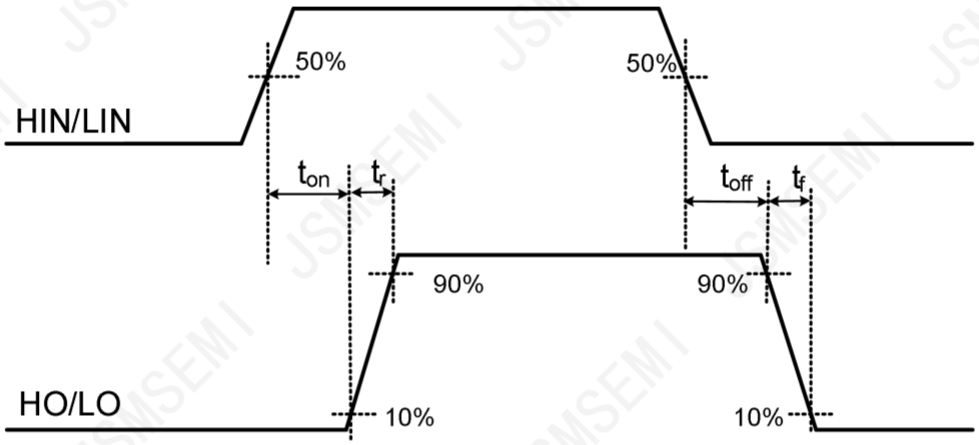


Figure 4. Propagation Time Waveform Definition

I/O logical table

HIN	LIN	HO	LO
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1
0	X	0	0
1	X	1	0
X	0	0	0
X	1	0	1

Note: X represents high input resistance. Due to the internal pull-down resistor, X is equivalent to zero input level.

Negative Transient Immunity (NTI) Operating Conditions

In any VS switching applications the VS node is often pulled under the ground during the switching operation because of parasitic inductances andinductive load.
These negative spikes may lead to malfunction or damageof the circuit.
Below schematics depicts parasitic and current circulation during switching operations that could create the negative deep of the VS node.

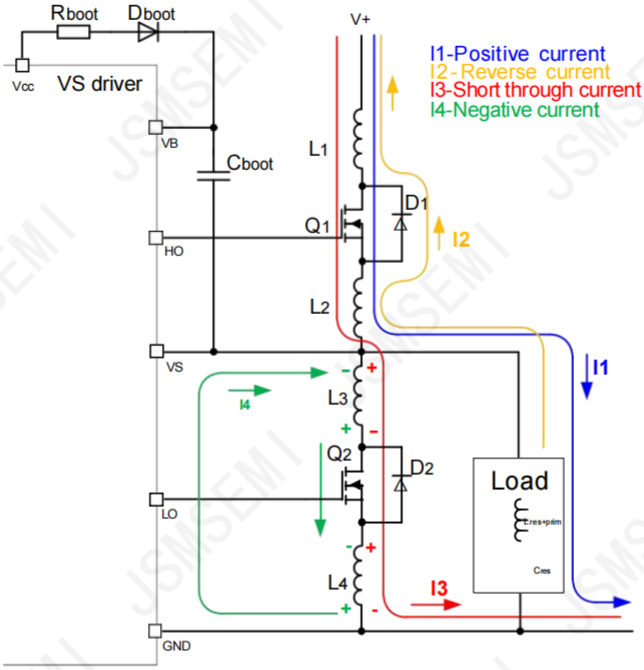


Figure 5 . VS Negative Voltage in an LLC Configuration

Layout Recommendation

The NCP5183 is high speed, high current (sink/source 4.3A/4.3A) driver suitable for high power application. To avoid any damage and/or malfunctio during switching it is very important to avoid a high parasitic inductances in high current paths. It is recommended to fulfill some rules in layout. Keep loop VS_pin – GND_pin – Q_LO as small as possible. This loop (parasitic inductance) has potential to increase negative spike on VS pin which can cause of malfunction or damage of VS driver. The negative voltage presented on VS pin is added to VCC-Vf voltage so VCboot is increased. In extreme case the Cboot voltage can be so high it will reach maximum rating value which can lead to device damage.

Keep loop VDD_pin – GND_pin – CVCC as small as possible. The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q_LO turn on and voltage drop on VCC pin which can result in UVLO activation. . Keep loop VB_pin – VS_pin – Cboot as small as possible. The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q_HI turn on and voltage drop on VB pin which can result in UVLO activation. . Do not let high current flow through trace between GND_pin and CVCC even a small parasitic inductance here will create high voltage drop if high current flows through this path. This voltage is added or subtracted from HIN and LIN signal, which results in incorrect thresholds or device damaging. .

Keep loops LO_pin – Q_LO – GND_pin and HO_pin – Q_HI – VS_pin as small as possible. Ahig h parasitic inductance in these paths will result in slow MOSFET switching and undesired resonance on gate terminal.

Typical application circuit

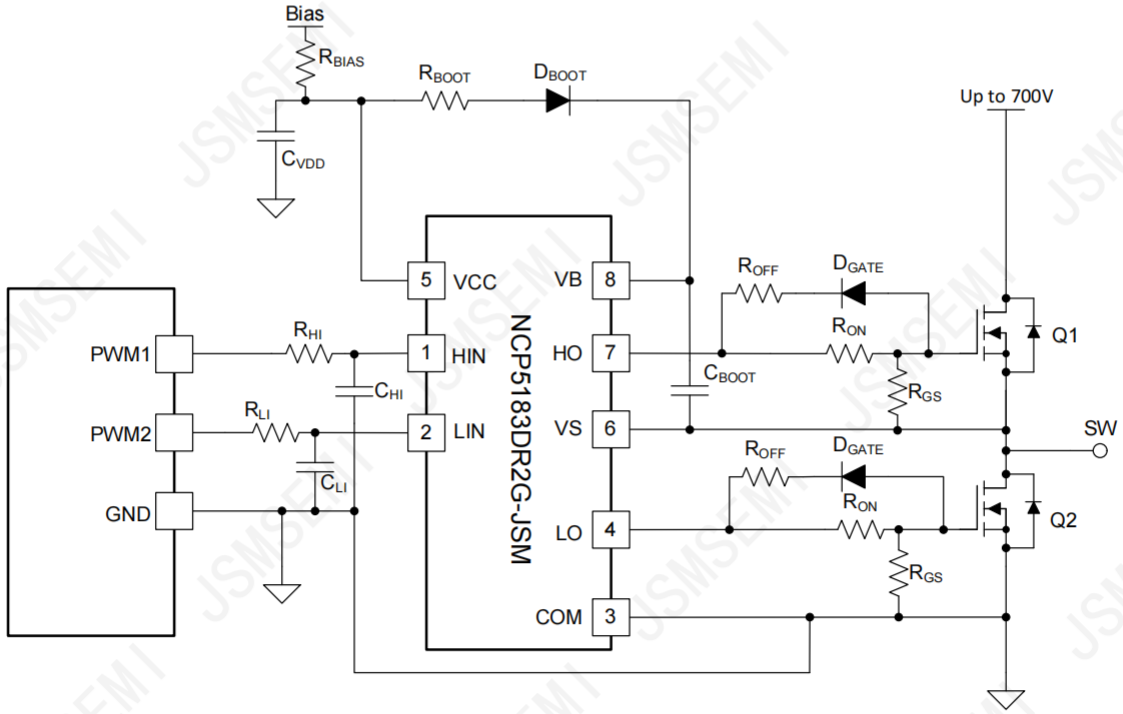


Figure 6 . Typical application circuit - 1

Typical application circuit

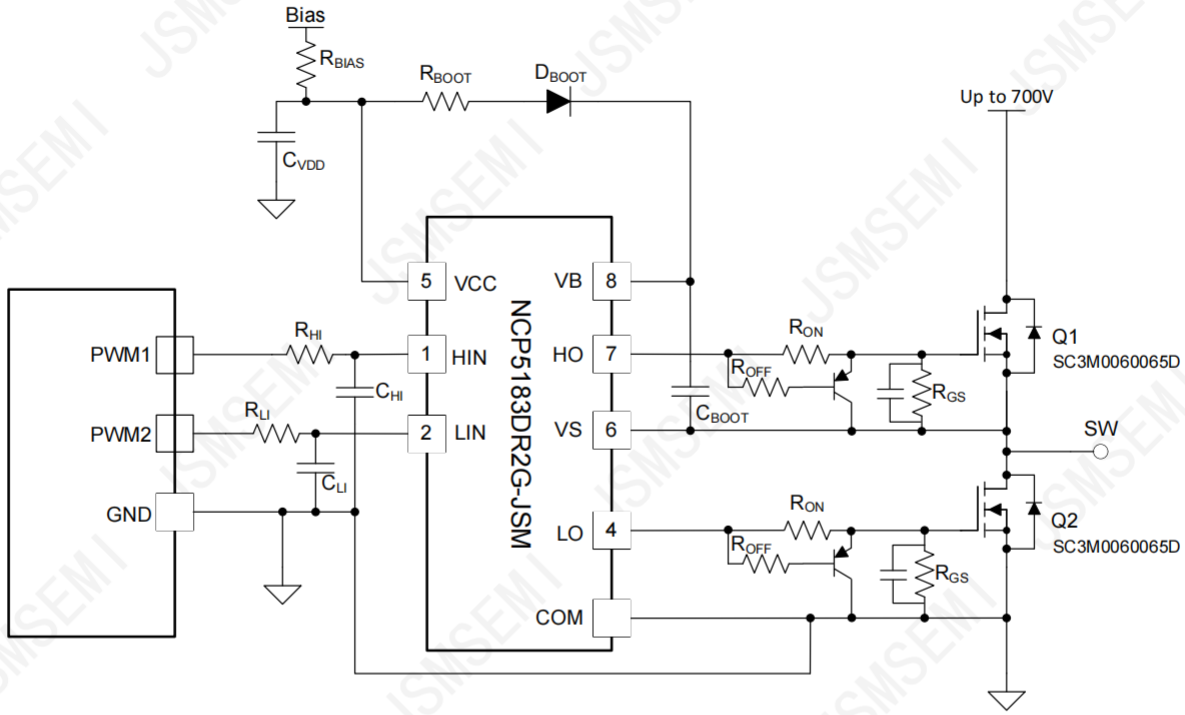


Figure 7 . Typical application circuit - 2

Bootstrap Circuit Design Guide

The structure of a general half-bridge circuit is shown in Figure 8, including bootstrap resistance, bootstrap diode and bootstrap capacitor. This scheme is the most commonly used and cost-effective scheme in the current motor drive.

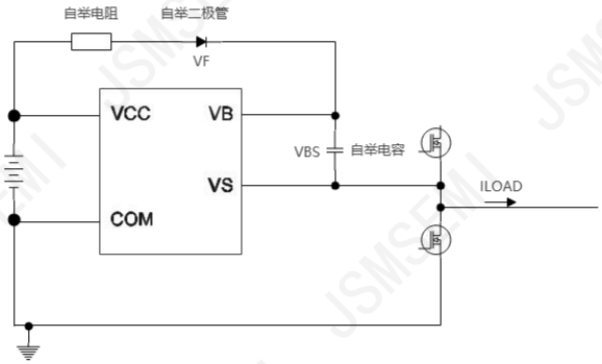


Figure 8 . Basic structure of the bootstrap circuit

Bootstrap circuit capacitance selection

In order to determine the size of the bootstrap capacitance, we first need to evaluate the following points：

-The gate charge required for MOS to turn on: Q_g;

-GS leakage of MOS: I_{LK_GS};

-Static operating current of the drive: I_{QBS};

-Leakage of bootstrap diode: I_{LK_DIODE};

-Bootstrap capacitor leakage: I_{LK_CAP};

-Upper bridge height time: T_{HON}.

I_{LK_CAP} is included in the calculation only when the bootstrappable capacitor uses an electrolytic capacitor. Other types of capacitors do not need to be considered. It is recommended to use at least one low ESR ceramic capacitor. Parallel electrolytic capacitor and low ESR ceramic capacitor can achieve better circuit performance.

By calculation, we can find the loss of capacitance for a single turn on：

$$Q_{TOT} = Q_G + (I_{LK\_GS} + I_{QBS} + I_{LK\_DIODE} + I_{LK\_CAP}) \times T_{HON}$$

Specifies the range that VBS can drop during bootstrapping: $\triangle V_{BS}$

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GSmin} - V_{DSon}$$

In the process, you need assurance：

$$V_{GSmin} > V_{BSUV-}$$

V_F MOS reverse diode voltage drop

V_{GEmin} Maintain the minimum gate voltage for MOS tube conduction

V_{DSon} On-off pressure drop of the lower bridge MOS

And with that, you can calculate it：

$$C_{BOOTmin} = \frac{Q_{TOT}}{\triangle V_{BS}}$$

Note: In the process of calculating bootstrap capacitance here, only the charge required for a pulse process is calculated, without considering the duty ratio and frequency of PWM. If the signal is controlled by PWM wave, please get the actual required bootstrap capacitance size based on the above calculation method through a certain equivalent conversion.

Note on bootstrap circuit

A. Bootstrap resistance

Bootstrap resistors are used in some bootstrap circuits and are not required. HO and LO may have abnormal jump during startup. At this time, the increase of bootstrap resistance will limit the current passing through the bootstrap diode when the bootstrap circuit is started, which can effectively suppress some bad signals and protect the circuit.

B. Bootstrap capacitor

ESR must be considered in the design of the circuit with the upper bridge arm open for a long time when the electrolytic capacitor is used as the bootstrap capacitor. When the upper bridge arm is opened for a long time, a bootstrap capacitor with a large capacity is required, and electrolytic capacitors are generally used. But the electrolytic capacitor has a certain internal resistance, which will reduce the partial voltage of bootstrap resistance and can not realize its function. This situation can be effectively avoided by connecting a ceramic capacitor with a low ESR.

C. Bootstrap diode

The bootstrap diode is used to maintain the voltage stability of the bootstrap circuit. It is necessary to ensure that the reverse voltage resistance of the diode is greater than the voltage of the driving power supply. On this basis, fast recovery

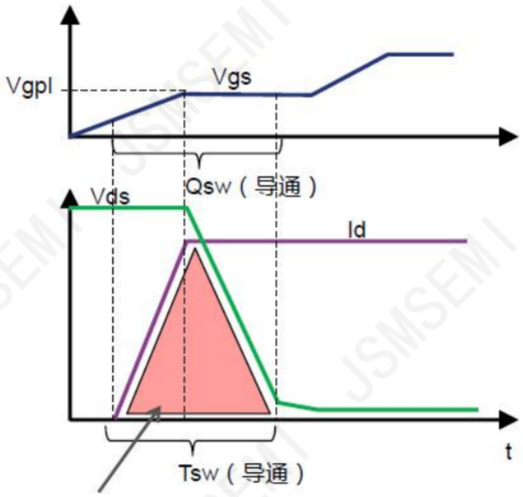
diodes such as Schottky diodes are selected as much as possible.

Bootstrap Circuit Design Guide

Gate resistance is used to control the switching speed of the driven MOS and the slope of the rising and falling edge, which will affect a number of application performance, such as loss, reliability and so on. This section describes how to select the driving resistance and discusses the impact of the driving resistance. The selection of grid resistance is closely related to the driver chip, MOSFET and even circuit design, and it needs to be re-selected according to the actual situation in different environments.

Common industrial brushless motors operate at a frequency of about 2kHz-10kHz. Based on this, grid resistors of 20-120 Ω are usually selected. This is determined by the following two factors：

（1） **Switching loss of MOS.** Part of the MOS loss is switching loss, and the other part is on-off loss, while the grid resistance mainly affects the loss of the switching process. The larger the resistance value, the slower the switching process, and the larger the overlap area of voltage and current, the greater the loss. The most direct impact of excessive loss is that the chip temperature will rise rapidly, and the device will face the risk of failure under the condition of higher than 150℃.



$$Psw(on) = \frac{1}{2} \times Id \times Vds \times Tsw(on)$$

Figure 9 . MOS switch loss under resistive load

（2） **Reliability.** As opposed to loss, the smaller the resistance value of the gate resistance, the faster the MOSFET will switch. In practical applications, the power end current is larger, more sensitive to parasitic parameters, too high switching speed will increase the signal instability, light will make the motor EMI is too large, heavy will make the circuit damage. Some of the most common are:

1) Grid signal rings, causing MOS damage (as shown in Figure 10);

2) The dv/dt is too fast, and the VS port will bear too high or too low voltage signal, resulting in drive damage.。

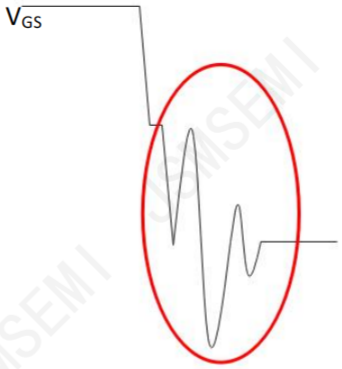


Figure 10 .Grid ringing

PCB layout guide

To achieve the outstanding performance of half bridge grid driver chips, the following printed circuit board (PCB) layout routing guidelines should be followed.

• Low ESR/ESL capacitors should be placed near the driver chip between the VCC and COM pins, and between the VB and VS pins to provide peak current for the VCC and VB pins.

• To prevent large voltage transients from high-side MOSFET drains, a low ESR electrolytic capacitor and a ceramic capacitor must be connected between the high-side MOSFET drain and the ground (COM).

• To avoid excessive negative voltage transients on switch node (VS) pins, the parasitic inductance between the high-side MOSFET source and the low-side MOSFET (synchronous rectifier) source must be minimized.

• Overlap of the VS layer with the ground (COM) layer should be avoided as much as possible to minimize the coupling of switching noise from the VS layer to the ground layer.

• The heat dissipation pad of the driver chip should be connected to a large area of thick copper layer to improve the heat dissipation performance of the driver chip. The heat dissipation pad is usually connected to the ground that is equal to the COM of the chip. It is recommended to connect the heat dissipation pad to the COM pin only.

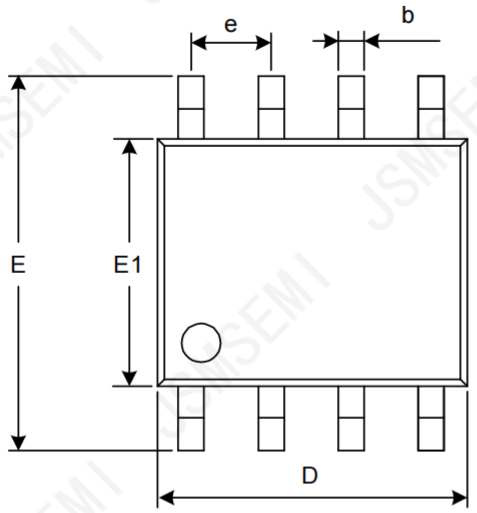
• Grounding precautions:

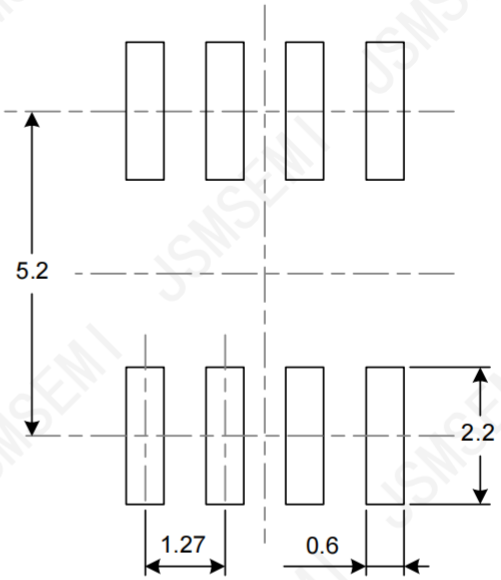
The primary goal of designing a ground connection is to limit the MOSFET gate charge and discharge loop to the smallest possible loop area. This method reduces the loop inductance and can effectively avoid the noise problem on the MOSFET gate. At the same time, the gate driver chip should be as close to the MOSFET as possible.

The second consideration is to ensure reasonable charging paths for bootstrap capacitors, including VCC bypass capacitors based on ground (COM), bootstrap diodes, bootstrap capacitors, and low-side MosFETs. Since the VCC bypass capacitor charges the bootstrap capacitor by cycle through the bootstrap diode, and each charge occurs in a very short period of time, this charge path passes through the peak current. Minimizing the loop length and area of the bootstrap circuit on PCB can make the bootstrap circuit work in a stable state, which is very important to ensure the reliable operation of the driver chip.

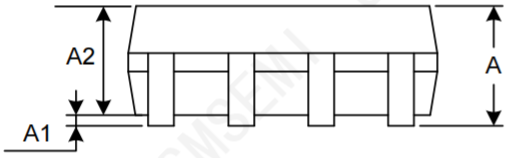
Package Information

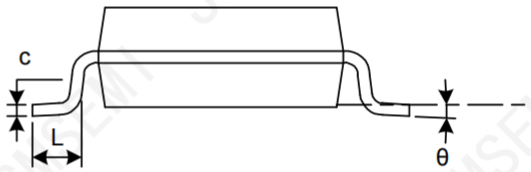
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	7/21/2020

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