

MOSFET – Power, Dual N-Channel Logic Level, Dual SO-8FL

60 V, 58 A, 13 mΩ

NVMFD5873NL

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5873NLWF – Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State $T_{mb} = 25^\circ\text{C}$ $T_{mb} = 100^\circ\text{C}$	58 41 A
P_D	Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State $T_{mb} = 25^\circ\text{C}$ $T_{mb} = 100^\circ\text{C}$	107 54 W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State $T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$	10 7.0 A
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)	Steady State $T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$	3.1 1.6 W
I_{DM}	Pulsed Drain Current $T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	190	A
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to 175	$^\circ\text{C}$
I_S	Source Current (Body Diode)	58	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $I_{L(pk)} = 28.3 \text{ A}$, $L = 0.1 \text{ mH}$, $R_G = 25 \Omega$)	40	mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$R_{\Psi J-mb}$	Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	1.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 3)	48	$^\circ\text{C}/\text{W}$

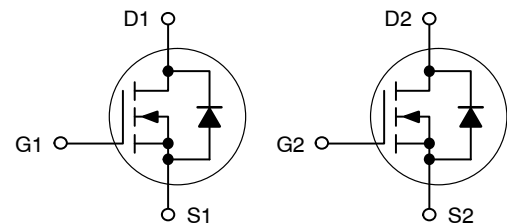
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	13 mΩ @ 10 V	58 A
	16.5 mΩ @ 4.5 V	

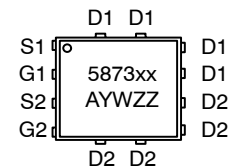


DFN8 5x6
(SO8FL)
CASE 506BT

Dual N-Channel



MARKING DIAGRAM



5873NL = Specific Device Code for NVMFD5873NL
5873LW = Specific Device Code for NVMFD5873NLWF
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been DISCONTINUED. Please refer to the table on page 5.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			54.9		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 7)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-5.8		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		10.7	13	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		13.6	16.5	
g_{FS}	Forward Transconductance	$V_{DS} = 5.0\text{ V}, I_D = 15\text{ A}$		15		S

CHARGES AND CAPACITANCES

C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1560		pF
C_{oss}	Output Capacitance			145		
C_{rss}	Reverse Transfer Capacitance			98		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 15\text{ A}$		16.5		nC
$Q_{G(TH)}$	Threshold Gate Charge			1.3		
Q_{GS}	Gate-to-Source Charge			4.0		
Q_{GD}	Gate-to-Drain Charge			8.8		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 15\text{ A}$		30.5		nC

SWITCHING CHARACTERISTICS (Note 8)

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 15\text{ A}, R_G = 2.5\text{ }\Omega$		10.8		ns
t_r	Rise Time			51		
$t_{d(off)}$	Turn-Off Delay Time			21		
t_f	Fall Time			42.6		
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 15\text{ A}, R_G = 2.5\text{ }\Omega$		9.5		ns
t_r	Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			25		
t_f	Fall Time			6.6		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 15 A	T _J = 25°C		0.8	1.0	V
			T _J = 125°C		0.7		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /d _t = 100 A/μs, I _S = 15 A			22.4		ns
t _a	Charge Time				14.5		
t _b	Discharge Time				9.0		
Q _{RR}	Reverse Recovery Charge					18	

5. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.
6. Switching characteristics are independent of operating junction temperatures.
7. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.
8. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

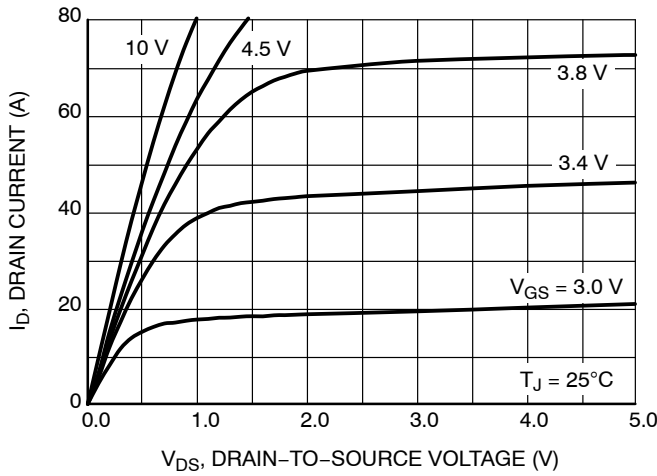


Figure 1. On-Region Characteristics

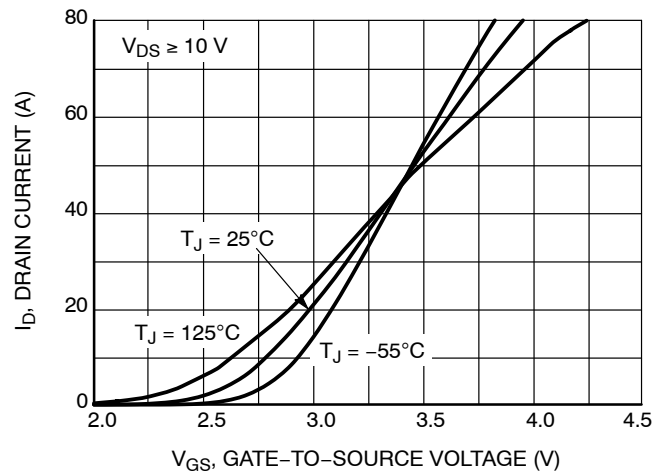


Figure 2. Transfer Characteristics

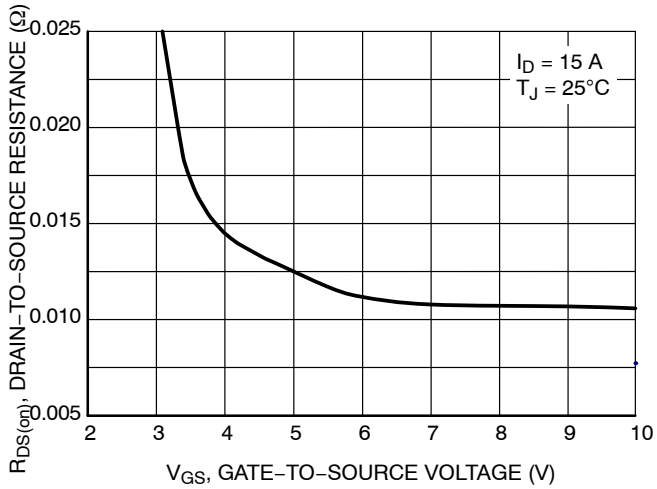


Figure 3. On-Resistance vs. V_{GS}

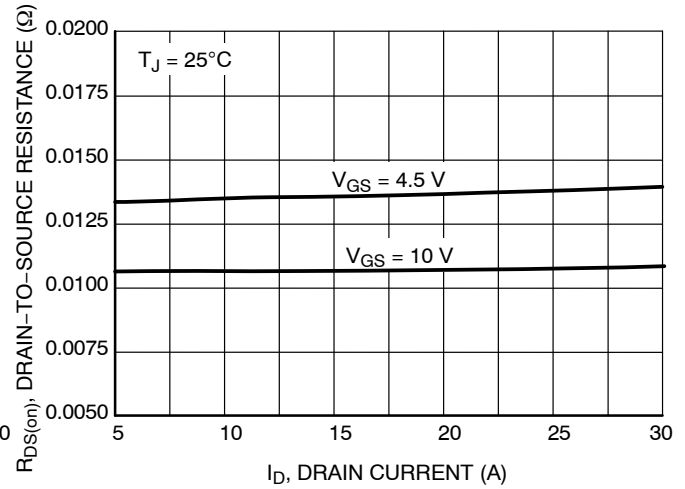


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

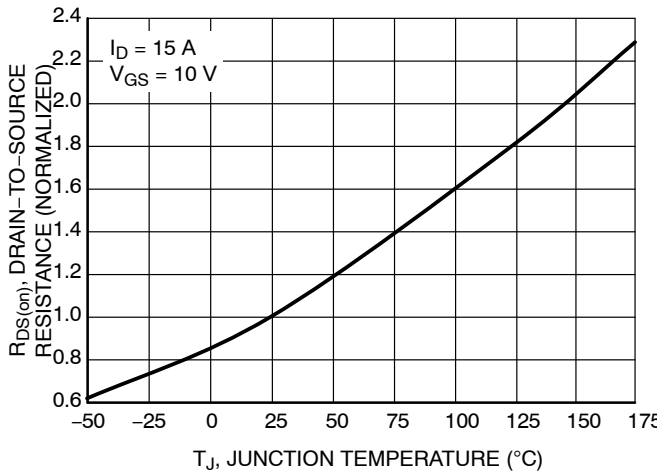


Figure 5. On-Resistance Variation with Temperature

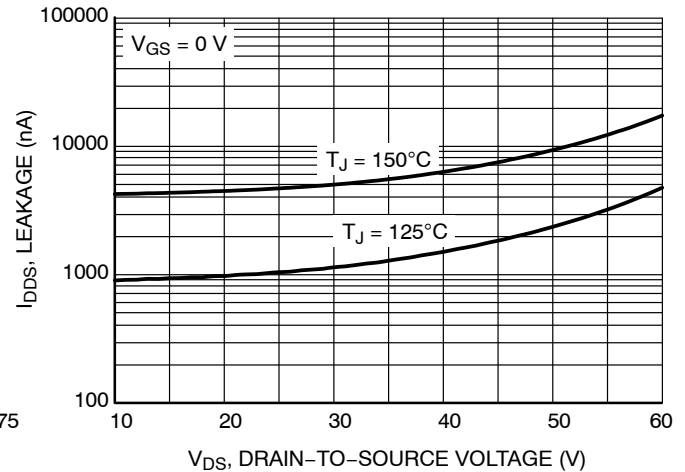


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

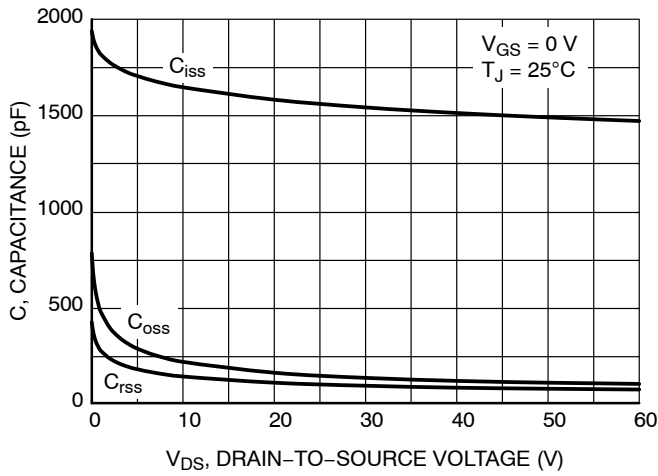


Figure 7. Capacitance Variation

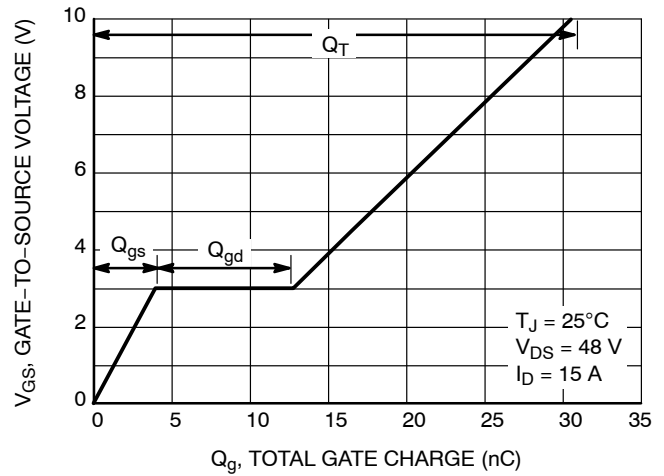


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

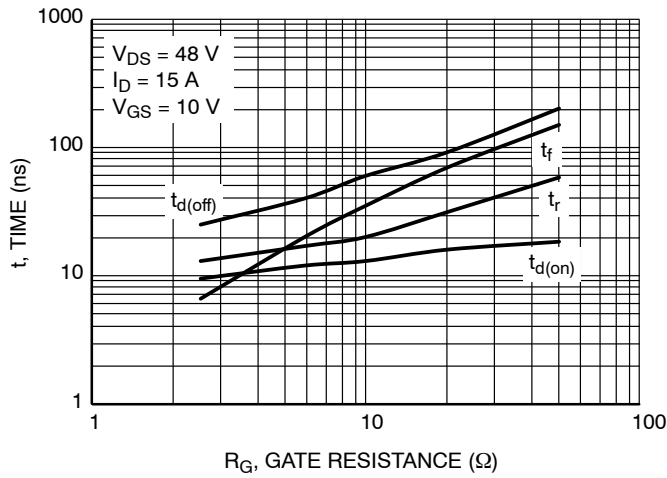


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

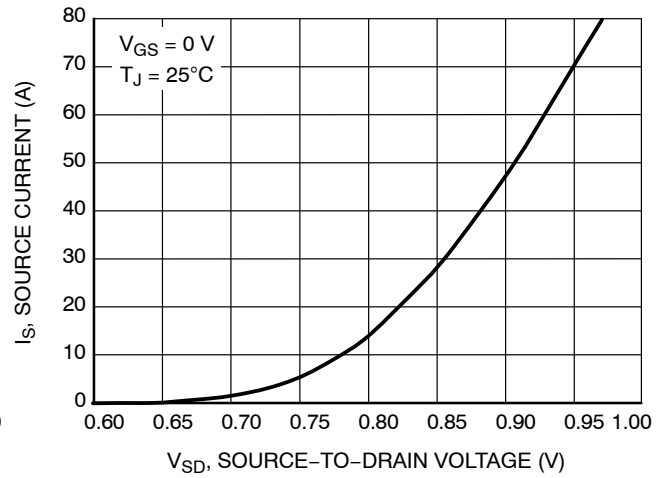


Figure 10. Diode Forward Voltage vs. Current

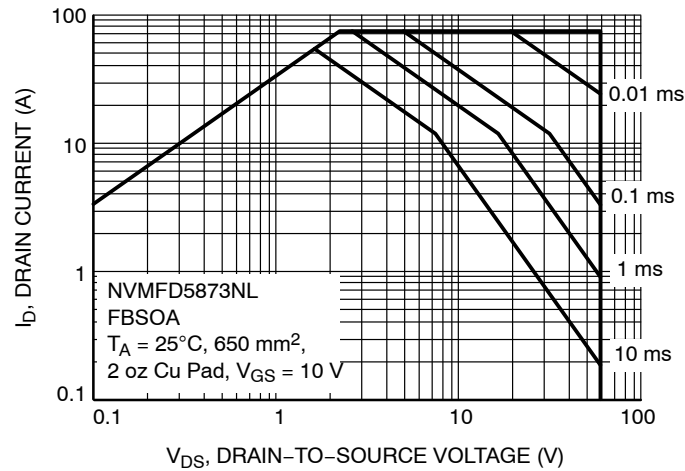


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NVMFD5873NL

TYPICAL CHARACTERISTICS (continued)

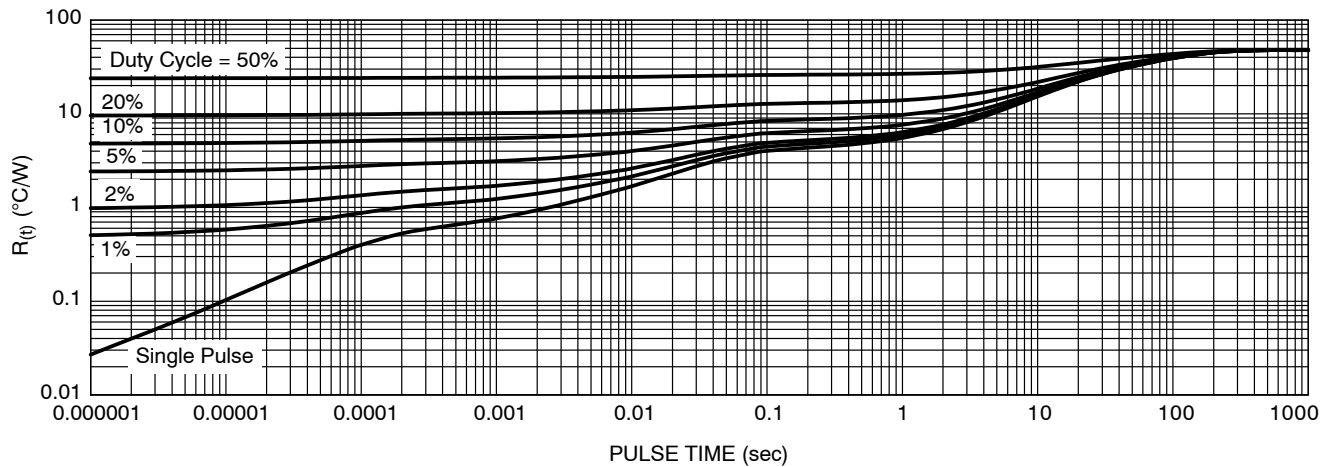


Figure 12. Thermal Response

DEVICE ORDERING INFORMATION

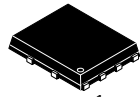
Device	Package	Shippingg [†]
NVMFD5873NLWFT1G-UM	DFN8 (Pb-Free)	1,500 / Tape & Reel

DISCONTINUED (Note 9)

NVMFD5873NLT1G	DFN8 (Pb-Free)	1,500 / Tape & Reel
NVMFD5873NLWFT1G	DFN8 (Pb-Free)	1,500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

9. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



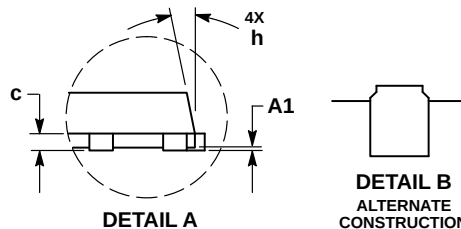
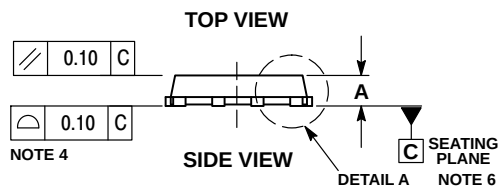
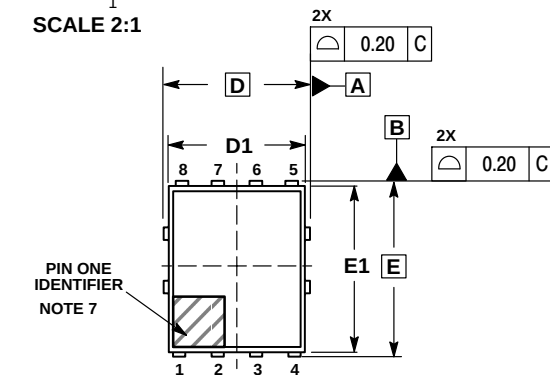
SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)
CASE 506BT
ISSUE F

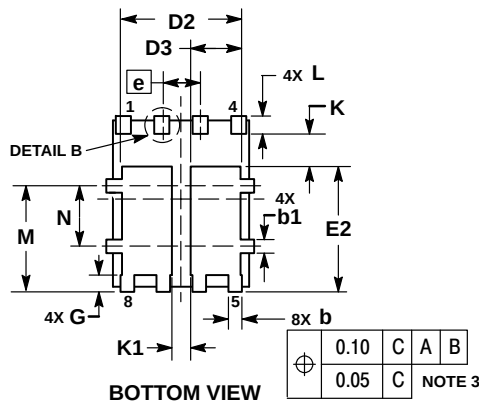
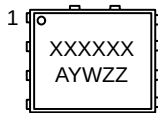
DATE 23 NOV 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

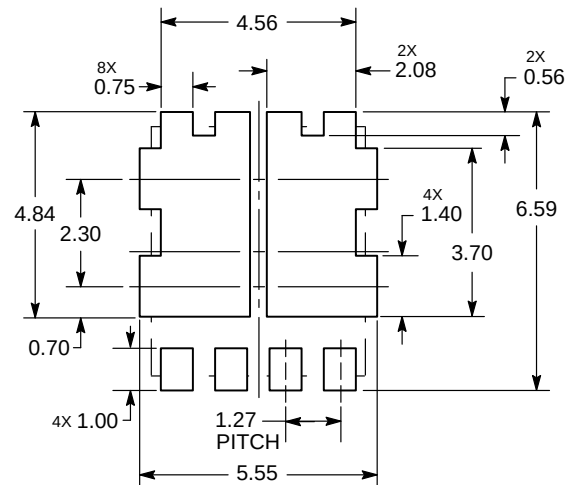


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20


GENERIC MARKING DIAGRAM*


XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*


DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)	PAGE 1 OF 1

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