Single Digital Potentiometer with SPI Interface

Features

- 256 Taps for Each Potentiometer
- INL: ±1 LSB max
- DNL: ±1 LSB max
- SINAD: 73 dB at 1 kHz
- SPI™ Serial Interface (mode 0,0 and 1,1)
- 1 µA maximum supply current in static operation
- Single Supply: 2.7 V ~ 5.5 V
- Package: TSOT23-8
- Extended Temperature Range: -40 °C to +125 °C

Applications

- Precision Data Acquisition
- Automated Testing
- Precision Instrument
- Medical Instrument

Typical Characteristics

Block Diagram

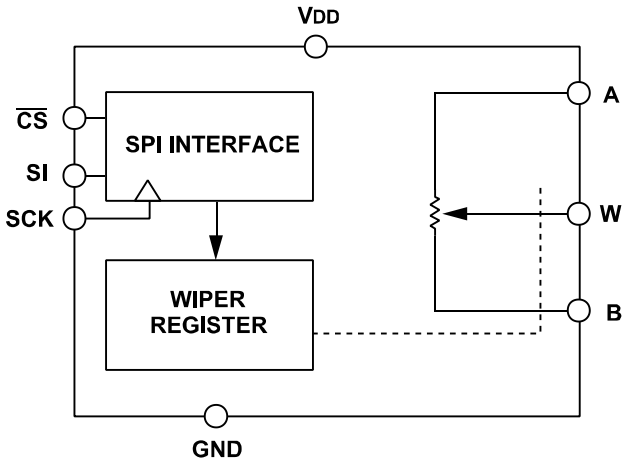


Figure 1. Block Diagram

Pin Configurations and Function Descriptions

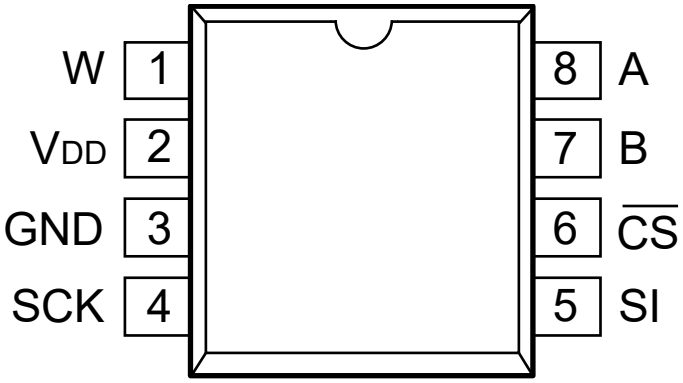


Figure 2. AD5160 Pin Configuration (8-lead TSOT23)

Mnemonic	Pin No.	I/O [1]	Description
W	1	AI	Wiper. Potentiometer Wiper Connection.
V_{DD}	2	P	Power Supply.
GND	3	P	Ground
SCK	4	DI	Serial Clock. Positive edge triggered.
SI	5	DI	Serial Data Input.
$\overline{CS}$	6	DI	Chip Select Input, Active Low. When CS returns high, data loads into the DAC register.
B	7	AI	Terminal B. Potentiometer Terminal B Connection.
A	8	AI	Terminal A. Potentiometer Terminal A Connection.

[1] AI: Analog Input; P: Power; DI: Digital Input.

Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD}	6.0 V
All inputs and outputs to GND	-0.3 V to V_{DD} +0.3 V
Storage Temperature Range	-60 °C to +150 °C
Junction Temperature Range	150 °C
Reflow Soldering	
Peak Temperature	260 °C
Electrostatic Discharge (ESD) [2]	
Human Body Model (HBM) [3]	1.5 kV

Thermal Resistance [4]

Package Type	θ_{JA}	θ_{JC}	Unit
TSOT23-8	195	47	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant.

[4] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

DC Characteristics: R_{AB} = 10 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance.

Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V. Typical specifications represent values for V_{DD} = 5 V, V_B = 0 V, T_A = +25 °C.

Parameter	Symbol	Conditions		Min	Typ. [1]	Max	Unit
Rheostat Mode							
Nominal Resistance [2]	R	T_A = +25 °C			10		kΩ
Rheostat Differential Nonlinearity [3]	R-DNL		●		±0.15		LSB
Rheostat Integral Nonlinearity [3]	R-INL		●		±0.25		LSB
Rheostat Tempcoef	$\Delta R_{AB}/\Delta T$		●		±10		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5.5 V, I_W = 1 mA, Code 00h	●		50		Ω
Wiper Current	I_W					6	mA
Potentiometer Divider							
Resolution	N			8			Bits
Monotonicity	N			8			Bits
Differential Nonlinearity	DNL		●		±0.1		LSB [4]
Integral Nonlinearity	INL		●		±0.2		LSB
Voltage Divider Tempcoef	$\Delta V_W/\Delta T$				±5		ppm/°C
Full Scale Error	V_{WFSE}	Code FFh	●		±0.4		LSB
Zero Scale Error	V_{WFSE}	Code 00h	●		1.2		LSB
Resistor Terminals							
Voltage Range [5]	$V_{A,B,W}$			0		V_{DD}	V
Capacitance (C_A or C_B)	$C_{A,B}$	f = 1 MHz, Code = 80h,			25		pF
Capacitance	C_W	f = 1 MHz, Code = 80h,			12		pF
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5 V)							
-3 dB Bandwidth	BW	V_B = 0 V, Measured at Code 80h, Output Load = 30 pF			3		MHz
Settling Time	T_S	V_A = V_{DD}, V_B = 0 V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF			2		µS
Resistor Noise Voltage	e_{NWB}	V_A = Open, Code 80h, f =1 kHz			9		nV/√Hz

[1] Typical values represent average readings at 25 °C, V_{DD} = 5 V.

[2] V_{AB} = V_{DD}, no connection on wiper.

[3] Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 µA for V_{DD} = 3 V and I_W = 400 µA for V_{DD} = 5 V for 10 kΩ version.

[4] INL and DNL are measured at VW with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions.

[5] Resistor terminals A,B and W have no restrictions on polarity with respect to each other.

DC Characteristics: R_{AB} = 100 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance.

Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V. Typical specifications represent values for V_{DD} = 5 V, V_B = 0 V, T_A = +25 °C.

Parameter	Symbol	Conditions		Min	Typ. [1]	Max	Unit
Rheostat Mode							
Nominal Resistance [2]	R	T_A = +25 °C			100		kΩ
Rheostat Differential Nonlinearity [3]	R-DNL		●		±0.1		LSB
Rheostat Integral Nonlinearity [3]	R-INL		●		±0.2		LSB
Rheostat Tempcoef	$\Delta R_{AB}/\Delta T$		●		35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5.5 V, I_W = 1 mA, Code 00h	●		50		Ω
Wiper Current	I_W		●			1.5	mA
Potentiometer Divider							
Resolution	N			8			Bits
Monotonicity	N			8			Bits
Differential Nonlinearity	DNL		●		±0.1		LSB [4]
Integral Nonlinearity	INL		●		±0.2		LSB
Voltage Divider Tempcoef	$\Delta V_W/\Delta T$				±5		ppm/°C
Full Scale Error	V_{WFSE}	Code FFh	●		-1.2		LSB
Zero Scale Error	V_{WFSE}	Code 00h	●		0.4		LSB
Resistor Terminals							
Voltage Range [5]	$V_{A,B,W}$			0		V_{DD}	V
Capacitance (C_A or C_B)	$C_{A,B}$	f = 1 MHz, Code = 80h,			12		pF
Capacitance	C_W	f = 1 MHz, Code = 80h,			5		pF
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5 V)							
-3 dB Bandwidth	BW	V_B = 0 V, Measured at Code 80h, Output Load = 30 pF			0.3		MHz
Settling Time	T_S	V_A = V_{DD}, V_B = 0 V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF			18		µS
Resistor Noise Voltage	e_{NWB}	V_A = Open, Code 80h, f =1 kHz			27		nV/√Hz

[1] Typical values represent average readings at 25 °C, V_{DD} = 5 V.

[2] V_{AB} = V_{DD}, no connection on wiper.

[3] Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions.

[4] INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions.

[5] Resistor terminals A, B and W have no restrictions on polarity with respect to each other.

Digital I/O and Power Characteristics

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance.

Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V. Typical specifications represent values for V_{DD} = 5 V, V_{SS} = 0 V, V_B = 0 V, T_A = +25 °C.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Digital Inputs/Outputs ($\overline{CS}$, SCK, SI)							
Schmitt Trigger High-Level Input Voltage	V_{IH}	V_{DD} = 5 V	●	0.7 × V_{DD}			V
Schmitt Trigger Low-Level Input Voltage	V_{IL}	V_{DD} = 5 V	●			0.3 × V_{DD}	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		●	0.1 × V_{DD}			V
High-Level Output Voltage	V_{OL}		●	V_{DD} - 0.2			V
High-Level Output Voltage	V_{OH}		●			0.2	V
Input Leakage Current	I_{LI}	$\overline{CS}$ = V_{DD}, VIN = V_{DD},				1	µA
Pin Capacitance (All Inputs/Outputs)	C_{IN}, C_{OUT}	V_{DD} = 5.0 V, T_A = +25 °C, f_C = 1 MHz			3		pF
Power Requirements							
Operating Voltage Range	V_{DD}		●	2.7		5.5	V
Supply Current, Static [1]	I_{DDS}		●		0.2		µA
Operating Voltage Range	V_{DD}		●	2.7		5.5	V
Temperature Range							
Specified Performance				-40		+125	°C

[1] Supply current is independent of current through the potentiometers.

Timing Specifications

Unless otherwise specified, V_{DD} = 2.7 V to 5.5 V, T_A = -40 °C to +125 °C

Parameter	Symbol	Min	Typ.	Max	Unit
Clock Frequency (V_{DD} = 5 V)	F_{CLK}			25	MHz
Clock High Time	t_{HI}	18			ns
Clock Low Time	t_{LO}	18			ns
$\overline{CS}$ Fall to First Rising SCK Edge	t_{CSSR}	40			ns
Data Input Setup Time	t_{SU}	10			ns
Data Input Hold Time	t_{HD}	10			ns
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	30			ns
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	10			ns
$\overline{CS}$ Rise to SCK Rise Hold	t_{CS1}	100			ns
$\overline{CS}$ High Time	t_{CSH}	40			ns
$\overline{CS}$ Low Time	t_{CSL}	10			ns

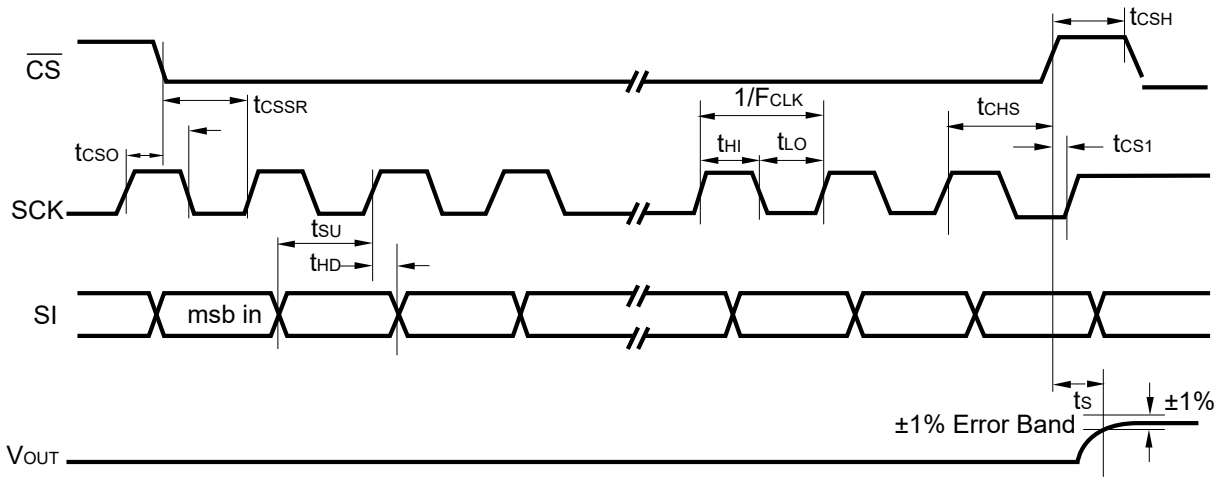


Figure 3. Detailed Serial Interface Timing

Outline Dimensions

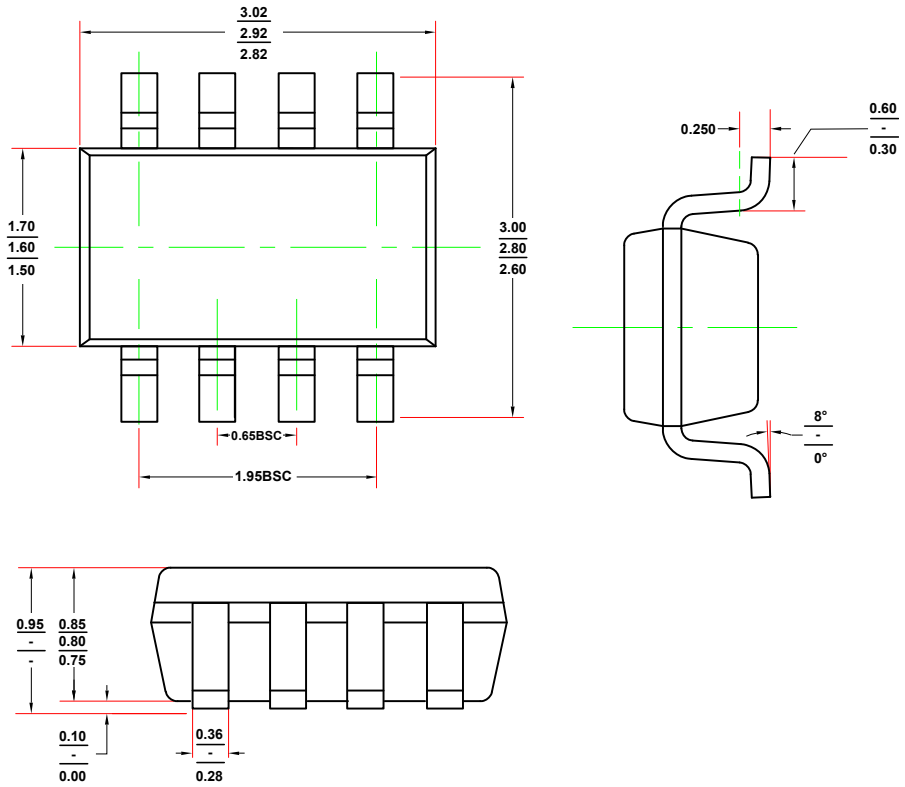


Figure 4. 8-Lead TSOT23 Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Package	Marking	Supply Voltage (V)	Temperature Range (°C)	External Package
AD5160-10	AD5160BRJZ10-R7	TSOT23-8	274113	2.7 to 5.5	-40 to +125	7”reel
AD5160-100	AD5160BRJZ100-R7	TSOT23-8	274114		-40 to +125	7”reel