

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

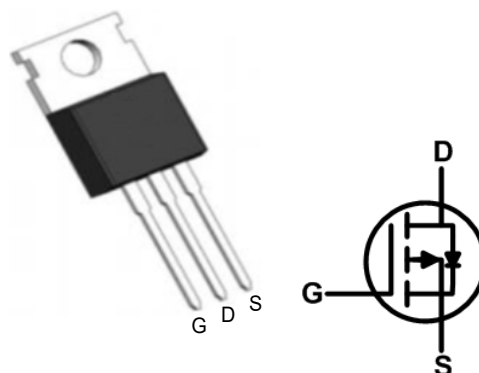
Product Summary


BVDSS	RDS(on)	ID
-100V	24.5mΩ	-80A

Description

The XR80P10T is the high cell density trenched P-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The XR80P10T meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

TO220AB Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	-80	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	-35	A
I _{DM}	Pulsed Drain Current ²	-200	A
EAS	Single Pulse Avalanche Energy ³	281	mJ
I _{AS}	Avalanche Current	-37	A
P _D @T _C =25°C	Total Power Dissipation ⁴	147	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	---	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	---	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	---	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V$, $I_D=-1A$	---	24.5	30	$m\Omega$
		$V_{GS}=-10V$, $I_D=-1A$	---	27	35	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-1.2	-1.85	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-100V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-100V$, $V_{GS}=0V$, $T_J=100^\circ\text{C}$	---	---	---	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-10V$, $I_D=-20A$	---	60	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	5	---	Ω
Q_g	Total Gate Charge	$V_{DS}=-50V$, $V_{GS}=-10V$, $I_D=-20A$	---	196	---	nC
Q_{gs}	Gate-Source Charge		---	25.5	---	
Q_{gd}	Gate-Drain Charge		---	41.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=-10V$, $V_{DS}=-50V$, $I_D=-20A$, $R_G=3\Omega$	---	20	---	ns
T_r	Rise Time		---	50	---	
$T_{d(off)}$	Turn-Off Delay Time		---	120	---	
T_f	Fall Time		---	198	---	
C_{iss}	Input Capacitance	$V_{DS}=-50V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	8650	---	pF
C_{oss}	Output Capacitance		---	250	---	
C_{rss}	Reverse Transfer Capacitance		---	215	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-30	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-20A$, $T_J=25^\circ\text{C}$	---	---	-1.2	V

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD}=-30V$, $V_{GS}=-10V$, $L=0.4\text{mH}$,
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Performance Characteristics

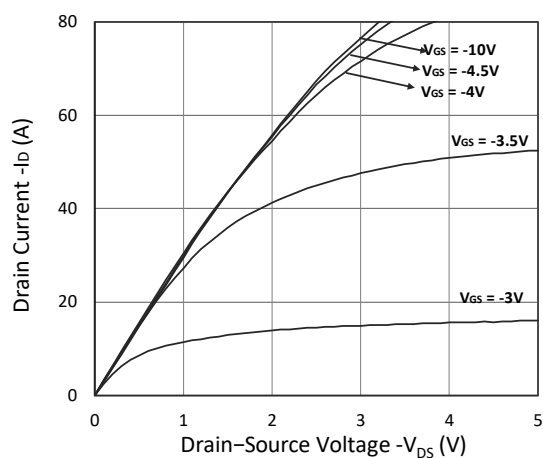


Figure 1. Output Characteristics

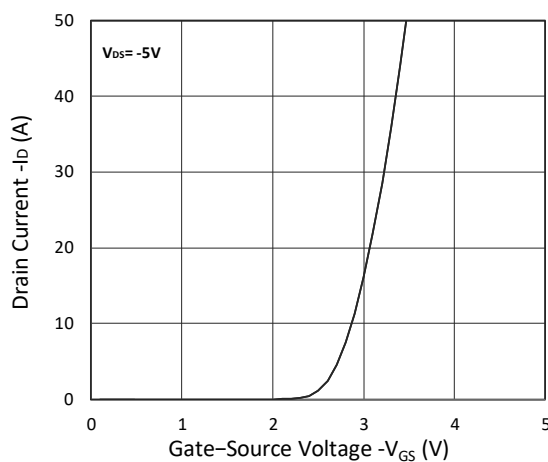


Figure 2. Transfer Characteristics

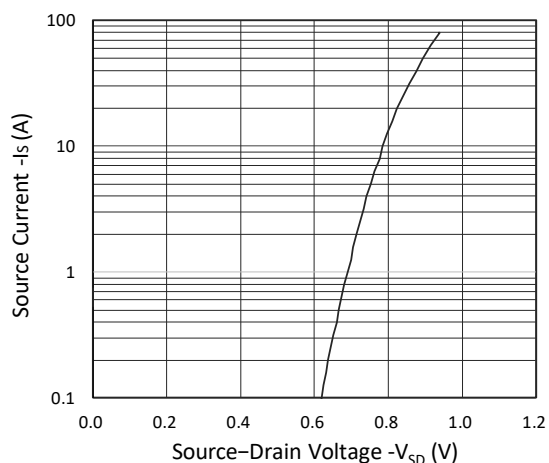


Figure 3. Forward Characteristics of Reverse

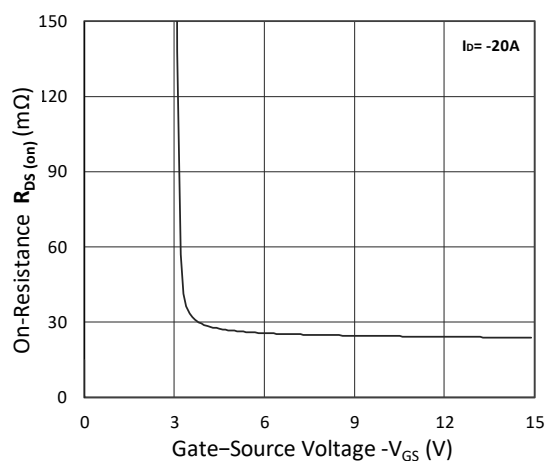


Figure 4. $R_{DS(on)}$ vs. V_{GS}

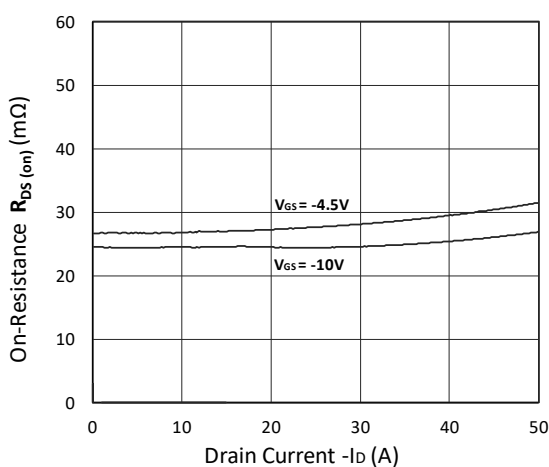


Figure 5. $R_{DS(on)}$ vs. I_D

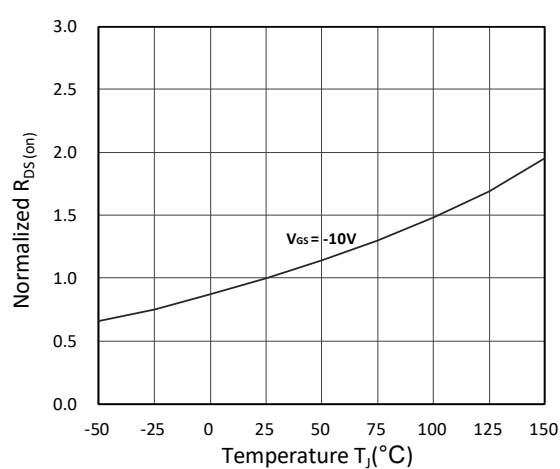


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

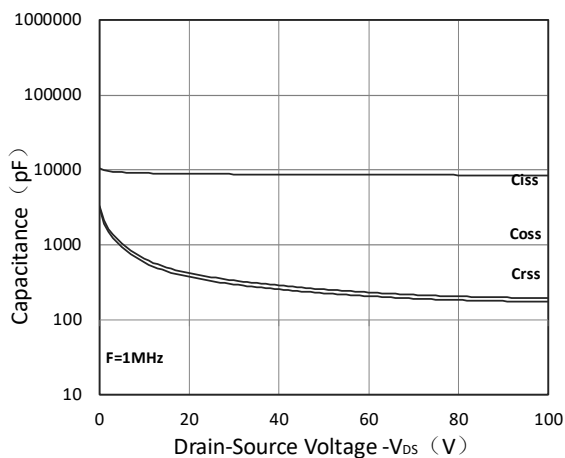


Figure 7. Capacitance Characteristics

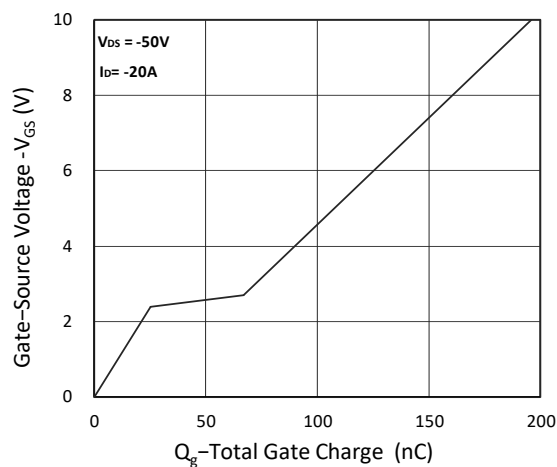


Figure 8. Gate Charge Characteristics

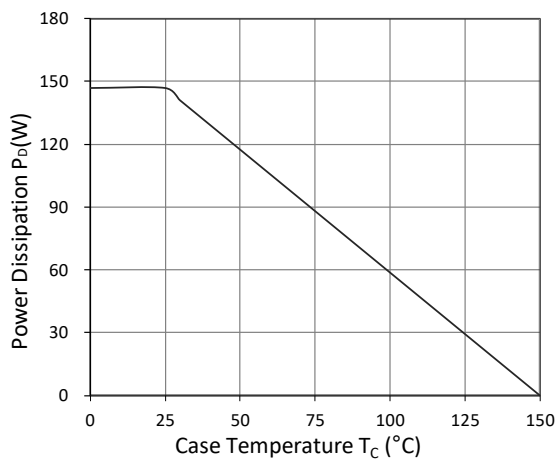


Figure 9. Power Dissipation

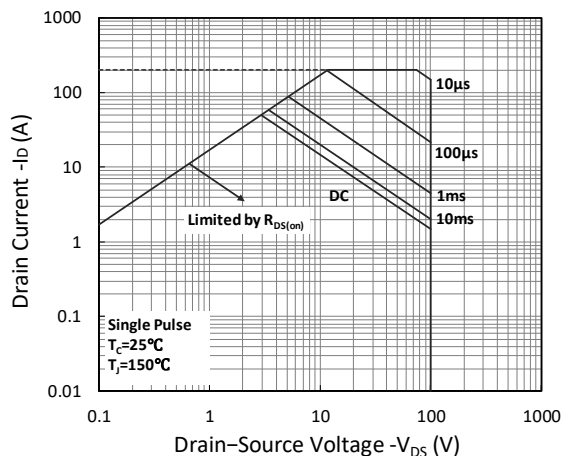


Figure 10. Safe Operating Area

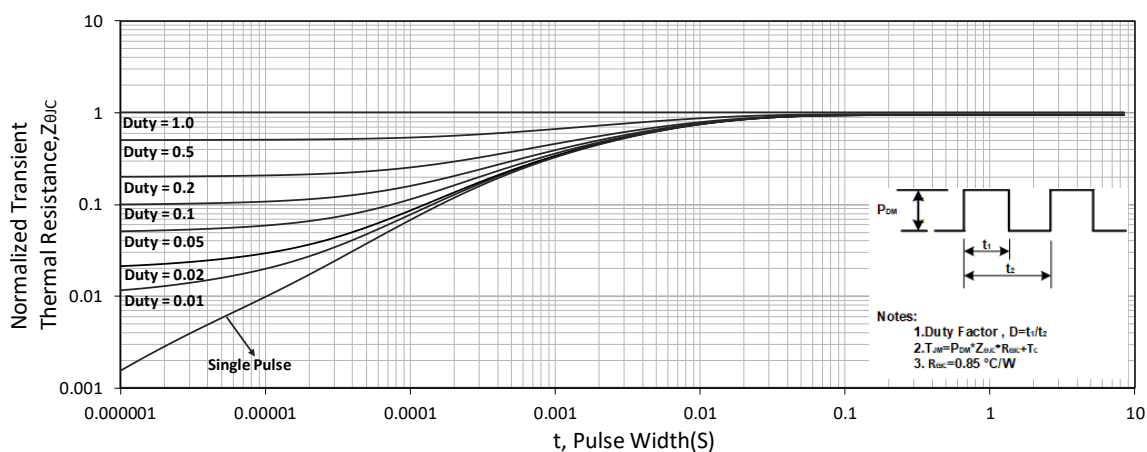
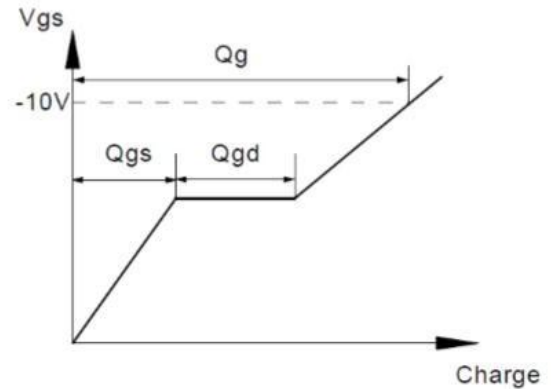
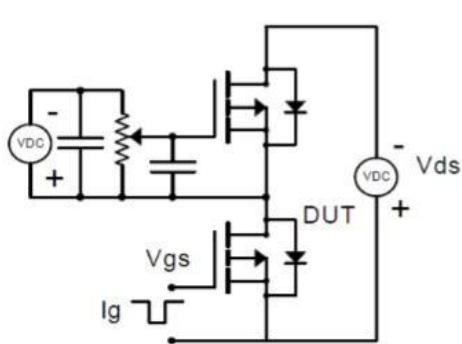


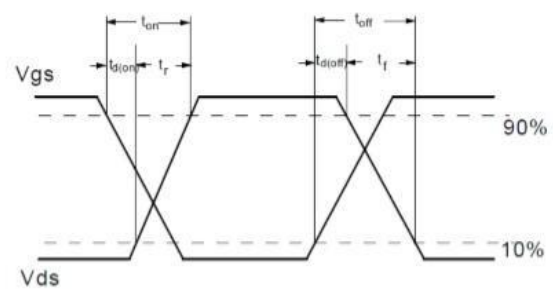
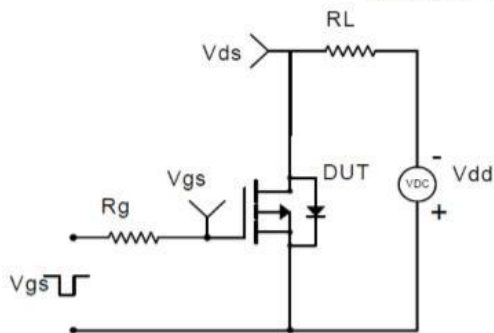
Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit & Waveform

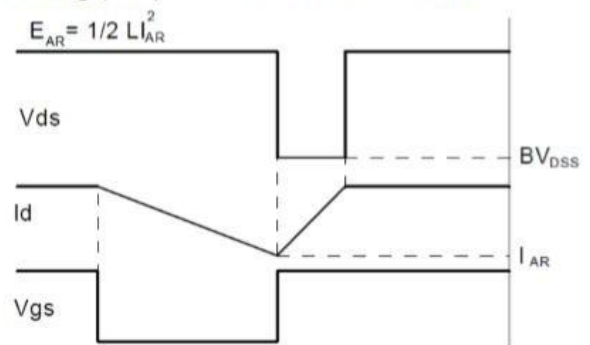
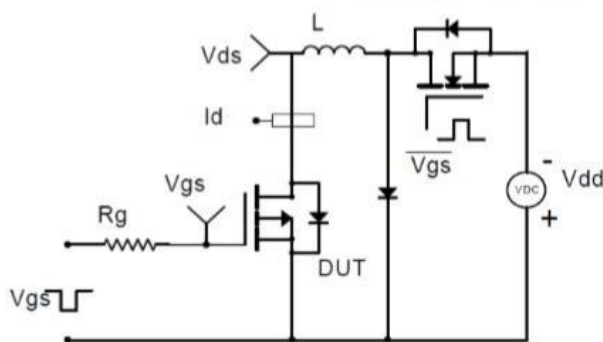
Gate Charge Test Circuit & Waveform



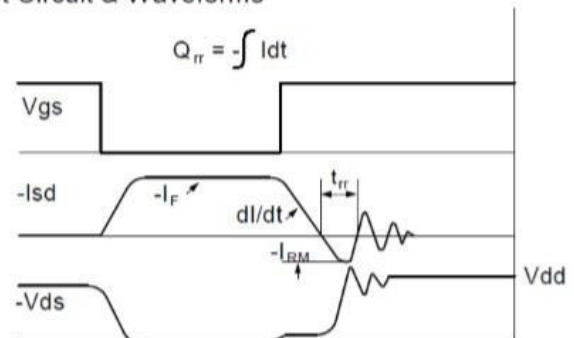
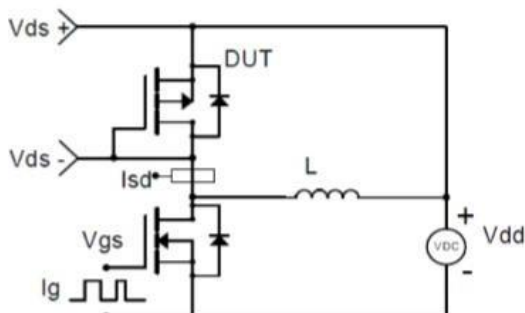
Resistive Switching Test Circuit & Waveforms



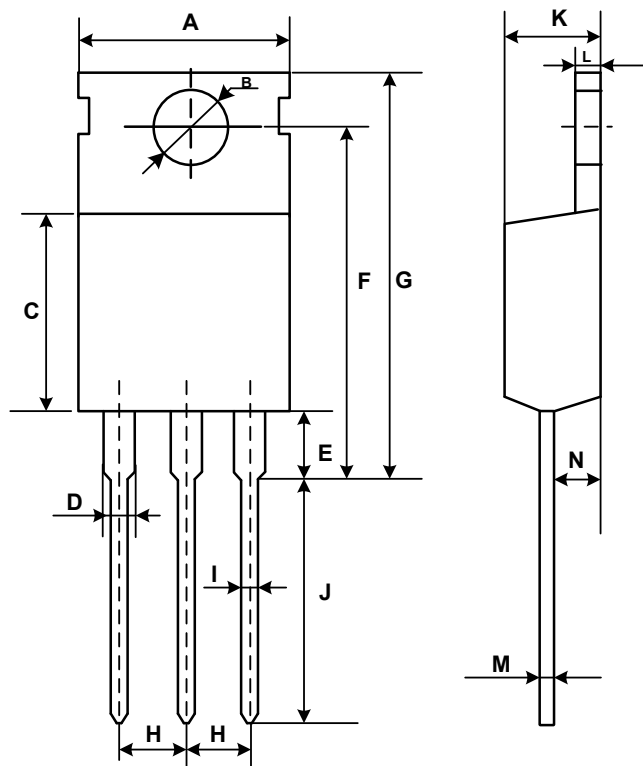
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Mechanical Dimensions for TO-220



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60