ICL7660SIPAZ-HX Super Voltage Converters

Description

The ICL7660SIPAZ-HX Super Voltage Converters are monolithic CMOS voltage-conversion ICs engineered to deliver significant performance advantages over comparable devices. They feature an extended operating supply voltage range of up to 12 V while consuming lower quiescent supply current. An integrated Frequency Boost pin enables users to achieve reduced output impedance—even when employing smaller external capacitors. Critical electrical parameters are fully specified and guaranteed across the entire commercial and industrial temperature ranges.

The ICL7660SIPAZ-HX performs efficient positive-to-negative voltage conversion for input voltages ranging from 1.5 V to 12 V, generating corresponding complementary output voltages from –1.5 V to –12 V. Only two non-critical external capacitors are required—one for the charge-pump function and one for the charge-reservoir function. Additionally, the device can be configured as a voltage doubler, delivering up to 22.8 V from a 12 V input. It also supports implementation as a voltage multiplier or voltage divider, offering versatile system-level design flexibility.

Each device integrates a series DC power-supply regulator, an RC oscillator, a voltage-level translator, and four output power MOSFET switches. The internal oscillator operates at a nominal frequency of 10 kHz when unloaded and supplied with 5.0 V. This frequency may be reduced by connecting an external capacitor to the "OSC" pin; alternatively, the oscillator can be overridden and driven synchronously by an external clock signal.

The "LV" pin may be connected to ground to bypass the internal series regulator—thereby optimizing performance under low-voltage (LV) operating conditions. For medium-to-high supply voltages (3.5 V to 12 V), the LV pin must remain unconnected (floating) to prevent device latch-up.

In some applications, an external Schottky diode from V OUT to CAP- is needed to ensure latchup free operation.Encapsulated as DIP-8

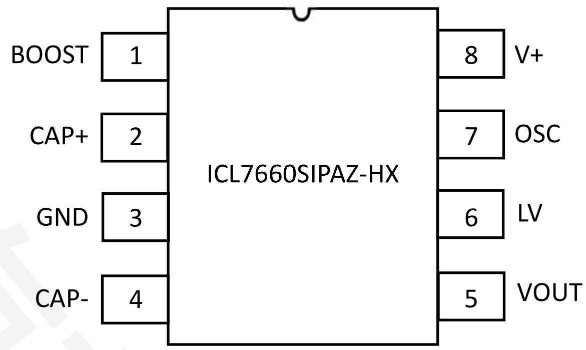
Features

- ★ Ensured Lower Max Supply Current for All Temperature Ranges
- ★ Wide Operating Voltage Range: 1.5V to 12V
- ★ 100% Tested at 3V
- ★ Boost Pin (Pin 1) for Higher Switching Frequency
- ★ Ensured Minimum Power Efficiency of 96%
- ★ Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%
- ★ Improved SCR Latchup Protection
- ★ Simple Conversion of +5V Logic Supply to ±5V Supplies
- ★ Simple Voltage Multiplication VOUT = (-)nVIN
- ★ Easy to Use; Requires Only Two External Non-Critical Passive Components
- ★ Pb-Free Available (RoHS Compliant)
- ★ Improved Direct Replacement for Industry Standard ICL7660SIPAZ-HX and Other Second Source Devices

Applications

- ★ Simple Conversion of +5V to ±5V Supplies
- ★ Voltage Multiplication VOUT = ±nVIN
- ★ Negative Supplies for Data Acquisition Systems and Instrumentation
- ★ Supply Splitter, VOUT = ±VS
- ★ RS232 Power Supplies

Pin Configurations



DIP-8

NOTES:
1. Add “-T*” suffix for tape and reel.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

Absolute Maximum Ratings

Supply Voltage	+13.0V
LV and OSC Input Voltage (Note 5)	
V+ < 5.5V	-0.3V to V+ + 0.3V
V+ > 5.5V	V+ -5.5V to V+ +0.3V
Current into LV (Note 5)	
V+ > 3.5V	20μA
Output Short Duration	
VSUPPLY ≤ 5.5V	Continuous

Thermal Information

Thermal Resistance (Typical, Notes 6, 7) θJA (°C/W) θJC (°C/W)	
Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile (Note 8)	TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:
5. Connecting any terminal to voltages exceeding V+ or falling below GND may trigger destructive latch-up. It is recommended that no input signals from externally powered sources be applied prior to powering up the ICL7660SIPAZ-HX .
6. θJA is measured with the device mounted on a low-effective-thermal-conductivity test board under free-air conditions. Refer to Technical Brief TB379 for detailed measurement methodology.
7. For θJC, the “case temperature” is defined as the temperature measured at the center of the package top surface.

Electrical Specifications (unless otherwise specified)

ICL7660SIPAZ-HX , V+ = 5V, TA = +25°C, OSC = Free running

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Supply Current (Note 11)	I+	RL = ∞, +25°C	-	80	160	µA
		0°C < TA < +70°C	-	-	180	µA
		-40°C < TA < +85°C	-	-	180	µA
		-55°C < TA < +125°C	-	-	200	µA
Supply Voltage Range - High (Note 12)	V+H	RL = 10k, LV Open, TMIN < TA < TMAX	3.0	-	12	V
Supply Voltage Range - Low	V+L	RL = 10k, LV to GND, TMIN < TA < TMAX	1.5	-	3.5	V
Output Source Resistance	ROUT	IOUT = 20mA	-	60	100	Ω
		IOUT = 20mA, 0°C < TA < +70°C	-	-	120	Ω
		IOUT = 20mA, -25°C < TA < +85°C	-	-	120	Ω
		IOUT = 20mA, -55°C < TA < +125°C	-	-	150	Ω
		IOUT = 3mA, V+ = 2V, LV = GND, 0°C < TA < +70°C	-	-	250	Ω
		IOUT = 3mA, V+ = 2V, LV = GND, -40°C < TA < +85°C	-	-	300	Ω
		IOUT = 3mA, V+ = 2V, LV = GND, -55°C < TA < +125°C	-	-	400	Ω
Oscillator Frequency (Note 10)	fOSC	COSC = 0, Pin 1 Open or GND	5	10	-	kHz
		COSC = 0, Pin 1 = V+	-	35	-	kHz
Power Efficiency	PEFF	RL = 5kΩ	96	98	-	%
		TMIN < TA < TMAX RL = 5kΩ	95	97	-	-
Voltage Conversion Efficiency	VOUTEFF	RL = ∞	99	99.9	-	%

Electrical Specifications unless otherwise specified. (Continued)

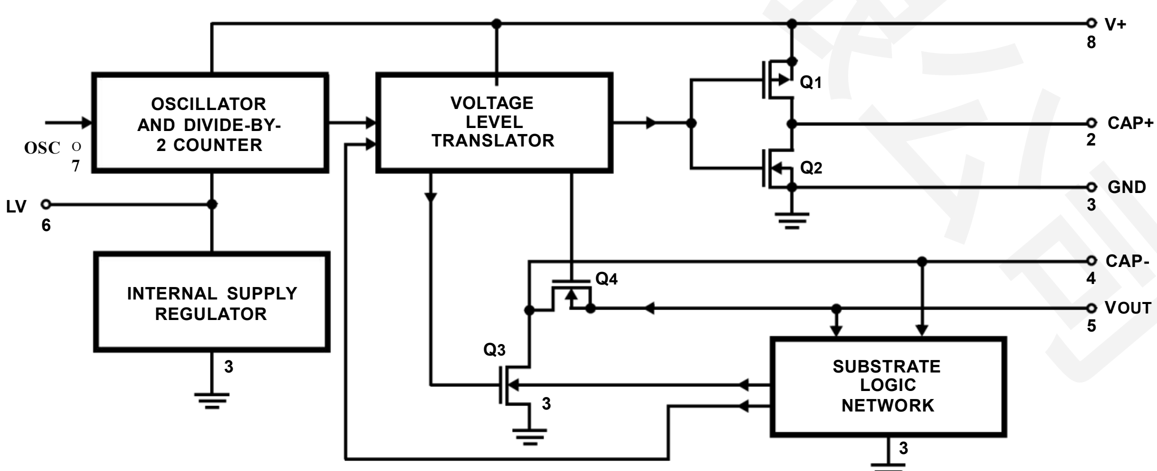
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Oscillator Impedance	ZOSC	V+ = 2V	-	1	-	MΩ
		V+ = 5V	-	100	-	kΩ
ICL7660SIPAZ-HX , V+ = 3V, TA = 25°C, OSC = Free running, Test Circuit Figure 13, unless otherwise specified						
Supply Current (Note 13)	I+	V+ = 3V, RL = ∞, +25°C	-	26	100	μA
		0°C < TA < +70°C	-	-	125	μA
		-40°C < TA < +85°C	-	-	125	μA
Output Source Resistance	ROUT	V+ = 3V, IOUT = 10mA	-	97	150	Ω
		0°C < TA < +70°C	-	-	200	Ω
		-40°C < TA < +85°C	-	-	200	Ω
Oscillator Frequency (Note 13)	fOSC	V+ = 3V (same as 5V conditions)	5.0	8	-	kHz
		0°C < TA < +70°C	3.0	-	-	kHz
		-40°C < TA < +85°C	3.0	-	-	kHz

ICL7660SIPAZ-HX , V+ = 5V, TA = +25°C, OSC = Free running

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, on the order of 5pF.
11. The ICL7660SIPAZ-HX can operate without an external diode over the full temperature and voltage range. This device will function in existing designs that incorporate an external diode with no degradation in overall circuit performance.
12. All significant improvements over the industry standard ICL7660SIPAZ-HX are highlighted.
13. Derate linearly above 50°C by 5.5mW/°C.

Functional Block Diagram



Typical Performance Curves

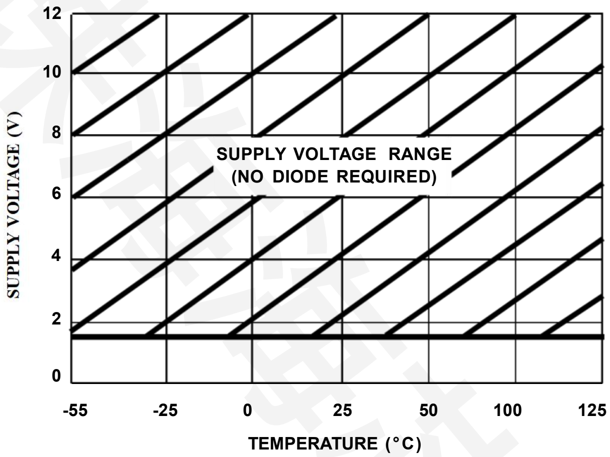


FIGURE 1. OPERATING VOLTAGE ASA FUNCTION OF TEMPERATURE

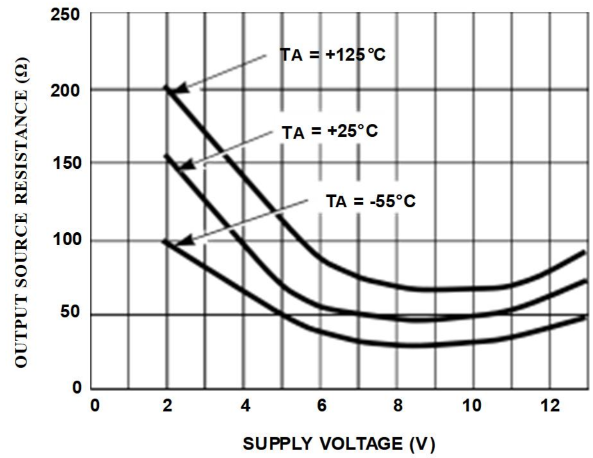


FIGURE 2.OUTPUT SOURCE RESISTANCE ASA FUNCTION OF SUPPLY VOLTAGE

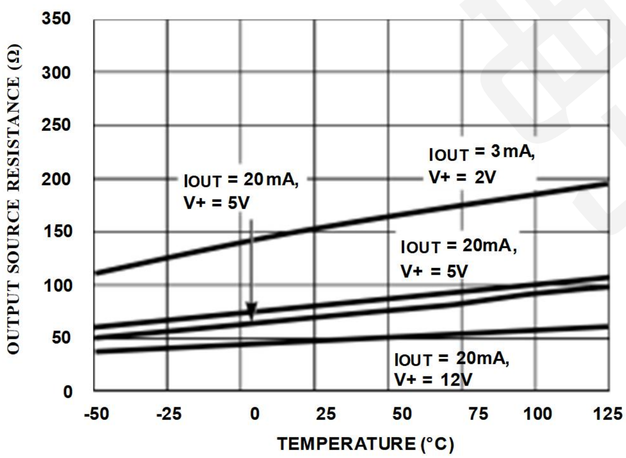


FIGURE 3. OUTPUT SOURCE RESISTANCE ASA FUNCTION OF TEMPERATURE

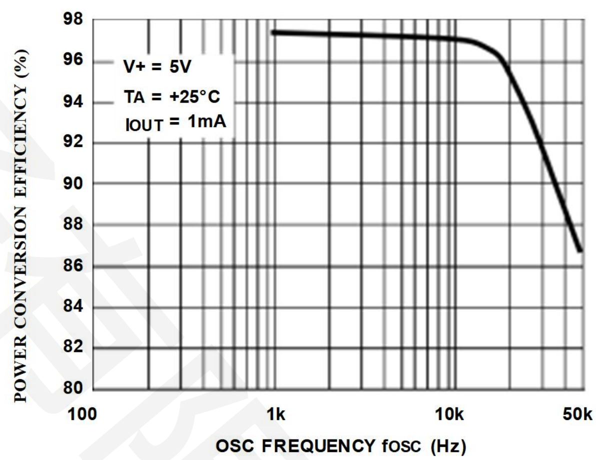


FIGURE 4. POWER CONVERSION EFFICIENCY ASA FUNCTION OF OSCILLATOR FREQUENCY

Typical Performance Curves

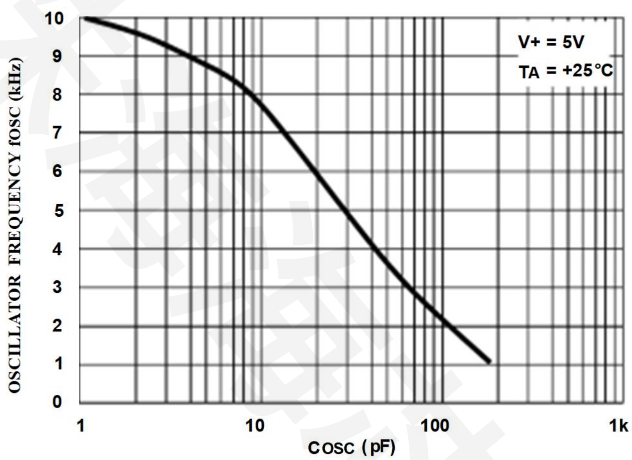


FIGURE 5. FREQUENCY OF OSCILLATION ASA FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE

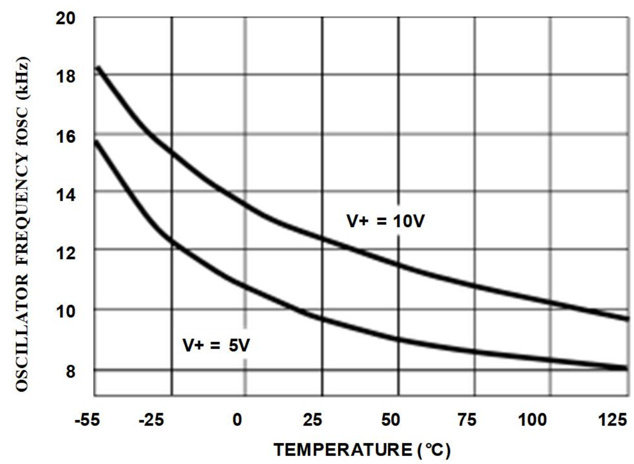


FIGURE 6. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

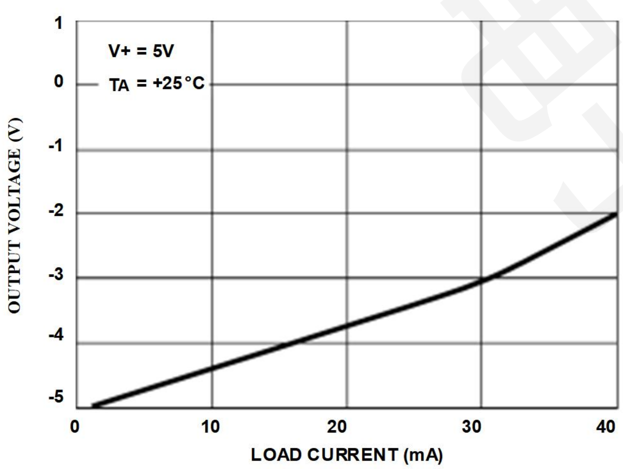


FIGURE 7. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

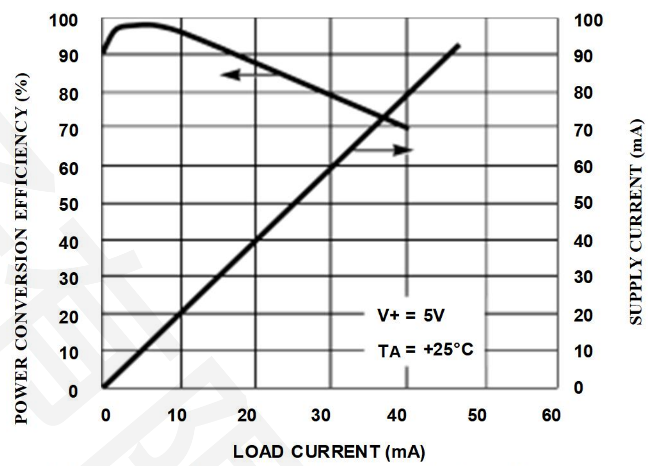


FIGURE 8. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

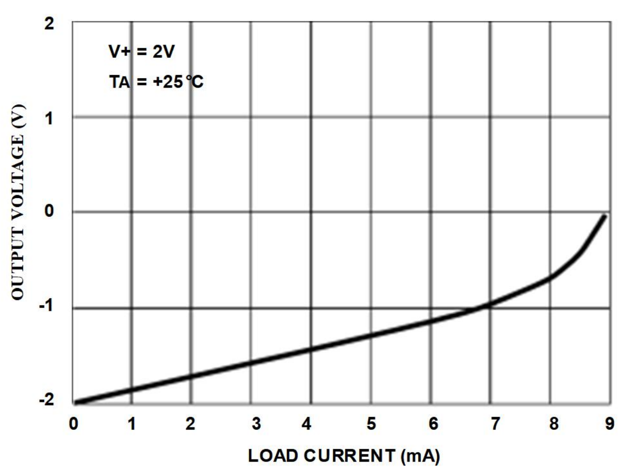


FIGURE 9. OUTPUT VOLTAGE ASA FUNCTION OF OUTPUT CURRENT

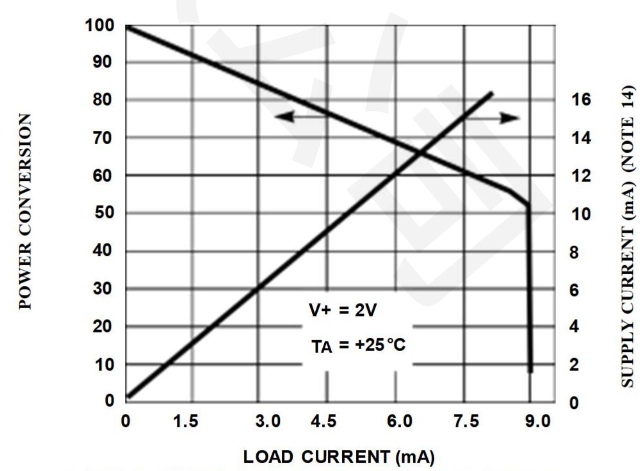


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY ASA FUNCTION OF LOAD CURRENT

Typical Performance Curves

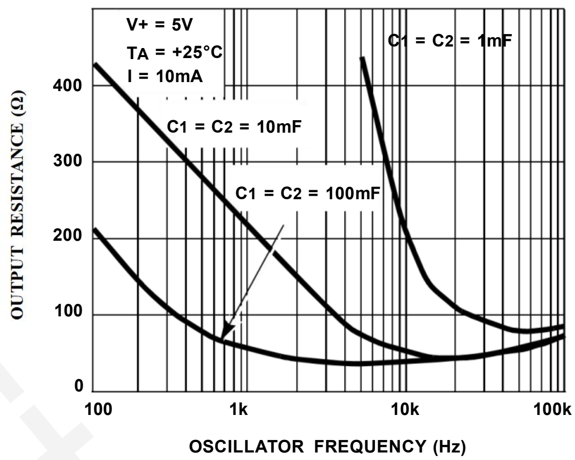
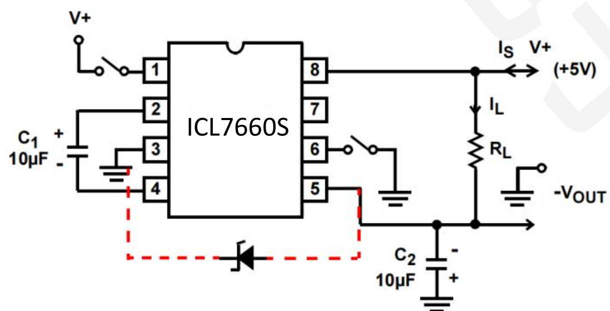


FIGURE 11. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY

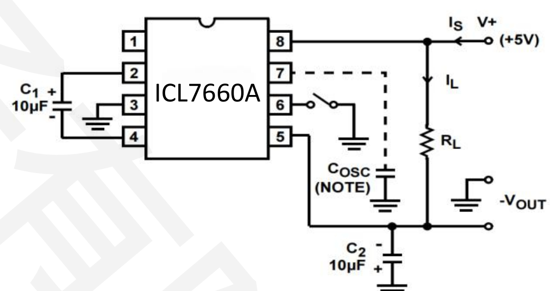
NOTE:

14. These curves include, in the supply current, that current fed directly into the load RL from the V+ (see Figure 12). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660SIPAZ-HX , goes to the negative side of the load. Ideally, VOUT $\simeq$ 2VIN, IS $\simeq$ 2IL, so VIN x IS $\simeq$ VOUT x IL.



NOTE: For large values of COSC (>1000pF), the values of C1 and C2 should be increased to 100μF.

FIGURE 12. ICL7660S TEST CIRCUIT



NOTE: For large values of COSC (>1000pF) the values of C1 and C2 should be increased to 100μF.

FIGURE 13. ICL7660A TEST CIRCUIT

Detailed Description

The ICL7660SIPAZ-HX contain all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors, which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may best be understood by considering Figure 14, which shows an idealized negative voltage converter. Capacitor C1 is charged to a voltage, V+, for the half cycle, when switches S1 and S3 are closed. (Note: Switches S2 and S4 are open during this half cycle). During the second half cycle of operation, switches S2and S4are closed, with S1 and S3 open, thereby shifting capacitor C1 to C2 such that the voltage on C2 is exactly V+, assuming ideal switches and no load on C2. The ICL7660SIPAZ-HX approach this ideal situation more closely than existing non-mechanical circuits.

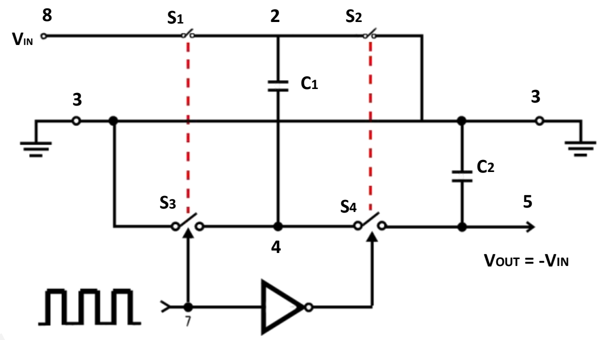


FIGURE 14. IDEALIZED NEGATIVE VOLTAGE CONVERTER

In the ICL7660SIPAZ-HX , the four switches of Figure 14 are MOS power switches; S1 is a P-Channel device; and S2, S_3 and S4 are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S4 must always remain reverse biased with respect to their sources, but not so much as to degrade their “ON”resistances. In addition, at circuit start-up, and under output short circuit conditions (VOUT = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latch-up.

This problem is eliminated in the ICL7660SIPAZ-HX by a logic network that senses the output voltage (VOUT) together with the level translators, and switches the substrates of S_3 and S4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660SIPAZ-HX is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation, the “LV” pin should be connected to GND, thus disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latchup-proof operation and to prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedance of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660SIPAZ-HX approach these conditions for negative voltage conversion if large values of C1 and C2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS**. The energy lost is defined as shown in Equation 1

$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2) \quad \text{(EQ. 1)}$$

where V1 and V2 are the voltages on C1 during the pump and transfer cycles. If the impedances of C1 and C2 are relatively high at the pump frequency (see Figure 14) compared to the value of RL, there will be a substantial difference in the

voltages, V1 and V2. Therefore it is not only desirable to make C2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C1 in order to achieve maximum efficiency of operation.

Do’s and Don’ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GND for supply voltage greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C1 must be connected to pin 2 of the ICL7660SIPAZ-HX , and the + terminal of C2 must be connected to GND.
5. If the voltage supply driving the ICL7660SIPAZ-HX has a large source impedance (25Ω to 30Ω), then a 2.2μF capacitor from pin 8 to ground may be required to limit the rate of rise of input voltage to less than 2V/μs.
6. If the input voltage is higher than 5V and it has a rise rate more than 2V/μs, an external Schottky diode from VOUT to CAP- is needed to prevent latchup (triggered by forward biasing Q4’s body diode) by keeping the output (pin 5) from going more positive than CAP- (pin 4).
7. User should ensure that the output (pin 5) does not go more positive than GND (pin 3). Device latch-up will occur under these conditions. To provide additional protection, a 1N914 or similar diode placed in parallel with C2 will prevent the device from latching up under these conditions, when the load on VOUT creates a path to pull up VOUT before the IC is active (anode pin 5, cathode pin 3).

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660SIPAZ-HX for generation of negative supply voltages. Figure 15 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltage below 3.5V.

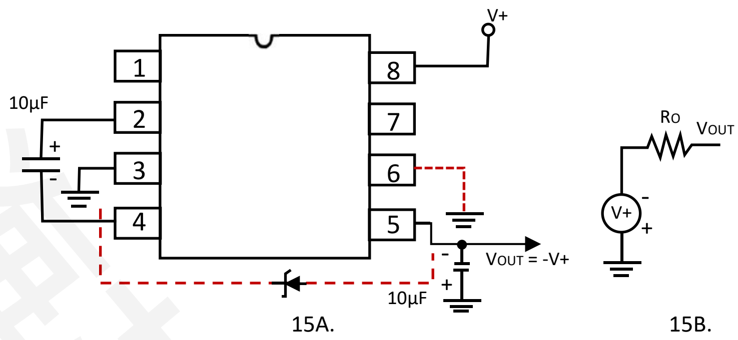


FIGURE 15. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

The output characteristics of the circuit in Figure 15 can be approximated by an ideal voltage source in series with aresistance as shown in Figure 15B. The voltage source has a value of -(V+). The output impedance (RO) is a function of the ON resistance of the internal MOS switches (shown in Figure 14), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R O is shown in Equation 2:

$$R_0 \cong 2((R_{SW1}+R_{SW3}+ESR_{C1}) + 2(R_{SW2}+R_{SW4}+ESR_{C1}))\frac{1}{f_{PUMP}\times C_1} + ESR_{C2} \quad \text{(EQ. 2)}$$

$$f_{PUMP} = \frac{f_{OSC}}{2} \quad (R_{SWX} = \text{MOSFET Switch Resistance})$$

Combining the four RSWX terms as RSW, we see in Equation 3 that:

$$R_0 \cong 2xR_{SW} + \frac{1}{f_{PUMP}\times C_1} + 4xESR_{C1} + ESR_{C2} \quad \text{(EQ. 3)}$$

RSW, the total switch resistance, is a function of supply voltage and temperature (see the output source resistance graphs, Figures 2, 3, and 11), typically 23Ω at +25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the 1/(fPUMP x C1) component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the 1/(fPUMP x C1) term, but may have the side effect of a net increase in output impedance when C1 > 10μF and is not long enough to fully charge the capacitors every cycle.

Equation 4 shows a typical application where fOSC = 10kHz and C = C1 = C2 = 10μF:

$$R_0 \cong 2x23 + \frac{1}{5\times10^3\times10\times10^{-6}} + 4xESR_{C1} + ESR_{C2} \quad \text{(EQ. 4)}$$

$$R_0 \cong 46 + 20 + 5 \times ESR_C$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low 1/fPUMP x C1 term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The peak-to-peak output ripple voltage is given by Equation 5:

$$V_{RIPPLE} \equiv \left(\frac{1}{2 \times f_{PUMP} \times C_2} + 2 ESR_{C2} \times I_{OUT}\right) \qquad \text{(EQ. 5)}$$

A low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7660SIPAZ-HX voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C2, serves all devices, while each device requires its own pump capacitor, C1. The resultant output resistance is approximated in Equation 6:

$$R_{OUT} = \frac{R_{OUT(of\ ICL7660S)}}{n(\text{number of devices})} \qquad \text{(EQ. 6)}$$

Cascading Devices

The ICL7660SIPAZ-HX may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined as shown in Equation 7:

$$V_{OUT} = -n(V_{IN}) \qquad \text{(EQ. 7)}$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660SIPAZ-HX ROUT values.

Changing the ICL7660SIPAZ-HX Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods.

By connecting the Boost Pin (Pin 1) to V+, the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately 3.5 times. The result is a decrease in the output impedance and ripple. This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, such as 0.1µF, can be used in conjunction with the Boost Pin to achieve similar output currents compared to the device free running with C1 = C2 = 10µF or 100µF. (see Figure 11).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 16. In order to prevent device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pull-up resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be one-half of the clock frequency. Output transitions occur on the positive going edge of the clock.

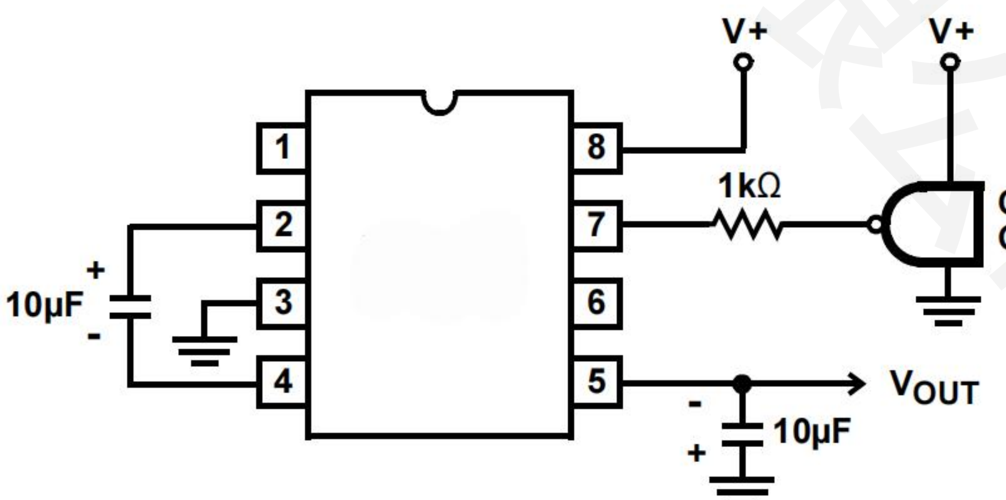


FIGURE 16. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660SIPAZ-HX at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 17. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C1) and reservoir (C2) capacitors; this is overcome by increasing the values of C1 and C2 by the same factor by which the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC and V+) will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C1 and C2 (from 10µF to 100µF).

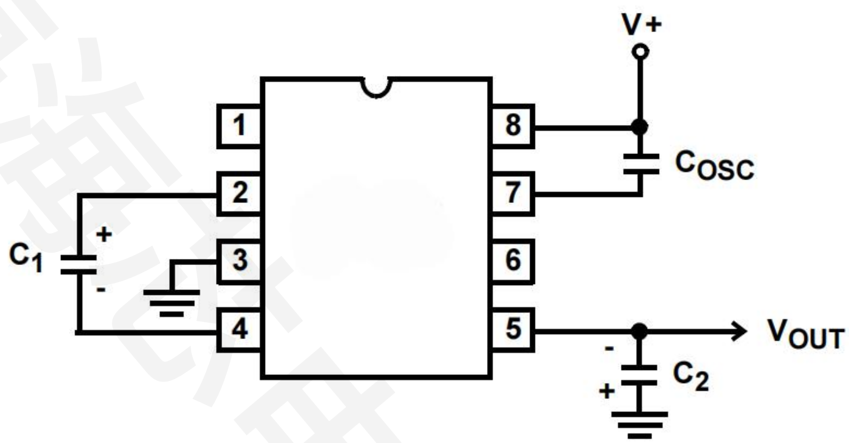
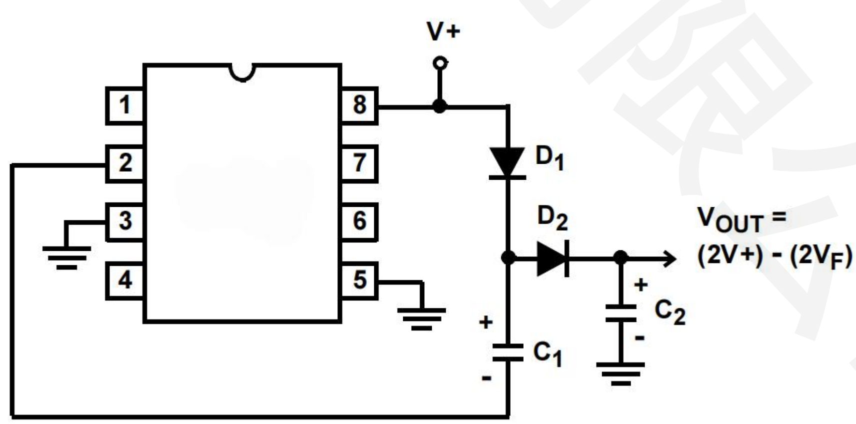


FIGURE 17. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7660SIPAZ-HX may be employed to achieve positive voltage doubling using the circuit shown in Figure 18. In this application, the pump inverter switches of the ICL7660SIPAZ-HX are used to charge C1 to a voltage level of V+ -VF, where V+ is the supply voltage and VF is the forward voltage on C1, plus the supply voltage (V+) is applied through diode D2to capacitor C2. The voltage thus created on C2 becomes (2V+) - (2VF) or twice the supply voltage minus the combined forward voltage drops of diodes D1 and D2.

The source impedance of the output (VOUT) will depend on the output current, but for V+ = 5V and an output current of 10mA, it will be approximately 60Ω.



NOTE: D1 AND D2 CAN BE ANY SUITABLE DIODE.

FIGURE 18. POSITIVE VOLTAGE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 19 combines the functions shown in Figure 15 and Figure 18 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be suitable, for example, for generating +9V and -5V from an existing +5V supply. In this instance, capacitors C1 and C_3 perform the pump and reservoir functions, respectively, for negative voltage generation, while capacitors C2 and C4 are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher, due to the finite impedance of the common charge pump driver at pin 2 of the device.

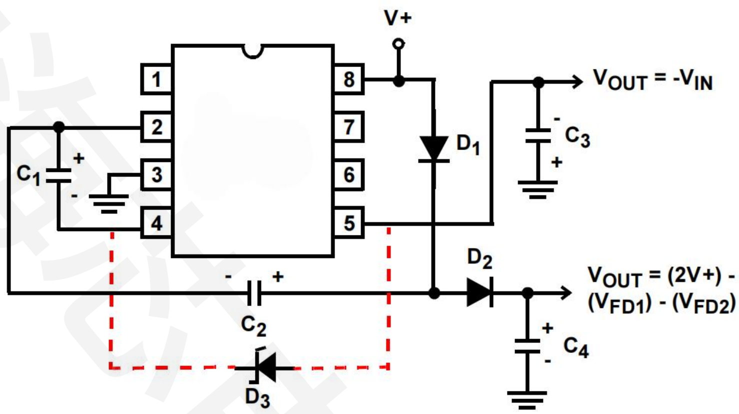


FIGURE 19. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a high supply in half, as shown in Figure 20. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 15, +15V can be converted, via +7.5 and -7.5, to a nominal -15V, although with rather high series output resistance (~250Ω).

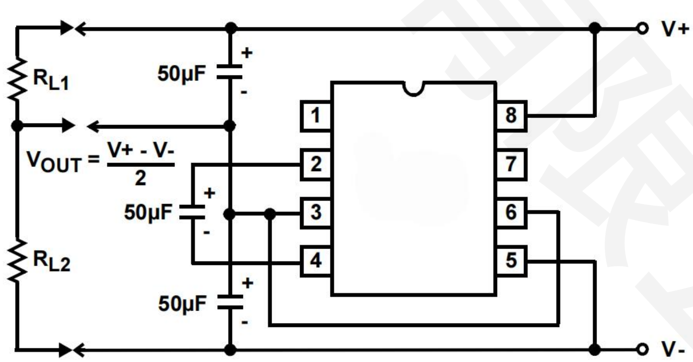


FIGURE 20. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660SIPAZ-HX can be a problem, particularly if the load current varies substantially. The circuit of Figure 21 can be used to overcome this by controlling the input voltage, via an ICL7611-HX low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660SIPAZ-HX output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660SIPAZ-HX , while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provide an output impedance of less than 5Ω to a load of 10mA.

Other Applications

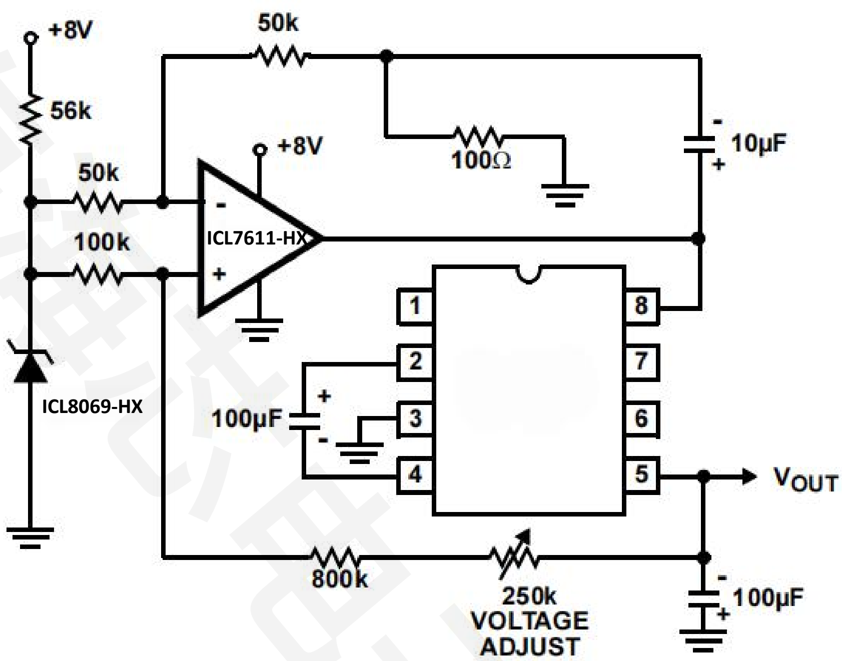
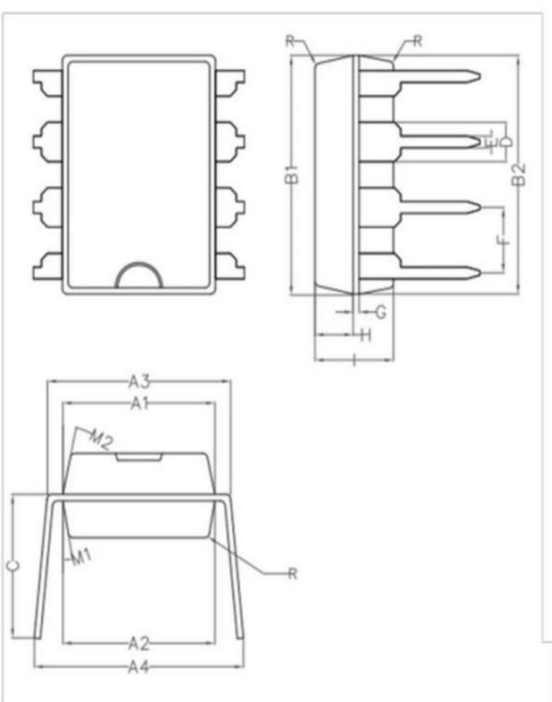


FIGURE 21. REGULATING THE OUTPU VOLTAGE

Packaging

DIP-8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°