

# CSNP512GCR01-AOW

Version: V1.0

Apr3, 2025



**Revision History**

| Version | Date     | Description  |
|---------|----------|--------------|
| V1.0    | 4/3/2025 | Origin Draft |



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## **1. Introduction**

### **1.1 Overview**

CSNP512GCR01-AOW is an 512Gb density of embedded storage based on NAND Flash and SD controller. This product has many advantages comparing to raw NAND, it has embedded bad block management, and stronger embedded ECC. Even on abnormal power down it keep your data safely.

CSNP512GCR01-AOW is LGA-16 package. The size is 9mm x 13mm x0.88mm.

### **1.2 Features**

- Interface: Fully compliant with the standards released by the SD Card Association
- The Command List: Part 1 Physical Layer Specification Ver6.10 Final
- Power supply: Vcc = 2.7V - 3.6V
- Operating Temperature: -25°C to +85°C
- Storage Temperature: -55°C to +125°C
- Standby Current: < 100uA
- Support SD SPI mode
- Bus Speed Mode (use 4 parallel data lines)
  - Non-UHS Mode
    - ◆ Defaultspeedmode:3.3V signaling, frequency up to25MHz, up to12.5MB/sec
    - ◆ Highspeedmode:3.3V signaling, frequency up to50MHz, up to25MB/sec
  - UHS Mode
    - ◆ SDR12:1.8V signaling, frequency up to25MHz, up to12.5MB/sec
    - ◆ SDR25:1.8V signaling, frequency up to50MHz, up to25MB/sec
    - ◆ SDR50:1.8V signaling, frequency up to100MHz, up to50MB/sec
    - ◆ SDR104:1.8V signaling, frequency up to208MHz, up to104MB/sec
    - ◆ DDR50:1.8Vsignaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/sec
- Correction of memory field errors
- Copyrights Protection Mechanism
- Password Protection of SDNAND
- Built-in write protection features (permanent and temporary)
- Application specific commands
- Comfortable erase mechanism

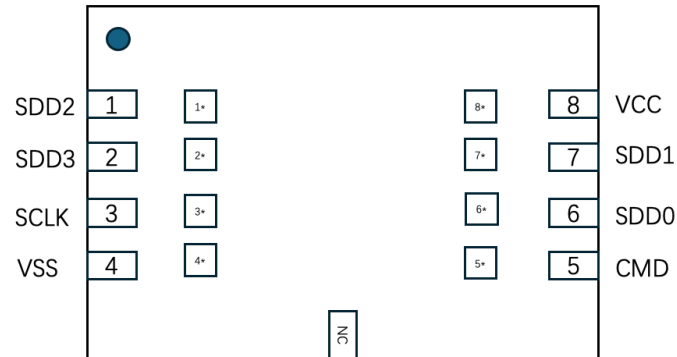


The diagram illustrates the Memory core interface. At the top is the **Memory core** (hatched box). Below it is the **Memory core interface** block, which contains a **Reset** signal and a **Controller** block. The **Controller** block is connected to the **Memory core** via a bidirectional arrow. The **Controller** block is also connected to a **Power on Detection** block via a bidirectional arrow. The **Controller** block has five output lines to the right: **SCR**, **CSD**, **DSR**, **RCA**, **CID**, and **OCR**. The **Controller** block has three input lines from below: **DAT0**, **CLK**, and **VSS**. The **Controller** block has two output lines to the right: **VCC** and **CMD**. The **Controller** block has two output lines to the right: **CD/DAT3** and **DAT2**. The **Controller** block has two output lines to the right: **DAT1** and **DAT0**. The **Controller** block has two output lines to the right: **DAT1** and **DAT0**. The **Controller** block has two output lines to the right: **DAT1** and **DAT0**.



## 2. Product Specifications

### 2.1 Pin Assignments (Top View)

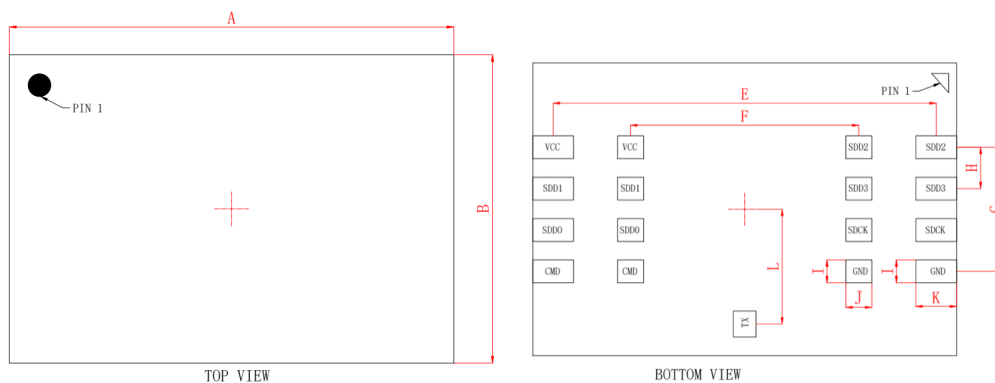


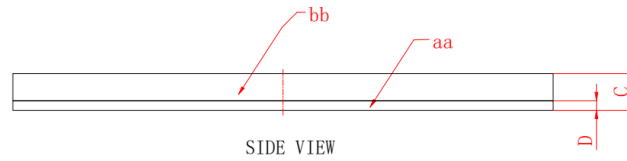
| PIN# | SD MODE              |                     |                                    | SPI MODE |                |                        |
|------|----------------------|---------------------|------------------------------------|----------|----------------|------------------------|
|      | NAME                 | TYPE <sup>1</sup>   | DESCRIPTION                        | NAME     | TYPE           | DESCRIPTION            |
| 1    | SDD2                 | I/O/PP              | Data Line [Bit2]                   | RSV      |                | Reserved               |
| 2    | CD/SDD3 <sup>2</sup> | I/O/PP <sup>3</sup> | SDNAND Detect/<br>Data Line [Bit3] | CS       | I <sup>3</sup> | Chip Select (Neg True) |
| 3    | SCLK                 | I                   | Clock                              | SCLK     | I              | Clock                  |
| 4    | VSS                  | S                   | Supply Voltage Ground              | VSS      | S              | Supply Voltage Ground  |
| 5    | CMD                  | PP                  | Command/Response                   | DI       | I              | Data In                |
| 6    | SDD0                 | I/O/PP              | Data Line [Bit0]                   | DO       | O/PP           | Data Out               |
| 7    | SDD1                 | I/O/PP              | Data Line [Bit1]                   | RSV      |                | Reserved               |
| 8    | VCC                  | S                   | Supply Voltage                     | VCC      | S              | Supply Voltage         |

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;

2) The extended SDD lines (SDD1-SDD3) are input on power up. They start to operate as SDD lines after SET\_BUS\_WIDTH command. The Host shall keep its own SDD1-SDD3 lines in input mode, as well, while they are not used. It is defined so, to keep compatibility to SDNAND.

### 2.2 Package Dimensions





| COMMON DIMENSIONS             |            |       |       |
|-------------------------------|------------|-------|-------|
| (UNITS OF MEASURE=MILLIMETER) |            |       |       |
| SYMBOL                        | MILLIMETER |       |       |
|                               | MIN        | NOM   | MAX   |
| A                             | 12.90      | 13.00 | 13.10 |
| B                             | 8.90       | 9.00  | 9.10  |
| C                             | 0.83       | 0.88  | 0.93  |
| D                             | 0.21       | 0.23  | 0.25  |
| E                             | 11.65      | 11.75 | 11.85 |
| F                             | 6.90       | 7.00  | 7.10  |
| G                             | 3.76       | 3.81  | 3.86  |
| H                             | 1.22       | 1.27  | 1.32  |
| I                             | 0.65       | 0.70  | 0.75  |
| J                             | 0.75       | 0.80  | 0.85  |
| K                             | 1.20       | 1.25  | 1.30  |
| L                             | 3.43       | 3.53  | 3.63  |
| aa                            | Substrate  |       |       |
| bb                            | Compound   |       |       |

SDNAND Package Dimensions (unit: mm)



### 3. Performance

| Test Item                    | Test Mode               | Result |
|------------------------------|-------------------------|--------|
| Crystal Disk Mark (1MB Q8T1) | Sequential Read (MB/s)  | 86.97  |
|                              | Sequential Write (MB/s) | 35.61  |
| ATTO (Direct IO 64KB)        | Sequential Read (MB/s)  | 91.09  |
|                              | Sequential Write (MB/s) | 76.47  |
| H2test                       | Sequential Read (MB/s)  | 57.4   |
|                              | Sequential Write (MB/s) | 29.8   |

| Parameter   | Range         |                           |
|-------------|---------------|---------------------------|
| Temperature | Work Model    | -25° ~ 85°C               |
|             | Storage Model | -55° ~ 125°C              |
| Humidity    | Work Model    | 8% to 95%, Non-condensing |
|             | Storage Model | 8% to 95%, Non-condensing |



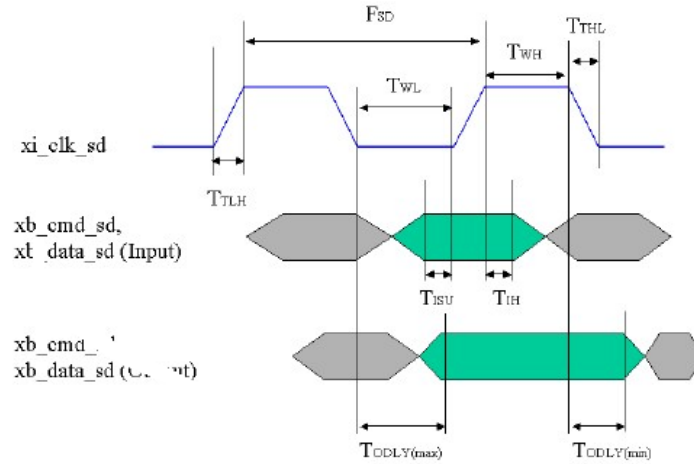
#### **4. DC Characteristics**

| Symbol            | PARAMETER                        | CONDITIONS                                     | MIN                  | TYP  | MAX                  | UNITS |
|-------------------|----------------------------------|------------------------------------------------|----------------------|------|----------------------|-------|
| V <sub>IL</sub>   | Input low voltage                |                                                | V <sub>SS</sub> -0.3 |      | 0.25V <sub>CC</sub>  | V     |
| V <sub>IH</sub>   | Input high voltage               |                                                | 0.625V <sub>CC</sub> |      | V <sub>CC</sub> +0.3 | V     |
| V <sub>OL</sub>   | Output low voltage               | I <sub>OL</sub> =100μA<br>@V <sub>CC_min</sub> |                      |      | 0.125V <sub>CC</sub> | V     |
| V <sub>OH</sub>   | Output high voltage              | I <sub>OH</sub> =100μA<br>@V <sub>CC_min</sub> | 0.75V <sub>CC</sub>  |      |                      | V     |
| I <sub>IN</sub>   | Input leakage current            | V <sub>IN</sub> =V <sub>CC</sub> or 0          | -10                  | +/-1 | 10                   | μA    |
| I <sub>OUT</sub>  | Tri-state output leakage current |                                                | -10                  | +/-1 | 10                   | μA    |
| I <sub>STBY</sub> | Standby current                  | 3.3V@clock stop                                |                      | 80   | 150                  | μA    |
| I <sub>OP</sub>   | Operation current                | 3.3v@30MB/S<br>(Write)                         |                      | 50   | 70                   | mA    |
|                   |                                  | 3.3v@25Mhz<br>(Write)                          |                      | 18   | 25                   | mA    |
|                   |                                  | 3.3v@70MB/S<br>(Read)                          |                      | 50   | 60                   | mA    |
|                   |                                  | 3.3v@25Mhz<br>(Read)                           |                      | 20   | 30                   | mA    |



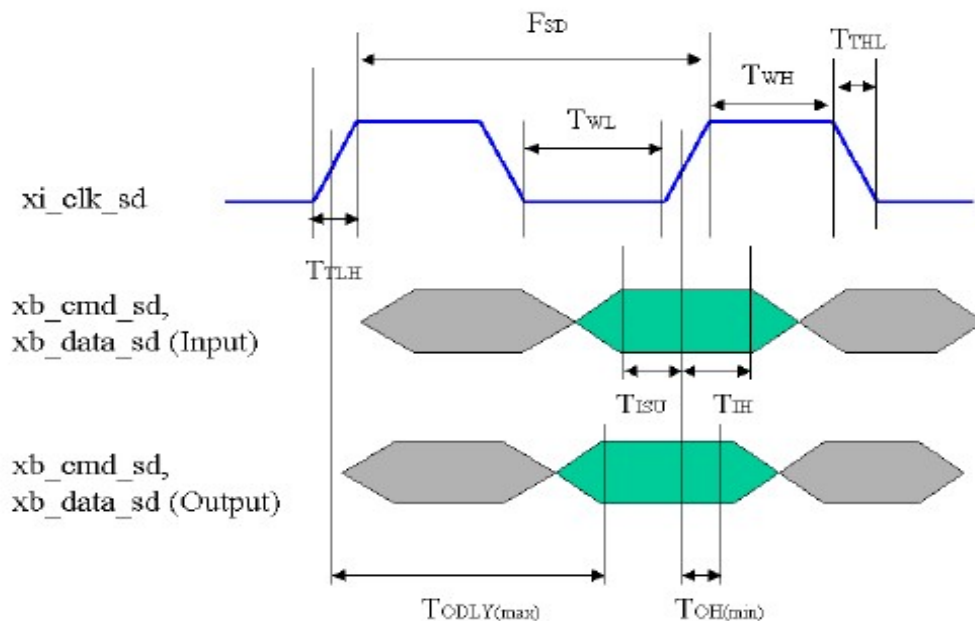
## 5. AC Characteristics

### 5.1 Bus Timing (Default Mode)



| SYMBOL     | PARAMETER          | MIN | MAX | UNIT | NOTE |
|------------|--------------------|-----|-----|------|------|
| $F_{SD}$   | SD clock frequency | 0   | 25  | MHz  |      |
| $T_{WL}$   | Clock low time     | 10  |     | ns   |      |
| $T_{WH}$   | Clock high time    | 10  |     | ns   |      |
| $T_{TLH}$  | Clock rise time    |     | 10  | ns   |      |
| $T_{THL}$  | Clock fall time    |     | 10  | ns   |      |
| $T_{ISU}$  | Input setup time   | 5   |     | ns   |      |
| $T_{IH}$   | Input hold time    | 5   |     | ns   |      |
| $T_{ODLY}$ | Output delay time  | 0   | 14  | ns   |      |

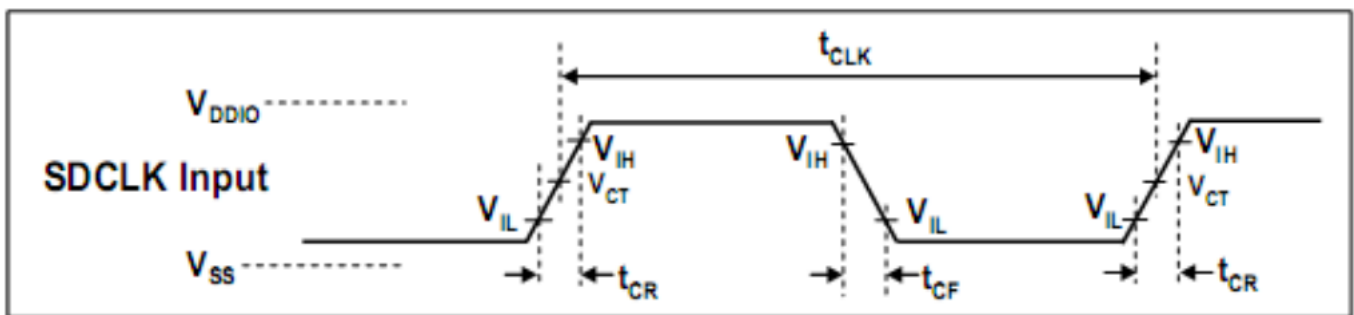
### 5.2 Bus Timing (High-speed Mode)





| SYMBOL     | PARAMETER          | MIN | MAX | UNIT | NOTE |
|------------|--------------------|-----|-----|------|------|
| $F_{SD}$   | SD clock frequency | 0   | 50  | MHz  |      |
| $T_{WL}$   | Clock low time     | 10  |     | ns   |      |
| $T_{WH}$   | Clock high time    | 10  |     | ns   |      |
| $T_{TLH}$  | Clock rise time    |     | 10  | ns   |      |
| $T_{THL}$  | Clock fall time    |     | 10  | ns   |      |
| $T_{ISU}$  | Input setup time   | 5   |     | ns   |      |
| $T_{IH}$   | Input hold time    | 5   |     | ns   |      |
| $T_{ODLY}$ | Output delay time  | 0   | 14  | ns   |      |
| $T_{OH}$   | Output hold time   | 2.5 |     | ns   |      |

### 5.3 Bus Timing (SDR12, SDR25, SDR50 and SDR104 Modes)



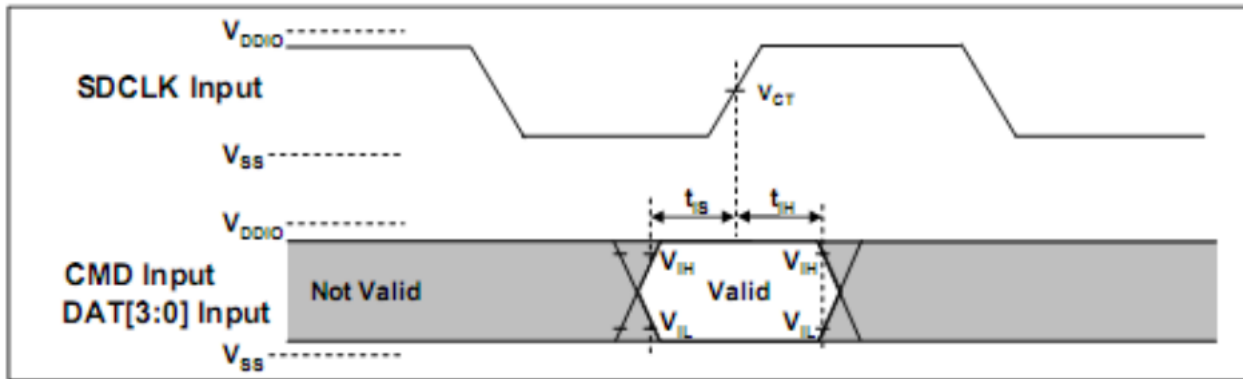
Clock signal timing

| Symbol           | Min  | Max                 | Unit | Remark                                                                                                                                                                                          |
|------------------|------|---------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $t_{CLK}$        | 4.80 |                     |      | 208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$                                                                                                                                           |
| $t_{CR}, t_{CF}$ |      | $0.2 \cdot t_{CLK}$ |      | $t_{CR}, t_{CF} < 0.96ns$ (max.) at 208MHz, $Q_{ARD} = 10pF$<br>$t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $Q_{ARD} = 10pF$<br>Value of $t_{CR}, t_{CF}$ is lons regardless of clock frequency |
| Clock Duty       | 30   | 70                  |      |                                                                                                                                                                                                 |

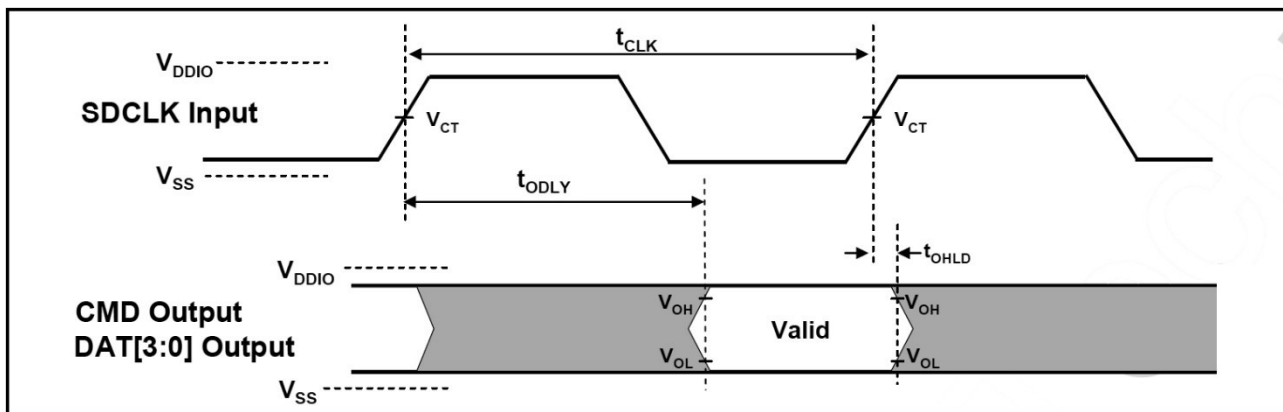
Clock Signal Timing



## SDR50 and SDR104 Input Timing



Card input timing

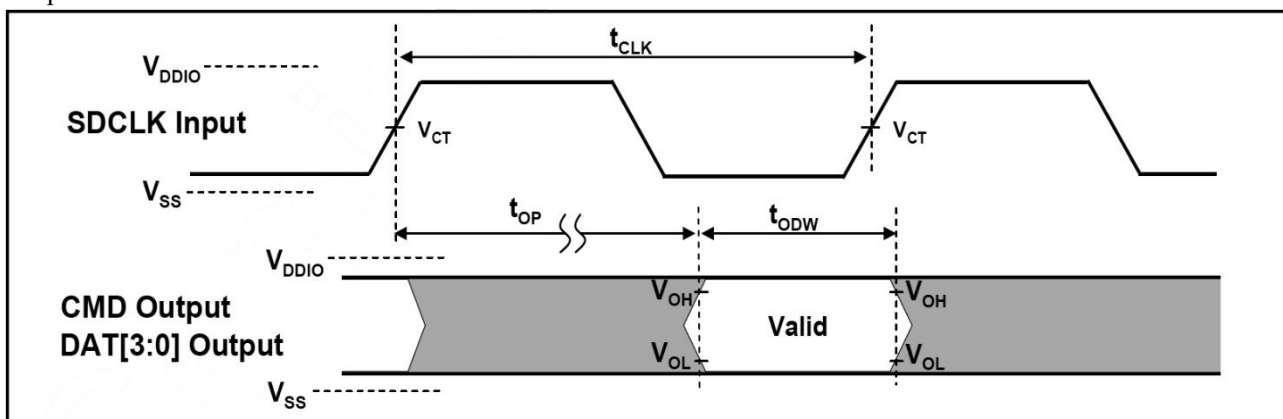


Output timing of Fixed Data window

| Symbol            | Min | Max | Unit | Remark                                                                        |
|-------------------|-----|-----|------|-------------------------------------------------------------------------------|
| t <sub>ODLY</sub> | -   | 7.5 | ns   | t <sub>CLK</sub> ≥ 10.0ns, CL=30pF, using driver Type B, for SDR50            |
| t <sub>ODLY</sub> | -   | 14  | ns   | t <sub>CLK</sub> ≥ 20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12, |
| TOH               | 1.5 | -   | ns   | Hold time at the t <sub>ODLY</sub> (min.), CL=15pF                            |

Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

## Output (SDR 104 mode)



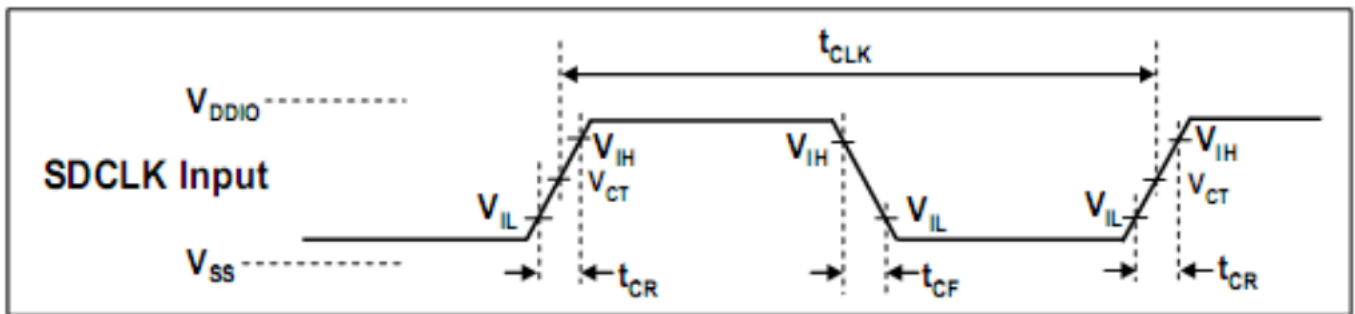
Output timing of Variable Data window



| Symbol       | Min  | Max   | Unit | Remark                                                |
|--------------|------|-------|------|-------------------------------------------------------|
| tOP          | 0    | 2     | UI   | Card Output Phase                                     |
| $\Delta tOP$ | -350 | +1550 | ps   | Delay variable due to temperature change after tuning |
| tODW         | 0.60 | -     | UI   | tODW = 2.88ns at 208MHz                               |

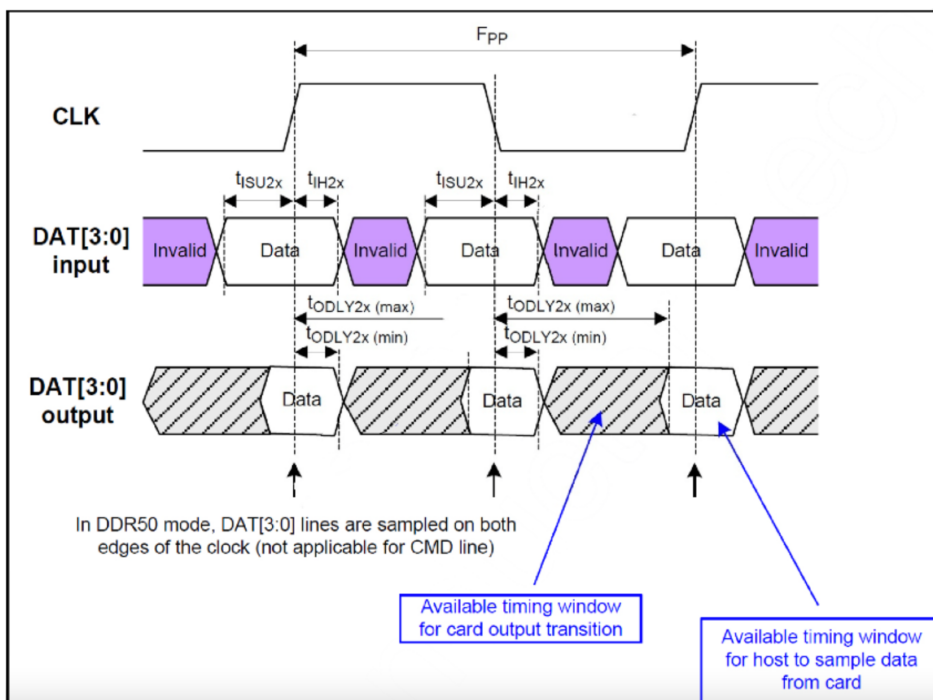
Output Timing of Variable Window (SDR104)

## Bus Timing (DDR50 Mode)



Clock Signal Timing

| Symbol     | Min | Max        | Unit | Remark                                       |
|------------|-----|------------|------|----------------------------------------------|
| tCLK       | 20  |            | ns   | 50MHz (Max.), Between rising edge            |
| tCR, tCF   |     | 0.2 * tCLK |      | tCR, tCF < 4.00ns (max.) at 50MHz, QARD=10pF |
| Clock Duty | 45% | 55%        |      |                                              |





Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode Table

| Parameter                                                       | Symbol  | Min | Max  | Unit | Remark                    |
|-----------------------------------------------------------------|---------|-----|------|------|---------------------------|
| <b>Input CMD (referenced to CLK rising edge)</b>                |         |     |      |      |                           |
| Input set-up time                                               | tISU    | 3   | -    | ns   | Ccard ≤ 10 pF<br>(1 card) |
| Input hold time                                                 | tIH     | 0.8 | -    | ns   | Ccard ≤ 10 pF<br>(1 card) |
| <b>Output CMD (referenced to CLK rising edge)</b>               |         |     |      |      |                           |
| Output Delay time during Data Transfer Mode                     | tODLY   |     | 13.7 | ns   | CL ≤ 30 pF<br>(1 card)    |
| Output Hold time                                                | TOH     | 1.5 | -    | ns   | CL ≥ 15 pF<br>(1 card)    |
| <b>Inputs DAT (referenced to CLK rising and falling edges)</b>  |         |     |      |      |                           |
| Input set-up time                                               | tISU2x  | 3   | -    | ns   | Ccard ≤ 10 pF<br>(1 card) |
| Input hold time                                                 | tIH2x   | 0.8 | -    | ns   | Ccard ≤ 10 pF<br>(1 card) |
| <b>Outputs DAT (referenced to CLK rising and falling edges)</b> |         |     |      |      |                           |
| Output Delay time during Data Transfer Mode                     | tODLY2x | -   | 7.0  | ns   | CL ≤ 25 pF<br>(1 card)    |
| Output Hold time                                                | TOH2x   | 1.5 | -    | ns   | CL ≥ 15 pF<br>(1 card)    |

Bus Timings – Parameters Values (DDR50 Mode)

## 6. SDNAND Initialization

After the bus is activated the host starts SDNAND initialization and identification process. The initialization process starts with SD\_SEND\_OP\_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports High Capacity SDNAND. The HCS (Host Capacity Support) bit set to 0 indicates that the host does not support High Capacity SDNAND.

Receiving of CMD8 expands the ACMD41 function; HCS in the argument and CCS (SDNAND Capacity Status) in the response. HCS is ignored by SDNANDs, which didn't respond to CMD8. However, the host should set HCS to 0 if the SDNAND returns no response to CMD8. Standard Capacity SDNAND ignores HCS. If HCS is set to 0, High Capacity SDNAND never return ready statue (keep busy bit to 0). The busy bit in the OCR is used by the SDNAND to inform the host that initialization of ACMD41 is completed. Setting the busy bit to 0 indicates that the SDNAND is still initializing. Setting the busy bit to 1 indicates completion of initialization. The host repeatedly issues ACMD41 until the busy bit is set to 1.

The SDNAND checks the operational conditions and the HCS bit in the OCR only at the first ACMD41. While repeating ACMD41, the host shall not issue another command except CMD0.

If the SDNAND responds to CMD8, the response of ACMD41 includes the CCS field information. CCS is valid when the SDNAND returns ready (the busy bit is set to 1). CCS=1 means that the SDNAND is a High Capacity SDNAND.

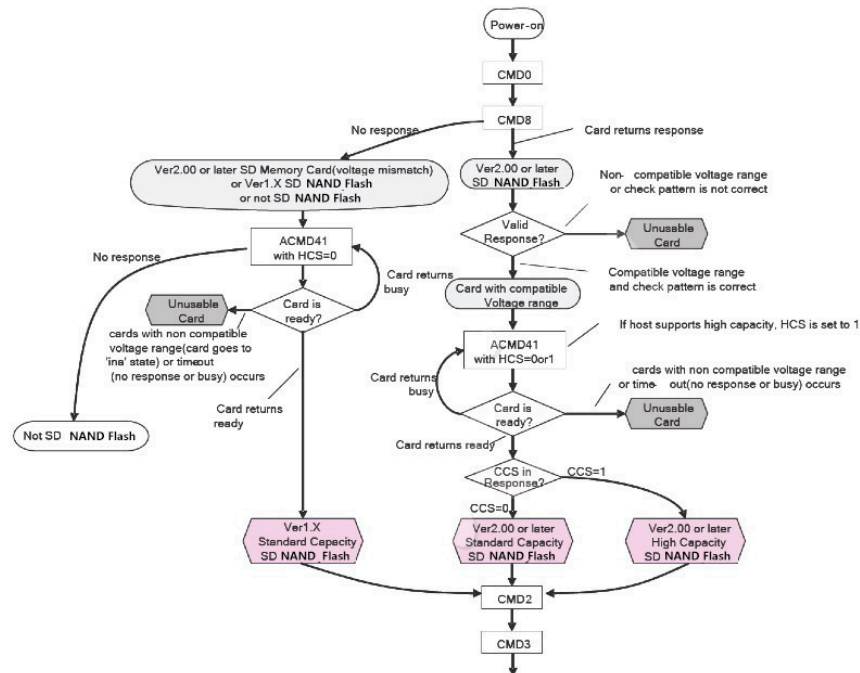
CCS=0 means that the SDNAND is a Standard Capacity SDNAND.

The host performs the same initialization sequence to all of the new SDNANDs in the system. Incompatible SDNANDs are sent



into Inactive State. The host then issues the command ALL\_SEND\_CID (CMD2), to each SDNAND to get its unique SDNAND identification (CID) number. SDNAND that is unidentified (i.e. which is in Ready State) sends its CID number as the response (on the CMD line). After the CID was sent by the SDNAND it goes into Identification State. Thereafter, the host issues CMD3 (SEND\_RELATIVE\_ADDR) asks the SDNAND to publish a new relative SDNAND address (RCA), which is shorter than CID and which is used to address the SDNAND in the future data transfer mode. Once the RCA is received the SDNAND state changes to the Stand-by State. At this point, if the host wants to assign another RCA number, it can ask the SDNAND to publish a new number by sending another CMD3 command to the SDNAND. The last published RCA is the actual RCA number of the SDNAND.

The host repeats the identification process, i.e. the cycles with CMD2 and CMD3 for each SDNAND in the system.



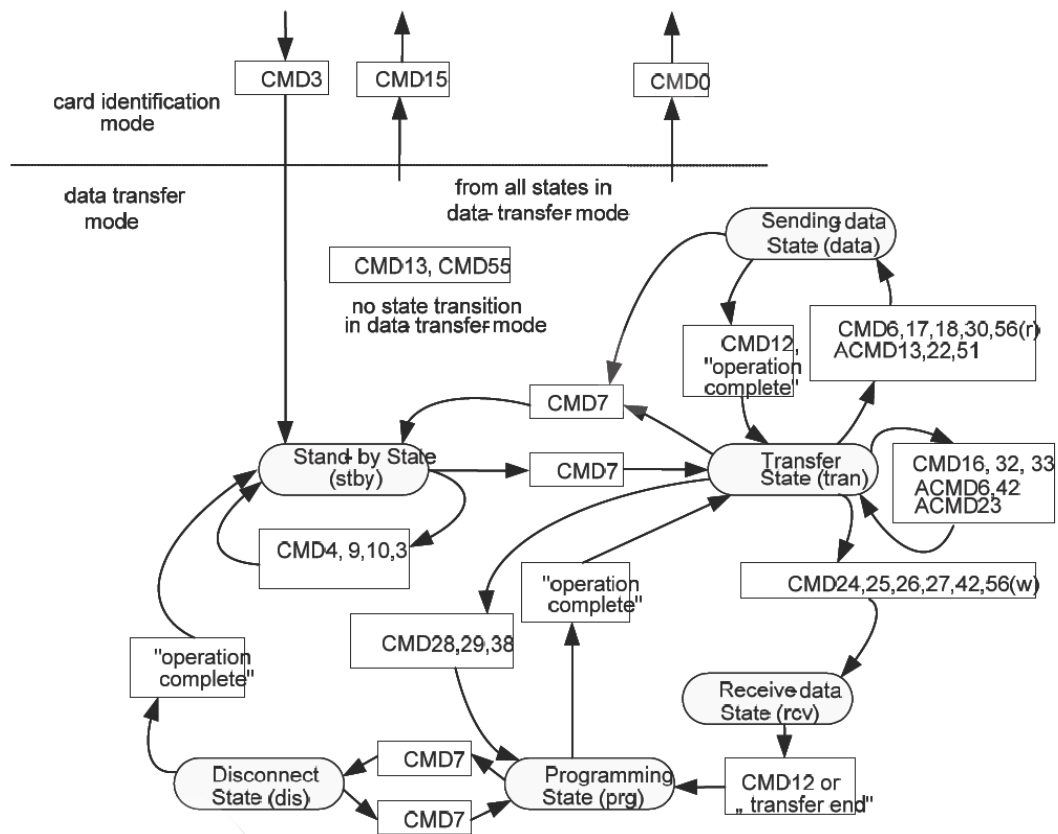
**SDNAND Initialization and Identification Flow**



## 7. Data Transfer Mode

Until the end of SDNAND Identification Mode the host shall remain at  $F_{OD}$  frequency because some SDNAND may have operating frequency restrictions during the SDNAND identification mode. In Data Transfer Mode the host may operate the SDNAND in  $f_{PP}$  frequency range. The host issues SEND\_CSD (CMD9) to obtain the SDNAND Specific Data (CSD register), e.g. block length, SDNAND storage capacity, etc.

The broadcast command SET\_DSR (CMD4) configures the driver stages of all identified SDNAND. It programs their DSR registers corresponding to the application bus layout (length) and the number of SDNAND on the bus and the data transfer frequency. The clock rate is also switched from  $F_{OD}$  to  $F_{PP}$  at that point. SET\_DSR command is an option for the SDNAND and the host.



**SDNAND State Diagram (data transfer mode)**



## 8. SDNAND Registers

Six registers are defined within the SDNAND interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the SDNAND/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. In order to enable future extension, The SDNAND shall return 0 in the reserved bits of the registers.

| Name | Width | Description                                                                                                                                   |
|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| CID  | 128   | SDNAND identification number; SDNAND individual number for identification                                                                     |
| RCA1 | 16    | Relative SDNAND address; local system address of a SDNAND, dynamically suggested by the SDNAND and approved by the host during initialization |
| DSR  | 16    | Driver Stage Register; to configure the SDNAND's output drivers                                                                               |
| CSD  | 128   | SDNAND Specific Data; information about the SDNAND operation conditions                                                                       |
| SCR  | 64    | SD Configuration Register; information about the SDNAND's Special Features capabilities                                                       |
| OCR  | 32    | Operation conditions register.                                                                                                                |
| SSR  | 512   | SD Status; information about the SDNAND proprietary features                                                                                  |
| CSR  | 32    | SDNAND Status; information about the SDNAND status                                                                                            |

### SDNAND Registers

#### 8.1 OCR register

The 32-bit operation conditions register stores the VCC voltage profile of the SDNAND. Additionally, this register includes status information bits. One status bit is set if the SDNAND power up procedure has been finished. This register includes another status bit indicating the SDNAND capacity status after set powerup status bit. The OCR register shall be implemented by the SDNAND. The 32-bit operation conditions register stores the VCC voltage profile of the SDNAND. Bit 7 of OCR is newly defined for Dual Voltage SDNAND and set to 0 in default. If a Dual Voltage SDNAND does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage SDNAND which received CMD8, sets this bit to 1. Additionally, this register includes 2 more status information bits. Bit 31 - SDNAND power up status bit, this status bit is set if the SDNAND power up procedure has been finished. Bit 30 - SDNAND capacity status bit, this status bit is set to 1 if SDNAND is High Capacity SDNAND. 0 indicates that the SDNAND is Standard Capacity SDNAND. The SDNAND Capacity status bit is valid after the SDNAND power up procedure is completed and the SDNAND powerup status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SDNAND. The OCR register shall be implemented by the SDNANDs.

| OCR bit position | VCC voltage window                | Initial Value                            |
|------------------|-----------------------------------|------------------------------------------|
|                  |                                   | 512Gb                                    |
| 31               | SDNAND powerup status bit (busy)  | "0" = busy<br>"1" = ready                |
| 30               | SDNAND Capacity Status            | "0" = SDNAND<br>"1" = SDHC Memory SDNAND |
| 29-25            | Reserved                          | All '0'                                  |
| 24               | Switching to 1.8V Accepted (S18A) | 0                                        |
| 23               | 3.6-3.5                           | 1                                        |
| 22               | 3.5-3.4                           | 1                                        |
| 21               | 3.4-3.3                           | 1                                        |
| 20               | 3.3-3.2                           | 1                                        |
| 19               | 3.2-3.1                           | 1                                        |
| 18               | 3.1-3.0                           | 1                                        |



|     |                                |         |
|-----|--------------------------------|---------|
| 17  | 3.0-2.9                        | 1       |
| 16  | 2.9-2.8                        | 1       |
| 15  | 2.8-2.7                        | 1       |
| 14  | Reserved                       | 0       |
| 13  | Reserved                       | 0       |
| 12  | Reserved                       | 0       |
| 11  | Reserved                       | 0       |
| 10  | Reserved                       | 0       |
| 9   | Reserved                       | 0       |
| 8   | Reserved                       | 0       |
| 7   | Reserved for Low Voltage Range | 0       |
| 6   | Reserved                       | 0       |
| 5   | Reserved                       | 0       |
| 4   | Reserved                       | 0       |
| 3-0 | Reserved                       | All '0' |

### 8.2 CID register

The SDNAND Identification (CID) register is 128 bits wide. It contains the SDNAND identification information used during the SDNAND identification phase. Every individual Read/Write (RW) SDNAND shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

| Name                  | Field | Width | CID-slice | Initial Value               |
|-----------------------|-------|-------|-----------|-----------------------------|
|                       |       |       |           | 512Gb                       |
| Manufacturer ID       | MID   | 8     | [127:120] | 66                          |
| OEM/Application ID    | OID   | 16    | [119:104] | 2346                        |
| Product name          | PNM   | 40    | [103:64]  | CS012                       |
| Product revision      | PRV   | 8     | [63:56]   | 01                          |
| Product serial number | PSN   | 32    | [55:24]   | (a) (Product serial number) |
| Reserved              | -     | 4     | [23:20]   | All "0b"                    |
| Manufacturing date    | MDT   | 12    | [19:8]    | (a)(Manufacture date)       |
| CRC7 checksum         | CRC   | 7     | [7:1]     | (b)(CRC)                    |
| Not used, always 1    | -     | 1     | [0:0]     | 1b                          |
|                       |       |       |           |                             |

### 8.3 CSD Register

The SDNAND-Specific Data register provides information regarding access to the SDNAND contents.

The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The types of the entries in the table below are coded as follows: R = readable, W (1) = writable once, W = multiple writable.

| Name          | Field         | Width | Value | Note   | CSD-slice |
|---------------|---------------|-------|-------|--------|-----------|
| CSD structure | CSD_STRUCTURE | 2     | 1 h   | Ver2.0 | [127:126] |
| Reserved      | ---           | 6     | ---   | ---    | [125:120] |



|                                               |                    |    |            |               |           |
|-----------------------------------------------|--------------------|----|------------|---------------|-----------|
| Data read access-time 1                       | TAAC               | 8  | 0E h       | 1ms           | [119:112] |
| Data read access-time2 in CLK cycles(NSA*100) | NSAC               | 8  | 0 h        |               | [111:104] |
| Max data transfer rate                        | TRAN_SPEED         | 8  | 32h<br>5ah |               | [103:96]  |
| Card command classes                          | CCC                | 12 | db5 h      |               | [95:84]   |
| Max. read data block length                   | READ_BL_LEN        | 4  | 9 h        | 512 Byte      | [83:80]   |
| Partial block read allowed                    | READ_BL_PARTIAL    | 1  | 0 h        | No            | [79]      |
| Write block misalignment                      | WRITE_BLK_MISALIGN | 1  | 0 h        | No            | [78]      |
| Read block misalignment                       | READ_BLK_MISALIGN  | 1  | 0 h        | No            | [77]      |
| DSR implemented                               | DSR_IMP            | 1  | 0 h        | No            | [76]      |
| Reserve                                       | ---                | 6  | ---        | ---           | [75:70]   |
| Device size                                   | C_SIZE             | 22 | 1cd0fh     | ---           | [69:48]   |
| Reserved                                      | ---                | 1  | ---        | ---           | [47]      |
| Erase single block enable                     | ERASE_BLK_EN       | 1  | 1 h        | Yes           | [46]      |
| Erase sector size                             | SECTOR_SIZE        | 7  | 7F h       | 128           | [45:39]   |
| Write protect group size                      | WP_GRP_SIZE        | 7  | 0 h        | Not supported | [38:32]   |
| Write protect group enable                    | WP_GRP_ENABLE      | 1  | 0 h        | No            | [31]      |
| Reserved                                      | ---                | 2  | ---        | ---           | [30:29]   |
| Write speed factor                            | R2W_FACTOR         | 3  | 2 h        | x4            | [28:26]   |
| Max. write data block length                  | WRITE_BL_LEN       | 4  | 9 h        | 512 Byte      | [25:22]   |
| Partial block write allowed                   | WRITE_BL_PARTIAL   | 1  | 0 h        | No            | [21]      |
| Reserved                                      | ---                | 5  | ---        | ---           | [20:16]   |
| File format group                             | FILE_FORMAT_GRP    | 1  | 0 h        | Not use       | [15]      |
| Copy flag                                     | COPY               | 1  | 0 h        | Original      | [14]      |
| Permanent write protection                    | PERM_WRITE_PROTECT | 1  | 0 h        | Not Protected | [13]      |
| Temporary write protection                    | TMP_WRITE_PROTECT  | 1  | 0 h        | Not Protected | [12]      |
| File format                                   | FILE_FORMAT        | 2  | 0 h        | Not use       | [11:10]   |
| Reserved                                      | ---                | 2  | ---        | ---           | [9:8]     |
| CRC                                           | CRC                | 7  | CRC7       |               | [7:1]     |
| Not used,always'1'                            | ---                | 1  | 1 h        | ---           | [0]       |



#### **8.4 RCA register**

The writable 16-bit relative SDNAND address register carries the SDNAND address that is published by the SDNAND during the SDNAND identification. This address is used for the addressed host-SDNAND communication after the SDNAND identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all SDNANDs into the Stand-by State with CMD7.

#### **8.5 DSR register**

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of SDNANDs). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

#### **8.6 SCR register**

In addition to the CSD register, there is another configuration register named SDNAND Configuration Register (SCR). SCR provides information on the SDNAND's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SDNAND

The following table describes the SCR register content.

| Description                     | Field                 | Width | Cell Type | SCR Slice |
|---------------------------------|-----------------------|-------|-----------|-----------|
| SCR Structure                   | SCR_STRUCTURE         | 4     | R         | [63:60]   |
| SD Memory Card - Spec. Version  | SD_SPEC               | 4     | R         | [59:56]   |
| DATA_STAT_AFTER_ERASE           | DATA_STAT_AFTER_ERASE | 1     | R         | [55:55]   |
| SD Security Support             | SD_SECURITY           | 3     | R         | [54:52]   |
| DAT Bus widths supported        | SD_BUS_WIDTHS         | 4     | R         | [51:48]   |
| Reserved                        | -                     | 16    | R         | [47:32]   |
| Reserved for manufacturer usage | -                     | 32    | R         | [31:0]    |

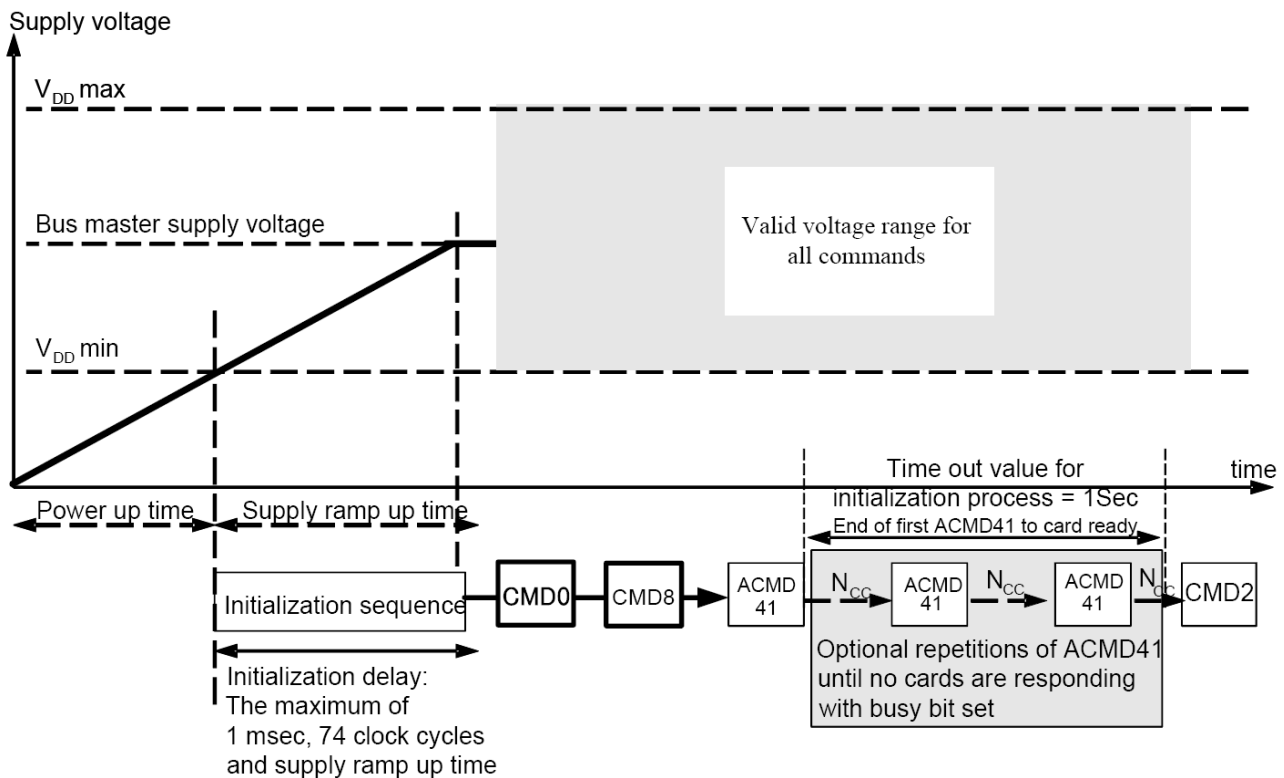
#### **The SCR Fields**

| SCR_STRUCTURE | SCR structure version | SD Physical Layer Specification Version |
|---------------|-----------------------|-----------------------------------------|
| 0             | SCR version No. 1.0   | Version 1.01-2.00                       |
| 1-15          | reserved              |                                         |

#### **SCR Register Structure Version**



## 9. Power Up



### Power-up Diagram

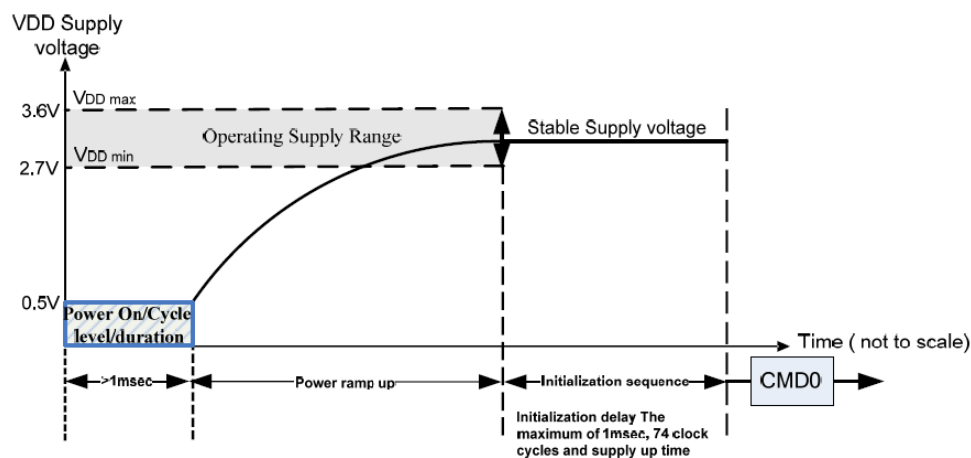
'Power up time' is defined as voltage rising time from 0 volt to VCC min.

'Supply ramp up time' provides the time that the power is built up to the operating level (Host SupplyVoltage) and the time to wait until the SDNAND can accept the first command,

The host shall supply power to the SDNAND so that the voltage is reached to Vcc\_min within 250ms and start to supply at least 74 SD clocks to the SDNAND with keeping CMD line to high.

### 9.2 Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



#### 9.2.1 Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SDNAND hard reset.

- (1) Voltage level shall be below 0.5V



(2) Duration shall be at least 1ms.

### 9.2.2 Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VCC (min.) and VCC (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

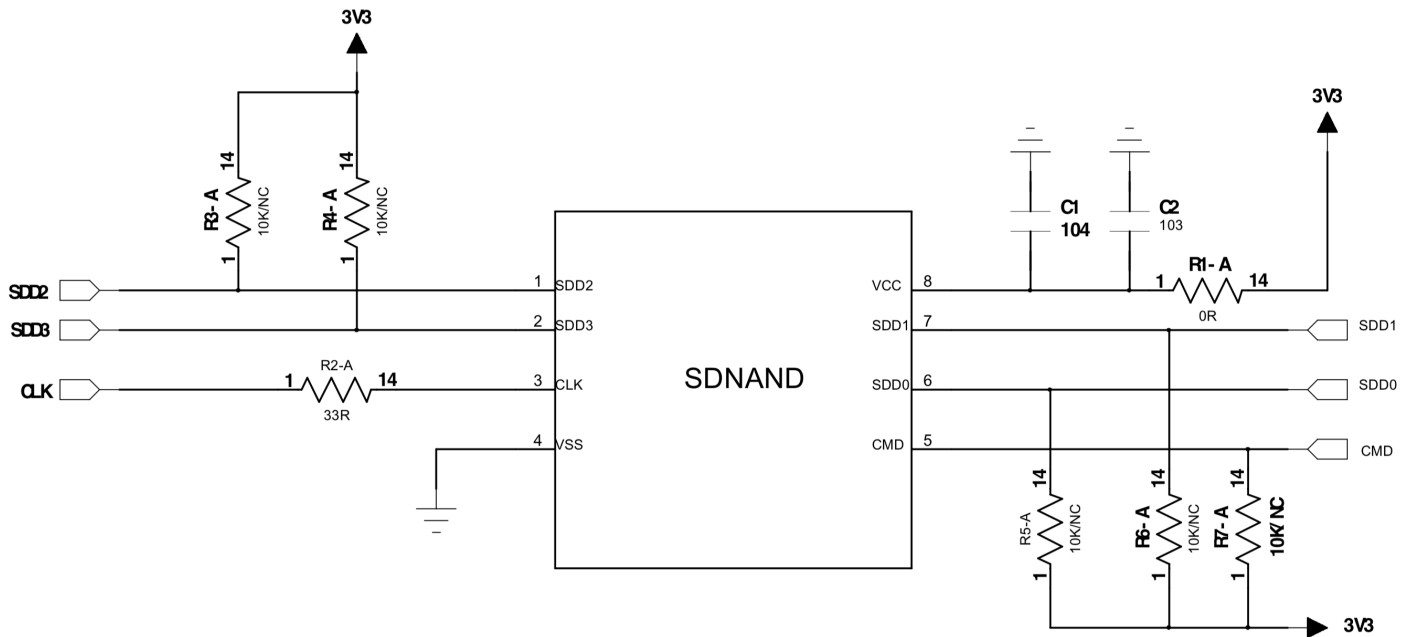
- (1) Voltage of power ramp up should be monotonic as much as possible.
- (2) The minimum ramp up time should be 0.1ms.
- (3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

When the host shuts down the power, the VCC shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing SDNAND that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the SDNAND (i.e. the VCC shall be once lowered to less than 0.5Volt for a minimum period of 1ms).



## 10. Reference Design



### Note:

$R_{DAT}$  and  $R_{CMD}$  (10K~100 k $\Omega$ ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SDNAND is in a high-impedance mode.

The host shall pull-up all DAT0-3 lines by  $R_{DAT}$ , even if the host uses the SDNAND as 1-bit mode only in SD mode. It is recommended to have 2.2 $\mu$ F capacitance on VCC.

$R_{CLK}$  reference 0~120  $\Omega$ .