



XTD25W02A

Dual IO Serial NOR Flash Datasheet

芯天下技术股份有限公司

XTX Technology Inc.

Tel: (+86 755) 28229862

Fax: (+86 755) 28229847

Web Site: <http://www.xtxtech.com/>

Technical Contact: fae@xtxtech.com

* Information furnished is believed to be accurate and reliable. However, XTX Technology Inc. assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent rights of XTX Technology Inc. Specifications mentioned in this publication are subjected to change without notice. This publication supersedes and replaces all information previously supplied. XTX Technology Inc. products are not authorized for use as critical components in life support devices or systems without express written approval of XTX Technology Inc. The XTX logo is a registered trademark of XTX Technology Inc. All other names are the property of their respective own.

Serial NOR Flash Memory

Wide Voltage Range Multi I/O with 512B, 4KB, 32KB & 64KB Sector/Block Erase

- **2M-bit Serial Flash**
 - 256K-byte
 - 256 bytes per programmable page
- **Standard, Dual SPI**
 - Standard SPI: SCLK, CS#, SI, SO
 - Dual SPI: SCLK, CS#, IO0, IO1
- **Flexible Architecture**
 - Sector of 512/4K-byte
 - Block of 32/64K-byte
- **Support 128 bits Unique ID**
- **Software Write Protection**
 - Top or Bottom Block Protection
- **Package Options**
 - See 1.1 Available Ordering OPN
 - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Allows XIP(execute in place)operation**
 - High speed Read reduce overall XiP instruction fetch time.
- **Temperature Range & Moisture Sensitivity Level**
 - Industrial Level Temperature. (-40 °C to +85 °C), MSL3
 - Industrial Plus Level Temperature. (-40 °C to +105 °C), MSL3
- **Power Consumption**
 - 0.3uA typ. Deep Power-Down current
- **Single Power Supply Voltage**
 - 1.65~3.6V
- **Endurance and Data Retention**
 - Minimum 100,000 Program/Erase Cycle
 - 20-year Data Retention typical
- **High Speed Clock Frequency**
 - 133MHz for fast read with 30pF load
 - Dual I/O Data transfer up to 266Mbit/s
- **Program/Erase Speed**
 - Page Program time: 1ms typical
 - Sector Erase time: 3.5ms typical
 - Block Erase time: 3.5ms typical
 - Chip Erase time: 14ms typical



CONTENTS

1.	GENERAL DESCRIPTION	5
1.1.	Available Ordering OPN	5
1.2.	Connection Diagram	5
1.3.	Pin Description.....	6
1.4.	Block Diagram	7
2.	MEMORY ORGANIZATION	8
3.	DEVICE OPERATION	9
3.1.	SPI Mode.....	9
4.	DATA PROTECTION	10
5.	STATUS REGISTER	11
6.	COMMANDS DESCRIPTION.....	12
6.1.	Register Access	15
6.1.1.	Read Status Register (05H).....	15
6.1.2.	Write Status Register (01H).....	16
6.1.3.	Read Manufacture ID/ Device ID (90H).....	17
6.1.4.	Read Unique ID (4BH)	18
6.1.5.	Read Identification (9FH)	19
6.2.	Array Access	20
6.2.1.	Normal Read (03H).....	20
6.2.2.	Fast Read (0BH)	20
6.2.3.	Dual Output Fast Read (3BH).....	21
6.2.4.	Dual I/O Fast Read (BBH).....	22
6.2.5.	Page Program (02H)	24
6.2.6.	Mini Sector Erase (82H)	25
6.2.7.	Sector Erase (20H).....	25
6.2.8.	32KB Block Erase (52H)	26
6.2.9.	64KB Block Erase (D8H)	27
6.2.10.	Chip Erase (60H or C7H)	27
6.3.	Device Operations	28
6.3.1.	Enable Reset (66H) and Reset (99H).....	28
6.3.2.	Write Enable (06H).....	28
6.3.3.	Write Enable for Volatile Status Register (50H)	29
6.3.4.	Write Disable (04H).....	29
6.3.5.	Deep Power-Down (B9H).....	30
6.3.6.	Release From Deep Power-Down (ABH).....	31
7.	ELECTRICAL CHARACTERISTICS.....	32
7.1.	Power-Down & Power-On Timing	32
7.2.	Initial Delivery State	32
7.3.	Absolute Maximum Ratings.....	33
7.4.	Capacitance Measurement Condition.....	34
7.5.	DC Characteristics.....	35
7.6.	AC Characteristics.....	36



8.	ORDERING INFORMATION	38
9.	PACKAGE INFORMATION	39
9.1.	Package SOP8 150mil	39
9.2.	Package DFN8 2x3x0.4mm	40
9.3.	Package TSSOP8 173mil	41
9.4.	Package DFN6 1.2x1.2x0.4mm	42
9.5.	Package FODFN6 1.2x0.7x0.4mm	43
10.	REVISION HISTORY	44

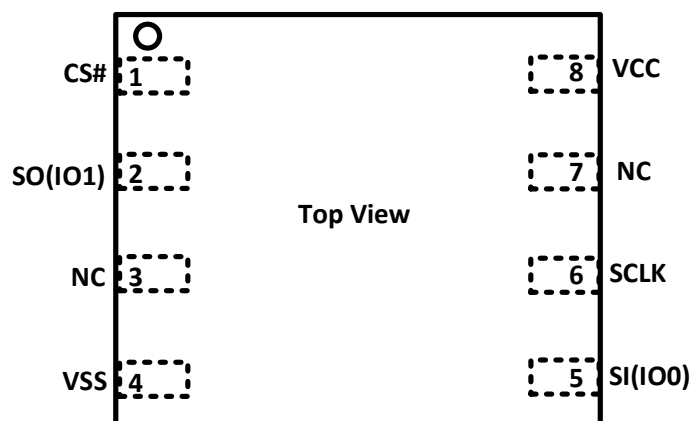
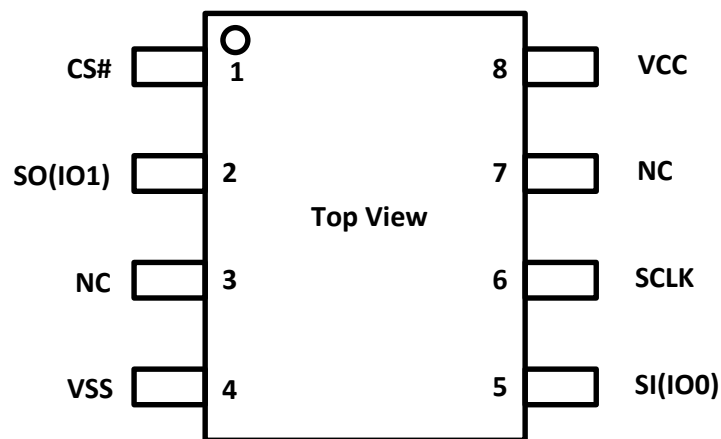
1. GENERAL DESCRIPTION

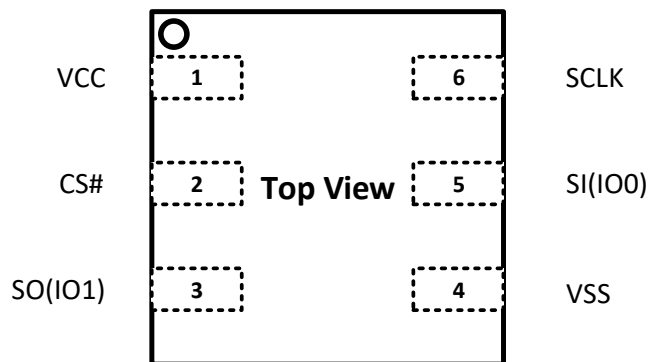
The XTD25W02A (2M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI) and I/O1 (SO).

1.1. Available Ordering OPN

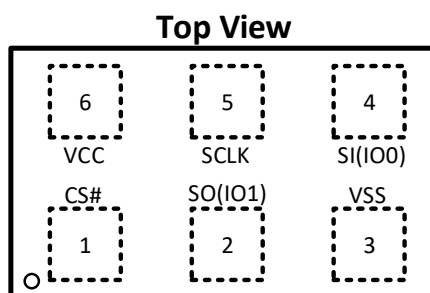
OPN	Temperature	Package Type	Package Carrier
XTD25W02A-WLHA	-40 ℃ ~ 105 ℃	Wafer	Cassette
XTD25W02ASOIGU	-40 ℃ ~ 85 ℃	SOP8 150mil	Tube
XTD25W02ASOIGT	-40 ℃ ~ 85 ℃	SOP8 150mil	Tape & Reel
XTD25W02ADTIGT	-40 ℃ ~ 85 ℃	DFN8 2x3x0.4mm	Tape & Reel
XTD25W02ATSIGT	-40 ℃ ~ 85 ℃	TSSOP8 173mil	Tape & Reel
XTD25W02ADUIGT	-40 ℃ ~ 85 ℃	DFN6 1.2x1.2x0.4mm	Tape & Reel
XTD25W02AFUIGT	-40 ℃ ~ 85 ℃	FODFN6 1.2x0.7x0.4mm	Tape & Reel

1.2. Connection Diagram





6-PIN DFN (1.2x1.2x0.40mm)

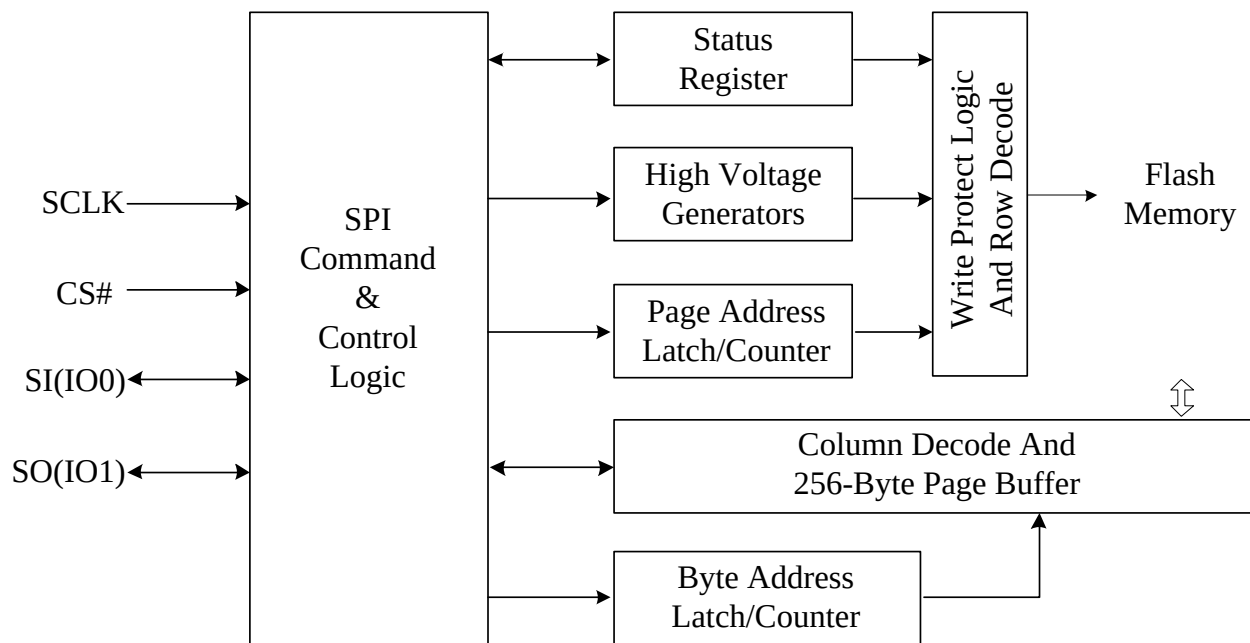


6-PIN DFN (1.2x0.7x0.40mm)

1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
VCC		Power Supply
NC		No connection

1.4. Block Diagram



2. MEMORY ORGANIZATION

Uniform Block / Sector Architecture

Block(64K-byte)	Block(32K-byte)	Sector(4K-byte)	Address Range	
3	7	63	03F000H	03FFFFH
				
		56	038000H	038FFFH
	6	55	037000H	037FFFH
				
		48	030000H	030FFFH
2	5	47	02F000H	02FFFFH
				
		40	028000H	028FFFH
	4	39	027000H	027FFFH
				
		32	020000H	020FFFH
1	3	31	01F000H	01FFFFH
				
		24	018000H	018FFFH
	2	23	017000H	017FFFH
				
		16	010000H	010FFFH
0	1	15	00F000H	00FFFFH
				
		8	008000H	008FFFH
	0	7	007000H	007FFFH
				
		0	000000H	000FFFH



3. DEVICE OPERATION

3.1. SPI Mode

Standard SPI

The device features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The device supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4. DATA PROTECTION

The device provides the following data protection methods:

- Write Enable (WREN) command: The WREN command sets the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
 - Power-Up / Software Reset (66H+99H)
 - Write Disable (WRDI)
 - Write Status Register (WRSR)
 - Page Program (PP)
 - Mini Sector Erase (MSE) / Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
 - Erase Security Register / Program Security Register
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but cannot be changed.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command (ABH) and software reset (66H+99H).

Table 1. XTD25W02A Protected area size

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	X	X	0	0	NONE	NONE	NONE	NONE
0	0	X	0	1	3	030000H-03FFFFH	64KB	Upper 1/4
0	0	X	1	0	2 and 3	020000H-03FFFFH	128KB	Upper 1/2
0	1	X	0	1	0	000000H-00FFFFH	64KB	Lower 1/4
0	1	X	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/2
0	X	X	1	1	0 to 3	000000H-03FFFFH	256KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000H-03FFFFH	4KB	Upper 1/64
1	0	0	1	0	3	03E000H-03FFFFH	8KB	Upper 1/32
1	0	0	1	1	3	03C000H-03FFFFH	16KB	Upper 1/16
1	0	1	0	X	3	038000H-03FFFFH	32KB	Upper 1/8
1	0	1	1	0	3	038000H-03FFFFH	32KB	Upper 1/8
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/64
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/32
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/16
1	1	1	0	X	0	000000H-007FFFH	32KB	Lower 1/8
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/8
1	X	1	1	1	0 to 3	000000H-03FFFFH	256KB	ALL

5. STATUS REGISTER

Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
DC	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Dummy Configuration Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Block Protect Bit	Write Enable Latch	Erase/Write In Progress
Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Volatile Read Only	Volatile Read Only

Note: For the initial delivery state, all Status Register bits are 0.

WIP

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 1 & 2) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed only if the Block Protect (BP4, BP3, BP2, BP1, BP0) are set to “None protected”.

DC

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy clocks between the end of address and the start of read data output. Dummy clocks provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system.

The following dummy clocks tables provide different dummy clocks settings that are configured.

Command	DC Bit	Dummy Clocks	Freq.
BBH	0 (Default)	4	104MHz
	1	8	133MHz

6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See the table below, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Commands

Command Name	Command Code	SPI	Address Byte					Dummy Clock	Data Byte
			Total ADD Byte	Byte1	Byte2	Byte3	Byte4		
Register Access									
Read Status Register_1	05H	√	0					0	1 to ∞
Write Status Register_1	01H	√	0					0	1
Read Manufacturer/ Device ID ^{Note1}	90H	√	3	ADD1	ADD2	ADD3		0	1 to ∞
Read Unique ID ^{Note1}	4BH	√	0	ADD1	ADD2	ADD3		8	1 to ∞
Read Identification	9FH	√	0					0	1 to ∞
Array Access									
Read Data	03H	√	3	ADD1	ADD2	ADD3		0	1 to ∞
Fast Read	0BH	√	3	ADD1	ADD2	ADD3		8	1 to ∞
Dual Output Fast Read	3BH	√	3	ADD1	ADD2	ADD3		8	1 to ∞
Dual I/O Fast Read	BBH	√	3	ADD1	ADD2	ADD3		4	1 to ∞
Page Program	02H	√	3	ADD1	ADD2	ADD3		0	1 to 256
Mini Sector Erase	82H	√	3	ADD1	ADD2	ADD3		0	0
4KB Sector Erase	20H	√	3	ADD1	ADD2	ADD3		0	0
32KB Block Erase	52H	√	3	ADD1	ADD2	ADD3		0	0
64KB Block Erase	D8H	√	3	ADD1	ADD2	ADD3		0	0
Chip Erase	C7/60H	√	0					0	0
Device Operations									
Enable Reset	66H	√	0					0	0
Reset	99H	√	0					0	0



Write Enable	06H	√	0					0	0
Write Enable for Volatile Status Register	50H	√	0					0	0
Write Disable	04H	√	0					0	0
Deep Power-Down	B9H	√	0					0	0
Release From Deep Power-Down	ABH	√	0					0	0
Release From Deep Power-Down/Read Device ID	ABH	√	0					24	0

Note:

- 1.For command 90H: 24 bit Address only supports 000000H and 000001H; For command 4BH: 24 bit Address (don't care).
- 2.M7-0 is counted for dummy clocks.

**Table of ID Definitions:**

XTD25W02A

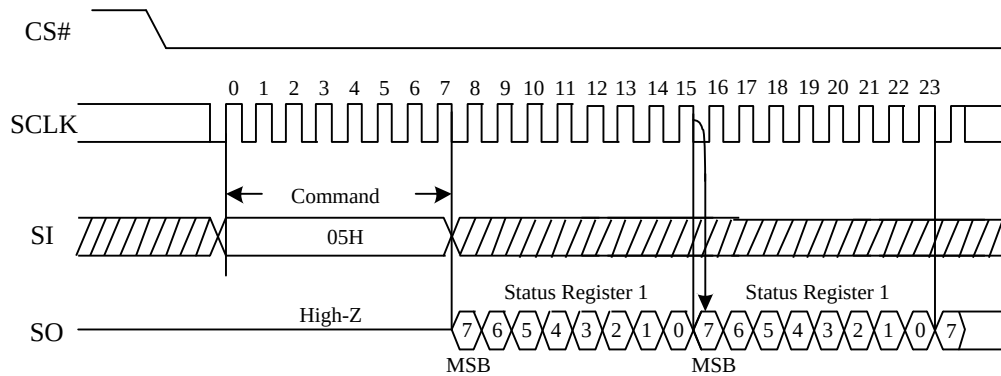
Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	0B	74	12
90H	0B		11
ABH			11

6.1. Register Access

6.1.1. Read Status Register (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously.

Figure 1. Read Status Register Sequence Diagram



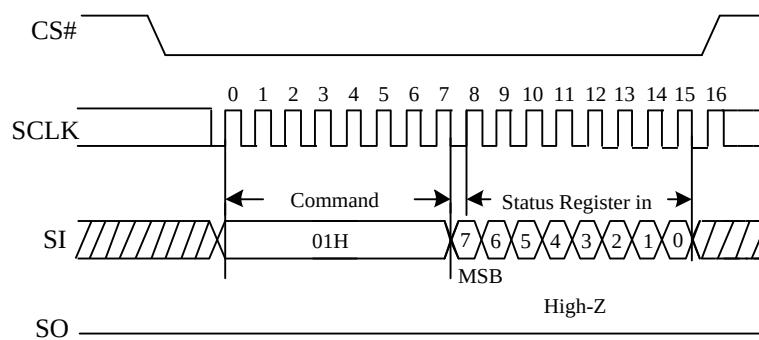
6.1.2. Write Status Register (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on the volatile bits of the Status Register. CS# must be driven high after the eighth or sixteenth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1 & 2.

Figure 2. Write Status Register Sequence Diagram

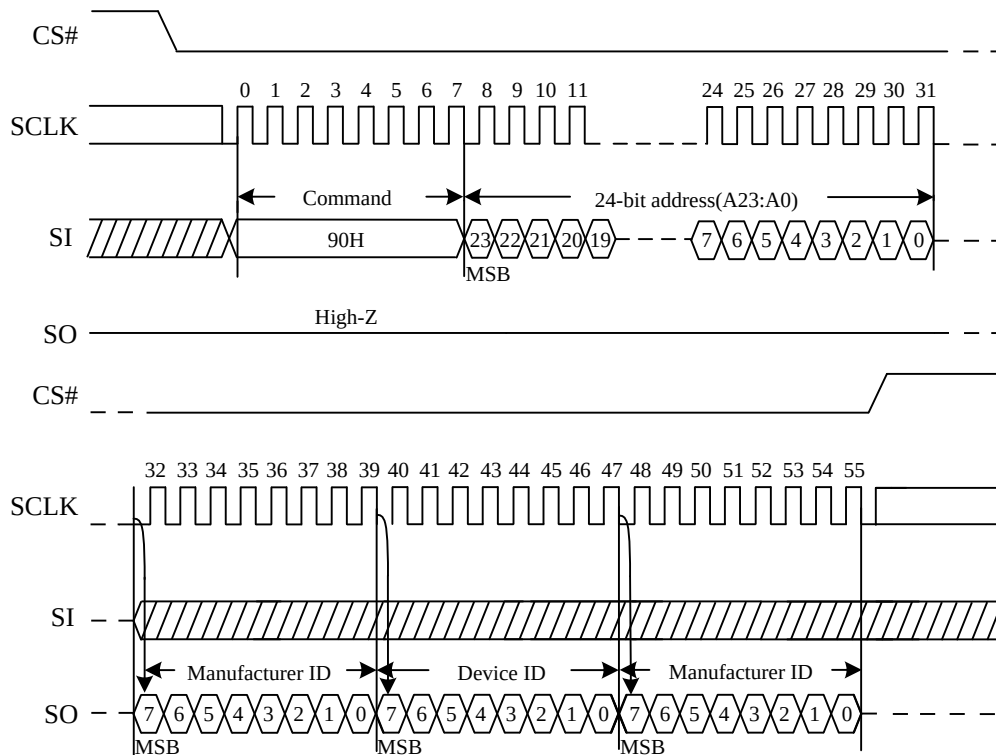


6.1.3. Read Manufacture ID/ Device ID (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Deep Power-Down and Read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in the figure below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 3. Read Manufacture ID/ Device ID Sequence Diagram



Note: For command 90H: 24-bit address only supports 000000H and 000001H.

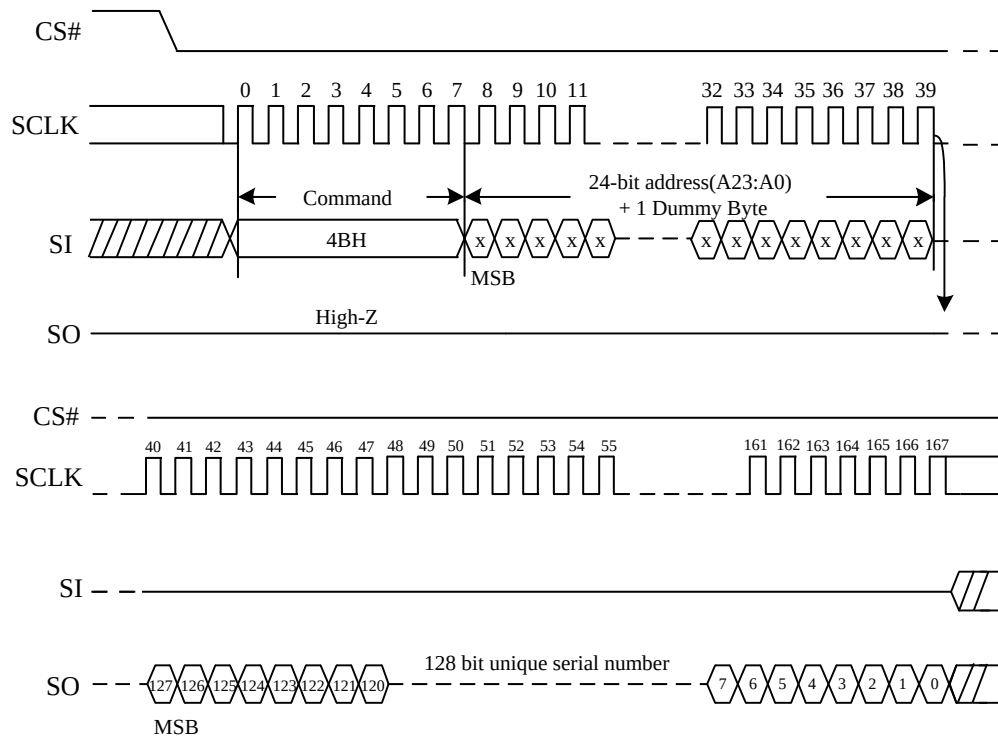
6.1.4. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → Sending Read Unique ID command → 24-bit Address(don't care)+1 dummy byte → 128bit Unique ID Out → CS# goes high.

The command sequence is shown below.

Figure 4. Read Unique ID (RUID) Sequence

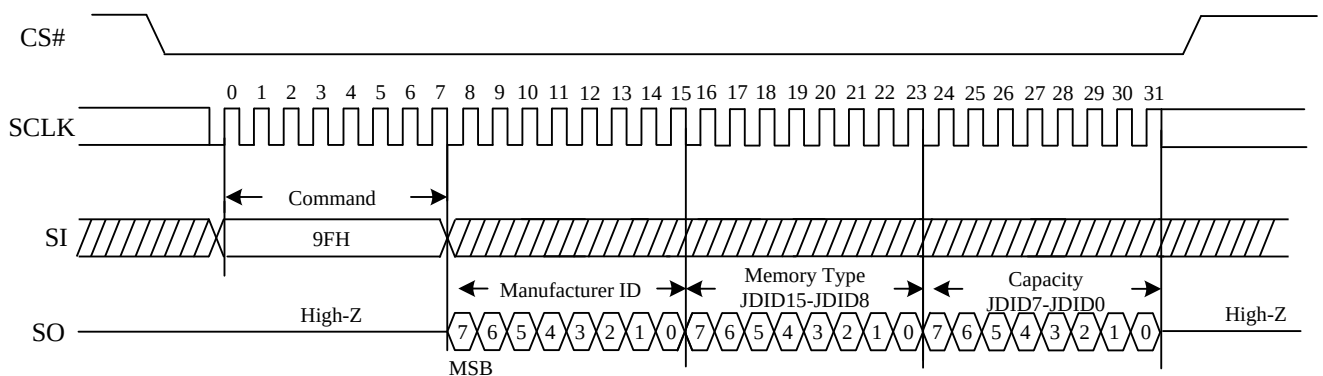


6.1.5. Read Identification (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress will not be decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit manufacture identification and device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in the figure below. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 5. Read Identification ID Sequence Diagram

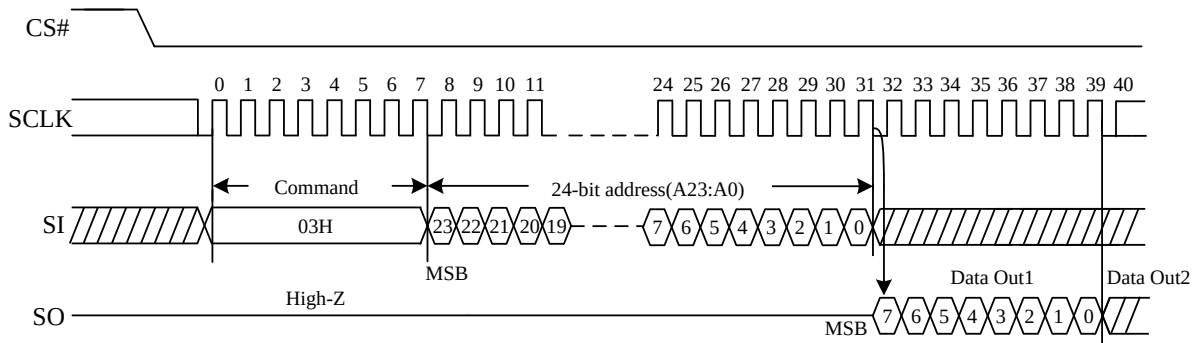


6.2. Array Access

6.2.1. Normal Read (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

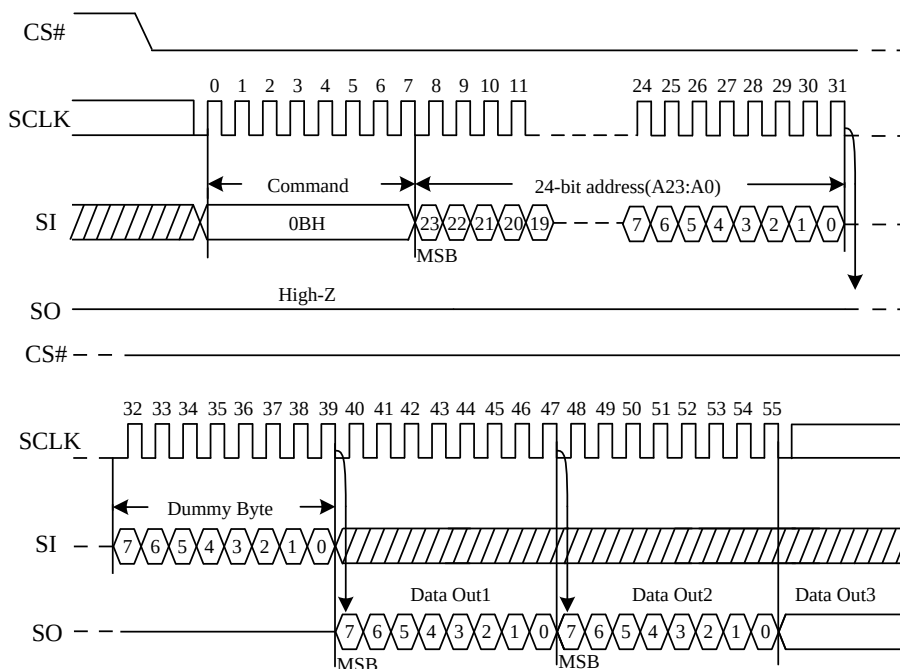
Figure 6. Read Data Bytes Sequence Diagram



6.2.2. Fast Read (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

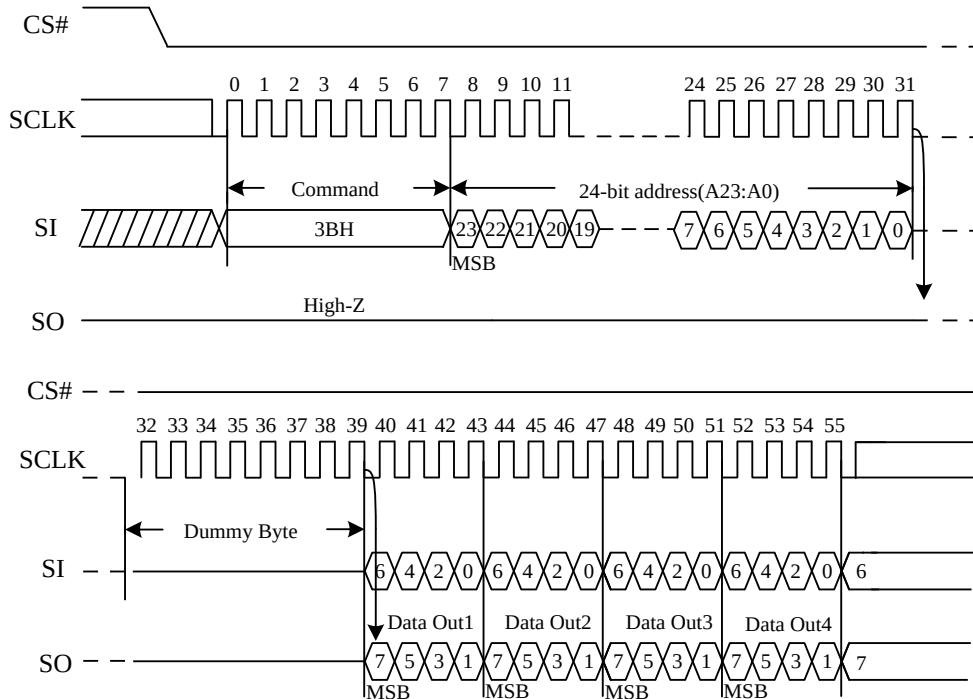
Figure 7. Read Data By test Higher Speed Sequence Diagram



6.2.3. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the following figure. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 8. Dual Output Fast Read Sequence Diagram

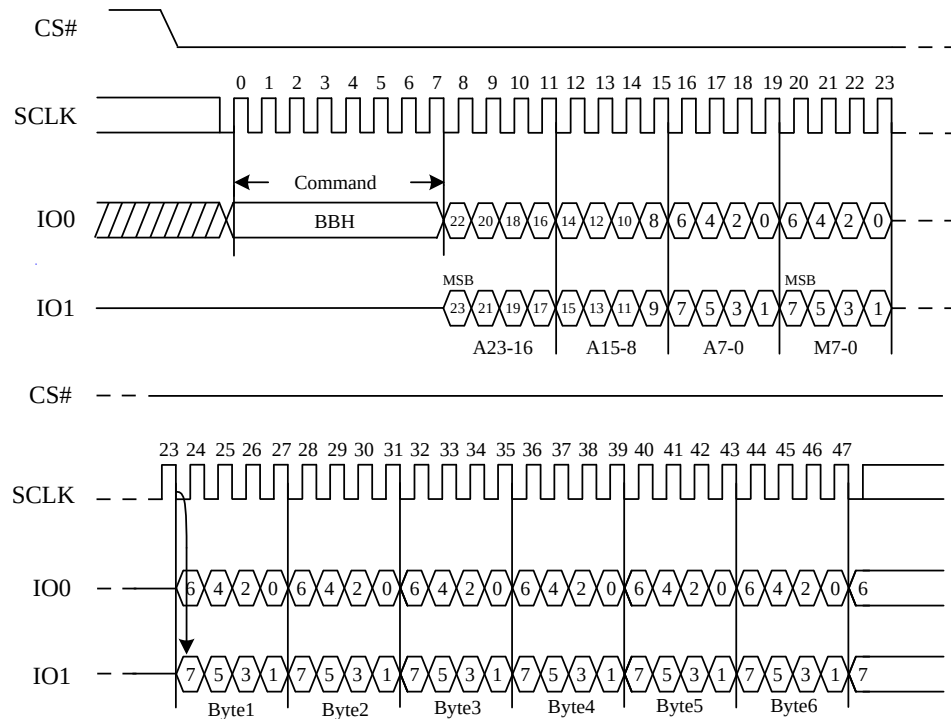


6.2.4.Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the following figure. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

The number of dummy clocks for “Dual I/O Fast Read” (BBH) are 4. The “Continuous Read Mode” bits M7-M0 are considered as dummy clocks.

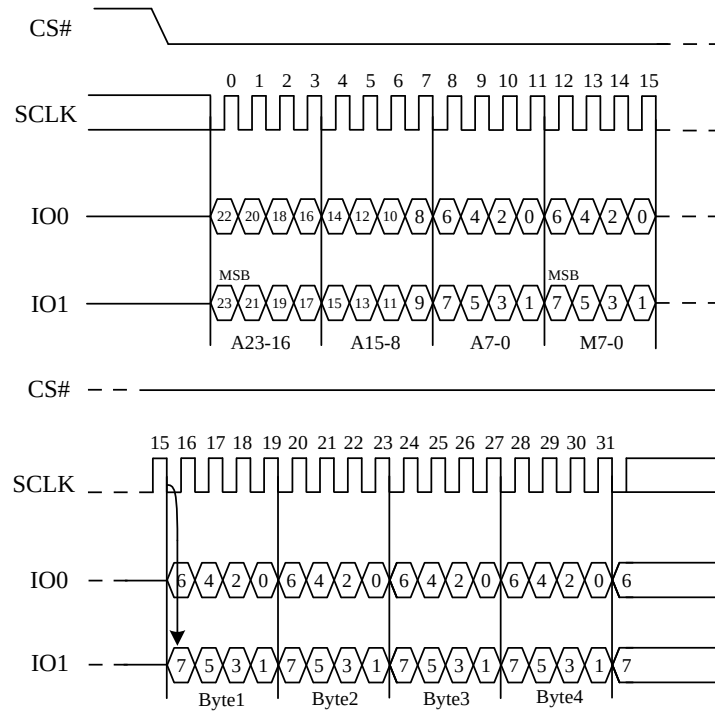
Figure 9. Dual I/O Fast Read Sequence Diagram (M5-4≠(1,0))



Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure below. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

Figure 10. Dual I/O Fast Read Sequence Diagram (M5-4=(1,0))



6.2.5. Page Program (02H)

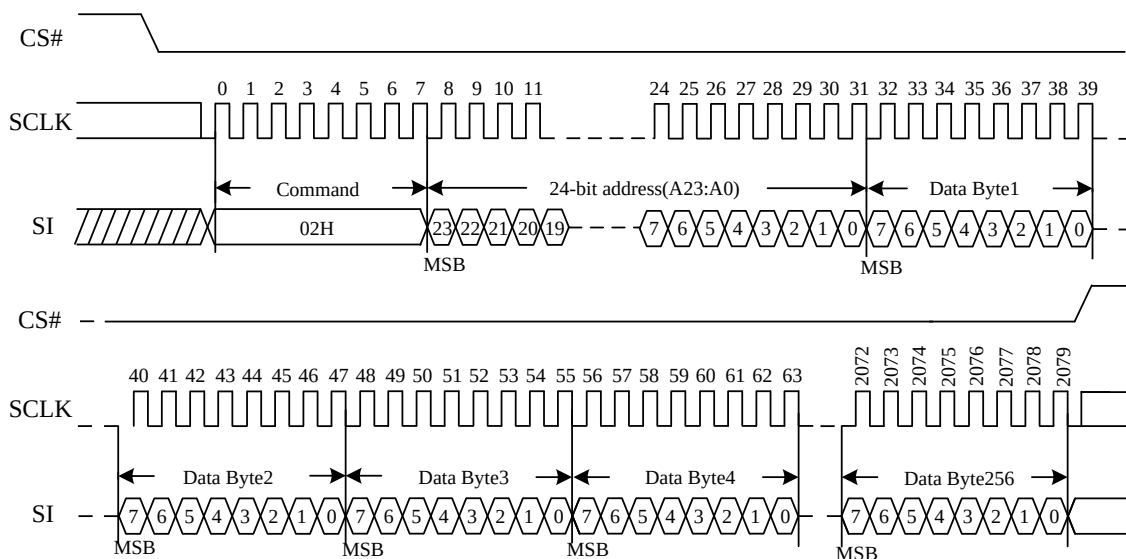
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → Sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in the figure below. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure 11. Page Program Sequence Diagram



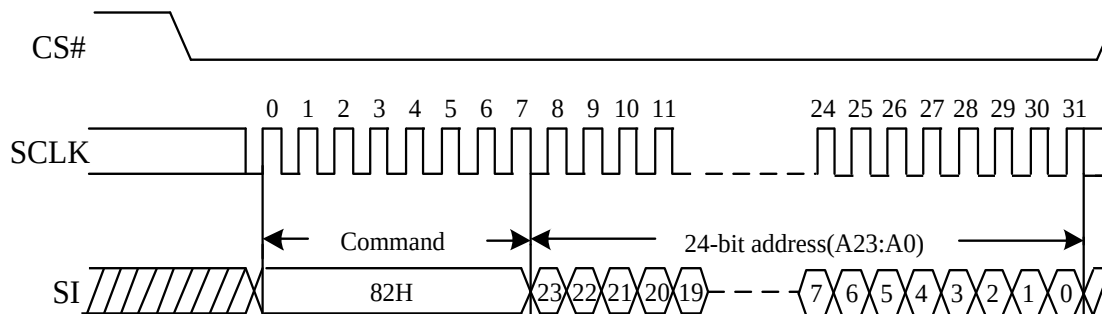
6.2.6. Mini Sector Erase (82H)

The Mini Sector Erase (MSE) command is for erasing all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase command. The Mini Sector Erase (MSE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Mini Sector Erase (MSE) command.

The Sector Erase command sequence: CS# goes low → Sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Mini Sector Erase (MSE) command will not be executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tMSE) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Mini Sector Erase (MSE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table 1 & 2) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 12. Sector Erase Sequence Diagram



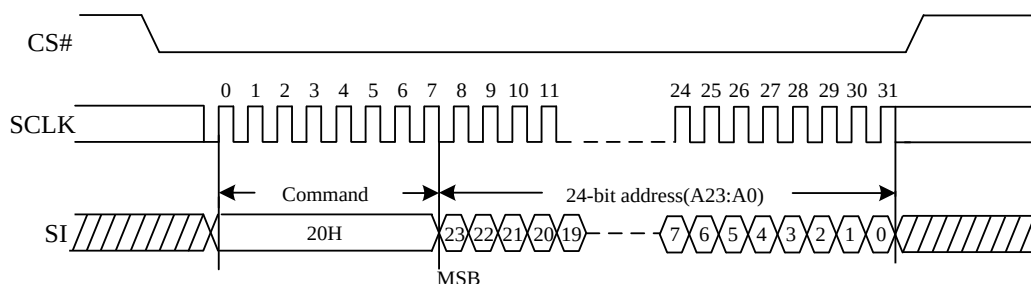
6.2.7. Sector Erase (20H)

The Sector Erase (SE) command is for erasing all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase command. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command.

The Sector Erase command sequence: CS# goes low → Sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command will not be executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table 1 & 2) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 13. Sector Erase Sequence Diagram



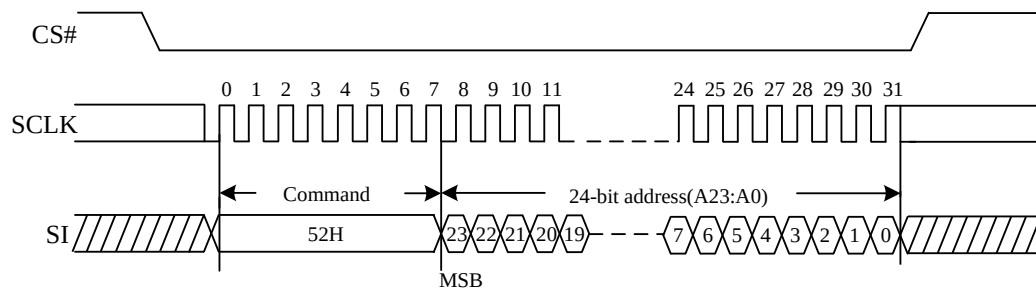
6.2.8.32KB Block Erase (52H)

The 32KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the 32KB Block Erase command. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high. Any address inside the block is a valid address for the 32KB Block Erase (BE) command.

The 32KB Block Erase command sequence: CS# goes low → Sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1 & 2) will not be executed.

Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 14. 32KB Block Erase Sequence Diagram



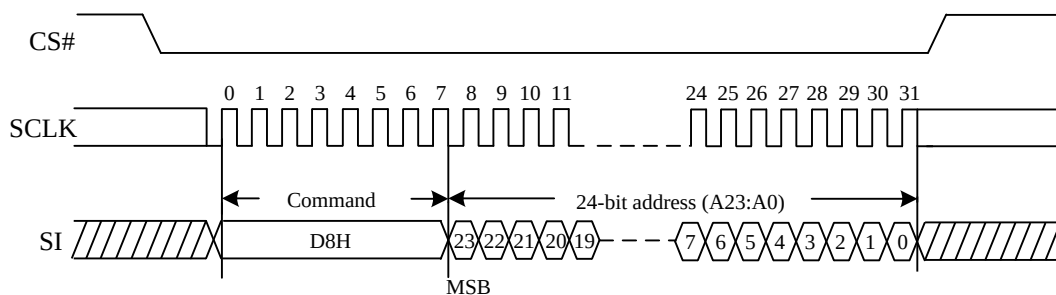
6.2.9.64KB Block Erase (D8H)

The 64KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the 64KB Block Erase command. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high. Any address inside the block is a valid address for the 64KB Block Erase (BE) command.

The 64KB Block Erase command sequence: CS# goes low → Sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table 1 & 2) will not be executed.

Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 15. 64KB Block Erase Sequence Diagram



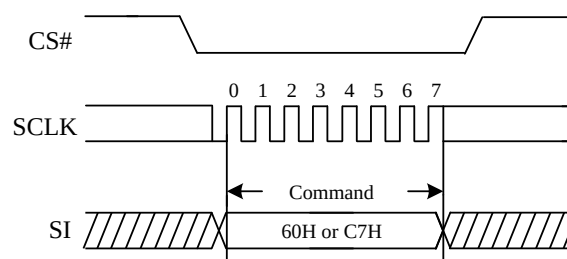
6.2.10. Chip Erase (60H or C7H)

The Chip Erase (CE) command is for erasing all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the Chip Erase command. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on SI.

The Chip Erase command sequence: CS# goes low → Sending Chip Erase command → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command will not be executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 16. Chip Erase Sequence Diagram



6.3. Device Operations

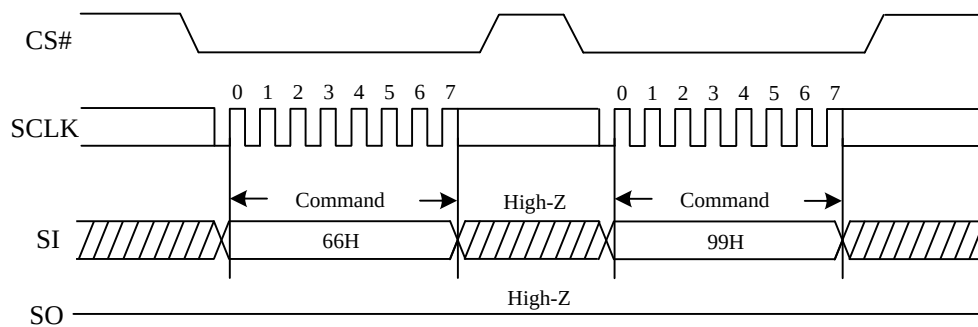
6.3.1. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0).

The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command sequence.

The Enable Reset (66H) command must be issued prior to a Reset (99H) command and any other commands can't be inserted between them. Otherwise, Enable Reset (66H) command will be cleared.

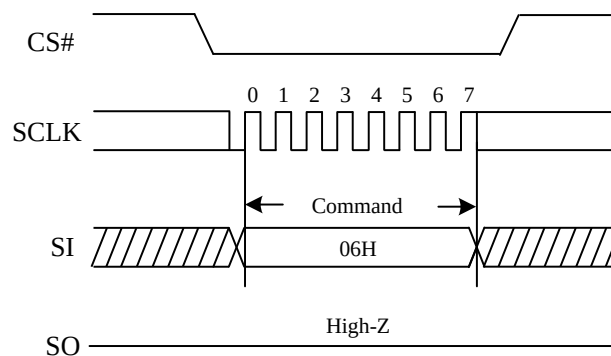
Figure 17. Enable Reset and Reset command Sequence Diagram



6.3.2. Write Enable (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Erase Security Register, Program Security Register and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low → Sending the Write Enable command → CS# goes high.

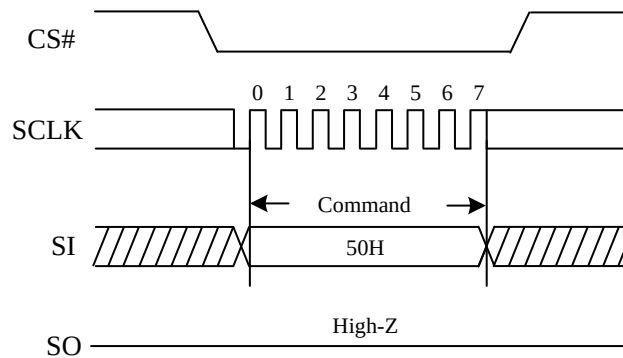
Figure 18. Write Enable Sequence Diagram



6.3.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

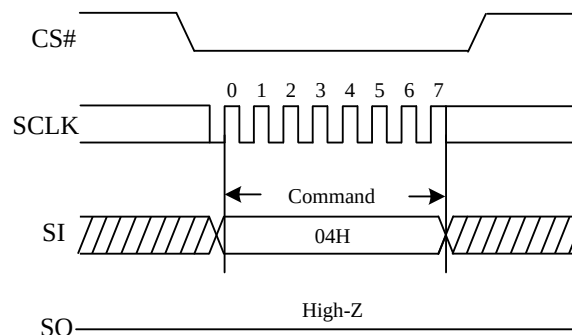
Figure 19. Write Enable for Volatile Status Register Sequence Diagram



6.3.4. Write Disable (04H)

The Write Disable (WRDI) command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Write Disable command; Power-up; upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

Figure 20. Write Disable Sequence Diagram



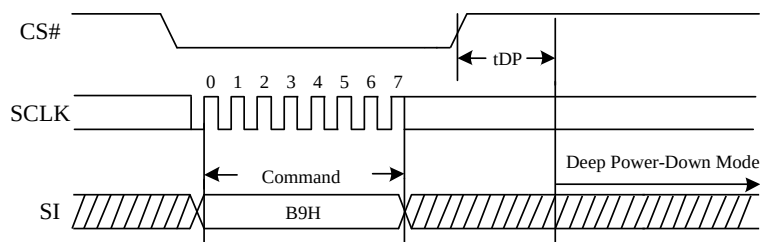
6.3.5. Deep Power-Down (B9H)

Executing the Deep Power-Down (DPD) command is the only way to put the device in the lowest power consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But the Standby Mode is different from the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DPD) command. Once the flash memory has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID command (ABH) and Software Reset (66H+99H). This command releases the flash memory from the Deep Power-Down Mode.

The Deep Power-Down Mode automatically stops at Power-Off, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DPD) command is entered by driving CS# low, followed by the command code on SI, driving CS# high.

The Deep Power-Down command sequence: CS# goes low → Sending Deep Power-Down command → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DPD) command will not be executed. As soon as CS# is driven high, it requires a time duration of t_{DP} before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any input of Deep Power-Down (DPD) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 21. Deep Power-Down Sequence Diagram



6.3.6. Release From Deep Power-Down (ABH)

The Release from Deep Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from Deep Power-Down Mode or obtain the devices electronic identification (ID) number.

To release the device from Deep Power-Down Mode, the command is issued by driving the CS# pin low, shifting the instruction code (ABH) and driving CS# high as shown in the figure below. Release from Deep Power-Down Mode will take the time duration of tRES1 (See AC Characteristics) before the device resume to normal state and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When the command is used only to obtain the Device ID while the flash memory is not in Deep Power-Down Mode, the command is initiated by driving the CS# pin low and shifting the instruction code (ABH) followed by 3 dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in the figure below. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When the command is used to release the device from Deep Power-Down Mode and obtain the Device ID, the command is the same as previously described, and shown in the figure below, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume to normal mode and other command will be accepted. If the Release from Deep Power-Down and Read Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals to 1) the command will be ignored and will not affect the current cycle.

Figure 22. Release Power-Down Sequence Diagram

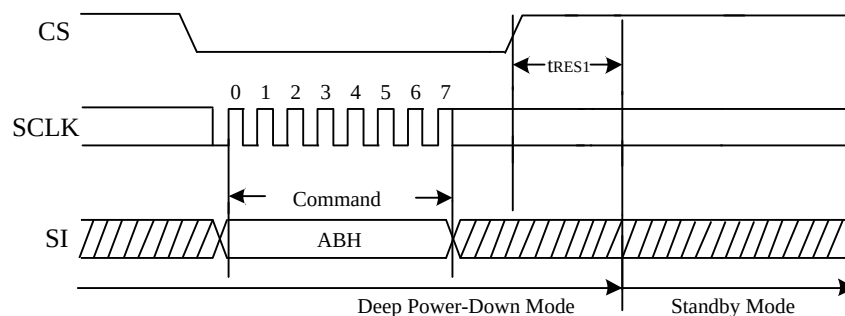
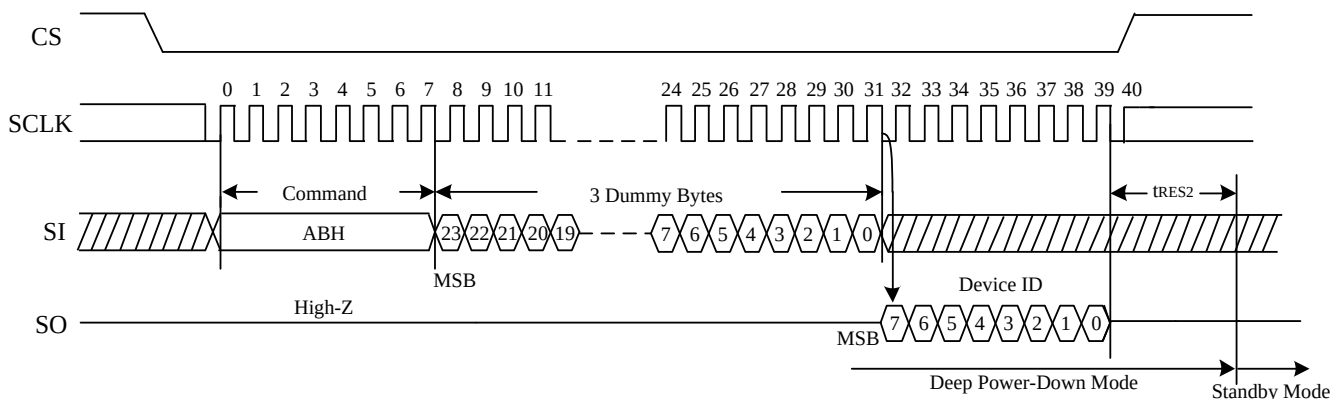
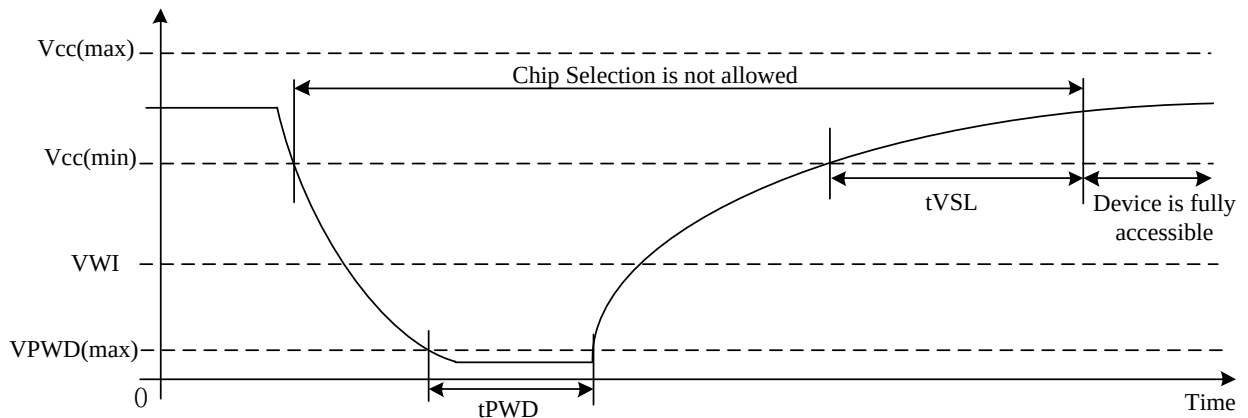


Figure 23. Release From Deep Power-Down/Read Device ID Sequence Diagram



7. ELECTRICAL CHARACTERISTICS

7.1. Power-Down & Power-On Timing



Power-Down & Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}	VCC(min) To CS# Low	100		μs
V_{WI}	Write Inhibit Voltage	1	1.5	V
V_{PWD}	VCC voltage needed to below V_{PWD} for initialization		-	V
t_{PWD}	The minimum duration for initialization	-		ms

7.2. Initial Delivery State

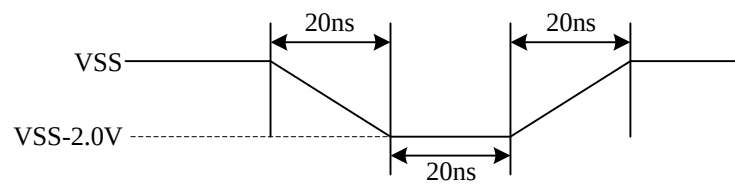
The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). All Status Register bits are 00H.

7.3. Absolute Maximum Ratings

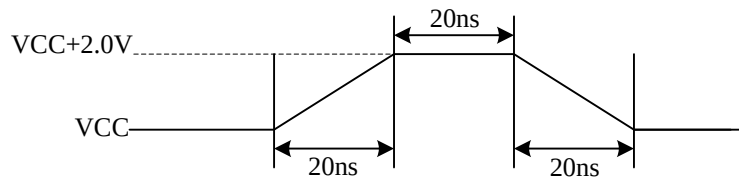
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85 -40 to 105	°C
Storage Temperature	-65 to 150	°C
Output Short Circuit Current	200	mA
Applied Input / Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform

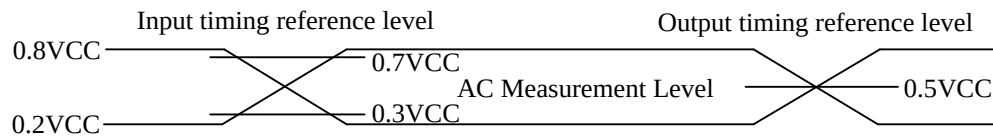


Maximum Positive Overshoot Waveform



7.4. Capacitance Measurement Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance	30			pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.2VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
	Output Timing Reference Voltage		0.5VCC		V	



Note: Input pulse rise and fall time are <5ns

7.5. DC Characteristics

Symbol	Parameter	Test Condition	1.65V-2.3V				2.3V-3.6V				Unit
			Min.	Typ. ⁽¹⁾	Max. (85 °C)	Max. (105 °C)	Min.	Typ. ⁽¹⁾	Max. (85 °C)	Max. (105 °C)	
ILI	Input Leakage Current				±1	±1			±2	±2	μA
ILO	Output Leakage Current				±1	±1			±2	±2	μA
ICC1	Standby Current	CS#=VCC VIN=VCC or VSS		7	15	25		7	20	30	μA
ICC2	Deep Power Down Current	CS#=VCC VIN=VCC or VSS		0.3	1	2		0.6	3.5	5	μA
ICC3	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 85MHz, Q=Open(*1 I/O)		1.7	2.5	3.5		3.2	4	5	mA
		CLK=0.1VCC/0.9VCC at 50MHz, Q=Open(*1 I/O)		1.2	1.7	2.5		2.2	2.7	4.5	mA
ICC3	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 33MHz, Q=Open(*1 I/O)		1	1.5	2.5		1.7	2.2	4	mA
		CLK=0.1VCC/0.9VCC at 1MHz, Q=Open(*1 I/O)		0.5	0.7	1.5		0.9	1.2	3	mA
ICC4	Operating Current(PP)	CS#=VCC		1.5	3	4		2.5	5	6	mA
ICC5	Operating Current(WRSR)	CS#=VCC		1.5	3	4		2.5	5	6	mA
ICC6	Operating Current(SE)	CS#=VCC		1.5	3	4		2.5	5	6	mA
ICC7	Operating Current(BE)	CS#=VCC		1.5	3	4		2.5	5	6	mA
ICC8	Operating Current(CE)	CS#=VCC		1.5	3	4		2.5	5	6	mA
VIL	Input Low Voltage		-0.5		0.3VCC	0.3VCC	-0.5		0.3VCC	0.3VCC	V
VIH	Input High Voltage		0.7 VCC				0.7 VCC				V
VOL	Output Low Voltage	IOL=100uA			0.2	0.2			0.2	0.2	V
VOH	Output High Voltage	IOH=-100uA	VCC-0.2				VCC-0.2				V

Note:

- Typical values given for TA=25 °C, VCC=3.0V.for the 2.3V-3.6V range
Typical values given for TA=25 °C, VCC=1.8V.for the 1.65V-2.3V range
- Value guaranteed by design and/or characterization, not 100% tested in production.

7.6. AC Characteristics

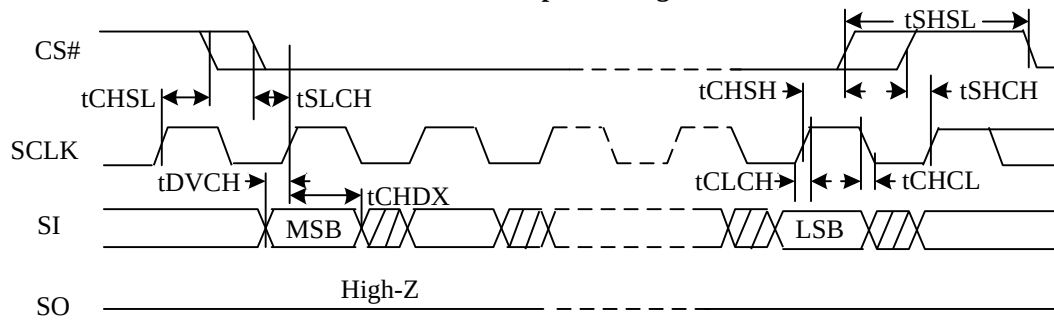
XTD25W02A (TA=-40 °C~85 °C/-40 °C~105 °C, VCC=1.65~3.6V, CL=30pF)

Symbol	Parameter	Min.	Typ. ⁽¹⁾	Max.	Unit
fC	Serial Clock Frequency For: all commands on 1.65-2.0V power supply except 03H			80	MHz
fC	Serial Clock Frequency For: all commands on 2.0-2.7V power supply except 03H			96	MHz
fC	Serial Clock Frequency For: all commands on 2.7-3.6V power supply except 03H			133	MHz
fC1	Serial Clock Frequency For 03H			50	MHz
tCLH ⁽²⁾	Serial Clock High Time	45% PC			ns
tCLL ⁽²⁾	Serial Clock Low Time	45% PC			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
tSLCH	CS# Active Setup Time (VCC=2.3V-3.6V)	5			ns
	CS# Active Setup Time (VCC=1.65V-2.3V)	10			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	1.2			ns
tCLQV	Clock Low To Output Valid (VCC=2.3V-3.6V)			6	ns
	Clock Low To Output Valid (VCC=1.65V-2.3V)			10	ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tDP	CS# High To Deep Power-Down Mode			3	µs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			50	µs
tRES2	CS# High To Standby Mode With Electronic Signature Read			50	µs
tRST_R	CS# High To Next Command After Reset (from read)			30	µs
tRST_P	CS# High To Next Command After Reset (from program)			30	µs
tRST_E	CS# High To Next Command After Reset (from erase)			30	µs
tW	Write Status Register Cycle Time		3.5	4	ms
tPP	Page Program Time		1	1.5	ms
tMSE	Mini Sector Erase Time (512 Bytes)		3.5	4	ms
tSE	Sector Erase Time (4K Bytes)		3.5	4	ms
tBE1	Block Erase Time (32K Bytes)		3.5	4	ms
tBE2	Block Erase Time (64K Bytes)		3.5	4	ms
tCE	Chip Erase Time		14	16	ms

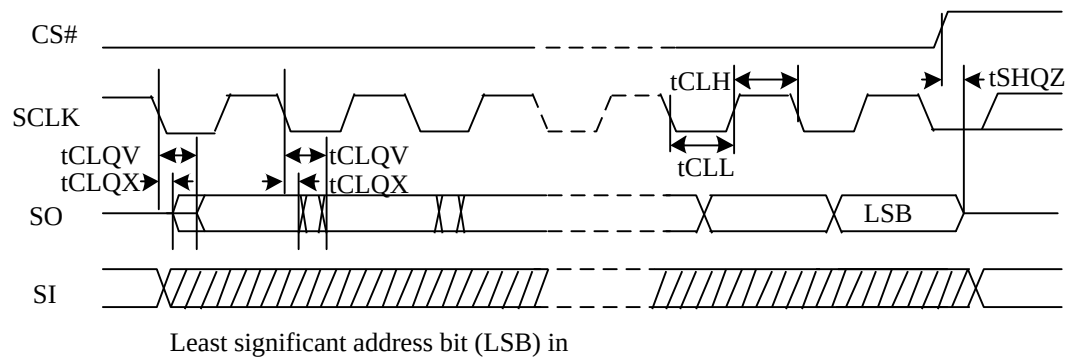
Note:

1. Typical values given for TA=25 °C, VCC = 3.3V.
2. Clock high or Clock low must be more than or equal to 45%PC. PC=1/fC(MAX).
3. Value guaranteed by design and/or characterization, not 100% tested in production.

Serial Input Timing



Output Timing



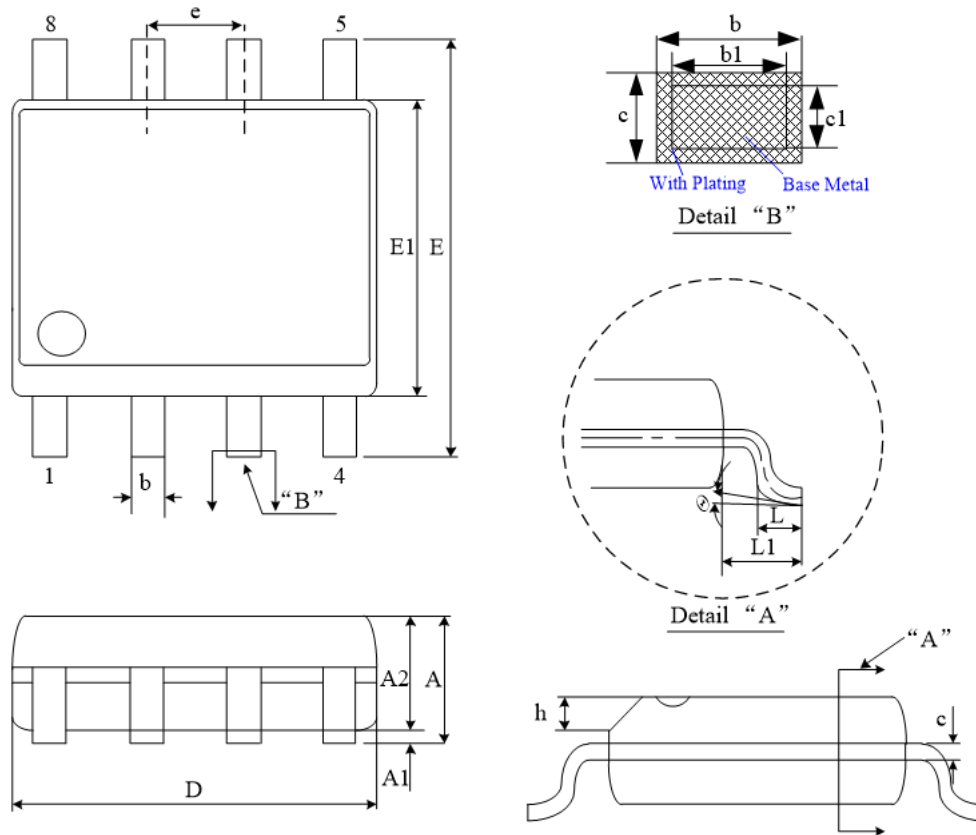
8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following

	<u>XTD</u>	<u>25W</u>	<u>02A</u>	<u>SO</u>	<u>I</u>	<u>G</u>	<u>U</u>
Company Prefix							
XT = XTX ETOX							
XTD = XTX NORD							
Product Family							
25W = 1.65~3.6V Serial Flash Memory with 4KB Uniform-Sector							
Product Density							
02A = 2M bit							
Product Package							
SO = SOP8 150mil							
DT = DFN8 2x3x0.4mm							
TS = TSSOP8 173mil							
DU = DFN6 1.2x1.2x0.4mm							
FU = FODFN6 1.2x0.7x0.4mm							
Temperature & Moisture Sensitivity Level							
I = Industrial Level Temperature. (-40°C to +85°C), MSL3							
H = Industrial Plus Level Temp. (-40°C to +105°C), MSL3							
Green Code							
G = Green/Reach Package							
Product Carrier							
U = Tube; T = Tape & Reel; A = Tray							

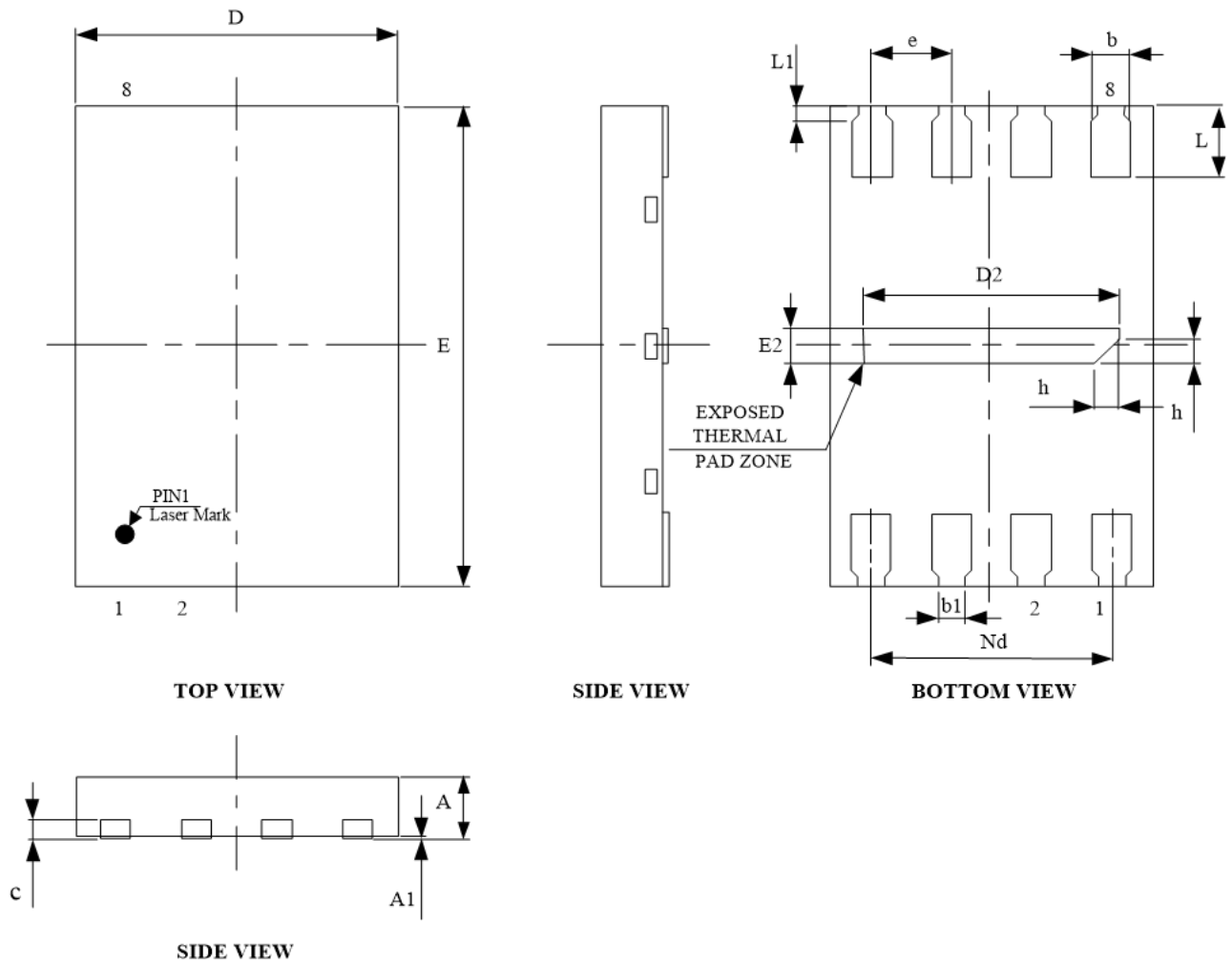
9. PACKAGE INFORMATION

9.1. Package SOP8 150mil



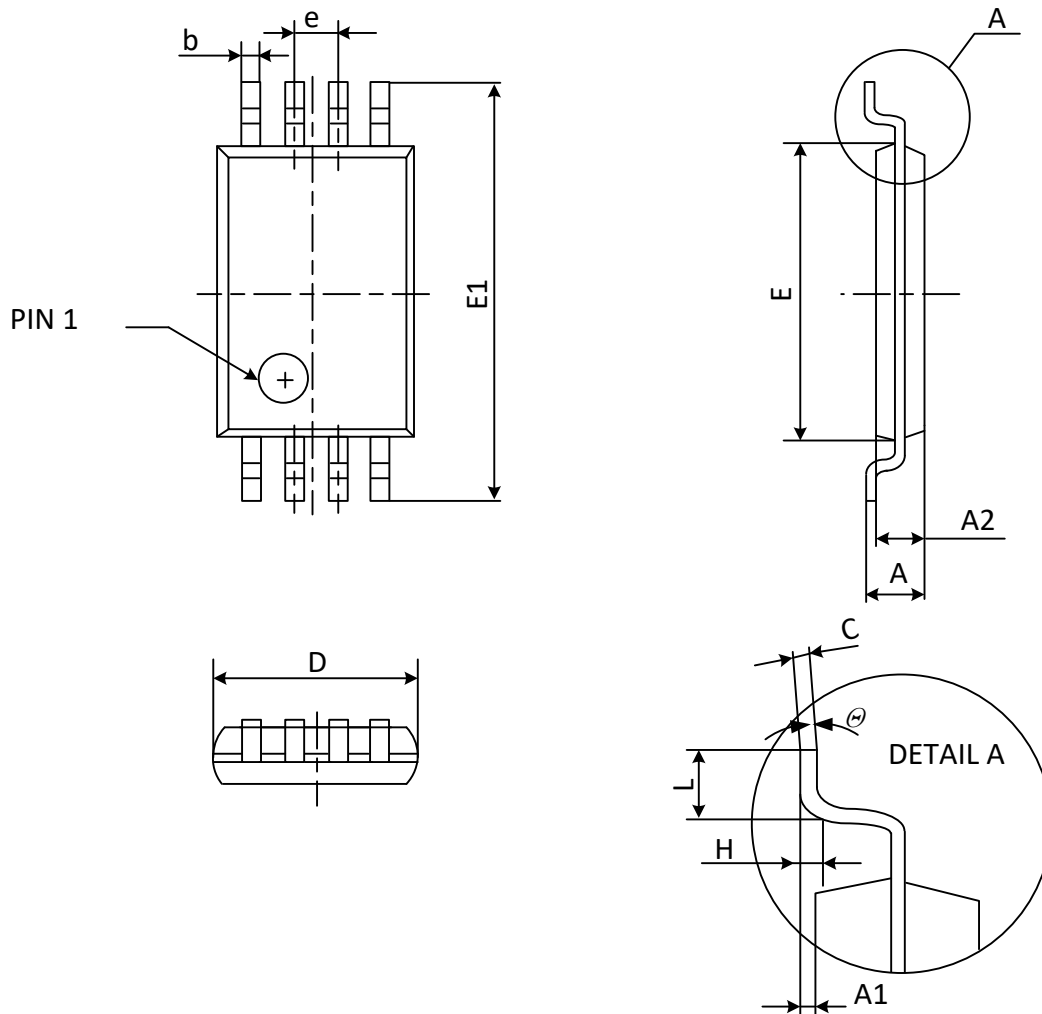
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.30	1.40	1.50
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0°	—	8°

9.2. Package DFN8 2x3x0.4mm



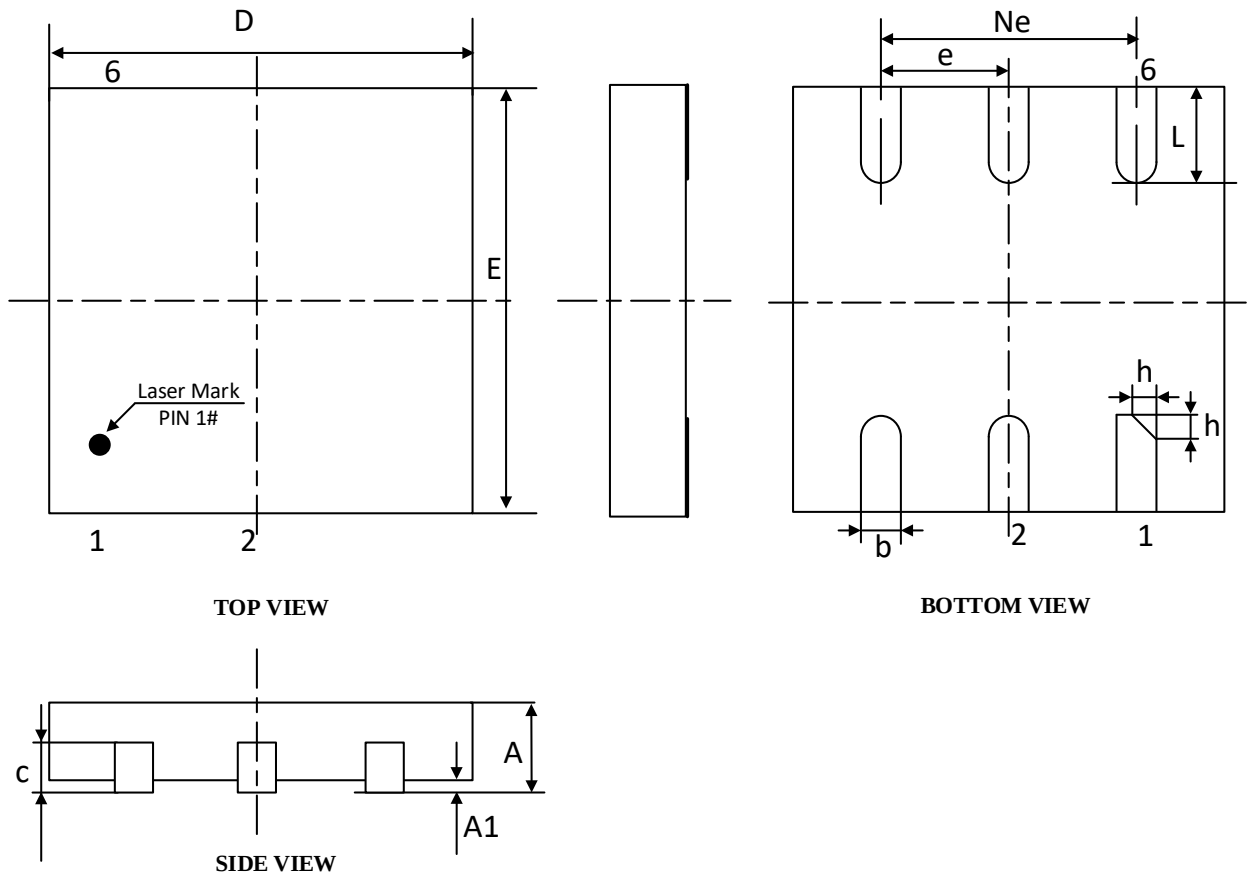
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	—	0.40
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.127REF		
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
L	0.40	0.45	0.50
L1	0.05	0.10	0.15
h	0.10	0.15	0.20

9.3. Package TSSOP8 173mil



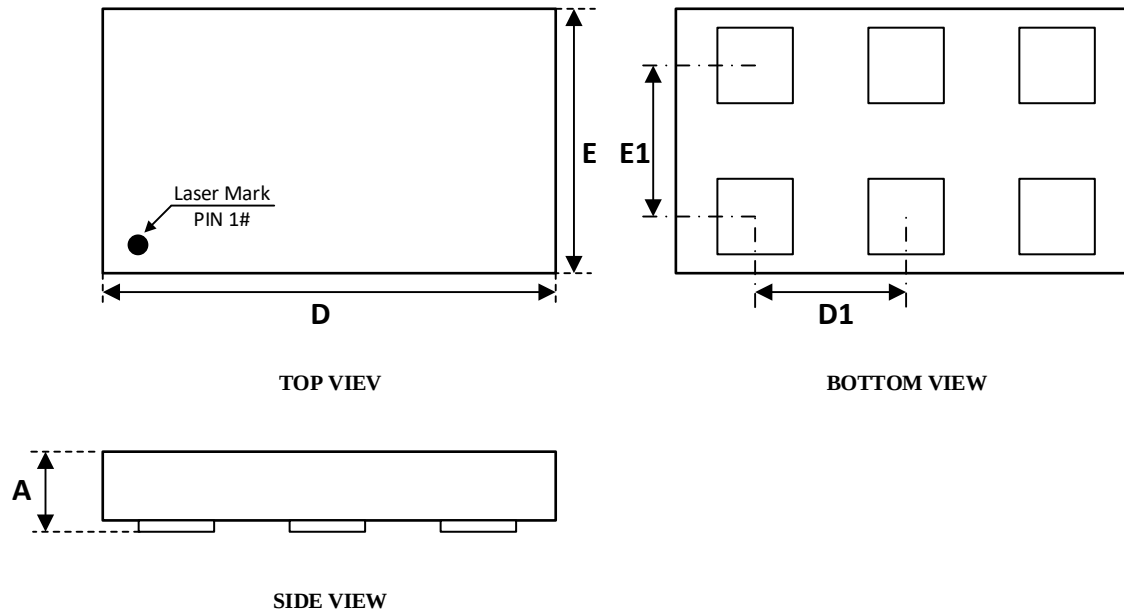
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

9.4. Package DFN6 1.2x1.2x0.4mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	—	0.40
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
c	0.127REF		
D	1.15	1.20	1.25
E	1.15	1.20	1.25
e	0.40BSC		
Ne	0.80BSC		
L	0.35	0.40	0.45
h	0.12REF		

9.5. Package FODFN6 1.2x0.7x0.4mm



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.350	-	0.400
D	1.200	1.225	1.250
D1	0.4		
E	0.700	0.725	0.750
E1	0.35		
Pad Size	0.2 x 0.2		



10. REVISION HISTORY

Revision	Description	Date
1.0	Initial version	Sep 26, 2025
1.1	Added OPNs: XTD25W02ADUIGT (DFN6 1.2x1.2x0.4mm), XTD25W02AFUIGT (FODFN6 1.2x0.7x0.4mm)	Apr 07, 2026

*Disclaimer: Information herein is furnished solely with the related products. The Company reserves the right to make changes to this document, products or services at any time without notice, and assumes no liability for any conflicts or incompatibilities resulting from such changes.