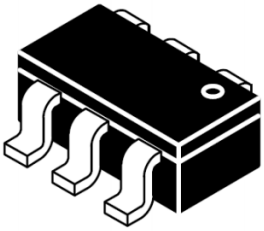
USRV05-4

4-Line Uni-directional TVS Diode

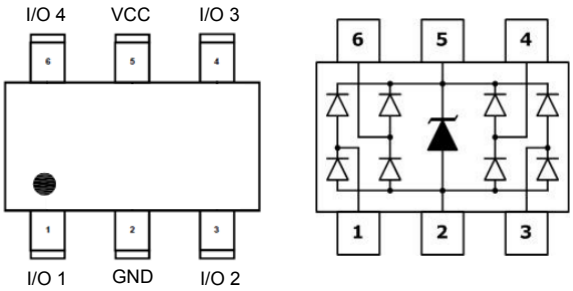
Features

- Ultra low leakage: nA level
- Operating voltage: 5V
- Low clamping voltage
- Up to 4 data lines and one power line protects
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±20kV
    - Contact discharge: ±20kV
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) 5A/17A (8/20μs)
- RoHS Compliant

Dimensions SOT-26



Pin Configuration



Applications

- USB 2.0 power and data line
- Set-top box and digital TV
- Digital video interface (DVI)
- Notebook Computers
- SIM Ports
- 10/100/1000 Ethernet

Mechanical Characteristics

- Package: SOT-26
- Lead Finish: Lead Free
- UL Flammability Classification Rating 94V-0
- Quantity Per Reel:3,000pcs
- Reel Size:7inch
- Device Marking: V05

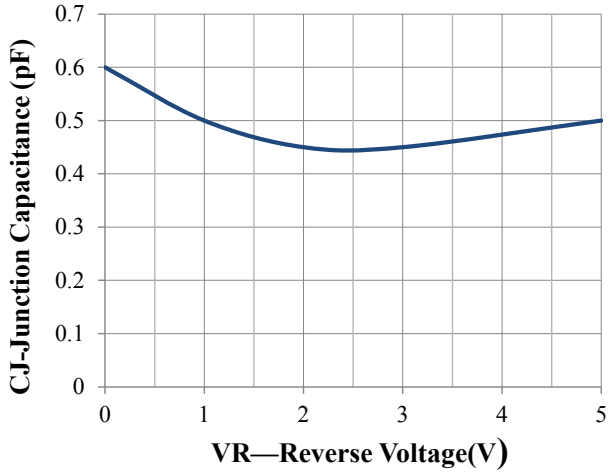
Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs,I/O-GND)	Ppk	60	W
Peak Pulse Power (8/20μs,Vcc-GND)	Ppk	300	W
Peak Pulse Current (8/20μs,I/O-GND)	IPP	5	A
Peak Pulse Current (8/20μs,Vcc-GND)	IPP	17	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	$V_{ESD,VDD}$ $V_{ESD,I/O}$	±20 ±20	kV
Operating Temperature Range	TJ	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

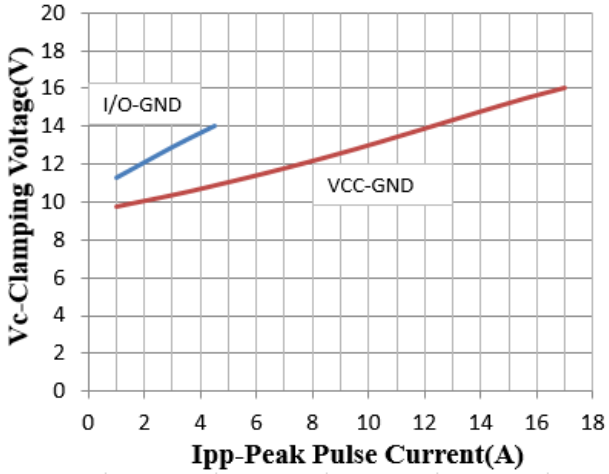
Electrical Characteristics(TA=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Pin 5 to GND,I/O-GND			5. 0	V
Breakdown Voltage	V_{BR}	I_T = 1mA(Pin 5 to GND,I/O-GND)	6.0	7.5	8.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5. 0V			0.5	µA
Forward Breakdown Voltage	V_F	I_F= 15mA,GND to Pin 5/IO		0.8	1.0	V
Clamping Voltage	V_C	IPP = 5A (8 x 20µs pulse, I/O to GND)		14.0	15.0	V
Clamping Voltage	V_C	IPP = 17A (8 x 20µs pulse,Pin 5 to GND)		16.0	18. 0	V
Junction Capacitance	C_J	V_{pin5} = 5V, I/O=0V, f = 1MHz,I/O-GND		0.6	0.7	pF
Junction Capacitance	C_J	V_{pin5} = 5V, I/O=0V, f = 1MHz,I/O-I/O pins		0.3	0.4	pF

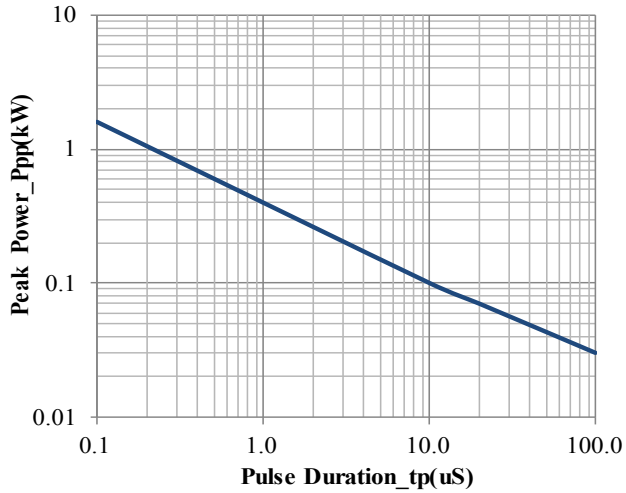
Typical Performance Characteristics(TA=25°C unless otherwise specified)



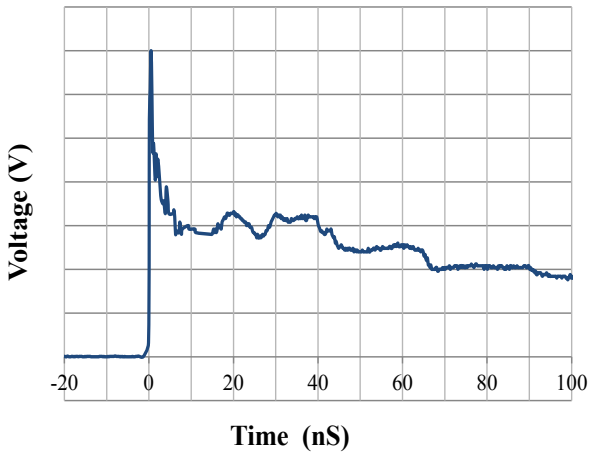
Junction Capacitance vs. Reverse Voltage



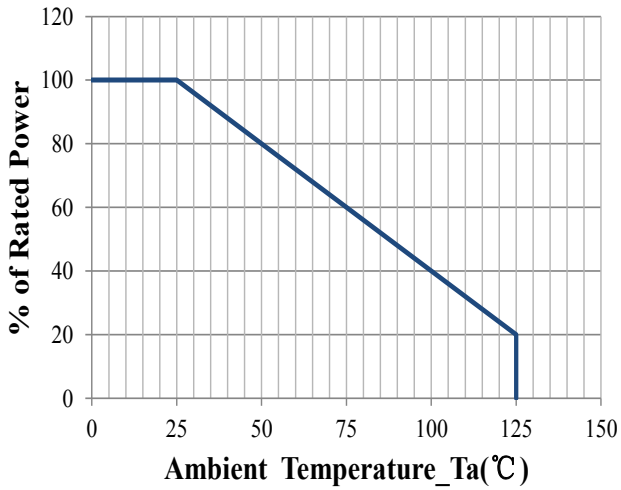
Clamping Voltage vs. Peak Pulse Current



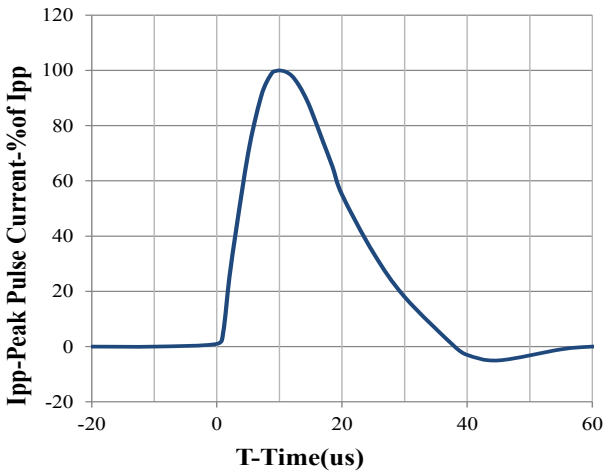
Peak Pulse Power vs. Pulse Time



IEC61000−4−2 Pulse Waveform



Power Derating Curve



8 X 20us Pulse Waveform

Applications Information

Figure 1. Data Line and Power Supply Protection Using V_{CC} as reference

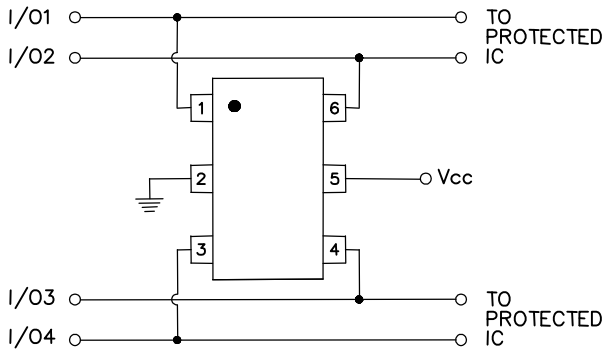


Figure 2. Data Line Protection with Bias and Power Supply Isolation Resistor

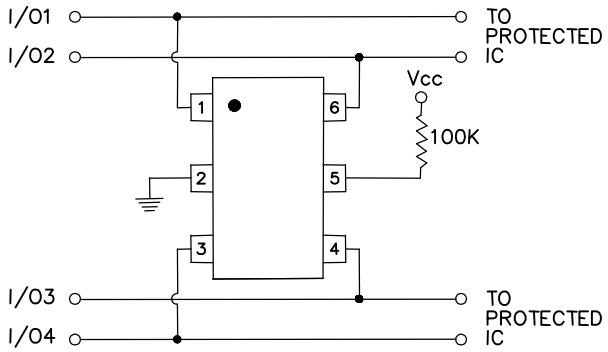
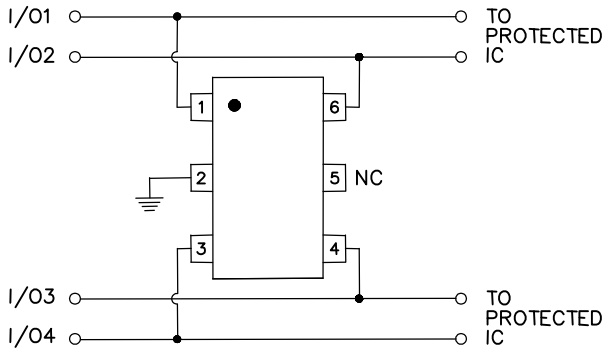


Figure 3. Data Line Protection Using Internal TVS Diode as Reference



Device Connection Options for Protection of Four High-Speed Data Lines

The USRV05-4 is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode VF) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (REF1) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail (See Figure1).

2. The USRV05-4 can be isolated from the power supply by adding a series resistor between pin 5 and VCC. A value of 100kΩ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance (See Figure2).

3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop) (See Figure3).

Applications Information (Continue)

Figure 4. Video Interface Protection

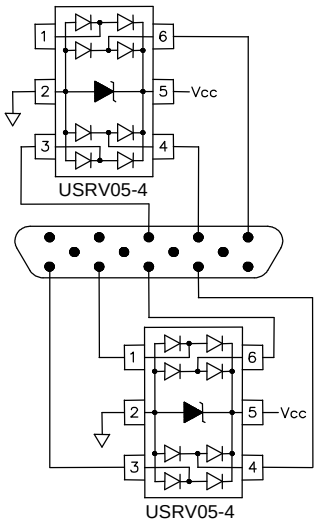


Figure 5 - Dual USB Port Protection

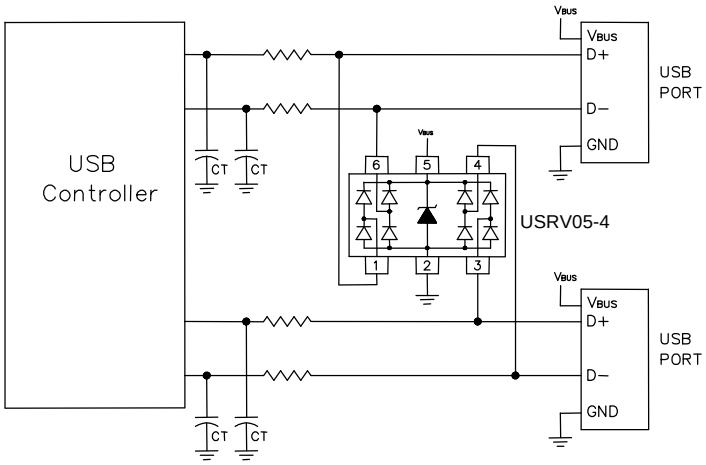
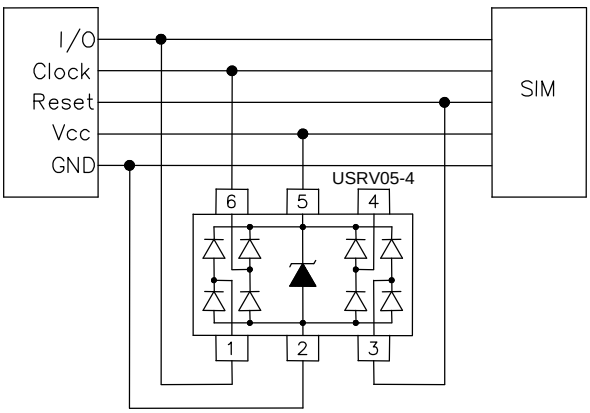


Figure 6 - SIM Port



Video Interface Protection

Video interfaces are susceptible to transient voltages resulting from electrostatic discharge (ESD) and "hot plugging" cables. If left unprotected, the video interface IC may be damaged or even destroyed. Protecting a high-speed video port presents some unique challenges. First, any added protection device must have extremely low capacitance and low leakage current so that the integrity of the video signal is not compromised. Second, the protection component must be able to absorb high voltage transients without damage or degradation. As a minimum, the device should be rated to handle ESD voltages per IEC61000-4-2, level 4 (±15kV air, ±8kV contact). The clamping voltage of the device (when conducting high current ESD pulses) must be sufficiently low enough to protect the sensitive CMOS IC. If the clamping voltage is too high, the "protected" device may latch-up or be destroyed. Finally, the device must take up a relatively small amount of board space, particularly in portable applications such as notebooks and handhelds. The USRV05-4 is designed to meet or exceed all of the above criteria. A typical video interface protection circuit is shown in Figure 4. All exposed lines are protected including R, G, B, H-Sync, V-Sync, and the ID lines for plug and play monitors.

Universal Serial Bus ESD Protection

The USRV05-4 may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure5). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

Applications Information (Continue)

DVI Protection

The small geometry of a typical digital-visual interface (DVI) graphic chip will make it more susceptible to electrostatic discharges (ESD) and cable discharge events (CDE). Transient protection of a DVI port can be challenging. Digital-visual interfaces can often transmit and receive at a rate equal to or above 1Gbps. The high-speed data transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the protected IC. The USRV05-4 has a low typical insertion loss of <0.4dB at 1GHz (I/O to ground) to ensure signal integrity and can protect the DVI interface to the 8kV contact and 15kV air ESD per IEC 61000-4-2 and CDE.

Figure 7 shows how to design the USRV05-4 into the DVI circuit on a flat panel display and a PC graphic card. The USRV05-4 is configured to provide common mode and differential mode protection. The internal TVS of the USRV05-4 acts as a 5 volt reference. The power pin of the DVI circuit does not come out through the connector and is not subjected to external ESD pulse; therefore, pin 5 should be left unconnected. Connecting pin 5 to Vcc of the DVI circuit may result in damage to the chip from ESD current.

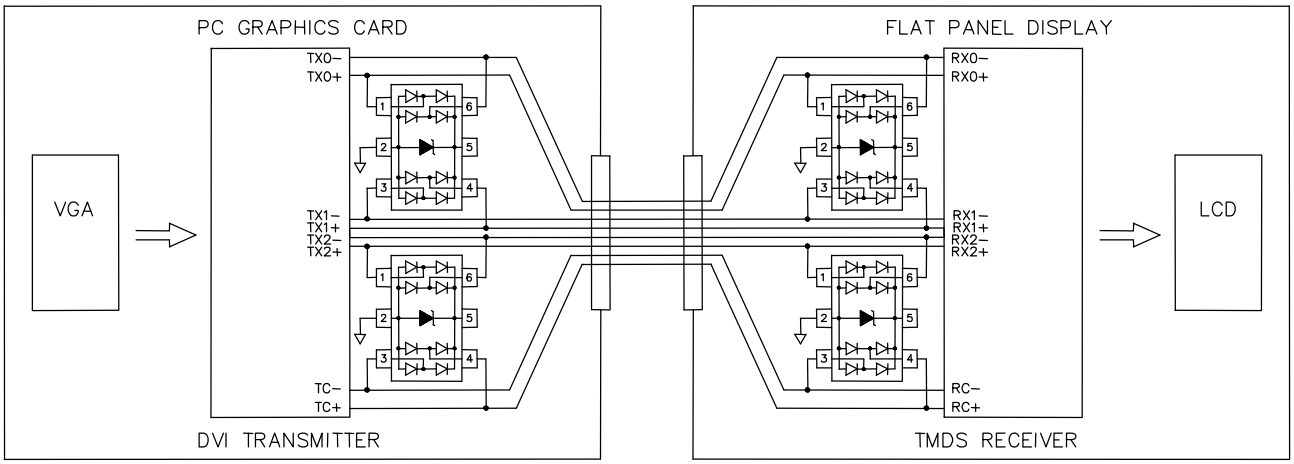


Figure 7 . Digital Video Interface (DVI) Protection

10/100 ETHERNET PROTECTION

Ethernet ICs are vulnerable to damage from electro-static discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC 61000-4-2. If the discharge is catastrophic, it will destroy theprotected IC. If it is less severe, it will cause latent failures that are very difficult to find.

10/100 Ethernet operates at 125MHz clock over a twisted pair interface. In a typical system, the twisted-pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmit or receive line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 8 shows how to design the USRV05-4 on the line side of a 10/100 ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. If more common mode protection is needed, figure 9 shows how to design the USRV05-4 on the IC side of the 10/100.

Applications Information (Continue)

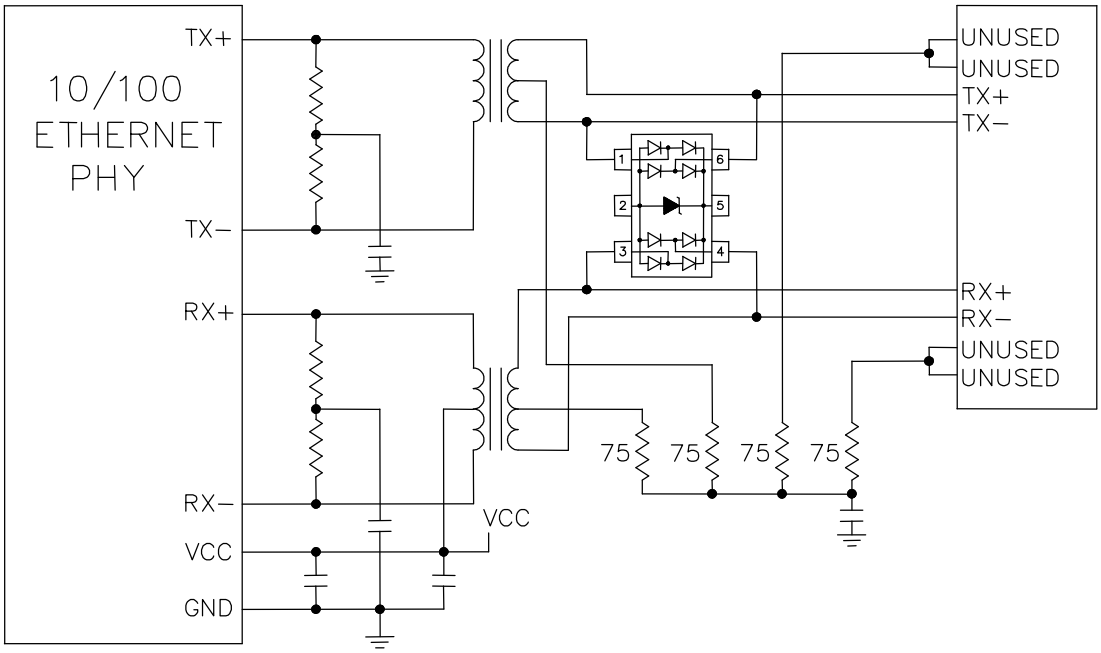


Figure 8 - 10/100 Ethernet Differential Protection

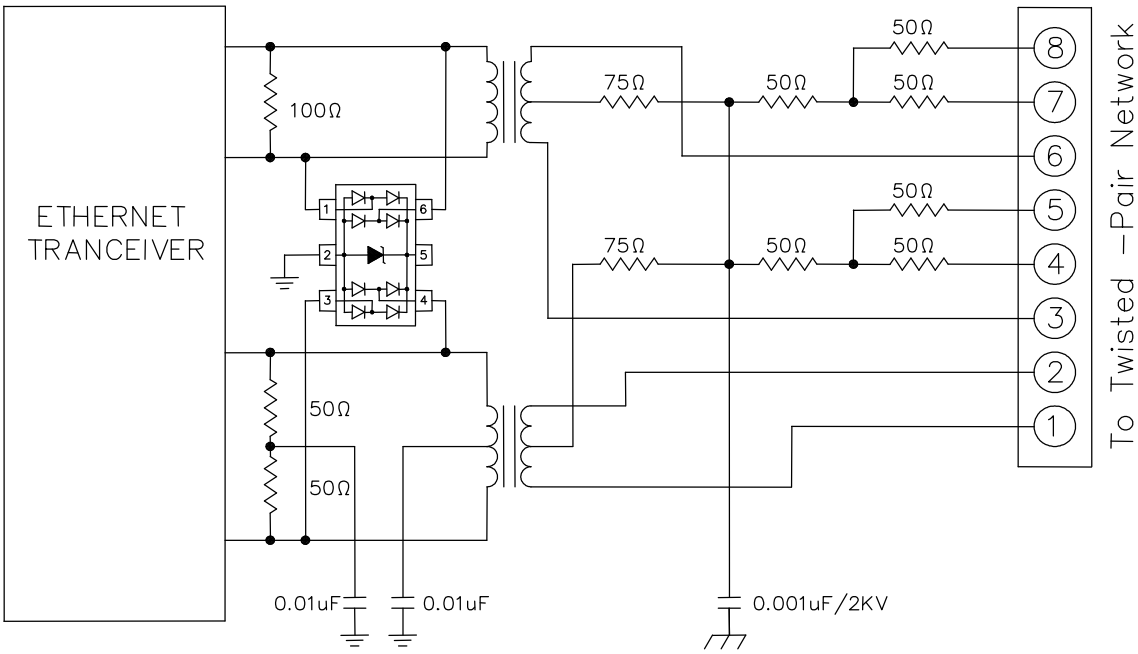
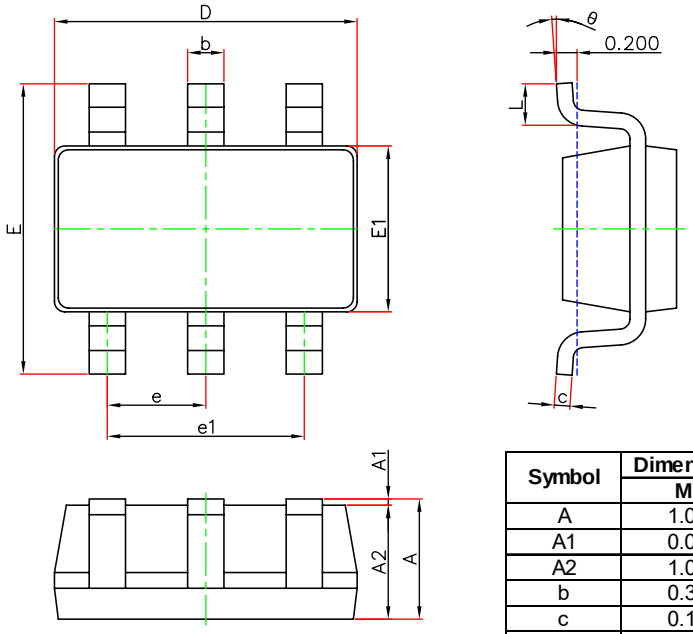


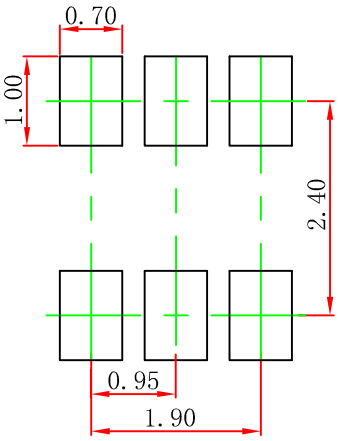
Figure 9 - 10/100 Ethernet Differential and Common Mode Protection

SOT-26 Package Outline Drawing



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Suggested Land Pattern



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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