FEATURES

- 10-Bit CMOS Voltage Output DAC in an
- 8-Terminal Package
- 5V Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range: 2 Times the Reference
- Input Voltage Internal Power-On Reset
- Low Power Consumption: 1.75mW Max
- Update Rate of 1.21MHz
- Settling Time to 0.5LSB: 12.5μs Typ
- Monotonic Over Temperature
- Battery-Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

DIP-8

SOP-8

MSOP-8

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
HGC5615CN	DIP-8	C5615C	TUBE	2000pcs/box
HGC5615CM/TR	SOP-8	C5615C	REEL	2500pcs/reel
HGC5615CMM/TR	MSOP-8	C5615C	REEL	3000pcs/reel
HGC5615IN	DIP-8	C5615I	TUBE	2000pcs/box
HGC5615IM/TR	SOP-8	C5615I	REEL	2500pcs/reel
HGC5615IMM/TR	MSOP-8	C5615I	REEL	3000pcs/reel

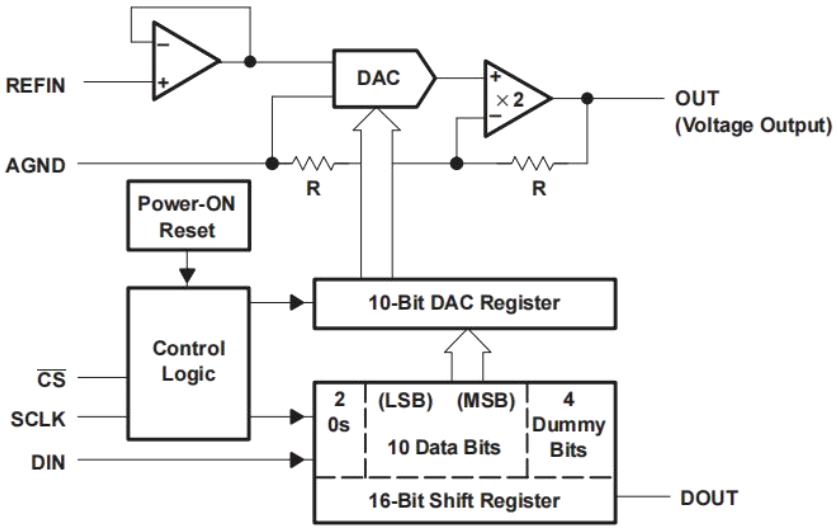
DESCRIPTION

The HGC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

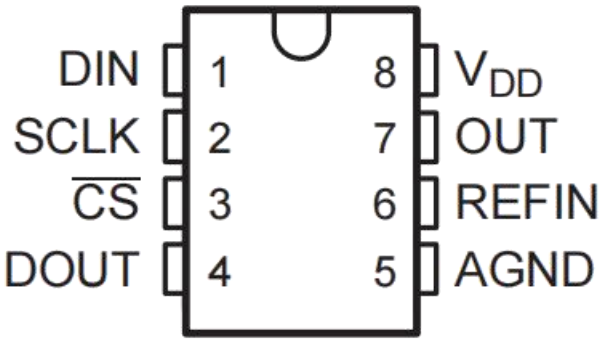
Digital control of the HGC5615 isover a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOP/MSOP

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
$\overline{CS}$	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
V_{DD}	8		Positive power supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage (V_{DD} to AGND)		7V
Digital input voltage range to AGND		–0.3V to V_{DD} + 0.3V
Reference input voltage range to AGND		–0.3V to V_{DD} + 0.3V
Output voltage at OUT from external source		V_{DD} + 0.3V
Continuous current at any terminal		20mA
Operating free-air temperature range, T_A	HGC5615C	0 °C to +70°C
	HGC5615I	–40°C to +85°C
Storage temperature range, T_{stg}		–65°C to +150°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		+260°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}		2.4			V
Low-level digital input voltage, V_{IL}			0.8		V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	V_{DD}–2	V
Load resistance, R_L			2		kΩ
Operating free-air temperature, T_A	HGC5615C	0		70	°C
	HGC5615I	-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, VDD = 5V±5%, Vref = 2.048V (unless otherwise noted)

STATIC DAC SPECIFICATIONS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10			bits
Integral nonlinearity, end point adjusted (INL)		Vref=2.048V, See(1)			±1	LSB
Differential nonlinearity (DNL)		Vref=2.048V, See(2)		±0.1	±0.5	LSB
EZS	Zero-scale error (offset error at zero scale)	Vref=2.048V, See(3)				LSB
Zero-scale-error temperature coefficient		Vref=2.048V, See(4)		3		ppm/°C
EG	Gain error	Vref=2.048V, See(5)			±3	LSB
Gain-error temperature coefficient		Vref=2.048V, See(6)		1		ppm/°C
PSRR Power-supply rejection ratio	Zero scale	See (7)(8)	80			dB
	Gain		80			
Analog full scale output		RL = 100k	2Vref(1023/1024)			V

(1) The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text). Tested from code 3 to code 1024.

(2) The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 3 to code 1024.

(3) Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).

(4) Zero-scale-error temperature coefficient is given by: EZS TC = [EZS (Tmax) – EZS (Tmin)]/Vref 106/(Tmax– Tmin).

(5) Gain error is the deviation from the ideal output (Vref – 1LSB) with an output load of 10k excluding the effects of the zero-scale error.

(6) Gain temperature coefficient is given by: EG TC = [EG(Tmax) – EG (Tmin)]/Vref 106/(Tmax– Tmin).

(7) Zero-scale-error rejection ratio (EZS-RR) is measured by varying the VDD from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the zero-code output voltage.

(8) Gain-error rejection ratio (EG-RR) is measured by varying the VDD from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

VOLTAGE OUTPUT (OUT)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L= 10k		0		V_{DD}–0.4	V
Output load regulation accuracy		$V_{O(OUT)}$ =2V R_L = 2k				0.5	LSB
I_{OSC}	Output short circuit current	OUT to V_{DD} or AGND			20		mA
$V_{OL(low)}$	Output voltage, low-level	$I_{O(OUT)}$≤5mA				0.25	V
$V_{OH(high)}$	Output voltage, high-level	$I_{O(OUT)}$≤– 5mA		4.75			V
REFERENCE INPUT (REFIN)							
V_I	Input voltage			0		V_{DD}–2	V
r_i	Input resistance			10			MΩ
C_i	Input capacitance				5		pF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)							
V_{IH}	High-level digital input voltage			2.4			V
V_{IL}	Low-level digital input voltage					0.8	V
I_{IH}	High-level digital input current	V_I = V_{DD}				±1	μA
I_{IL}	Low-level digital input current	V_I = 0				±1	μA
C_i	Input capacitance				8		pF
DIGITAL OUTPUT (DOUT)							
V_{OH}	Output voltage, high-level	I_O = –2mA		VDD-1			V
V_{OL}	Output voltage, low-level	I_O = 2mA				0.4	V
POWER SUPPLY							
V_{DD}	Supply voltage			4.5	5	5.5	V
I_{DD}	Power supply current	V_{DD} = 5.5V, No load, All inputs=0V or V_{DD}	V_{ref} = 0		150	250	μA
		V_{DD}= 5.5V, No load, All inputs=0V or V_{DD}	V_{ref} = 2.048V		230	350	μA
ANALOG OUTPUT DYNAMIC PERFORMANCE							
Signal-to-noise + distortion, S/(N+D)		V_{ref} = 1V_{PP} at 1kHz +2.048Vdc, code = 11 1111 1111(1)		60			dB

(1) The limiting frequency value at 1V

DIGITAL INPUT TIMING REQUIREMENTS (See Figure 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(DS)}$	Setup time, DIN before SCLK high	45			ns
$t_{h(DH)}$	Hold time, DIN valid after SCLK high	0			ns
$t_{su(CSS)}$	Setup time, $\overline{CS}$ low to SCLK high	1			ns
$t_{su(CS1)}$	Setup time, $\overline{CS}$ high to SCLK high	50			ns
$t_{h(CSH0)}$	Hold time, SCLK low to $\overline{CS}$ low	1			ns
$t_{h(CSH1)}$	Hold time, SCLK low to $\overline{CS}$ high	0			ns
$t_{w(CS)}$	Pulse duration, minimum chip select pulse width high	20			ns
$t_{w(CL)}$	Pulse duration, SCLK low	25			ns
$t_{w(CH)}$	Pulse duration, SCLK high	25			ns

OUTPUT SWITCHING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(DOUT)}$ Propagation delay time, DOUT	C_L = 50pF			50	ns

OPERATING CHARACTERISTICS

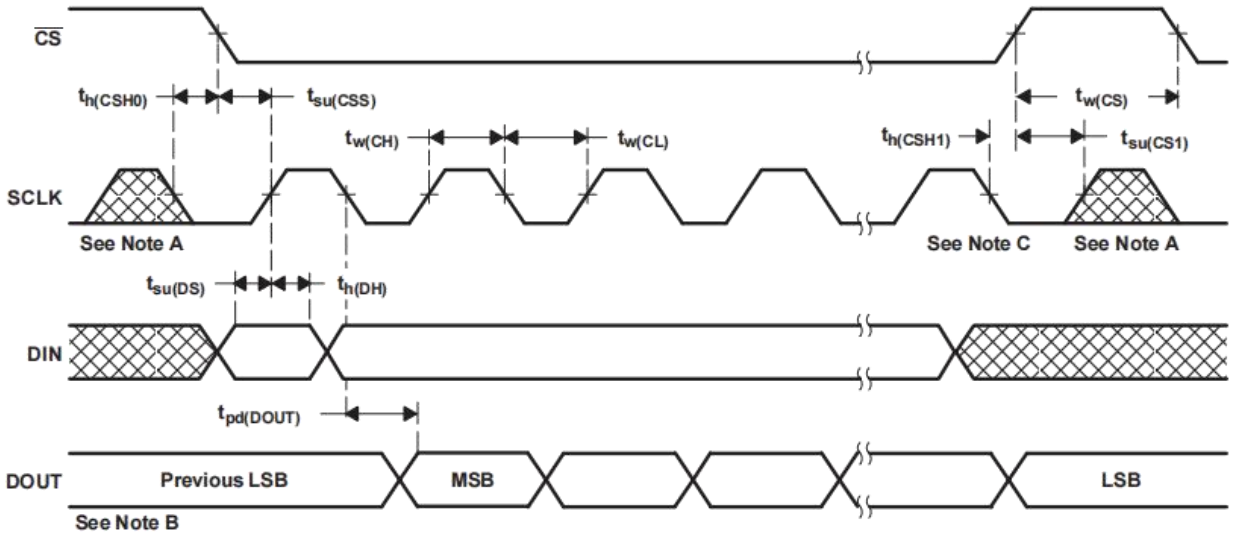
over recommended operating free-air temperature range, V_{DD}=5V±5%, Vref = 2.048V(unless otherwise notde)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG OUTPUT DYNAMIC PERFORMANCE							
SR	Output slew rate	C_L = 100pF, T_A= +25°C	R_L= 10kΩ,	0.3	0.5		V/μs
t_s	Output settling time	To 0.5LSB, R_L = 10kΩ,	C_L = 100pF, (1)		12.5		μs
Glitch energy		DIN = All 0s to all 1s			5		nV-s
REFERENCE INPUT (REFIN)							
Reference feedthrough		REFIN = 1VPP at 1kHz + 2.048Vdc (2)			-80		dB
Reference input bandwidth (f–3dB)		REFIN = 0.2VPP + 2.048Vdc			30		kHz

(1) Settling time is the time for the output signal to remain within 0.5LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

(2) Reference feedthrough is measured at the DAC output with an input code = 000 hex and a Vref input = 2.048Vdc + 1Vpp at 1kHz.

PARAMETER MEASUREMENT INFORMATION



NOTES:

A. The input clock, applied at the SCLK terminal, should be inhibited low when $\overline{CS}$ is high to minimize clock feedthrough.

B. Data input from preceeding conversion cycle.

C. Sixteenth SCLK falling edge

Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

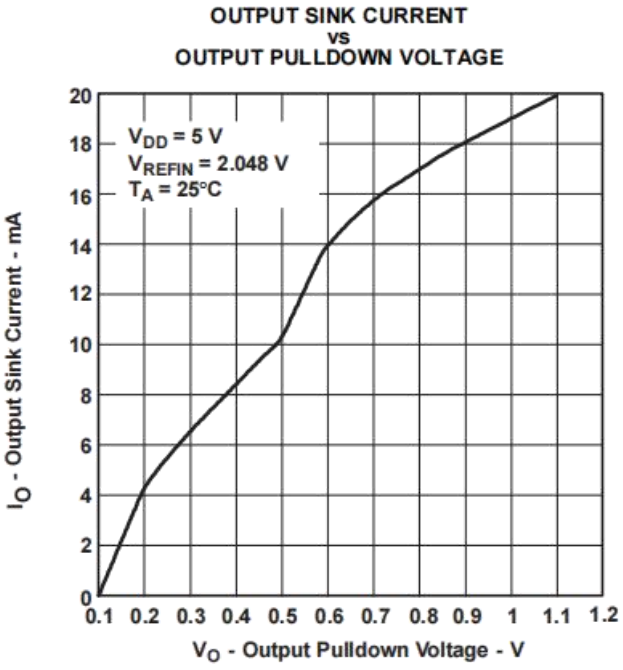


Figure 2.

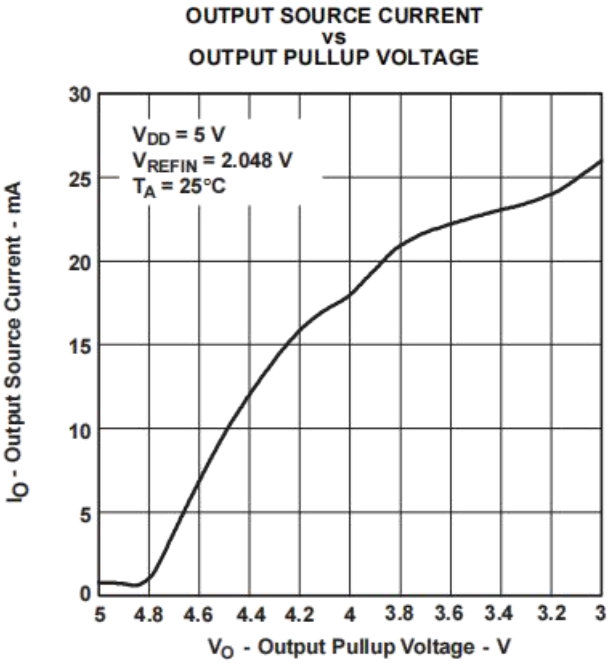


Figure 3.

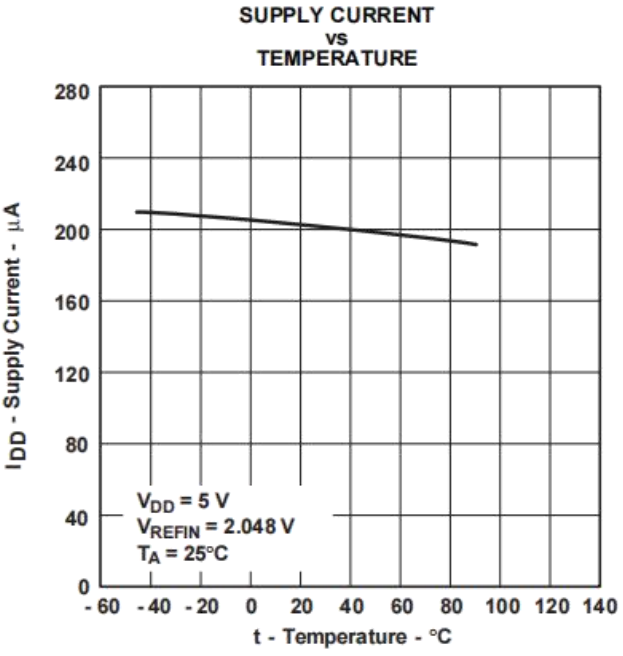


Figure 4.

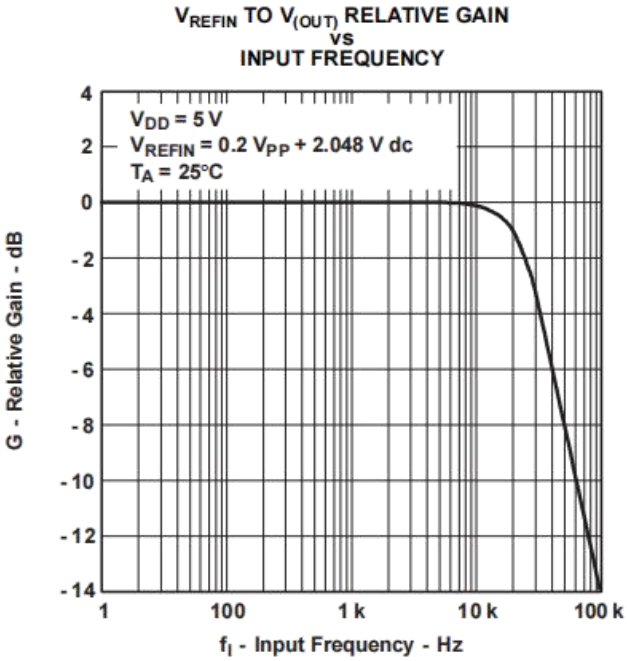


Figure 5.

TYPICAL CHARACTERISTICS (continued)

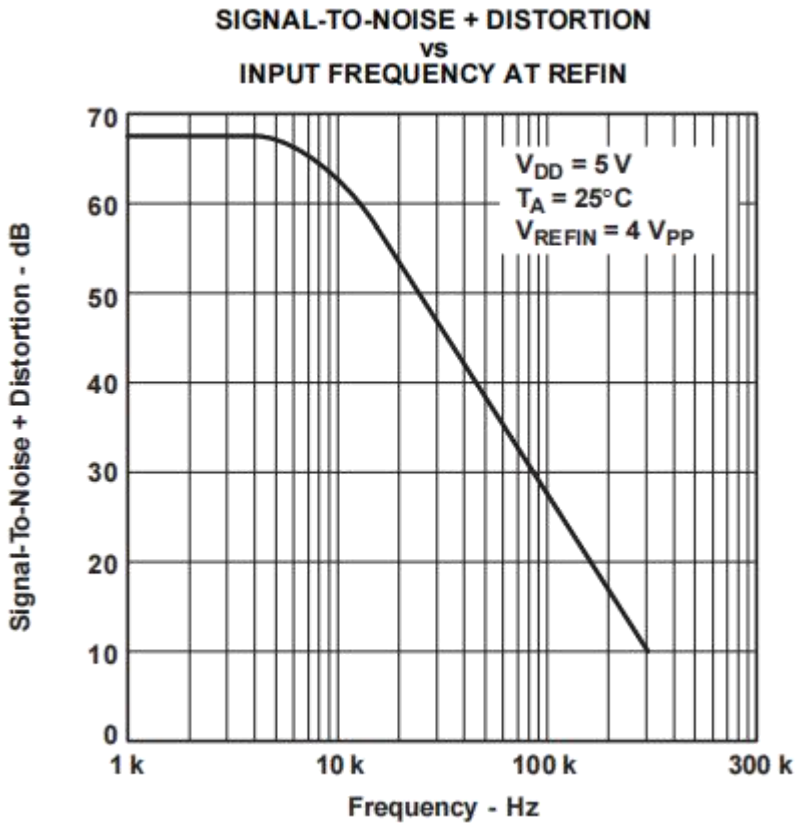


Figure 6.

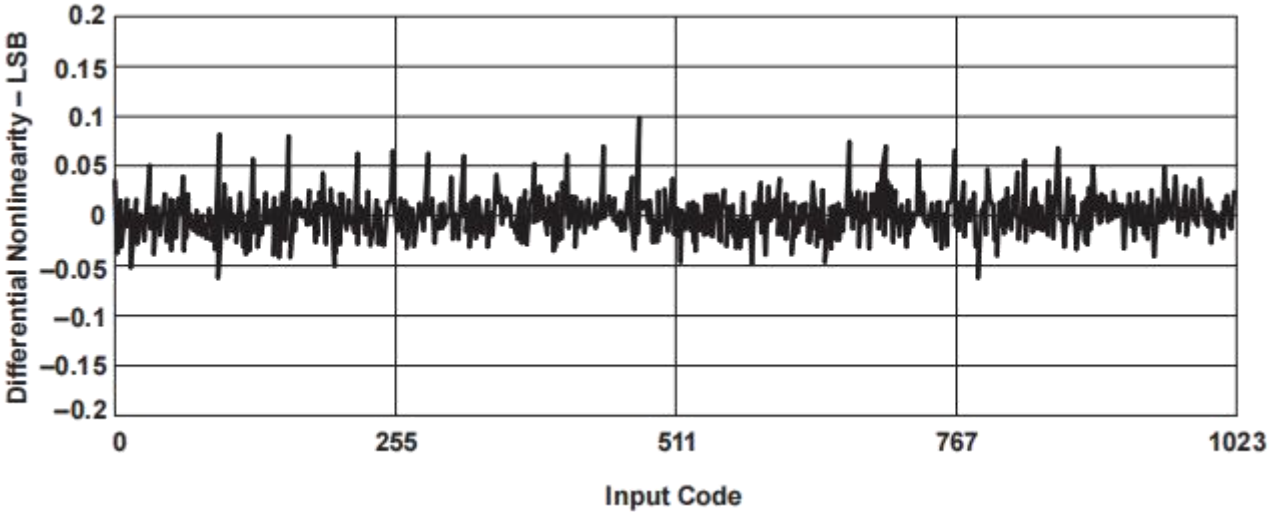


Figure 7. Differential Nonlinearity With Input Code

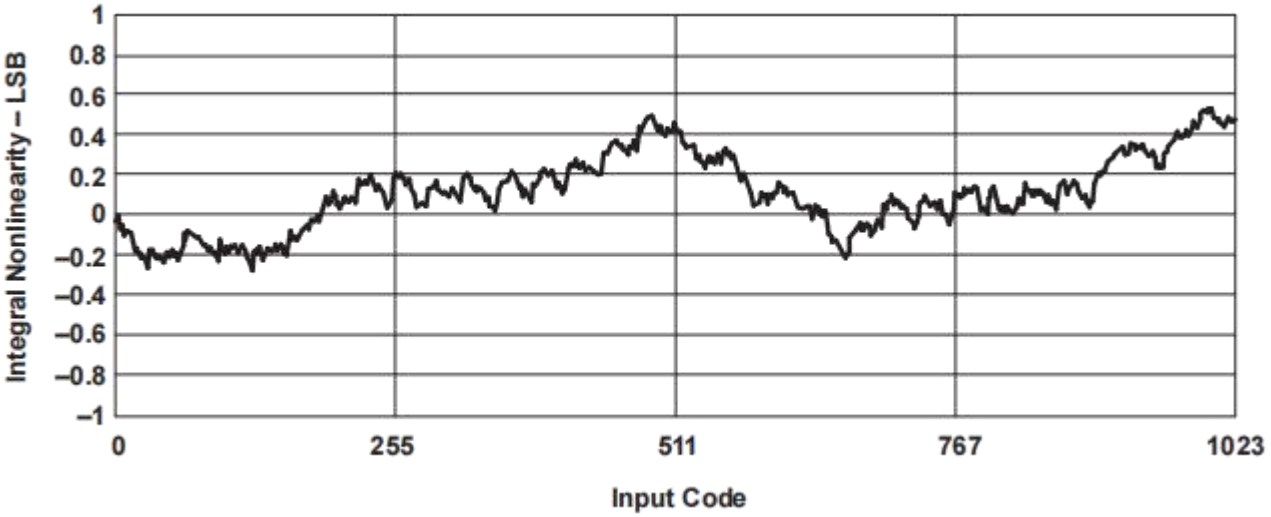


Figure 8. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

GENERAL FUNCTION

The HGC5615 uses a resistor stringnetwork buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the HGC5615 is the same polarity as the reference input (see Table 1). An internal circuit resets the DAC register to all zeros on power up.

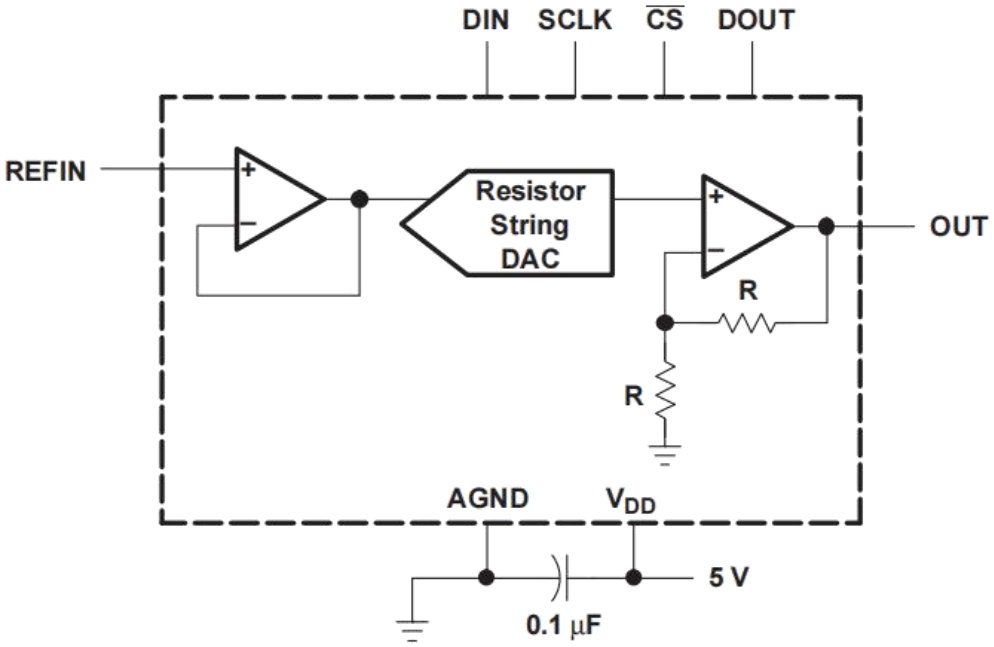


Figure 9. HGC5615Typical Operating Circuit

Table 1. Binary Code Table (0V to 2VREFINOutput), Gain = 2

INPUT(1)			OUTPUT
1111	1111	11(00)	$2(V_{REFIN})\frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2(V_{REFIN})\frac{513}{1024}$
1000	0000	00(00)	$2(V_{REFIN})\frac{512}{1024} = V_{REFIN}$
0111	1111	11(00)	$2(V_{REFIN})\frac{511}{1024}$
	:		:
0000	0000	01(00)	$2(V_{REFIN})\frac{1}{1024}$
0000	0000	00(00)	0 V

1. A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.

BUFFER AMPLIFIER

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2k load with a 100pF load capacitance. Settling time is 12.5 s typical to within 0.5LSB of final value.

EXTERNAL REFERENCE

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10M and the REFIN input capacitance is typically 5pF independent of input code. The reference voltage determines the DAC full-scale output.

LOGIC INTERFACE

The logic inputs function with either TTL or CMOS logic levels. However, using rail-to-rail CMOS logic achieves the lowest power dissipation. The power requirement increases by approximately 2 times when using TTL logic levels.

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the HGC5615 timing. The maximum serial clock rate is:

$$f_{(SCLK)max} = \frac{1}{t_{w(CH)} + t_{w(CL)}}$$

or approximately 14MHz. The digital update rate is limited by the chip-select period, which is:

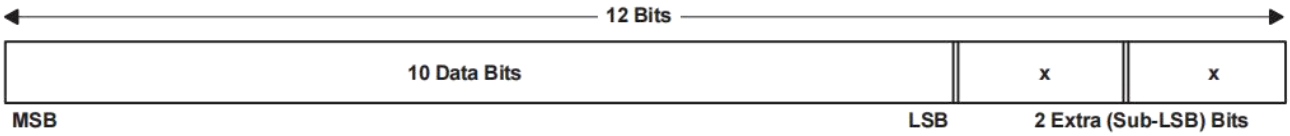
$$t_{p(CS)} = 16 \times \left(t_{w(CH)} + t_{w(CL)}\right) + t_{w(CS)}$$

and is equal to 820ns which is a 1.21MHz update rate. However, the DAC settling time to 10 bits of 12.5μs limits the update rate to 80kHz for full-scale input step transitions.

SERIAL INTERFACE

When chip select ($\overline{CS}$) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The rising edge of the SLCK input shifts the data into the input register.
The rising edge of $\overline{CS}$ then transfers the data to the DAC register. When$\overline{CS}$ is high, input data cannot be clocked into the input register. All$\overline{CS}$ transitions should occur when the SCLK input is low.

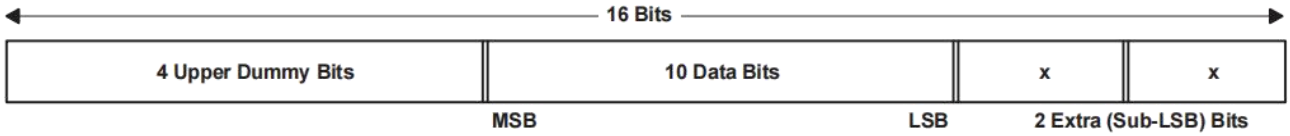
If the daisy chain (cascading) function (see daisy-chaining devices section) is not used, a 12-bit input data sequence with the MSB first can be used as shown in Figure 10:



x = don’t care

Figure 10. 12-Bit Input Data Sequence

or 16 bits of data can be transferred as shown in Figure 11 with the 4 upper dummy bits first.



x = don’t care

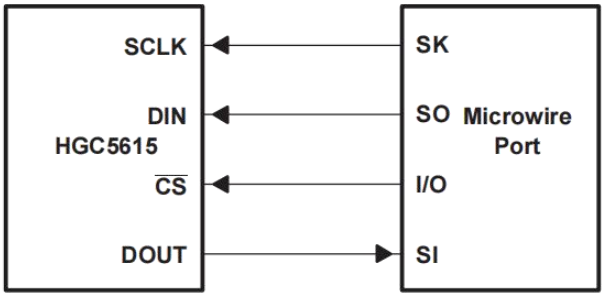
Figure 11. 16-Bit Input Data Sequence

The data from DOUT requires 16 falling edges of the input clock and, therefore, requires an extra clock width. When daisy chaining multiple HGC5615 devices, the data requires 4 upper dummy bits because the data transferrequires 16 input-clock cycles plus one additional input-clock falling edge to clock out the data at the DOUTterminal (see Figure 1).

The two extra (sub-LSB) bits are always required to provide hardware and software compatibility with 12-bit data converter transfers.

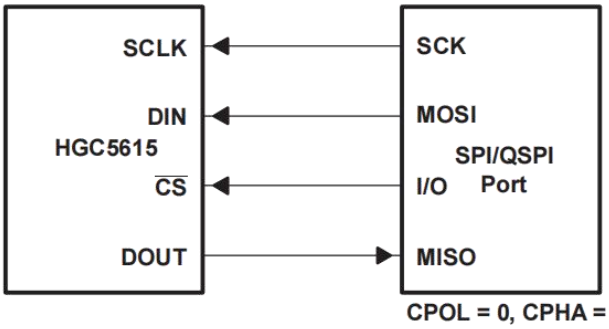
The HGC5615 three-wire interface is compatible with the SPI, QSPI, and Microwire serial standards. Thehardware connections are shown in Figure 12 and Figure 13.

The SPI and Microwire interfaces transfer data in 8-bit bytes; therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.



NOTE A: The DOUT-SI connection is not required for writing to the HGC5615 but may be used for verifying datatransfer if desired.

Figure 12. Microwire Connection



NOTE A: The DOUT-MISO connection is not required for writing to the HGC5615 but may be used for verifying data transfer.

Figure 13. SPI/QSPI Connection

DAISY-CHAINING DEVICES

DACs can be daisy-chained by connecting the DOUT terminal of one device to the DIN of the next device in the chain, providing that the setup time, tsu(CSS) ($\overline{CS}$ low to SCLK high), is greater than the sum of the setup time, tsu(DS), plus the propagation delay time, tpd(DOUT), for proper timing (see digital input timing requirements section). The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. DOUT is a totem-poled output for low power. DOUT changes on the SCLK falling edge when$\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains at the value of the last data bit and does not go into a high-impedance state.

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE-ENDED SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

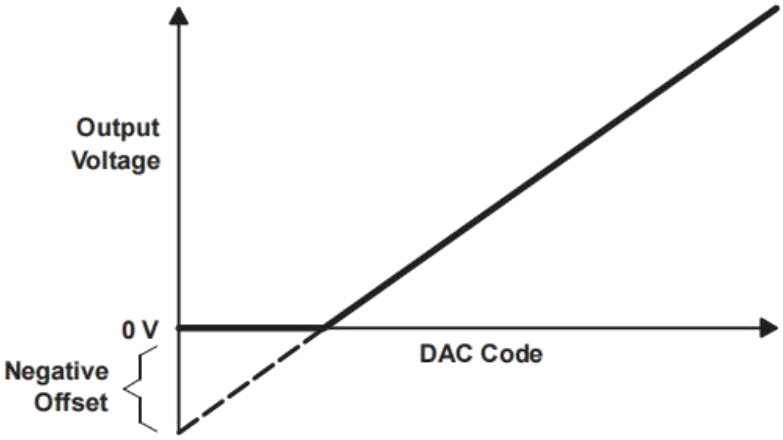


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs '0') and full-scale code (all inputs '1') after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. For the HGC5615, the zero-scale (offset) error is ±3LSB maximum. The code is calculated from the maximum specification for the negative offset.

POWER-SUPPLY BYPASSING AND GROUND MANAGEMENT

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1μF ceramic-capacitor bypass should be connected between VDD and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 15 shows the ground plane layout and bypassing technique.

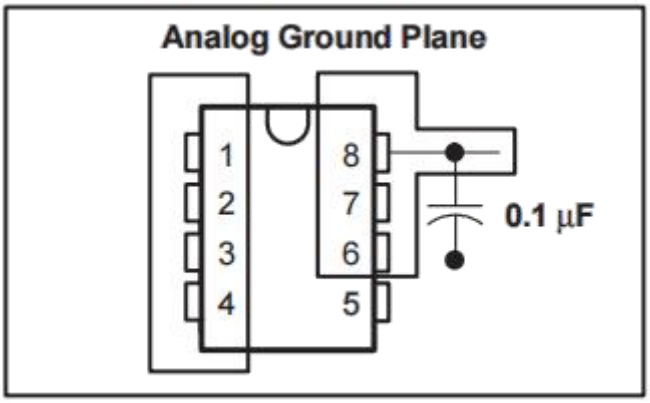


Figure 15. Power-Supply Bypassing

SAVING POWER

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

AC CONSIDERATIONS

Digital Feedthrough

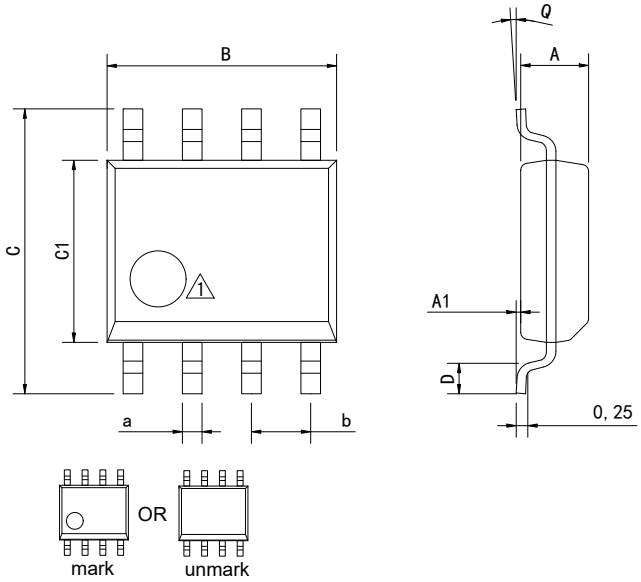
Even with $\overline{CS}$ high, high-speed serial data at any of the digital input or output terminals may couple through the DAC package internal stray capacitance and appear at the DAC analog output as digital feedthrough. Digital feedthrough is tested by holding $\overline{CS}$ high and transmitting 0101010101 from DIN to DOUT.

Analog Feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

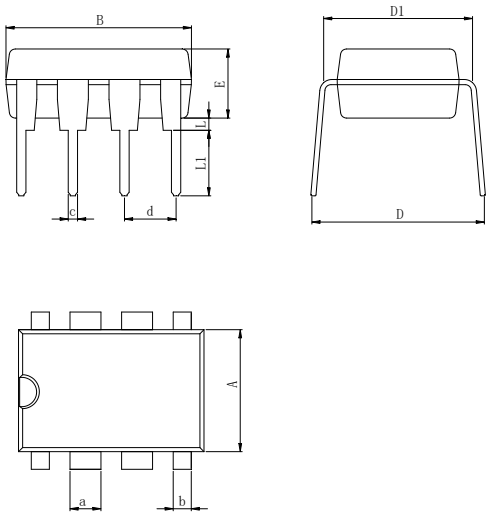
PHYSICAL DIMENSIONS

SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

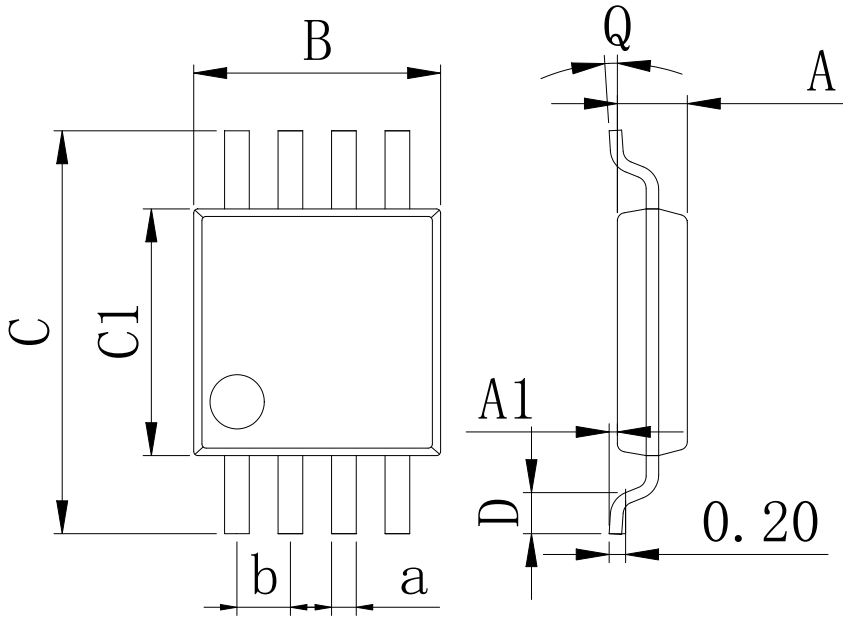
DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

PHYSICAL DIMENSIONS

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2015-8	New	1-19
V1.1	2021-8	Update encapsulation type、Updated DIP-8 dimension	1、16
V1.2	2024-11	Update Lead Temperature	4
V1.3	2025-12	Update important statements、Update SOP-8 Dimension drawing	16、19

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