

具有IEC ESD保护功能的 $\pm 18\text{V}$ 故障保护、3V至3.3V半双工RS-485收发器

SP3485EEN-Y SOP8

1 描述

SP3485EEN-Y是一款具备 $\pm 18\text{V}$ 故障保护功能的半双工RS-485收发器，采用3V至3.6V单电源供电。总线接口引脚在所有工作模式下均受到过压保护，确保在严苛工业环境中实现稳健的通信。

SP3485EEN-Y支持12Mbps传输速率。该器件具有集成式保护，无需外部系统级保护组件。在更长的电缆敷设长度和/或存在大接地环路电压的情况下，更宽的 $\pm 15\text{V}$ 输入共模范围可实现可靠的数据通信。增强型250mV接收器迟滞可提供高噪声抑制。此外，当总线开路或短路时，接收器失效防护功能可确保输出逻辑高电平。

SP3485EEN-Y采用SOP8封装，专为空间受限型应用设计。

2 特性

- 符合或超过TIA/EIA-485A标准的要求
- 3V至3.6V电源电压
- 总线I/O保护
- 闩锁性能超过800mA，符合JEDEC 78 规范
- 适用于热插拔功能的无干扰上电/断电
- 欠压锁定
- 超2.1V差分输出电压，可在5V供电条件下满足 PROFIBUS兼容
- 工作环境温度范围： -40°C to 85°C
- 增强型接收器迟滞，可获得抗噪能力
- 开路、短路和空闲总线失效防护
- 热关断
- 1/8单位负载（多达256个总线节点）
- 最高传输速率：12Mbps

3 Applications

- Automotive data links
- Industrial-Control Local Area Networks
- Integrated Services Digital Networks
- Building automation
- Electricity meters
- Transceivers for EMI-Sensitive applications

4 Selection Guide

Part Number	Data Rate (Mbps)	V _{CC} Range (V)
SP3485EEN-Y	12	3.0 to 3.6

5 Ordering Information

SP3485EEN-Y	SP3485EEN-Y	SOP8	3000pcs/13Inch Tape & Reel
-------------	-------------	------	----------------------------

6 Pin Configuration and Function

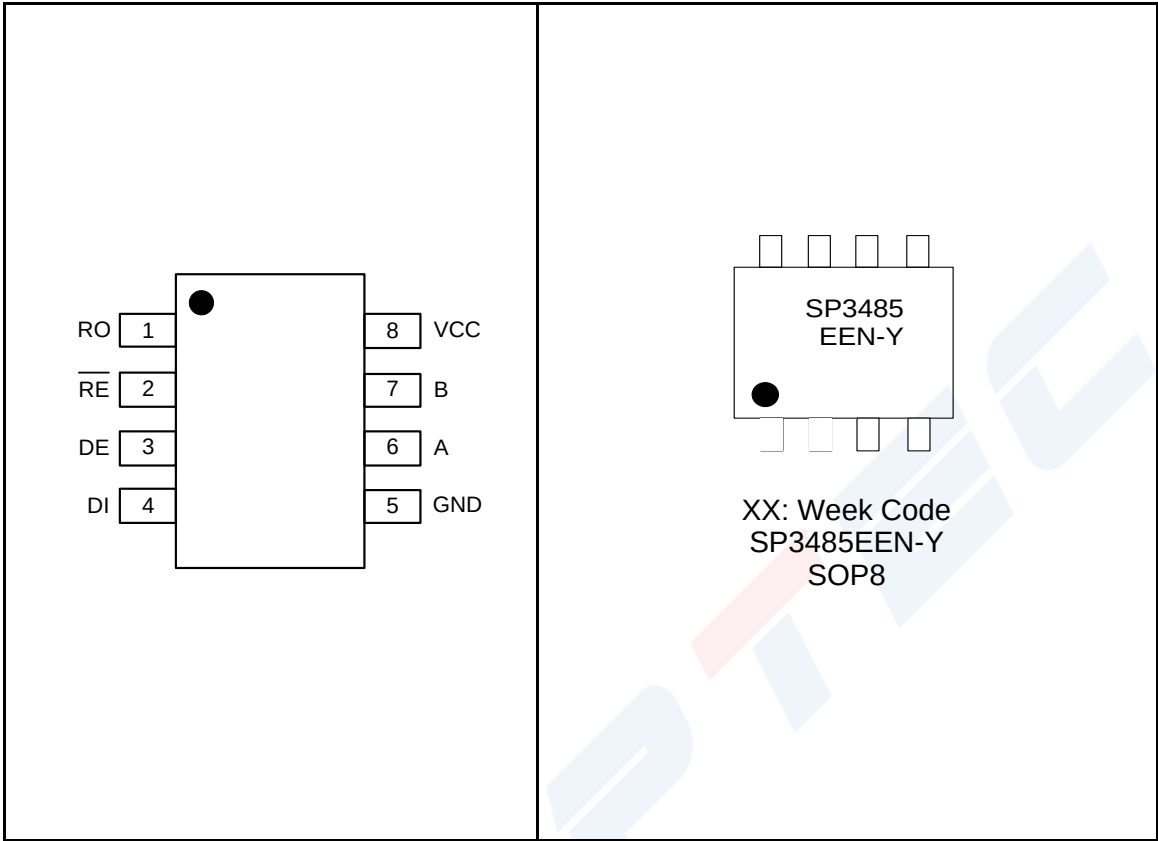


Table 6. Pin Functions of SP3485EEN-Y

Pin No.	Pin Name	Function
1	RO	Receive data output
2	$\overline{RE}$	Receiver enable, active low; integrated pull-up
3	DE	Driver enable, active high; integrated pull-down
4	DI	Driver data input; integrated pull-up
5	GND	Local device ground
6	A	Driver output or receiver input (complementary to B)
7	B	Driver output or receiver input (complementary to A)
8	VCC	Supply voltage

7 Specifications

7.1 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	Supply Voltage		3		3.6	V
V _I	Input voltage at any bus terminal (separately or common mode)	Note1	-15		15	V
V _{ID}	Differential input voltage		-15		15	V
V _{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus terminals and GND		±18		kV
		All pins except bus terminals and GND		±8		kV
		Contact discharge, per IEC 61000-4-2		±9		kV
I _O	Output current, driver		-60		60	mA
I _{OR}	Output current, receiver	SP3485EEN-Y	-8		8	mA
R _L	Differential load resistance		54	60		Ω
1/ t _{UI}	Signaling rate					
		SP3485EEN-Y			10	Mbps
T _A	Operating free-air temperature (see application section for thermal information)		-40		125	℃
T _J	Junction temperature		-40		150	℃

Note 1: The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

7.2 Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	Supply voltage		-0.5		6.5	V
V _I	Voltage on A, B		-18		18	V
	Voltage on any logic pin (D, DE, $\overline{\text{RE}}$)		-0.3		6.5	V
I _O	RXD output current		-24		24	mA
T _{STG}	Storage temperature		-65		150	°C
T _L	Lead Temperature for Soldering 10 Seconds				260	°C

Note 1: Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

7.3 Electrical Characteristics (Static) (Note 1)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC}= 5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V _{UVD(VCC)RISING}	Rising under-voltage threshold on VCC			2.6	2.8	V
V _{UVD(VCC)FALLING}	Falling under-voltage threshold on VCC		1.95	2.4		V
V _{UVD(VCC)HYS}	Hysteresis on under-voltage of VCC			170		mV

7.3 Electrical Characteristics (Static) (Note 1) (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}=5\text{ V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{CC}	Supply current, $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$\overline{RE} = 0\text{ V}$, $DE = V_{CC}$, No load (Driver and receiver enabled)		1.6	3	mA
		$\overline{RE} = V_{CC}$, $DE = V_{CC}$, No load (Driver enabled, receiver disabled)		1.6	3	mA
		$\overline{RE} = 0\text{ V}$, $DE = 0\text{ V}$, No load (Driver disabled, receiver enabled)		0.8	2.4	mA
		$\overline{RE} = V_{CC}$, $DE = 0\text{ V}$, D = open, No load (Driver and receiver disabled)		0.6	3	μA
I_{CC}	Supply current, $V_{CC} = 3\text{ V to }3.6\text{ V}$	$\overline{RE} = 0\text{ V}$, $DE = V_{CC}$, No load (Driver and receiver enabled)		1.45	3	mA
		$\overline{RE} = V_{CC}$, $DE = V_{CC}$, No load (Driver enabled, receiver disabled)		1.45	3	mA
		$\overline{RE} = 0\text{ V}$, $DE = 0\text{ V}$, No load (Driver disabled, receiver enabled)		0.7	2.4	mA
		$\overline{RE} = V_{CC}$, $DE = 0\text{ V}$, D = open, No load (Driver and receiver disabled)		0.3	3	μA

7.3 Electrical Characteristics (Static) (Note 1) (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60\ \Omega$, $-15\text{ V} \leq V_{TEST} \leq 15\text{ V}$, See Figure 8-1	1.5	3.4		V
		$R_L = 60\ \Omega$, $-15\text{ V} \leq V_{TEST} \leq 15\text{ V}$, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, See Figure 8-1	2.1	3.4		V
		$R_L = 100\ \Omega$, See Figure 8-2	2	4		V
		$R_L = 54\ \Omega$, See Figure 8-2	1.5	3.4		V
$\Delta V_{OD} $	Change in magnitude of driver differential output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$ See Figure 8-2	-50		50	mV
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$ See Figure 8-2	1	$V_{CC}/2$	3	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$ See Figure 8-2	-50		50	mV
I_{OS}	Short-circuit output current	$DE = V_{CC}$, $-15\text{ V} \leq (V_A \text{ or } V_B) \leq 15\text{ V}$	-250		250	mA
Receiver						
I_I	Bus input current	$DE = 0\text{ V}$, $V_{CC} = 0\text{ V}$ or 5.5 V , $V_I = 12\text{ V}$		70	125	μA
		$DE = 0\text{ V}$, $V_{CC} = 0\text{ V}$ or 5.5 V , $V_I = -7\text{ V}$	-100	-60		
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of $\pm 15\text{ V}$	40	125	200	mV
V_{TH-}	Negative-going input threshold voltage		-200	-125	-40	
V_{HYS}	Input hysteresis			250		
$V_{TH(FSH)}$	Input fail-safe threshold		-40		40	
$C_{A,B}$	Input differential capacitance	Measured between A and B, $f = 1\text{ MHz}$		50		pF

7.3 Electrical Characteristics (Static) (Note 1) (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}=5\text{ V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	$I_{OH} = -8\text{ mA}$	$V_{CC}-0.4$	$V_{CC}-0.1$		V
V_{OL}	Output low voltage	$I_{OL} = 8\text{ mA}$		0.1	0.4	V
I_{OZ}	Output high-impedance current	$V_O = 0\text{ V}$ or V_{CC} , $R_E = V_{CC}$	-1		1	μA
Logic						
V_{IH}	Input High Voltage	DE, D, $\overline{RE}$	$0.7V_{CC}$			V
V_{IL}	Input low Voltage	DE, D, $\overline{RE}$			$0.3V_{CC}$	V
I_I	Input current on DE pin	$1.65\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{CC}\text{V}$			5	μA
	Input current on D, $\overline{RE}$ pin	$1.65\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{CC}\text{V}$	-5			μA
Thermal Protection						
T_{SD}	Thermal shutdown threshold	Temperature rising	150	170		°C
T_{HYS}	Thermal shutdown hysteresis			10		°C

7.4 Electrical Characteristics (Dynamic)—12Mbps (Note 1)

over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC}=5V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Driver							
t_R, t_F	Driver differential output rise/fall time	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, see Figure 8-3	$V_{CC} = 3\ \text{to}\ 3.6\ \text{V}$, Typical at 3.3 V	4	12	20	ns
			$V_{CC} = 4.5\ \text{to}\ 5.5\ \text{V}$, Typical at 5 V	4	13	20	ns
t_{PHL}, t_{PLH}	Driver propagation delay time		$V_{CC} = 3\ \text{to}\ 3.6\ \text{V}$, Typical at 3.3 V	6	18	30	ns
			$V_{CC} = 4.5\ \text{to}\ 5.5\ \text{V}$, Typical at 5 V	4	15	25	ns
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $		$V_{CC} = 3\ \text{to}\ 3.6\ \text{V}$, Typical at 3.3 V		1	3	ns
			$V_{CC} = 4.5\ \text{to}\ 5.5\ \text{V}$, Typical at 5 V		0.5	3	ns
t_{PHZ}, t_{PLZ}	Disable time		See Figure 8-4 and Figure 8-5		25	70	ns
t_{PZH}, t_{PZL}	Enable time		$\overline{RE} = 0\ \text{V}$, See Figure 8-4 and Figure 8-5		23	70	ns
t_{PSH}, t_{PSL}		$\overline{RE} = V_{CC}$, See Figure 8-4 and Figure 8-5		2.4	4.5	μs	
t_{PHS}, t_{PLS}	Time to shutdown	$\overline{RE} = V_{CC}$, See Figure 8-4 and Figure 8-5	50		500	ns	
Receiver							
t_R, t_F	Receiver output rise/fall time	$C_L = 15\ \text{pF}$, see Figure 8-6		4	8	ns	
t_{PHL}, t_{PLH}	Receiver propagation delay time		10	18	58	ns	
$t_{SK(P)}$	Receiver output pulse skew, $ t_{PHL} - t_{PLH} $			0.5	5	ns	

7.4 Electrical Characteristics (Dynamic)—12Mbps (continued) (Note 1)
over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC}=5V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
t_{PHZ}, t_{PLZ}	Receiver disable time			15	35	ns
t_{PZL}, t_{PZH}	Receiver enable time	DE = VCC, see Figure 8-7		15	82	ns
t_{PSH}, t_{PSL}		DE = 0 V, see Figure 8-8		2.5	5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	$C_L = 15\text{ pF}$, see Figure 8-9	7	11	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation		13	23	60	ns
t_{PHS}, t_{PLS}	Time to shutdown	DE = 0 V, see Figure 8-8	50		500	ns

8 Parameter Measurement Information

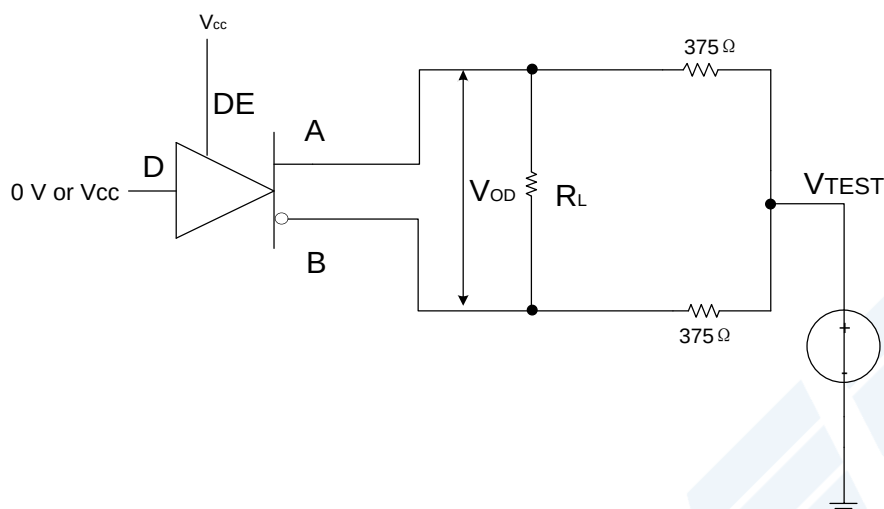


Figure 8-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

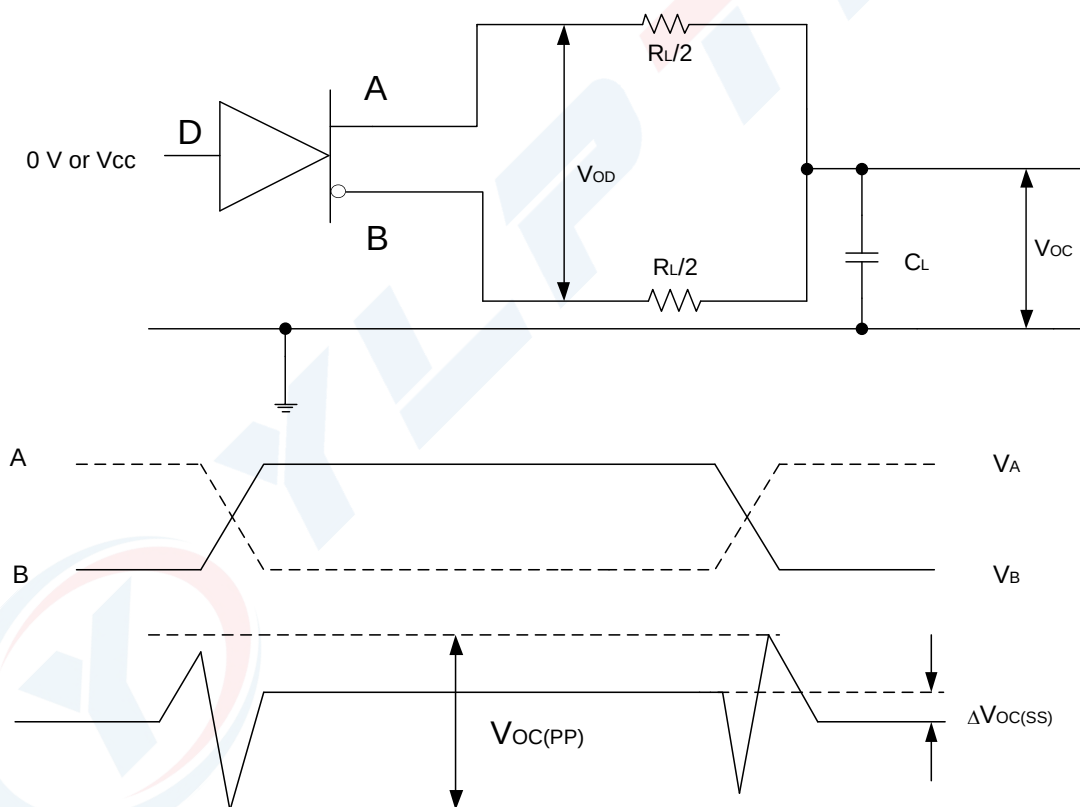


Figure 8-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

8 Parameter Measurement Information (continued)

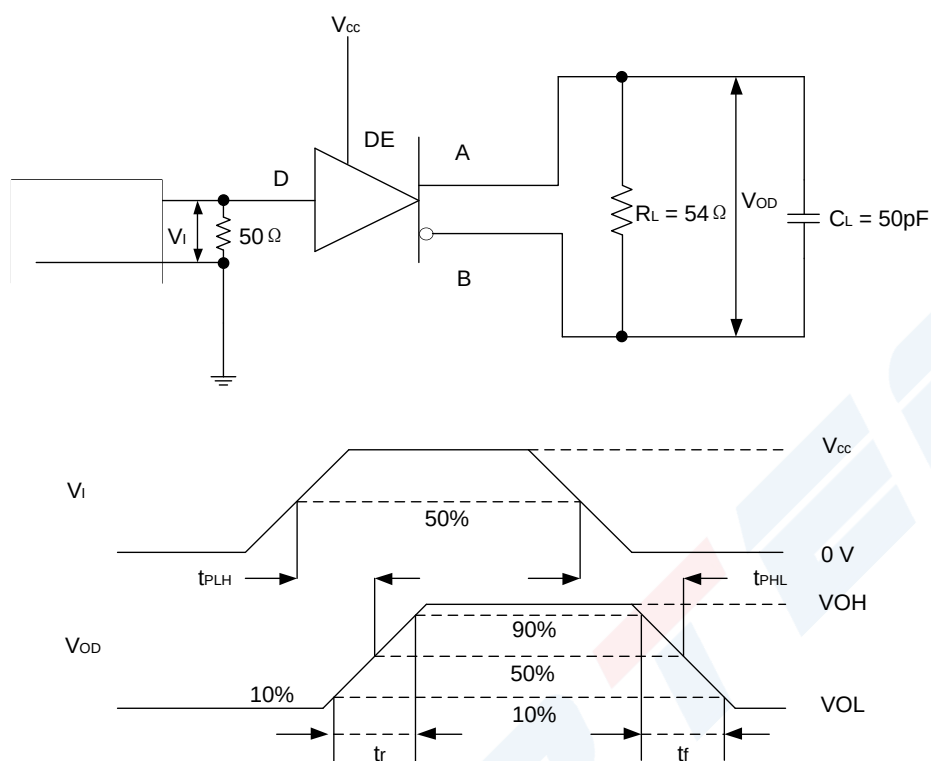


Figure 8-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

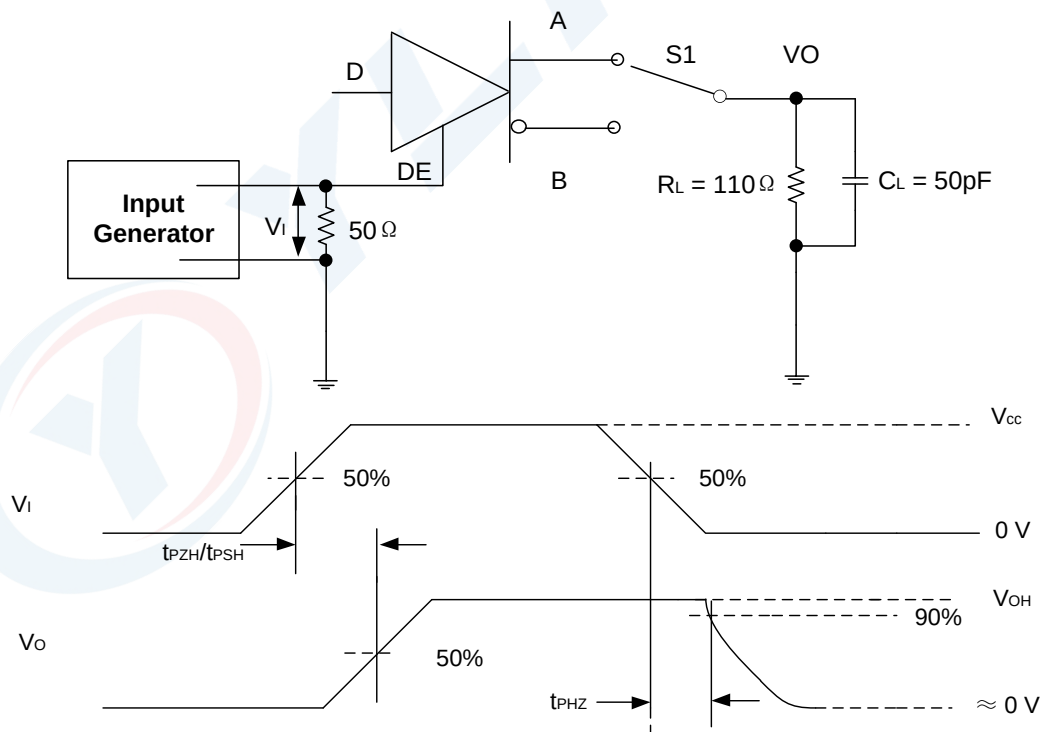


Figure 8-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

8 Parameter Measurement Information (continued)

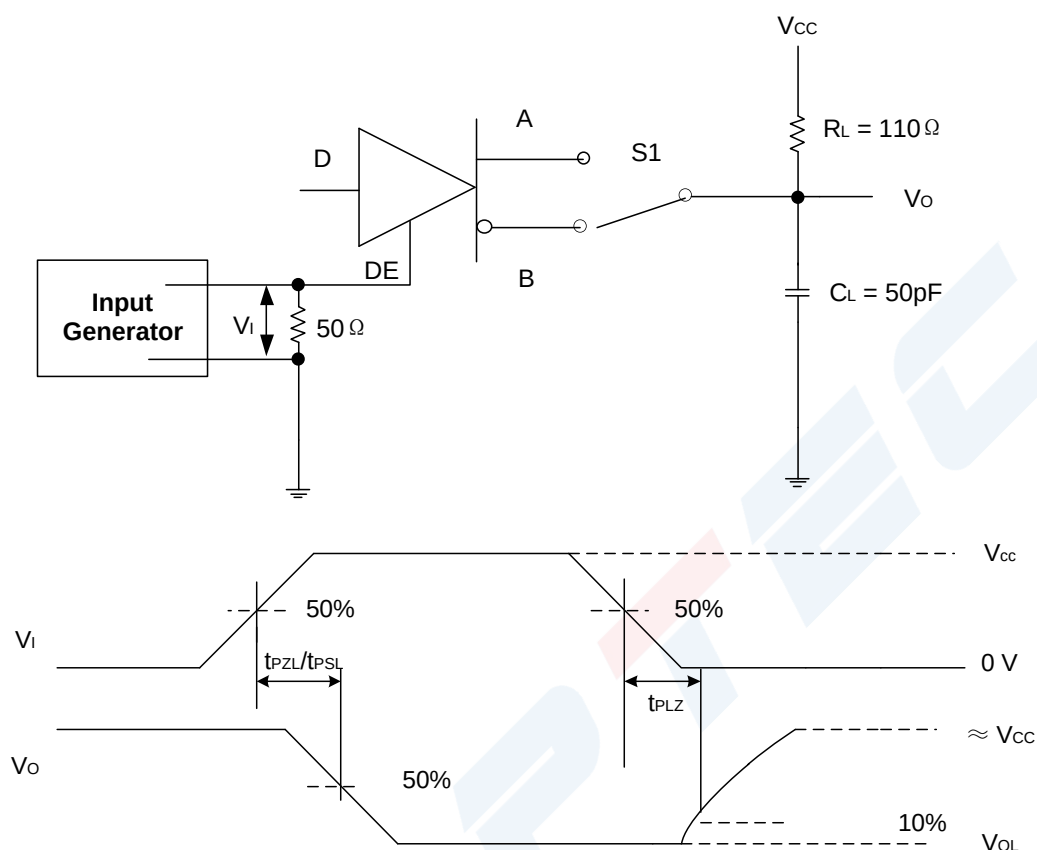


Figure 8-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

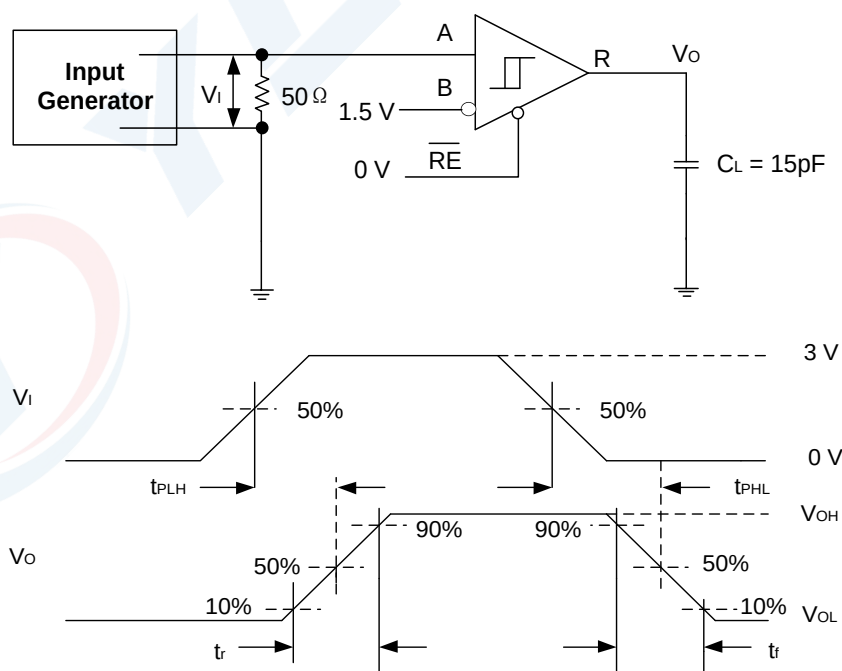


Figure 8-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

The circuit diagram shows a 74VHC14 inverter with its input connected to an input generator through a 50 Ω resistor. The input signal is V_i . The output is connected to a 1 kΩ resistor and a 15 pF load capacitor C_L . The output signal is V_o . The inverter's output is also connected to a switch S1, which can be connected to V_{CC} or GND.

The timing diagram shows the input signal V_i and the output signal V_o for two cases: V_i at V_{CC} and V_i at 0 V. The output signal V_o is shown for both cases, with the output voltage V_o and the output signal V_o labeled. The timing parameters are defined as follows:

- t_{PZH} : Propagation delay from input high to output high.
- t_{PHZ} : Propagation delay from input high to output high (for the second case).
- t_{PZL} : Propagation delay from input low to output low.
- t_{PLZ} : Propagation delay from input low to output low (for the second case).

The output signal V_o is shown for both cases, with the output voltage V_o and the output signal V_o labeled. The timing parameters are defined as follows:

- 50%: 50% voltage level.
- 90%: 90% voltage level.
- 10%: 10% voltage level.

The circuit diagram shows an Input Generator connected to the A and B inputs of a Schmitt trigger. The output of the Schmitt trigger is connected to a feedback resistor (1kΩ) and a load capacitor (CL = 15pF). The output voltage is labeled Vo. The timing diagram shows the input voltage (Vi) and output voltage (Vo) waveforms. The input voltage Vi is a square wave with a 50% duty cycle. The output voltage Vo is a square wave with a 50% duty cycle. The timing parameters are labeled: tPSH (propagation delay from input high to output high), tPSL (propagation delay from input low to output low), tPHZ (hold time from output high to input high), tPLZ (hold time from output low to input low), and tPLZ (propagation delay from input low to output low). The threshold levels are indicated by dashed lines at 50%, 90%, and 10% of the supply voltage Vcc.

页码：第 14 页；共 21 页

8 Parameter Measurement Information(continued)

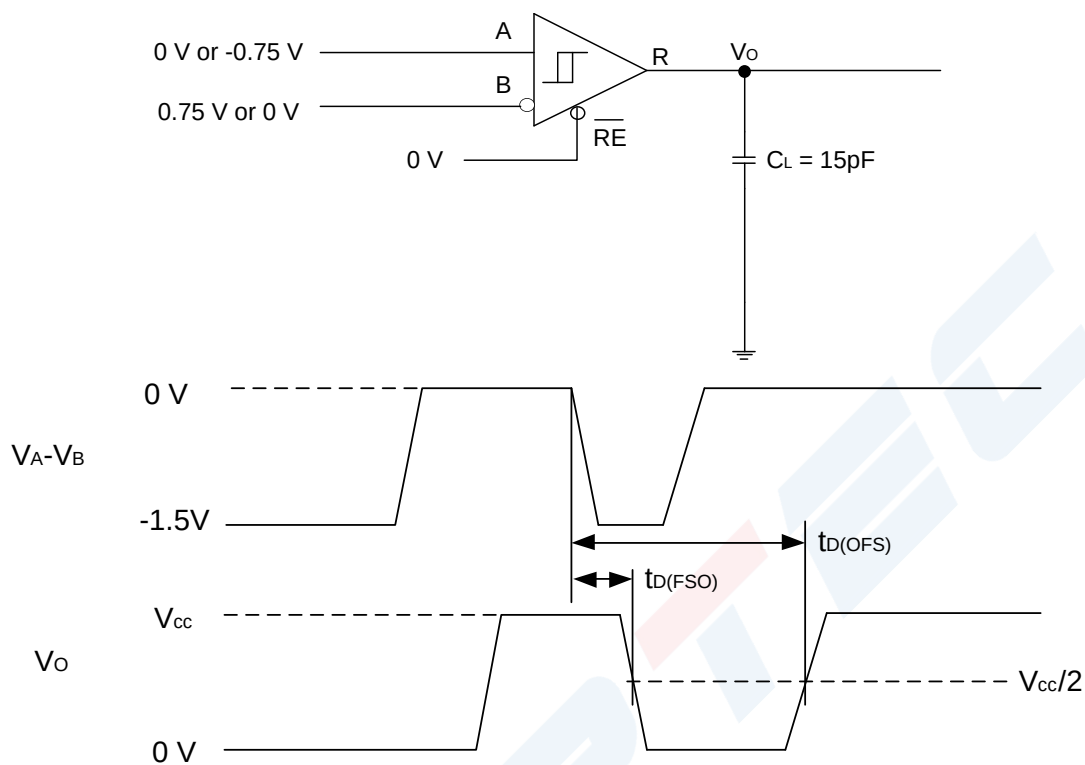


Figure 8-9. Measurement of Fail-Safe Delay

9 Detailed Description

9.1 Overview

SP3485EEN-Y is a fault-protected, half-duplex RS-485 transceiver available in a speed grade suitable for data transmission up to 12 Mbps.

9.2 Functional Block Diagram

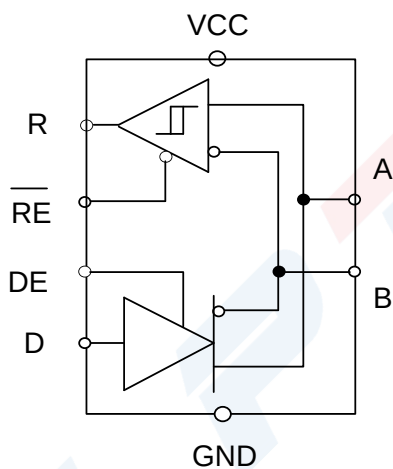


Figure 9-1. SP3485EEN-Y Block Diagram

10 Feature Description

10.1 Receiver Fail-Safe Operation

The receiver is fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH(FSH)}|$.

10.2 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500 ns puts the device into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The device does not enter the shutdown mode if the enable pins are in disable state for less than 50 ns. This feature prevents the device from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

10.3 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 10-1. Driver Function Table

Enable	Input	Output		Function
DE	D	A	B	
H	H	H	L	Actively drive bus high
H	L	L	H	Actively drive bus low
H	Open	H	L	Actively drive bus high by default
L	X	Z	Z	Driver disabled
Open	X	Z	Z	Driver disabled by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+} , the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-} , the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} , the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), or the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

10.3 Device Functional Modes (continued)

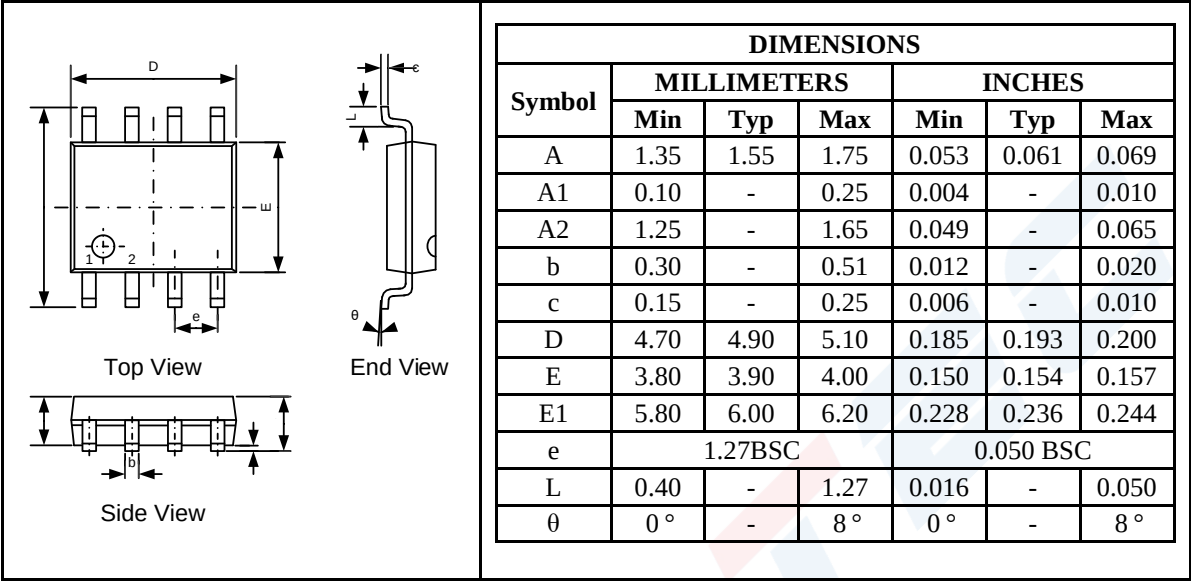
Table 10-2. Receiver Function Table

Enable	Differential Input	Output	Function
$\overline{\text{RE}}$	$V_{\text{ID}} = V_{\text{A}} - V_{\text{B}}$	R	
L	$V_{\text{TH}+} < V_{\text{ID}}$	H	Receive valid bus high
L	$V_{\text{TH-}} < V_{\text{ID}} < V_{\text{TH}+}$	N/A	Indeterminate bus state
L	$V_{\text{ID}} < V_{\text{TH-}}$	L	Receive valid bus low
L	Open-circuit bus	H	Fail-safe high output
L	Short-circuit bus	H	Fail-safe high output
L	Idle (terminated) bus	H	Fail-safe high output
H	X	Z	Receiver disabled
Open	X	Z	Receiver disabled by default

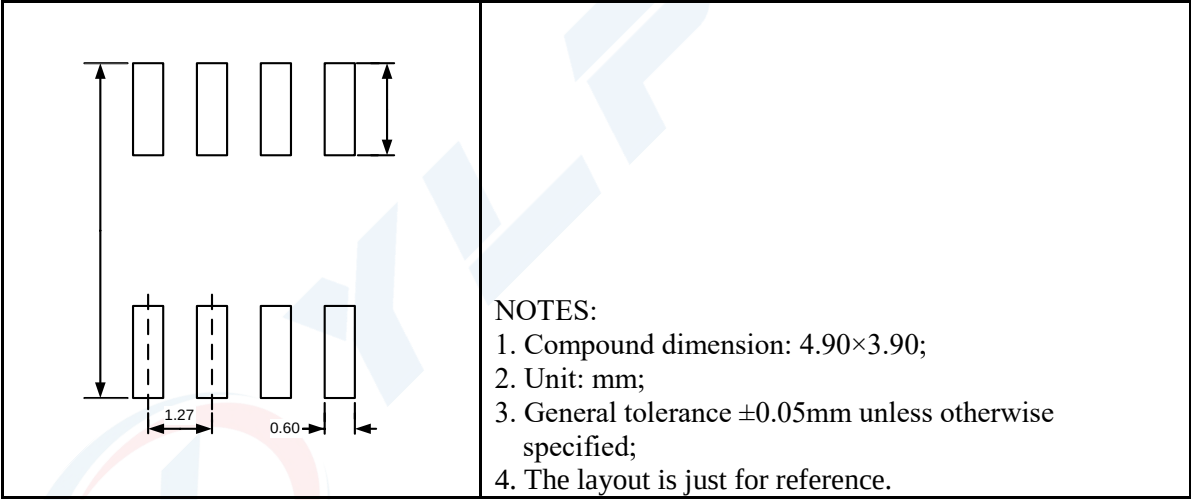
Package Information

SOP8

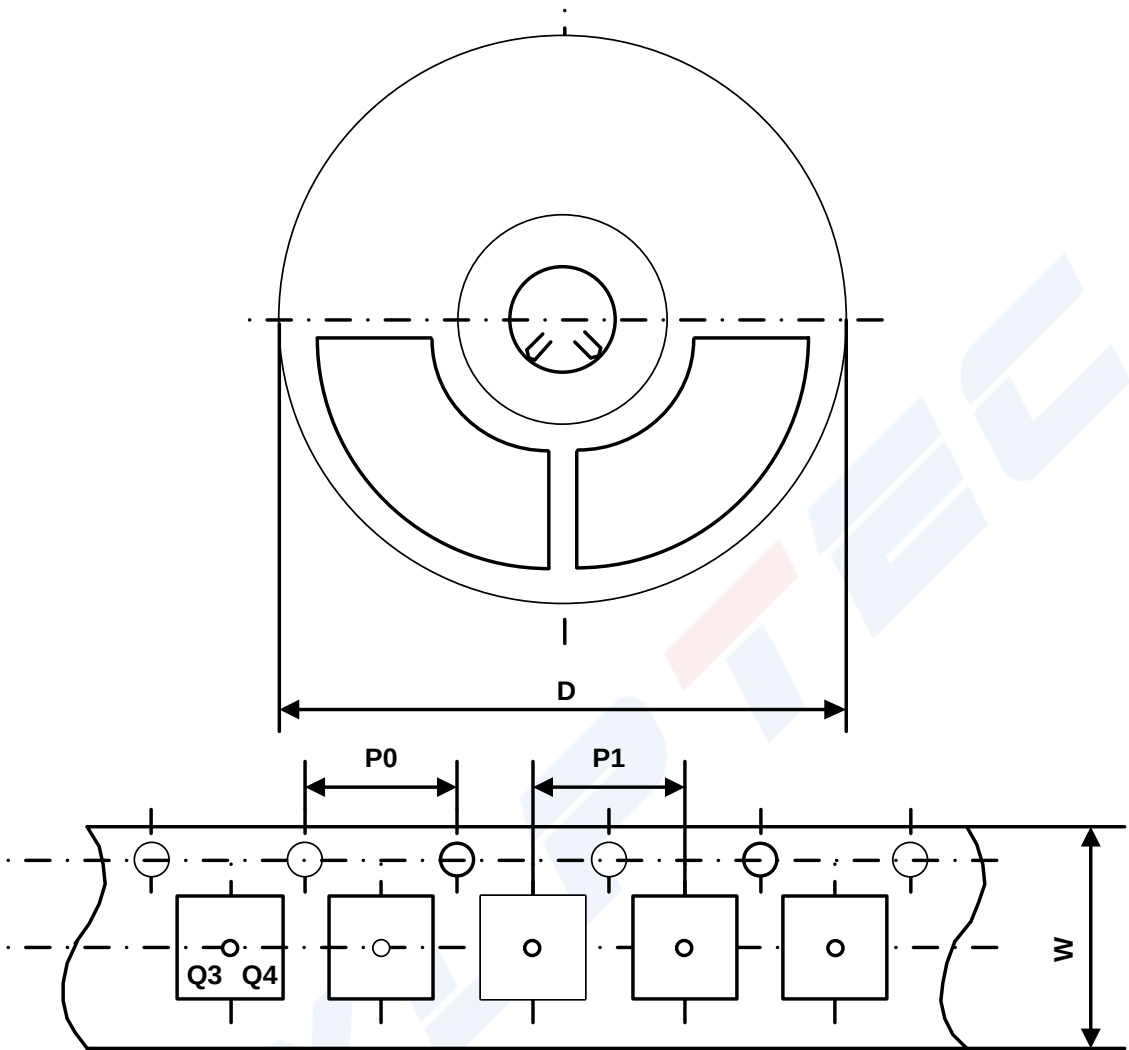
Outline Drawing



Land Pattern



Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
SP3485EEN-Y	SOP8	12 mm	4 mm	8 mm	330 mm	Q1

GREEN COMPLIANCE

YLPTEC is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.

All YLPTEC components are compliant with the RoHS directive, which helps to support customers in their compliance with environmental directives.

IMPORTANT NOTICE

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. YLPTEC assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any update. YLPTEC reserves the right to make changes, at any time, in order to improve reliability, function or design and to attempt to supply the best product possible.