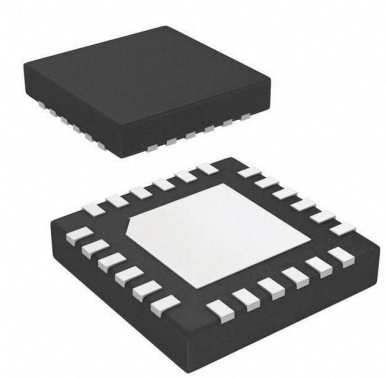
Three Phase Brushless Motor Driver

Chip Description

GC4928 is a three phase brushless motor driver with a 33V power supply voltage rating and a 1.5A output current rating. It generates a driving signal from the Hall sensor and drives PWM through the input control signal. In addition, the power supply can use 12V or 24V and it has various controls and built-in protection functions, making it useful for variety of purposes. Since the IC adopts small packages, it can be used on small diameter motors.

Chip Application

- OA machines
- Other consumer products

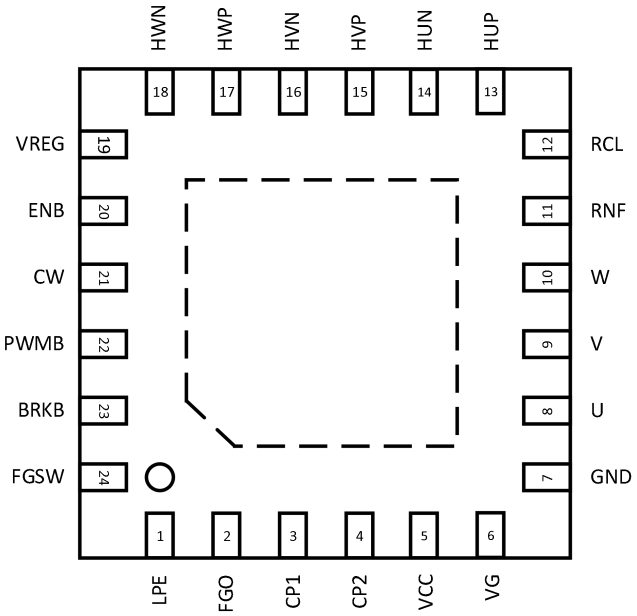


Chip Features

- Power supply voltage rating: 33V
- Output current rating: 1.5A
- Built-in 120° Commutation Logic Circuit
- Low ON Resistance DMOS Output
- PWM Control Mode (low side arm switching)
- Built-in Power-saving Circuit
- CW/CCW Function
- Short Brake Function
- FG Output (1FG/3FG conversion)
- Built-in Protection Circuit for Current Limiting (CL), Overheating (TSD), Over Current (OCP), Under Voltage (UVLO), Over Voltage (OVLO), Motor Lock (MLP)

Part Number	Package Type	Body Size
GC4928	QFN24	4.0*4.0, e=0.5

Pin Map



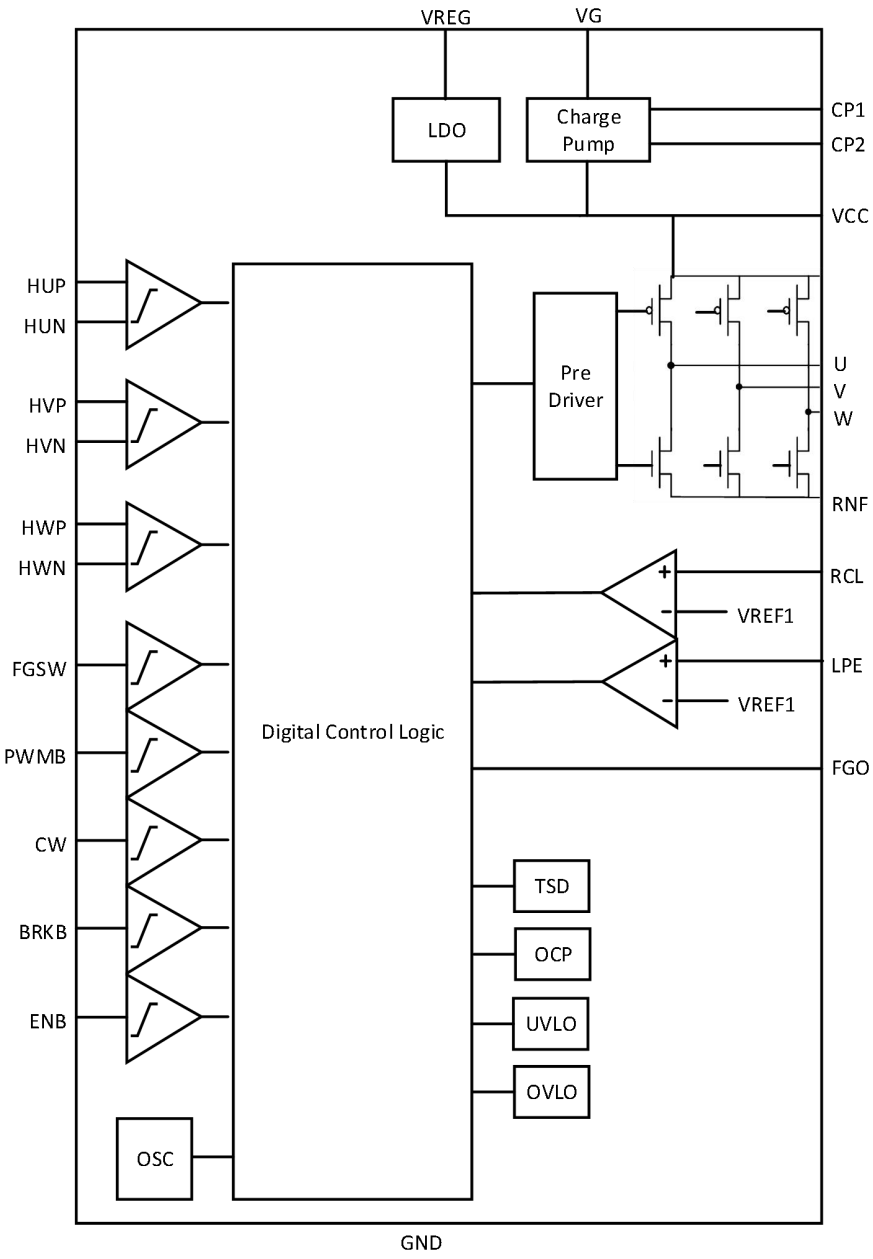
Pin Description

Pin.num	Pin Name	I/O	Pin Function
1	LPE	I	Setting about motor lock protection(H/M/L input)
2	FGO	O	FG output (1FG or 3FG)
3	CP1	I/O	Charge pump setting 1
4	CP2	I/O	Charge pump setting 2
5	VCC	Power	Power supply
6	VG	O	Charge pump output
7	GND	Ground	Ground
8	U	O	U phase output
9	V	O	V phase output
10	W	O	W phase output
11	RNF	I/O	Detect resistor for over current
12	RCL	I	Detect voltage input for over current
13	HUP	I	U phase Hall input+
14	HUN	I	U phase Hall input-
15	HVP	I	V phase Hall input+
16	HVN	I	V phase Hall input-
17	HWP	I	W phase Hall input+
18	HWN	I	W phase Hall input-
19	VREG	O	Regulator output (OFF at stand-by)
20	ENB	I	Enable input (negative logic)
21	CW	I	CW/CCW input (H:CW, L:CCW)
22	PWMB	I	PWM input (negative logic)

Pin Description (continued)

Pin.num	Pin Name	I/O	Pin Function
23	BRKB	I	Brake input (negative logic)
24	FGSW	I	1FG/3FG switching (H:3FG, L:1FG)

Block Diagram



Absolute Maximum Ratings

(over operating free-air temperature range, unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{VCC}	Power supply voltage	-0.3~33.0	V
V_{VG}	VG voltage	-0.3~38.0	V
V_{IN}, V_{IN2}	Control input voltage	-0.3~5.5	V
V_{FGO}	FGO terminal voltage	-0.3~7.0	V
V_{RNF}	RNF maximum apply voltage	0.7	V
I_{VREG}	VREG output current	-30	mA
I_{FGO}	FGO output current	5	mA
$I_{OUT(DC)}$	Driver output current	1.5	A
T_{OPR}	Operating temperature	-40~100	°C
T_{STG}	Storage temperature	-55~150	°C
T_{JMAX}	Junction temperature	150	°C
ESD	Human body model	±5000	V

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply voltage	V_{VCC}		8	24	28	V
Ambient temperature	T_A		-40		100	°C

Electrical Characteristics

(unless otherwise specified, T_A=25°C, V_{VCC}=24V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit current	I_{CC}	V_{ENB}=0V		2.8	5.2	mA
Stand-by current	I_{STBY}	ENB=Open		1.0	1.7	mA
VREG voltage	V_{VREG}	I_{VREG}=-10mA	4.5	5.0	5.5	V
Driver output						
Output on resistance	R_{ON}	I_{OUT}=±1.0A(Upper + Lower)		0.8	1.2	Ω
Hall input						
Input bias current	I_{HALL}	V_{HALL}=0V	-2.0	-0.1	2	uA
Range of in-phase input voltage1	$V_{HALLCM1}$		0		V_{VREG}-1.7	V
Range of in-phase input voltage2	$V_{HALLCM2}$	When one hall Input is bias	0		V_{VREG}	V
Minimum input voltage	$V_{HALLMIN}$		50			mVp-p
HYS Level +	$V_{HALLHY+}$		5	15	25	mV
HYS Level -	$V_{HALLHY-}$		-25	-15	-5	mV
Input of control - ENB						
Input current	I_{ENB}	V_{ENB}=0V	-80	-60	-40	uA
Standby voltage	V_{STBY}		2.0		V_{VREG}	V
Enable voltage	V_{ENA}		0		0.8	V
Input of control - PWMB, CW, BRKB, FGSW						
Input current	I_{IN}	V_{IN}=0V	-80	-60	-40	uA
Voltage input H	V_{INH}		2.0		V_{VREG}	V
Voltage input L	V_{INL}		0		0.8	V
Minimum input pulse width	t_{PLSMIN}	CW, BRKB	1			msec
Input of control - LPE						
Input current	I_{IN2}	V_{IN2}=0V	-80	-60	-40	uA
Voltage input H	V_{INH2}		0.8* V_{VREG}		V_{VREG}	V
Voltage input M	V_{INM2}		0.4* V_{VREG}		0.6* V_{VREG}	VS
Voltage input L	V_{INL2}		0		0.2* V_{VREG}	V
FG output						
Output voltage L	V_{FGOL}	I_{FGO}=2mA	0	0.1	0.3	V
Current limit						
Detect voltage	V_{CL}		0.18	0.20	0.23	V
UVLO						
Release voltage	V_{UVH}		6.5	7.0	7.5	V
Lockout voltage	V_{UVL}		5.5	6.0	6.5	V

Electrical Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVLO						
Release voltage1	V_{OVL1}	LPE="M"	14.0	15.0	16.0	V
Lockout voltage1	V_{OVH1}	LPE="M"	15.0	16.0	17.0	V
Release voltage2	V_{OVL2}	LPE="H" or "L"	29.0	30.5	32.0	V
Lockout voltage2	V_{OVH2}	LPE="H" or "L"	29.5	31.0	32.5	V
OCP						
Overcurrent protection	Iocp		3.1	3.5	3.7	A
triggering time	t_{ocp}		3.3	3.6	4	us
TSD						
triggering time	T_{JTSD}		155	165	175	℃
Thermal Shutdown Hysteresis	ΔTJ			20		℃

Function Description

1. Commutation Logic

GC4928 adopts 120° commutation mode, and the truth table is as follows:

HU	HV	HW	CW (CW=H or Open)			CCW (CW=L)			FGO	
			U	V	W	U	V	W	1FG	3FG
H	L	H	PWM*	H	Hi-z	H	PWM*	Hi-z	L	Hi-z
H	L	L	PWM*	Hi-z	H	H	Hi-z	PWM*	L	L
H	H	L	Hi-z	PWM*	H	Hi-z	H	PWM*	L	Hi-z
L	H	L	H	PWM*	Hi-z	PWM*	H	Hi-z	Hi-z	L
L	H	H	H	Hi-z	PWM*	PWM*	Hi-z	H	Hi-z	Hi-z
L	L	H	Hi-z	H	PWM*	Hi-z	PWM*	H	Hi-z	L

* When PWMB="L", PWM="L" ,When PWMB="H", PWM="H".

2. Regulator Output Terminal (VREG)

This is constant voltage output terminal of 5V(Typ). It is recommended to connect capacitors of 0.01μF to 1μF. Please be careful that VREG current does not exceed ratings in case of being used for bias power supply of hall elements.

3. Enable Input Terminal (ENB)

Output of each phase can be set to ON/OFF (negative logic) through ENB terminal. When applied voltage is V_{ENA}, the motor is driven (enable). When applied voltage is V_{STBY} or OPEN, the motor stops (stand-by). Stand-by mode has precedence to other control input signal and VREG output is OFF. In addition, ENB terminal is pulled up by internal power supply through a resistance of 100kΩ (Typ) ±30kΩ .

ENB	Operation
H or OPEN	Stand-by
L	Enable

4. PWM Input Terminal (PWMB)

Speed can be controlled by inputting PWM signal into PWMB terminal (negative logic). Synchronous rectifier PWM can be achieved through lower switching. When PWMB="L", driver output that belongs to Hall input logic is "L". When PWMB="H" or open, driver output is "H". When PWMB="H" or OPEN status is detected 104μs (Typ), the synchronous rectifier is OFF (Hi-z). Synchronous rectifier is ON through falling edges of subsequent PWMB. Additionally, PWMB terminal is pulled up by VREG through a resistance of 100kΩ (Typ) ±30kΩ.

PWMB	Driver Output
H or OPEN	H (Hi-z)
L	L

5. Brake Input Terminal (BRKB)

Motor rotation can be quickly stopped by BRKB terminal (negative logic). When BRKB="L", all driver outputs are "L" (short brake). When BRKB="H" or OPEN, then short brake action is released. In addition, BRKB terminal is pulled up by VREG through a resistance of 100kΩ (Typ) ±30kΩ.

BRKB	Operation
H or OPEN	Normal
L	Short brake

6. CW/CCW Input Terminal (CW)

Rotation direction can be switched with CW terminal. When CW="H" or OPEN, the direction is Clockwise. When CW="L", the direction is Counterclockwise. We do not recommend changing the direction of rotation while the motor is rotating. However if direction of rotation is changed while rotating, a short brake action is active until the rotation speed becomes equal to the hall frequency, which is less than approximately 40Hz (Typ). After a short brake, the rotation direction will switch to a new setting. In addition, CW terminal is pulled up by VREG through resistance of 100kΩ (Typ) ±30kΩ.

CW	Direction
H or OPEN	Clockwise
L	Counterclockwise

7. 1FG/3FG Switching Terminal (FGSW)

FG signal that is output from FGO terminal can be switched to 1FG/3FG. It becomes 3FG by FGSW="H" or OPEN, and 1FG by FGSW="L". Moreover, FGSW terminal is pulled up by VREG through resistance of 100kΩ (Typ)±30kΩ.

FGSW	Direction
H or OPEN	3FG
L	1FG

8. Hall Input (HALL: HUP, HUN, HVP, HVN, HWP, HWN)

Hall comparator is designed with hysteresis (±15mV (Typ)) in order to prevent incorrect action due to noise inside. So please set bias current for Hall element to make amplitude of Hall input voltage over minimum input voltage ($V_{HALLMIN}$). Here, we recommend you to connect the ceramic capacitor with about 100pF to 0.01μF between difference input terminals of Hall comparator. The in-phase input voltage range designed for Hall comparator is $V_{HALLCM1,2}$, so please set within this range when applying bias to Hall element.

Moreover, "H" or "L" of HU, HV and HW in Commutation Logic means the following.

HU	HV	HW	HUP	HUL	HVP	HVN	HWP	HWN
H	L	H	H	L	L	H	H	L
H	L	L	H	L	L	H	L	H
H	H	L	H	L	H	L	L	H
L	H	L	L	H	H	L	L	H
L	H	H	L	H	H	L	H	L
L	L	H	L	H	L	H	H	L

When HU, HV and HW become all "H" or "L", detect circuit detects these Hall input abnormalities and makes all driver outputs "Hi-z".

9. FG Output Terminal (FGO)

1FG or 3FG signal that is reshaped by hall signal is output from FGO terminal. It is does not have output in stand-by mode. In addition, because FG terminal is output from open drain, please use resistance of about 10kΩ to 100kΩ pulled up from outside. In that case, please be careful that FGO voltage or current never exceed rating.

10. Power Supply Terminal (VCC)

Please make low impedance thick and short since motor drive current flows. Please stabilize VCC by placing bypass capacitor near terminal as much as possible because VCC might be changed considerably by motor BEMF and PWM switching. Please add capacity of capacitor as necessary when using large current and motor with large BEMF. Moreover, it is recommended to place laminated ceramic capacitor of around 0.01μF to 0.1μF in parallel on the purpose of decreasing impedance of power supply broadband. Please be careful that VCC

never exceeds ratings.

VCC terminal has clamp element for preventing ESD damage. If applying steep pulse signal and voltage such as surge more than ratings, this clamp element operates, which might be a cause of destruction. It is effective to put zener diode that corresponds to VCC absolute maximum ratings. Diode for preventing ESD damage is inserted between VCC and GND terminals. Please note that IC might be destroyed when the backward voltage is applied to VCC and GND terminals.

11. Ground Terminal (GND)

Wiring impedance from this terminal should be as low as possible for reducing noise of switching current and stabilizing basic voltage inside of IC, and the impedance also should be the lowest potential in any operating condition. In addition, please do pattern design not to have common impedance as other GND pattern.

12. Driver Output Terminal (U, V, W)

When driver output converts "L"→"H" or "H"→"L", for example when synchronous rectification PWM is operating, a dead time (1μs(Typ)) will be set to prevent simultaneous ON of output top & bottom MOS.

Please be careful about the following points in using driver output.

・Wiring should be thick, short, and low Impedance due to motor drive current.

・In applying steep pulse signal or voltage that will surge more than ratings, the clamp element which is built-in the driver output terminal operates in order to prevent ESD damage. Then it might cause destruction of IC. Do not exceed ratings.

When using large current, in case that driver current changes considerably toward positive and negative (when BEMF is large), malfunction or destruction of IC might occur. Please add Schottky diode to the driver output terminal.

13. Capacitor Connection Terminal for Boosting, Boosting Output Terminal (CP1, CP2, VG)

Charge pump is built-in for upper Nch MOS drive signal of driver output. Boosting voltage of V_{VCC}+5V (Typ) occurs in VG terminal by connecting capacitor between CP1 to CP2 terminals and VG to VCC terminals. It is recommended to use capacitor more than 0.1μF. In addition, because there is built-in protection circuit for insufficient booster, when VG voltage is below V_{GUVON} (V_{VCC}+2V (Typ.)), driver outputs all become “Hi-z”.

14. Resistor Connection Terminal for Detecting Output Current (RNF)

Please insert resistor for detecting current 0.15Ω to 0.5Ω between RNF and GND. When deciding resistor value, it should be careful that consumption electricity of resistor for detecting current I_{OUT}^2・R[W] does not exceed rating of resistor. In addition, please do not have common impedance as other GND patterns by using low impedance wiring, since motor drive current flows into pattern of RNF terminal to resistor for detecting current to GND. In case that RNF voltage goes over rating (0.7V), circuit malfunction might occur. Therefore please do not exceed rating. When RNF terminal is shorted to GND, big current flows due to a lack of normal current limit operation. Please be careful that OCP or TSD might operate in that case. Similarly, if RNF terminal is OPEN, output current might not flow, which also becomes a cause of malfunction.

15. Comparator Input Terminal for Detecting Output Current (RCL)

RCL terminal is placed individually as input terminal of current detect comparator in order to avoid deterioration of current detect accuracy by wire impedance inside IC of RNF terminal. Therefore, when operating current limit, please be sure to connect RNF terminal and RCL terminal. Moreover, it is possible to reduce deterioration of current detect accuracy by impedance of board pattern between RNF terminal and resistor for detecting current by connecting wiring from RCL terminal most adjacent to resistor for detecting current. Please design pattern considering wiring that is less influenced by noise. Additionally, when RCL terminal is shorted to GND, big current might flow due to a lack of normal current limit operation. Please be careful that OCP or TSD might operate in that case.

16. Control Signal Sequence

Though we recommend you input control signals of ENB, PWMB, BRKB, FGSW, CW, LPE terminals after inputting VCC, there is no problem if you input control signals before inputting VCC. If LPE terminal is set to "H" or "M" when being started, please be informed that if motor rotation cannot be detected within the set time (edge of FGO signal cannot be input), then the MLP circuit starts and motor fails to start. Moreover, the order of priority is set to control signal and IC internal signal. Please refer to the following table.

Priority	Input / Internal Signals
1st	ENB, UVLO
2nd	BRKB, CW, PWMB
3rd	TSD, OCP, MLP, HALLERR
4th	OVLO
5th	VG_UVLO
6th	BRKB
7th	CL
8th	PWMB, CW

17. Protection Circuit

17.1 Current Limit Circuit (CL circuit)

Current limit of output (Current Limit: CL) can be achieved by changing voltage of output current with resistor between RNF and GND, and then inputting the voltage into RCL terminal. In order to avoid error detection of current detection comparator by RNF spike noise that occurs at output ON, using mask time (0.5μs (Typ)) can be efficient. Current detection is invalid during mask time after RCL voltage becomes more than 0.2V (Typ). Then please turn OFF all lower MOS of driver output, which is returned automatically after specified time (32μs (Typ)). This operation is not synchronized with PWM signal that is input into PWMB terminal.

17.2 Thermal Shut Down Circuit (TSD Circuit)

When chip temperature of driver IC rises and exceeds the set temperature (165°C (Typ)), the thermal shut down circuit (Thermal Shut Down: TSD) begins to work. At this time, the driver outputs all become "Hi-z". In addition, the TSD circuit is designed with hysteresis (20°C (Typ)), therefore, when the chip temperature drops, it returns to normal working condition. Moreover, the purpose of the TSD circuit is to protect driver IC from thermal breakdown, therefore, temperature of this circuit will be over working temperature when it is started up. Thus, thermal design should have sufficient margin, so do not take continuous use and action of the circuit as a precondition.

17.3 Over Current Protection Circuit (OCP Circuit)

Over current protection (Over Current Protection: OCP) is built-in in order to prevent from destruction when being shorted between output terminals and also being VCC/GND shorted. Therefore output current exceeds ratings and specified current flows. In that case, driver outputs are all latched to Hi-z condition. Latch can be released by going through stand-by condition or switching BRKB/CW logic. However, output current rating is exceeded when this circuit operates. Thus, please design sufficient margin not to take continuous use and action of the circuit as a precondition.

17.4 Under Voltage Lock Out Circuit (UVLO Circuit)

There is a built-in under voltage lock out circuit (Under Voltage Lock Out: UVLO) used to ensure the lowest power supply voltage for drive IC to work and to prevent error action of IC. When VCC declines to V_{UVL} (6V (Typ)), all of the driver outputs should be "Hi-z". At the same time, UVLO circuit is designed with hysteresis (1V (Typ)), so when VCC reaches more than V_{UVH} (7V (Typ)), it enters normal working condition.

17.5 Over Voltage Lock Out Circuit (OVLO circuit)

There is built-in over voltage lock out circuit (Over Voltage Lock Out: OVLO) used to restrain rise of VCC when motor is decelerating. When LPE terminal is at "M" and VCC is over V_{OVH1} (16V (Typ)), and when LPE terminal is at "H" or "L" and VCC is over V_{OVH2} (31V (Typ)), a certain time (4ms (Typ)) of short brake action is conducted. What's more, because OVLO circuit is designed with hysteresis, therefore, when V_{OVH1} is below V_{OVL1} (15V (Typ)) and when V_{OVH2} is below V_{OVL2} (30.5V (Typ)), it can return to normal working condition after a certain time of short brake action.

17.6 Motor Lock Protection Circuit (MLP circuit)

There is built-in motor lock protection circuit (Motor Lock Protection: MLP). The Enable/Disable of MLP circuit and OVLO threshold can be set by the LPE terminal.

In monitoring Hall signals, when the LPE = "H" or "M" and Hall signal logic does not change to more than 1.1sec(Typ), all driver outputs are latched as "Hi-z".

There are three ways to release the latch.

・The latch is released by putting IC in standby mode.

・The latch is released by changing BRKB/CW logic.

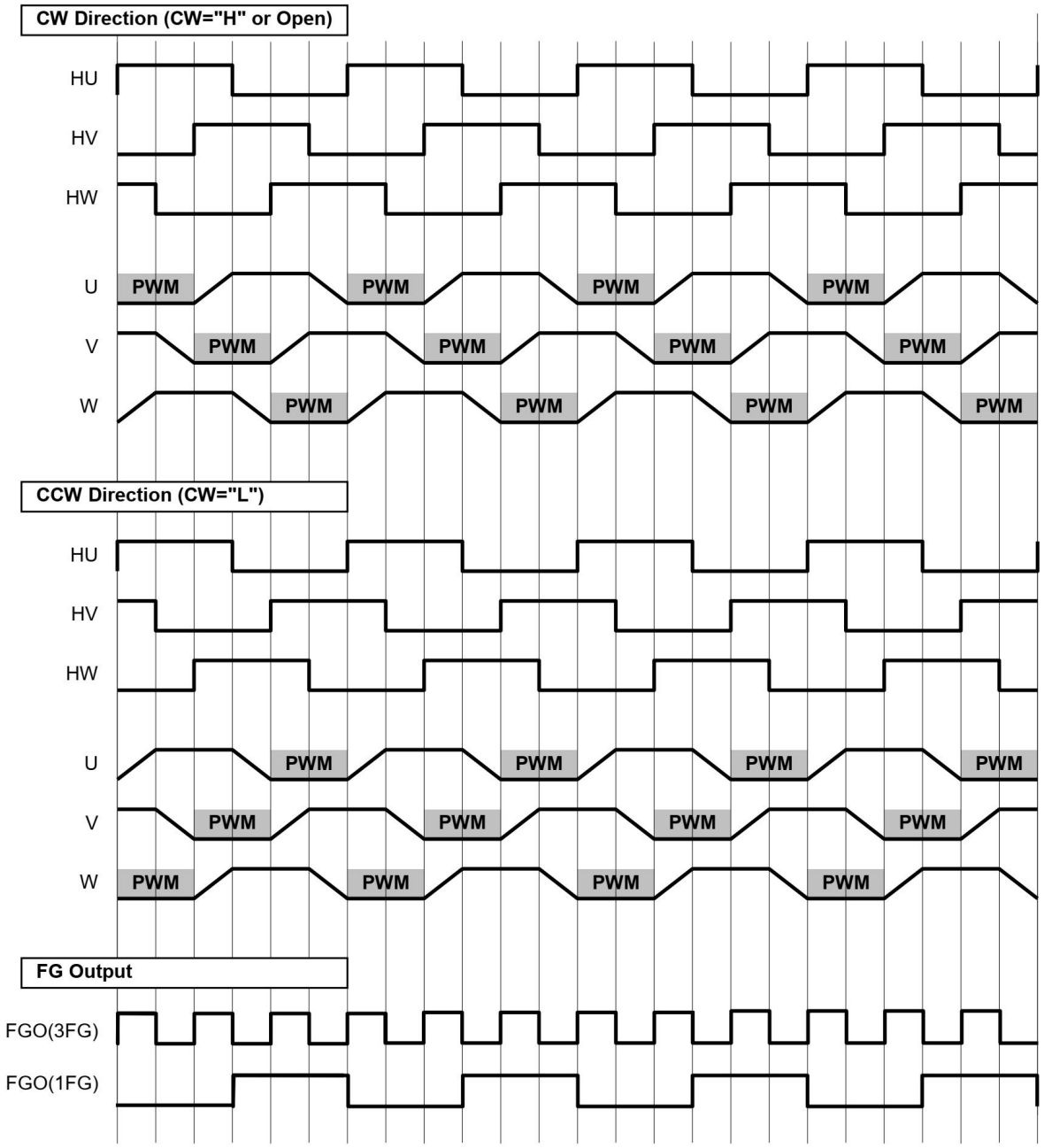
・After PWMB = "H" or OPEN state is detected for about 15ms(Typ), the latch is released by falling edge of subsequent PWMB.

However, when LPE = "L", short brake action (including switching rotation direction) enables or TSD circuit works, MLP circuit does not work.

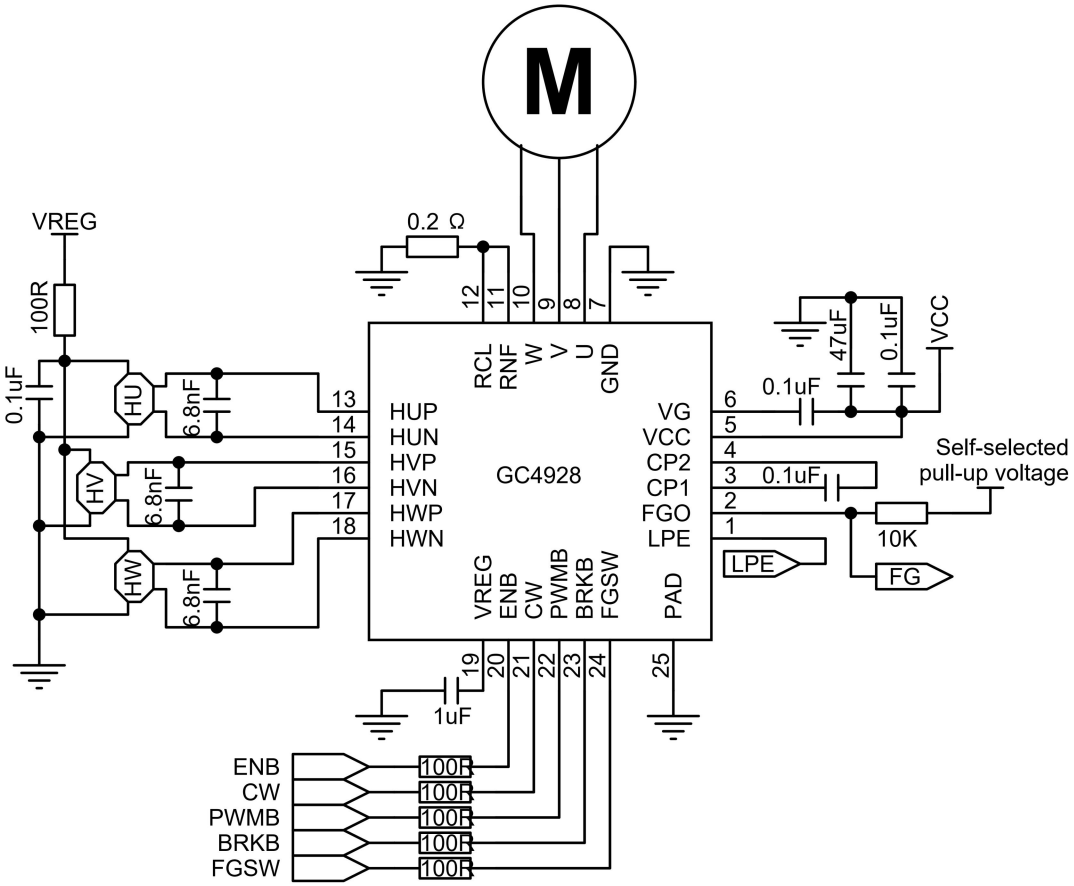
LPE terminal is pulled up by VREG through a resistance of 100kΩ (Typ) ±30 kΩ.

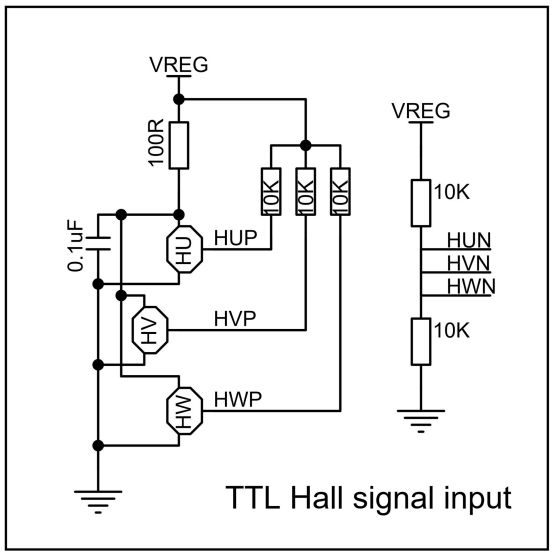
LPE	Direction	OVLO Threshold
H or OPEN	0.9sec(Typ) ±30%	V_{OVH2}, V_{OVL2}
M	0.9sec(Typ) ±30%	V_{OVH1}, V_{OVL1}
L	Disable	V_{OVH2}, V_{OVL2}

18. Timing Chart



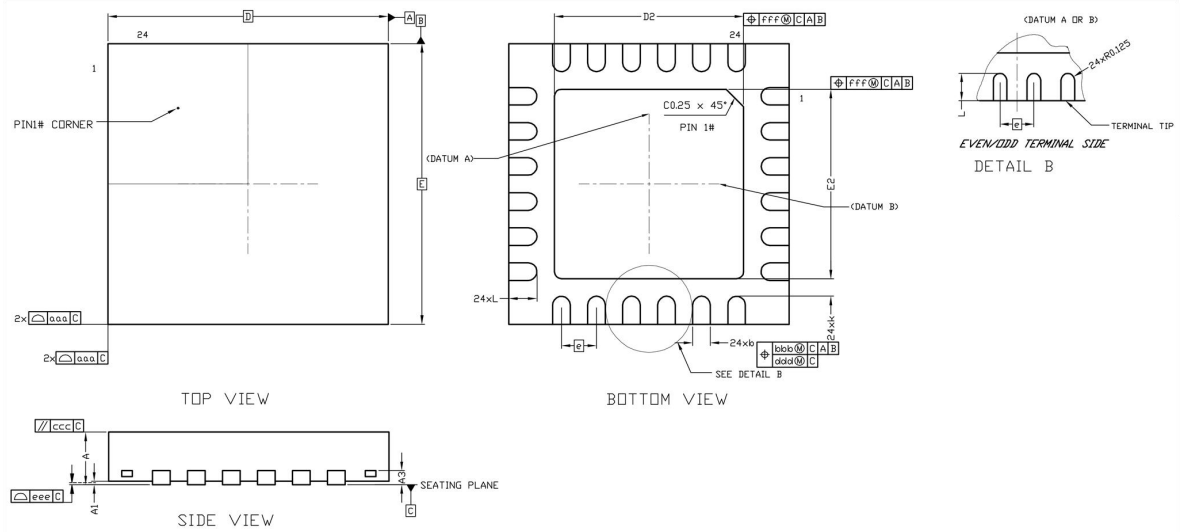
Typical Application





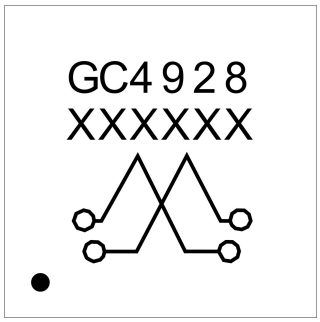
Package Information

QFN24 **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20 REF	-
B	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	-	-
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Description of Lot Code



Printing instructions:

1. The first line GC4928 represents the product model;
2. The second line represents the traceability code.

Revision History

Version	Description
V0.5	Initial version
V0.6	Update electrical data