RoHS HAL Green

1 MHz, Low-Power Op Amp

The Htcsemi Technology Inc. HT6001/2/4 family of operational amplifiers (op amps) is specifically designed for general purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90°
phase margin (typical). It also maintains a 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single-supply voltage as low as 1.8V, while drawing 100 µA (typical) quiescent current. Additionally, the HT6001/2/4 supports rail-to-rail input and output swing, with a Common-mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of op amps is designed with Htcsemi's advanced CMOS process.

Features

- Available in 5-Lead SOT-23 Packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I_Q = 100 µA (typical)
- Phase Margin: 90° (typical)
- Available in Single, Dual and Quad Packages

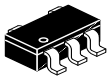
Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

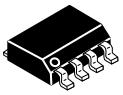
Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer and Analog Simulator
- Htcsemi Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

ORDERINGINFORMATION

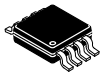


SOT23-5
T SUFFIX
HT6001ARTZ



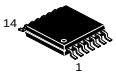
SOP–8
R SUFFIX
HT6002ARZ

DFN–8
D SUFFIX
HT6002ARDZ



MSOP–8
M SUFFIX
HT6002ARMZ

SOP14 R SUFFIX
HT6004ARZ

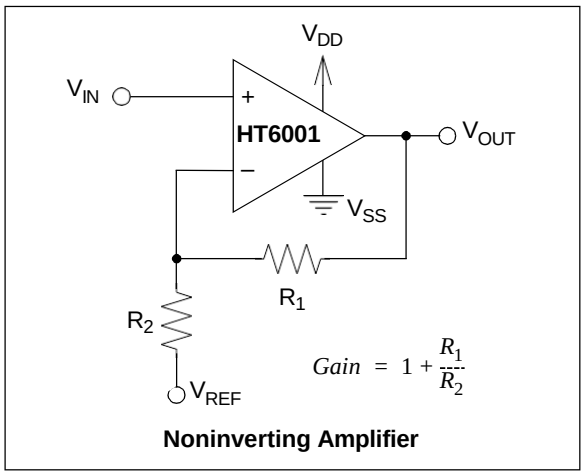


TSSOP14
T SUFFIX
HT6004ARTZ

&HT600x	= Specific Device Code
&A	= Version
&R,RD,RM,RT	= Packaging
&Z	= Pb–Free Package
&#	=Date Code

T_A = -40° to 125°C for all packages

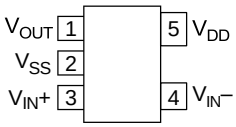
Typical Application



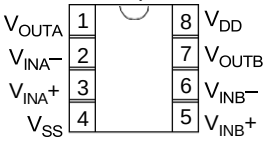
Noninverting Amplifier

Pin Configuration

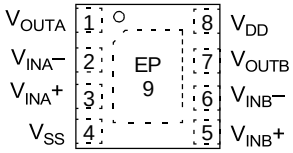
HT6001
SOT-23-5



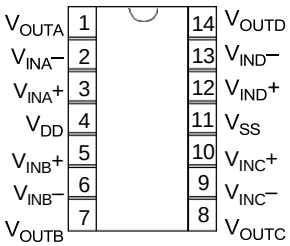
HT6002
SOP,MSOP



HT6002
2x3 DFN



HT6004
SOP, TSSOP



* Includes Exposed Thermal Pad (EP); see Table 3-1.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

$V_{DD} - V_{SS}$ V
Current at Analog Input Pins (V_{IN}+, V_{IN}-) ..... ±2 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current ..... Continuous
Current at Output and Supply Pins ..... ±30 mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 4 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and $V_{OUT} \approx V_{DD}/2$ (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	±1.0	—	pA	
Industrial Temperature	I_B	—	19	—	pA	T_A = +85°C
Extended Temperature	I_B	—	1100	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common-Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common-Mode						
Common-Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common-Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB	V_{OUT} = 0.3V to V_{DD} – 0.3V, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	6.0	V	**Note 2**
Quiescent Current per Amplifier	I_Q	50	100	170	µA	I_O = 0, V_{DD} = 5.5V, V_{CM} = 5V

Note 1: HT6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

2: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_L = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1 V/V
Slew Rate	SR	—	0.6	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	6.1	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Industrial Temperature Range	T_A	-40	—	+85	°C	
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5-Lead SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8-Lead PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8-Lead SOIC (150 mil)	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8-Lead MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8-Lead DFN (2x3)	θ_{JA}	—	68	—	°C/W	
Thermal Resistance, 14-Lead PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14-Lead SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14-Lead TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's Common-mode voltage ((V_P + V_M)/2) and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	= Differential-Mode Gain	(V/V)
V_{CM}	= Op Amp's Common-Mode Input Voltage	(V)
V_{OST}	= Op Amp's Total Input Offset Voltage	(mV)

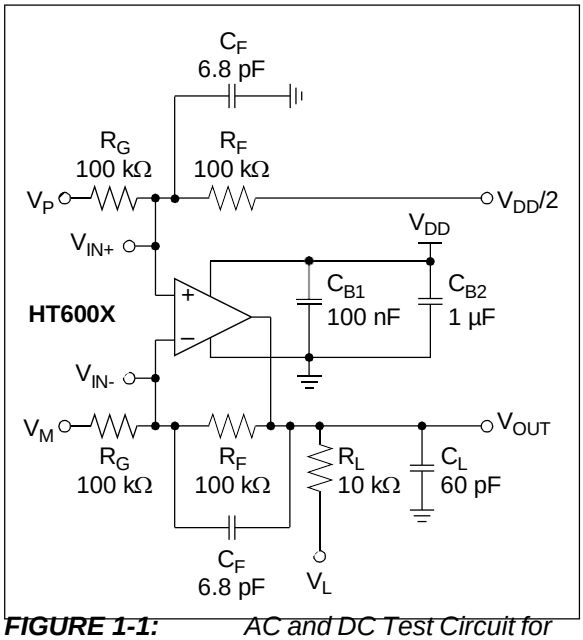


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

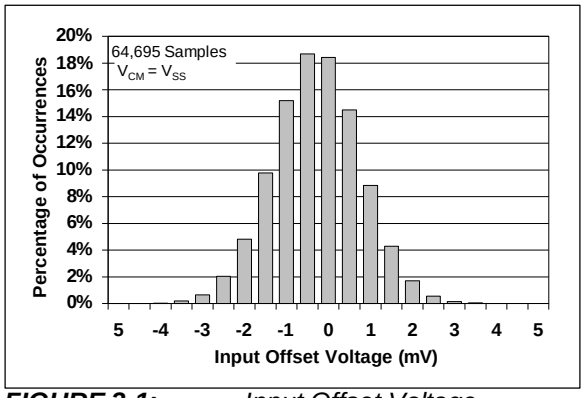


FIGURE 2-1: *Input Offset Voltage.*

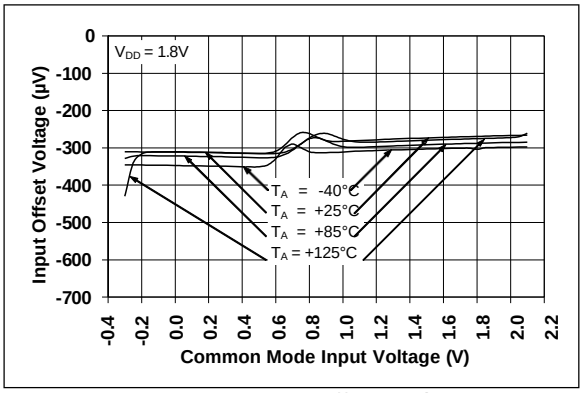


FIGURE 2-4: *Input Offset Voltage vs. Common-Mode Input Voltage at V_{DD} = 1.8V.*

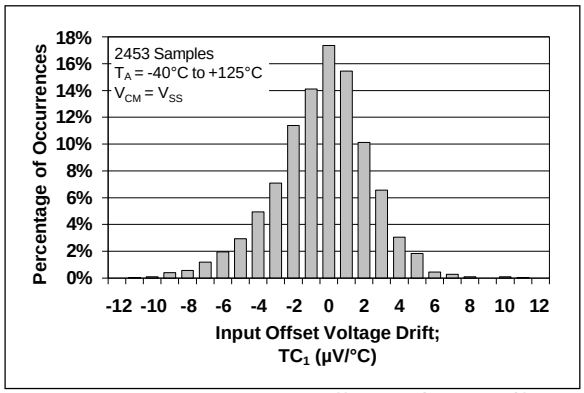


FIGURE 2-2: *Input Offset Voltage Drift.*

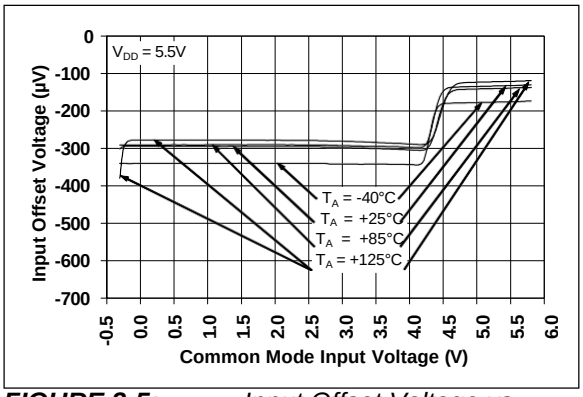


FIGURE 2-5: *Input Offset Voltage vs. Common-Mode Input Voltage at V_{DD} = 5.5V.*

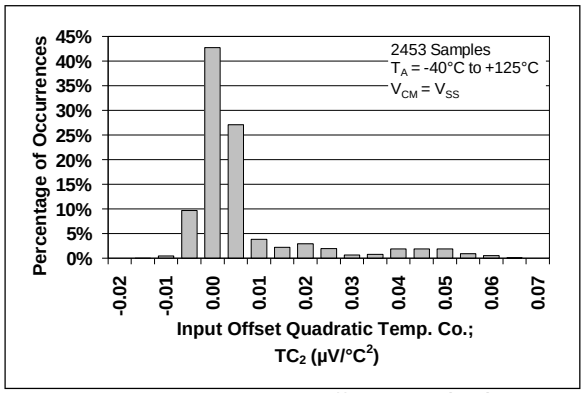


FIGURE 2-3: *Input Offset Quadratic Temp. Co.*

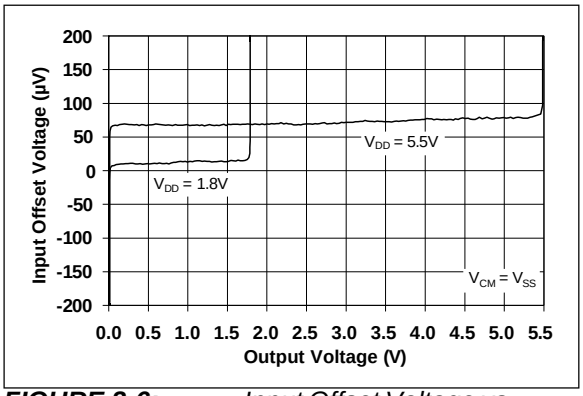


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

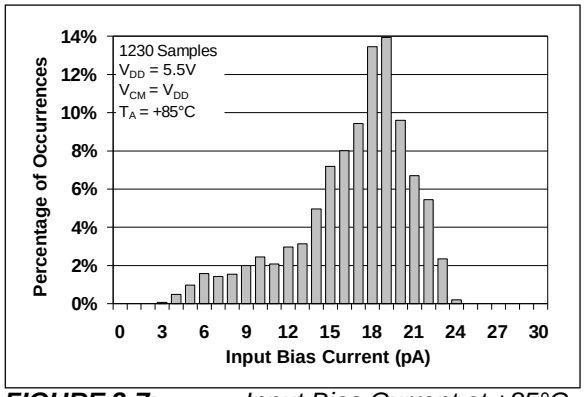


FIGURE 2-7: *Input Bias Current at +85°C.*

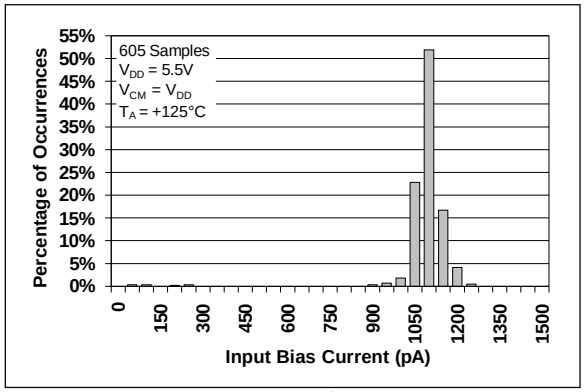


FIGURE 2-8: *Input Bias Current at +125°C.*

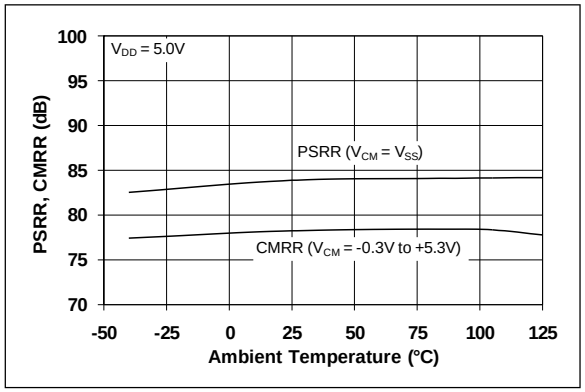


FIGURE 2-9: *CMRR, PSRR vs. Ambient Temperature.*

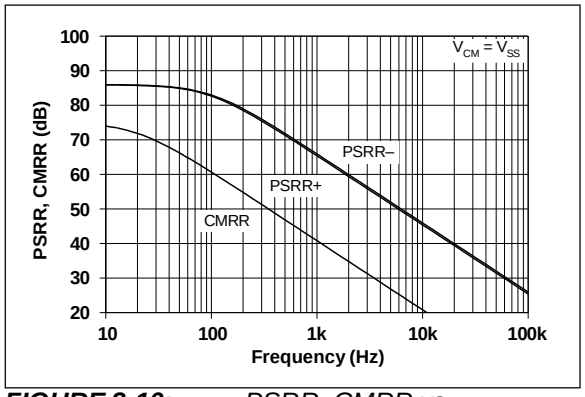


FIGURE 2-10: *PSRR, CMRR vs. Frequency.*

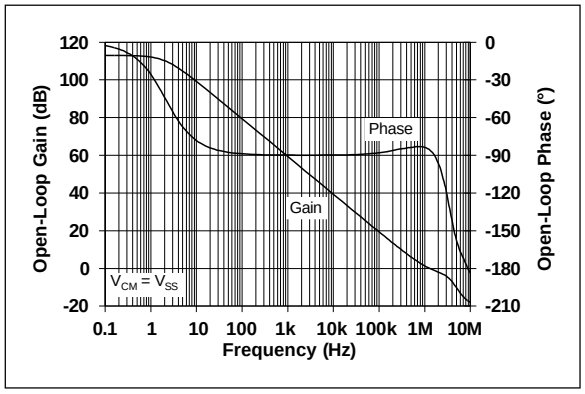


FIGURE 2-11: *Open-Loop Gain, Phase vs. Frequency.*

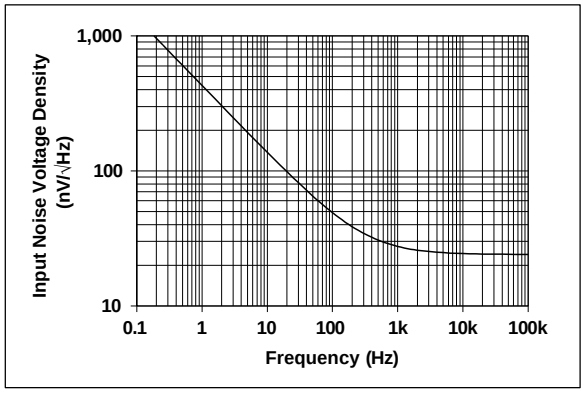


FIGURE 2-12: *Input Noise Voltage Density vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

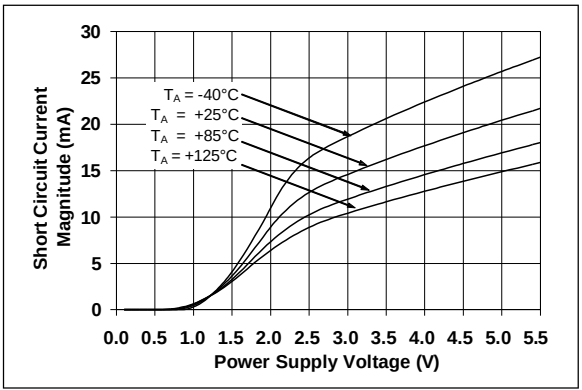


FIGURE 2-13: *Output Short-Circuit Current vs. Power Supply Voltage.*

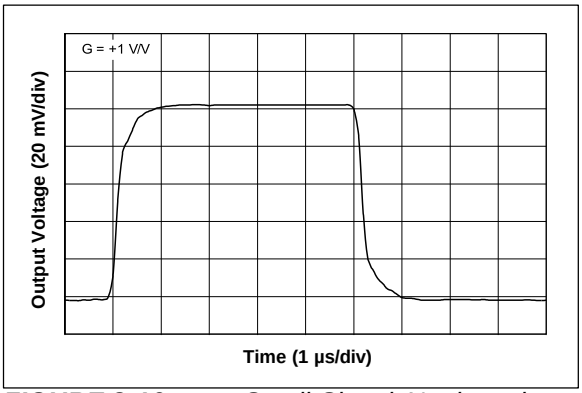


FIGURE 2-16: *Small-Signal, Noninverting Pulse Response.*

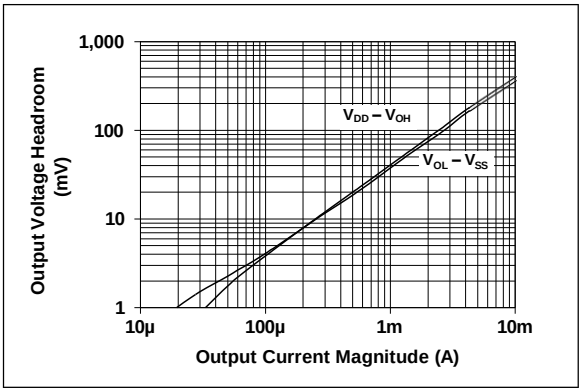


FIGURE 2-14: *Output Voltage Headroom vs. Output Current Magnitude.*

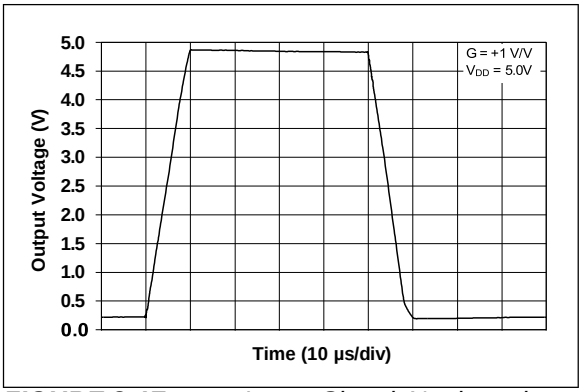


FIGURE 2-17: *Large-Signal, Noninverting Pulse Response.*

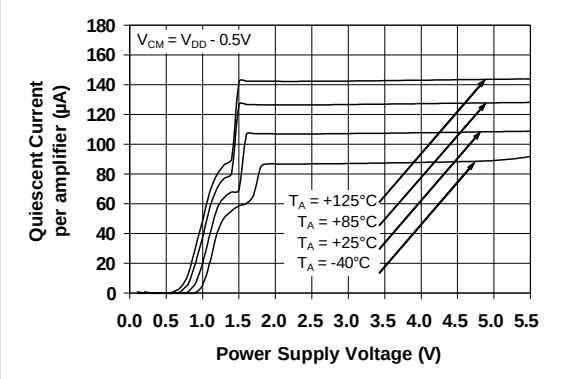


FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage.*

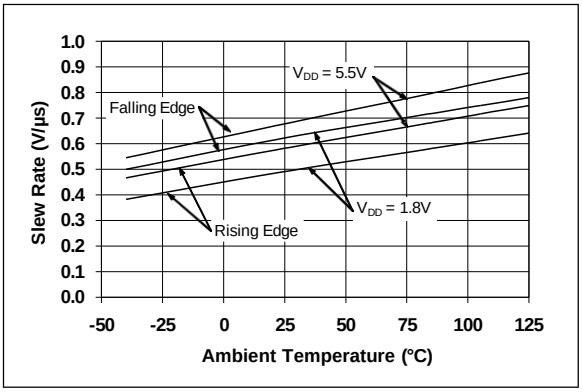


FIGURE 2-18: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

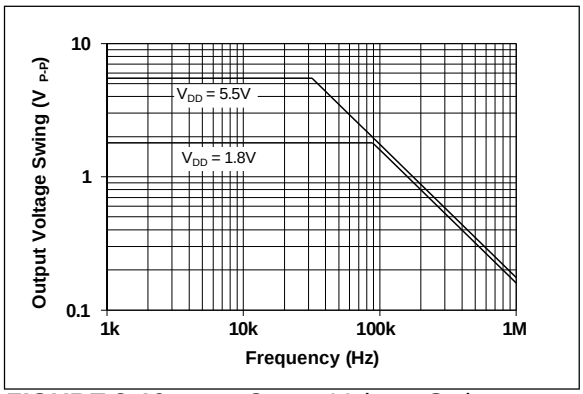


FIGURE 2-19: *Output Voltage Swing vs. Frequency.*

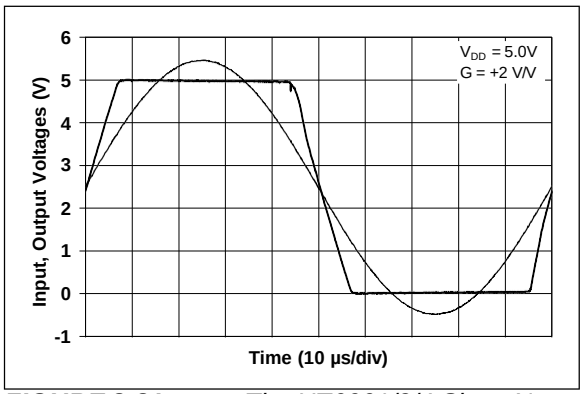


FIGURE 2-21: *The HT6001/2/4 Show No Phase Reversal.*

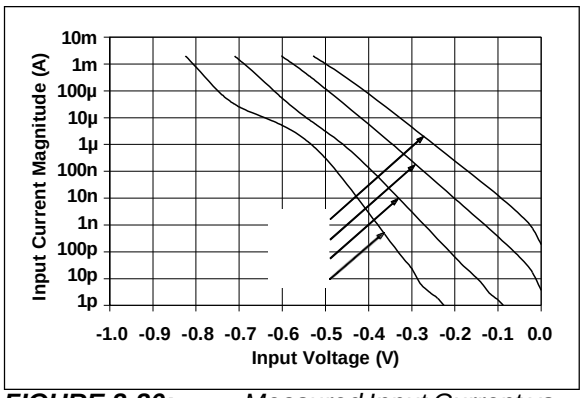


FIGURE 2-20: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

4.0 APPLICATION INFORMATION

The HT6001/2/4 family of op amps is manufactured using Htcsemi's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the HT6001/2/4 ideal for battery-powered applications. These devices have high phase margin, which makes them stable for larger capacitive load applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The HT6001/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-21 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize Input Bias (I_B) current. The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation and low enough to bypass quick ESD events within the specified limits.

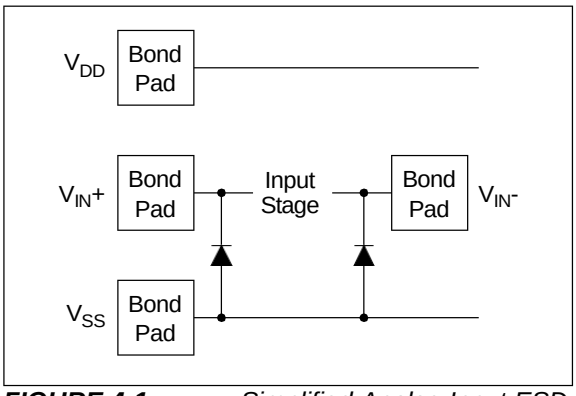


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V_{IN}+ and V_{IN}- pins (see **Absolute Maximum Ratings†** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, and the resistors, R_1 and R_2, limit the possible current drawn out of the input pins. Diodes, D_1 and D_2, prevent the input pins (V_{IN}+ and V_{IN}-) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors, R_1 and R_2, also limit the current through D_1 and D_2.

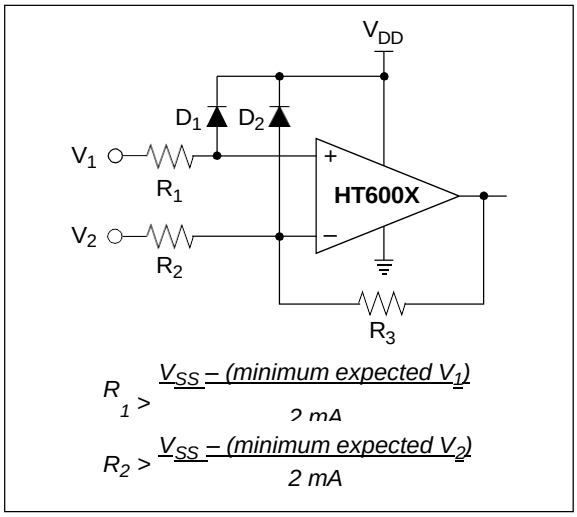


FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors, R_1 and R_2. In this case, current through the diodes, D_1 and D_2, needs to be limited by some other mechanism. The resistors then serve as inrush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}-) should be very small.

A significant amount of current can flow out of the inputs when the Common-Mode Voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-20. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the HT6001/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low Common-mode input voltage (V_{CM}), while the other operates at high V_{CM}. With this topology, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS}.

The transition between the two input stages occurs when $V_{CM} = V_{DD} – 1.1V$. For the best distortion and gain linearity, with noninverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the HT6001/2/4 op amps is $V_{DD} – 25$ mV (minimum), and $V_{SS} + 25$ mV (maximum) when $R_L = 10$ kΩ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figure 2-14 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., >100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

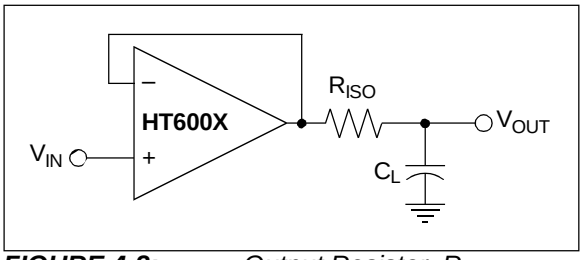


FIGURE 4-3: *Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For noninverting gains, G_N and the signal gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

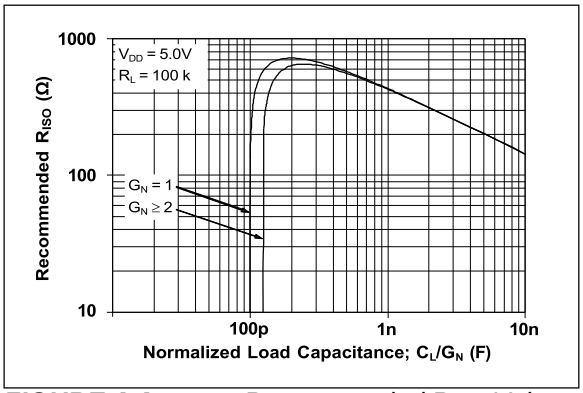


FIGURE 4-4: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the HT6001/1R/1U/2/4 SPICE macro model are very helpful.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (HT6004) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

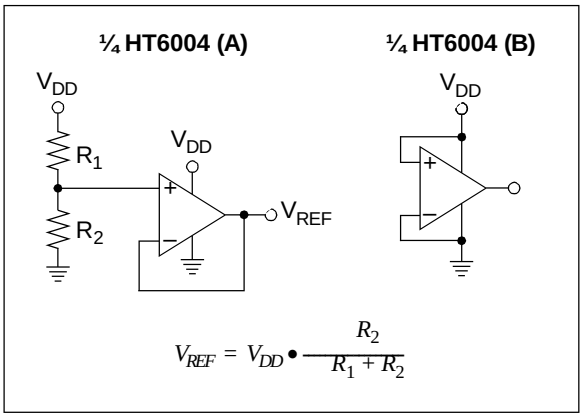


FIGURE 4-5: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the HT6001/1R/1U/2/4 family's bias current at +25°C (typically 1 pA).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

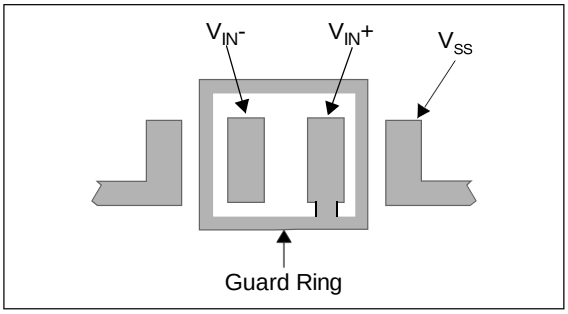


FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

1. Noninverting Gain and Unity Gain Buffer:
   a. Connect the noninverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}-). This biases the guard ring to the Common-mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}-) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 UNITY GAIN BUFFER

The rail-to-rail input and output capability of the HT6001/2/4 op amp is ideal for unity gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-7.

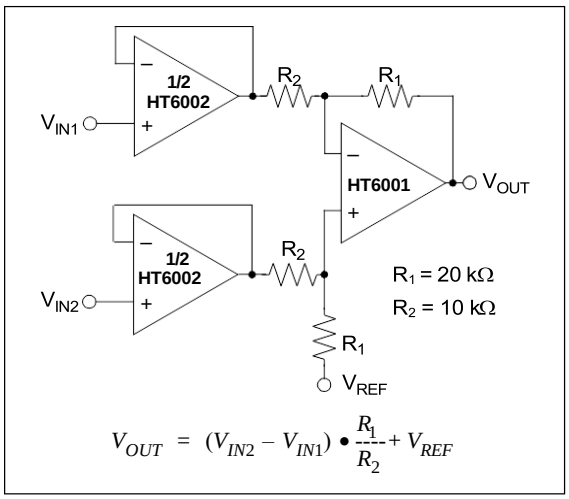


FIGURE 4-7: *Instrumentation Amplifier with Unity Gain Buffer Inputs.*

4.7.2 ACTIVE LOW-PASS FILTER

The HT6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100x the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10x higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-8 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10x higher than the cutoff frequency. The component values were selected using Htcsemi's FilterLab® software.

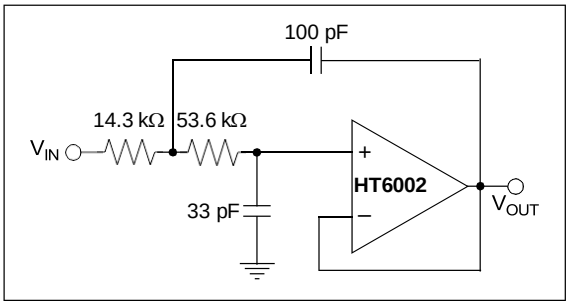


FIGURE 4-8: *Active Second-Order Low-Pass Filter.*

4.7.3 PEAK DETECTOR

The HT6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. Figure 4-9 shows a peak detector circuit with clear and sample switches. The peak detection cycle uses a clock (CLK), as shown in Figure 4-9.

At the rising edge of the CLK, the sample switch closes to begin sampling. The peak voltage stored on C_1 is sampled to C_2 for a sample time defined by t_{SAMP}. At the end of the sample time (falling edge of sample signal), the clear signal goes high and closes the clear switch. When the clear switch closes, C_1 discharges through R_1 for a time defined by t_{CLEAR}. At the end of the clear time (falling edge of the clear signal), Op Amp A begins to store the peak value of V_{IN} on C_1 for a time defined by t_{DETECT}.

In order to define t_{SAMP} and t_{CLEAR}, it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R_1 ($\tau = R_1C_1$). t_{DETECT} is the time that the input signal is sampled on C_1 and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C_1 and C_2), could create slewing limitations as the Input Voltage (V_{IN}) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short-circuit current of I_{SC} = 25 mA and a load capacitor of C_1 = 0.1 µF, then:

EQUATION 4-1:

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25mA}{0.1\mu F}$$

$$\frac{dV_{C1}}{dt} = 250mV/\mu s$$

This voltage rate of change is less than the HT6001/2/4 slew rate of 0.6 V/µs. When the input voltage swings below the voltage across C_1, D_1 becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 µF capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40 µF and a stabilizing resistor (R_{ISO}) needs to be properly selected. (Refer to **Section 4.3 "Capacitive Loads"**.)

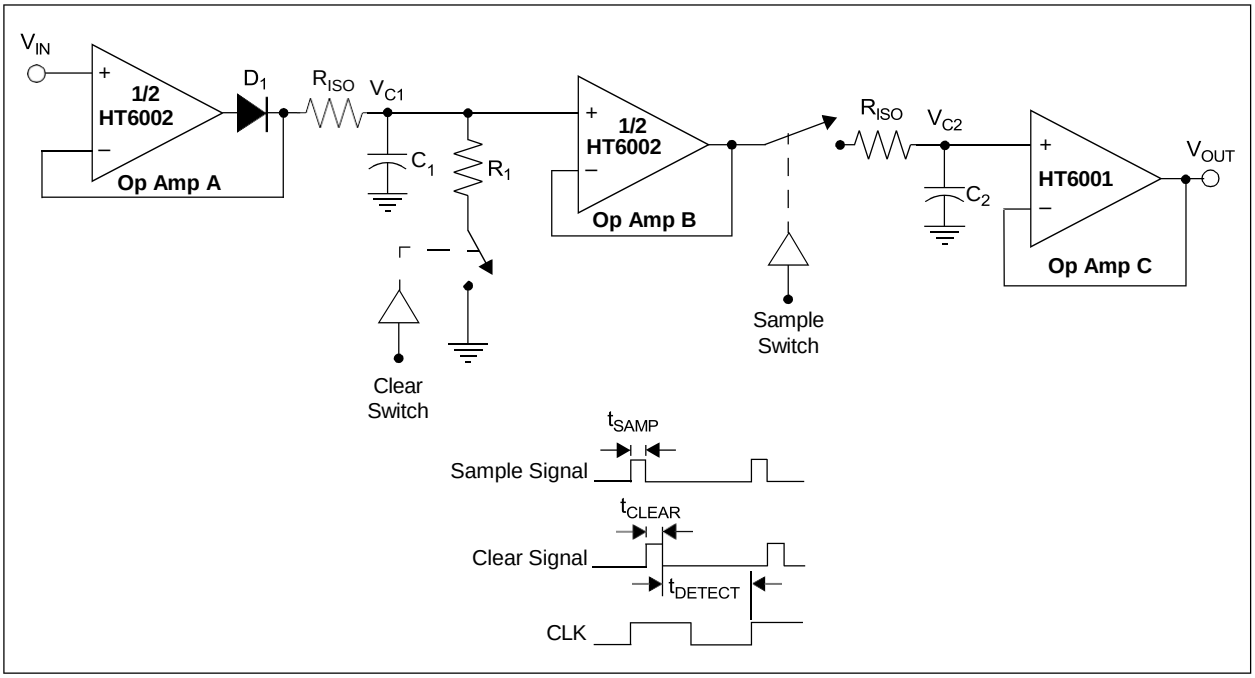
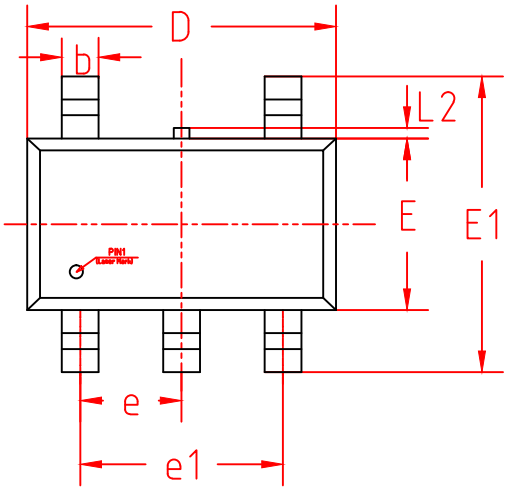


FIGURE 4-9: *Peak Detector with Clear and Sample CMOS Analog Switches.*

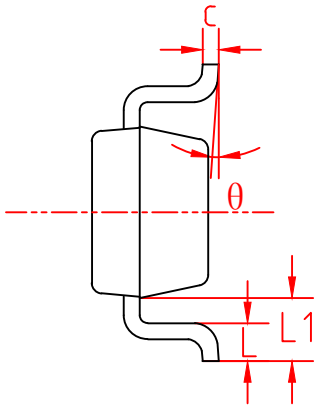
PACKAGE OUTLINE DIMENSIONS

SOT23-5

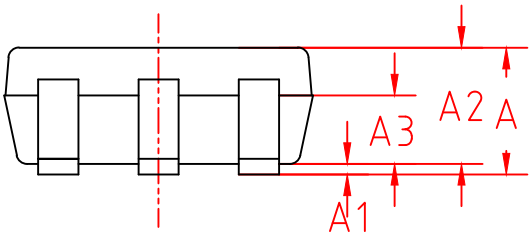
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图

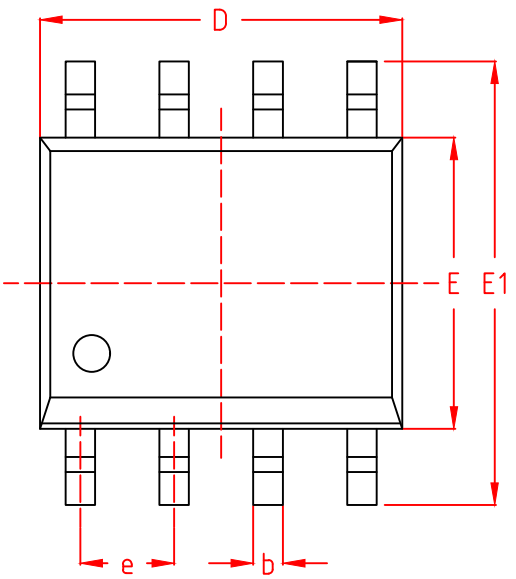


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.25
A1	0.00	–	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	–	0.50
c	0.14	–	0.20
D	2.82	2.92	3.02
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
e	0.95 BSC		
e1	1.90 BSC		
L1	0.59 REF		
L2	–	–	0.15
L	0.35	0.45	0.60
θ	0°	–	8°

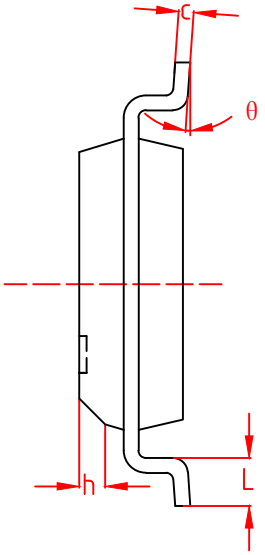
PACKAGE OUTLINE DIMENSIONS

SOP8

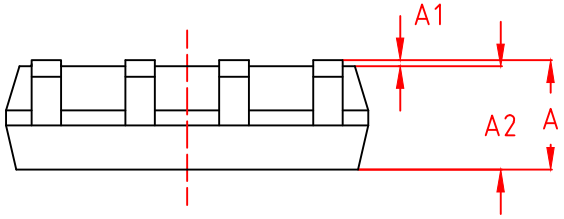
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图

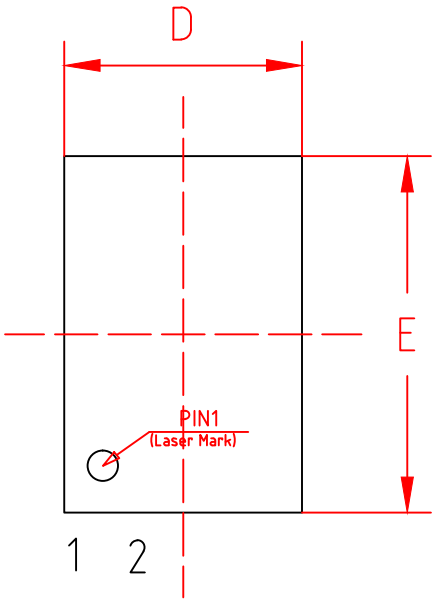


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
b	0.35	–	0.50
c	0.19	–	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.25	–	0.45
L	0.50	–	0.80
θ	0°	–	8°

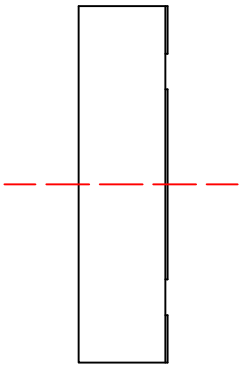
PACKAGE OUTLINE DIMENSIONS

DFN8L(2x3x0.75-P0.5)

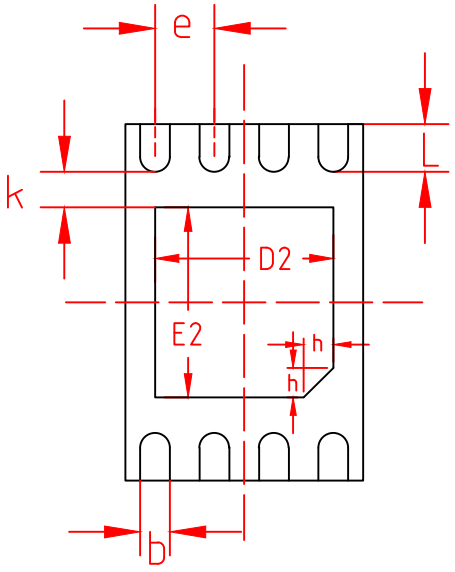
TOP VIEW
正视图



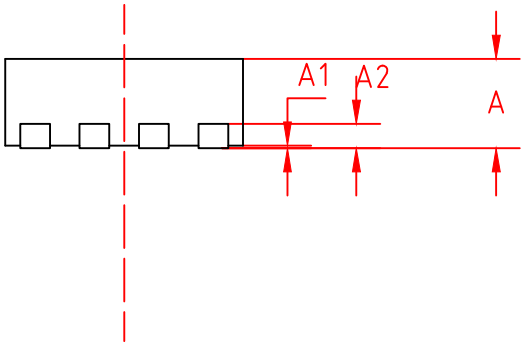
SIDE VIEW
侧视图



BOTTOM VIEW
背视图



SIDE VIEW
侧视图

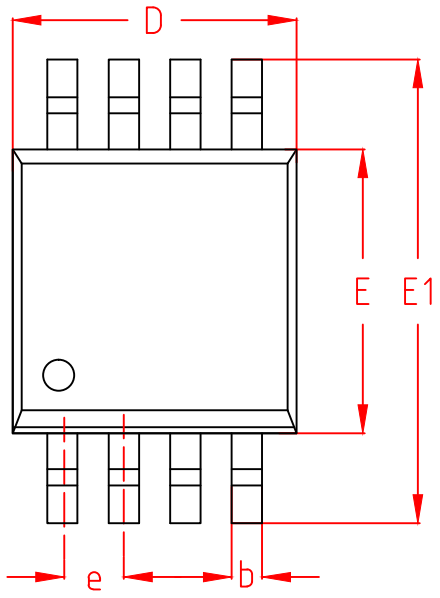


机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	–	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
e	0.50 BSC		
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30
K	0.25	0.30	0.35

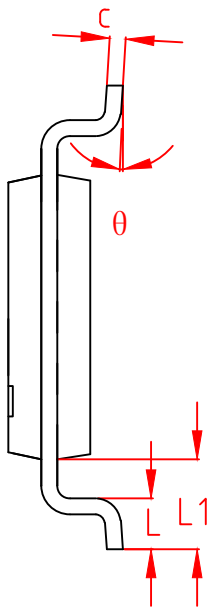
PACKAGE OUTLINE DIMENSIONS

MSOP8L

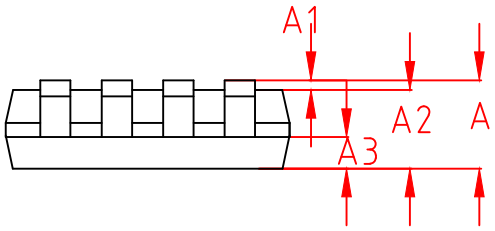
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图

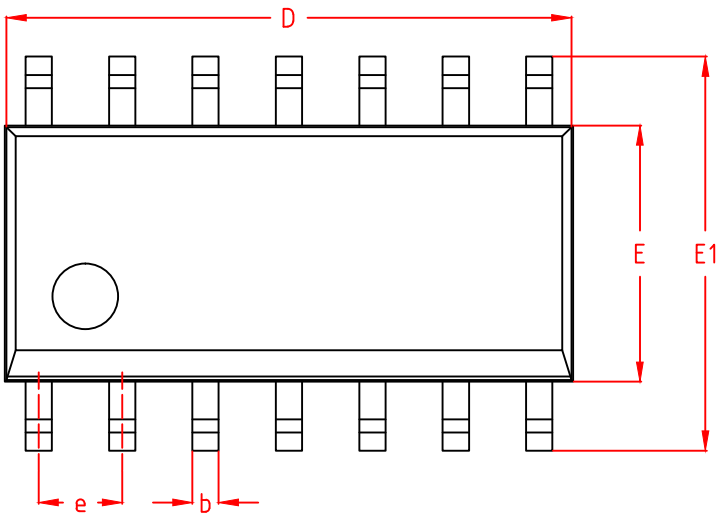


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.10
A1	0.05	–	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	–	0.36
c	0.15	–	0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.65 BSC		
L1	0.95 REF		
L	0.40	–	0.70
θ	0°	–	8°

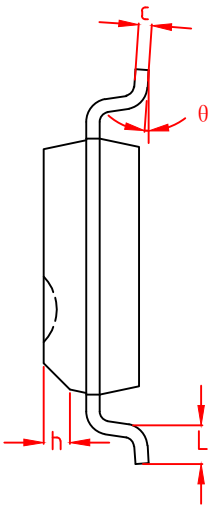
PACKAGE OUTLINE DIMENSIONS

SOP14L

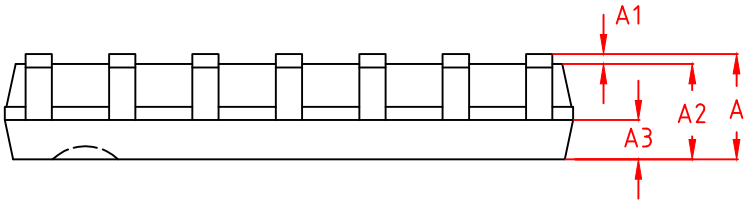
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图



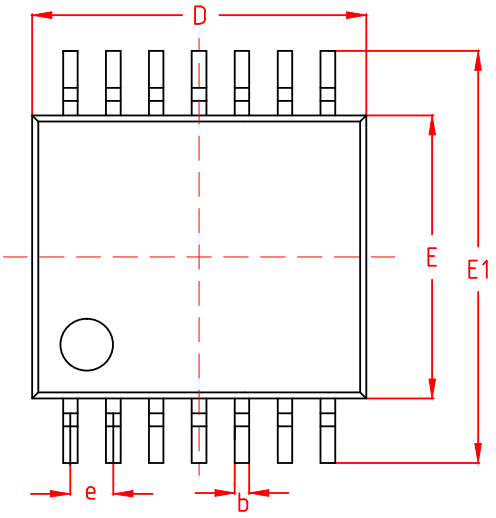
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	–	0.50
c	0.19	–	0.25
D	8.50	8.60	8.70
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°

PACKAGE OUTLINE DIMENSIONS

TSSOP14L

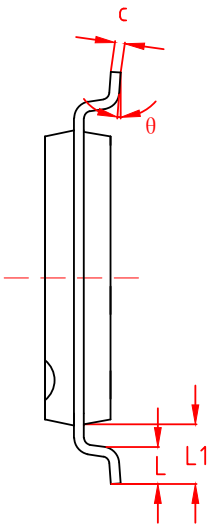
TOP VIEW

正视图



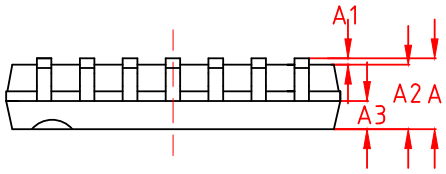
SIDE VIEW

侧视图



SIDE VIEW

侧视图



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	–	0.28
c	0.13	–	0.17
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00REF		
L	0.45	0.60	0.75
θ	0°	–	8°