40V 1A, 1MHz Synchronous Step-Down DCDC Converter

1 FEATURES

- Wide Input Range: 4.6V-40V
- Up to 1A Continuous Output Current
- 0.61V Feedback Reference Voltage
- Integrated 400mΩ High-Side and 200mΩ Low-Side Power MOSFETs
- Fixed Frequency 1MHz
- Pulse Skipping Mode (PSM) at Light Load
- 80uA Quiescent Current in Sleep Mode
- 80ns Minimum On-time
- 1ms Internal Soft-start Time
- Protections with Input UVLO, OCP, OT and OVP

2 APPLICATIONS

- Industrial 24V Distributed Power Bus
- Power Meter
- Elevator, PLC, Servo
- Automatic Control

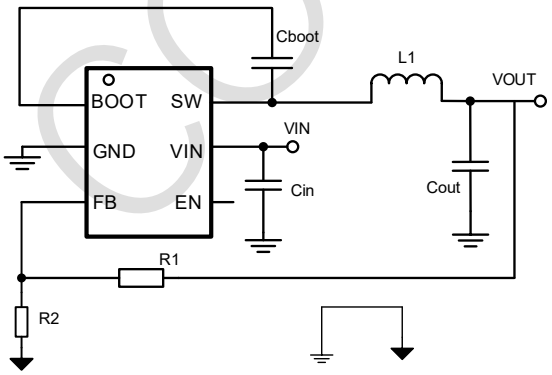
3 ORDERING INFORMATION

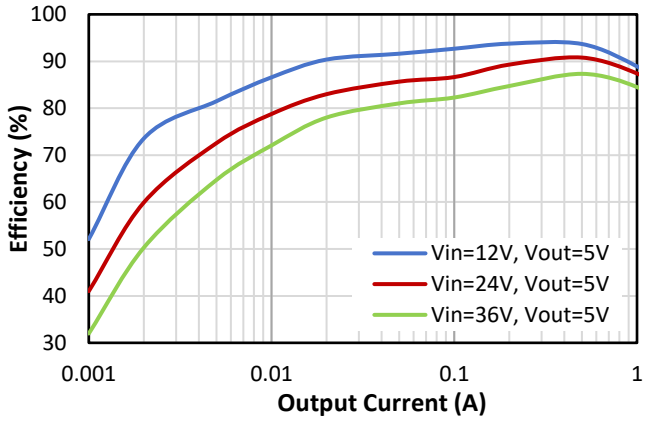
TYPE	MARKING	PACKAGE
GBI1412TKBR	1412	TSOT23-6L

4 DISCRIPTION

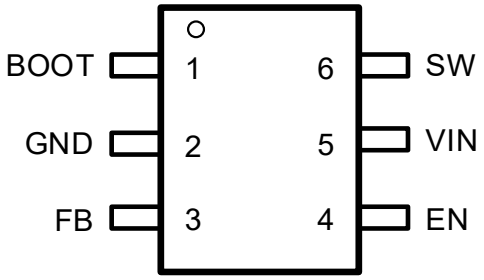
The GBI1412 is 40V, 1A buck converter with an integrated 400 mΩ high-side MOSFET and 200 mΩ low-side MOSFET. The GBI1412 has wide input range from 4.6V to 40V, the GBI1412 is suitable for variable applications which is from unregulated sources, like industrial or automotive applications. The device adopts peak current mode and has the fixed switching frequency. The quiescent current of this device is 80uA in sleep mode and the shutdown current is 1uA, making it suitable for battery-powered system. The device integrates protections, like cycle-by-cycle current limit, thermal shutdown, short-circuit and over-voltage protection. It' s available in a cost effective TSOT23-6L package.

5 TYPICAL APPLICATION





6 PIN CONFIGURATION AND FUNCTIONS



Top View: GBI1412 TSOT23-6L

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
BOOT	1	I	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
GND	2	-	Power ground.
FB	3	I	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.61V typically.
EN	4	I	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.25V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
VIN	5	I	Power supply input. Must be locally bypassed.
SW	6	O	Switching node of the buck converter.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	PARAMETER	MIN	MAX	UNIT
Input Voltage	VIN to GND	-0.3	45	V
	EN to GND	-0.3	45	V
	FB to GND	-0.3	6	V
Input Voltage	BOOT to SW	-0.3	6	V
Output Voltage	SW to GND	-1	45	V
	SW to GND(≤ 30ns transients)	-3	45	V
Junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-55	160	°C

7.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)		±2000	V
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)		±500	V

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
VIN	Supply voltage range	4.6	40	V
BOOT	BOOT voltage range	5	46	V
BOOT to SW	BOOT to SW voltage	-0.3	6	V
SW	SW voltage range	-1	40	V
FB	FB voltage range	0	6	V
EN	EN voltage range	0	40	V
T_J	Operating junction temperature	-40	125	°C

7.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT-6L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	102	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	36.9	°C/W
ψ_{JB}	Junction to board characterization parameter	28.4	°C/W

7.5 ELECTRICAL CHARACTERISTICS

VIN=EN=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
VIN	Operating input voltage		4.6		40	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.3 450	4.5	V mV
I_{SHDN}	Shutdown current	EN=0, No load, V_{IN}=12		1	3	uA
I_Q	Quiescent current	EN=floating, No load, No switch, V_{IN}=12V, BOOT-SW=5V		80		uA
Enable and Feedback						
V_{EN_H}	Enable high threshold		1.21	1.25	1.29	V
V_{EN_L}	Enable low threshold			1.1		V
V_{FB}	Feedback Voltage		0.59	0.61	0.63	V
Power MOSFET						
R_{DSON_H}	High side FET on-resistance		340	400	740	mΩ
R_{DSON_L}	Low side FET on-resistance		170	200	350	mΩ
Switching Characteristics						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V		1000		KHz
t_{ON_MIN}	Minimum on-time			80		ns
Soft Start Time and Protection						
t_{SS}	Internal soft-start time			1		ms
I_{LIM_HSD}	HSD peak current limit			1.9		A
I_{LIM_LSD}	LSD valley current limit			1.4		A
T_{SD}	Thermal shutdown threshold			170		°C
	Hysteresis			30		

8 TYPICAL CHARACTERISTICS

VIN=12V, L=15uH, Cout= 2x10uF, T_A= 25°C, unless otherwise noted.

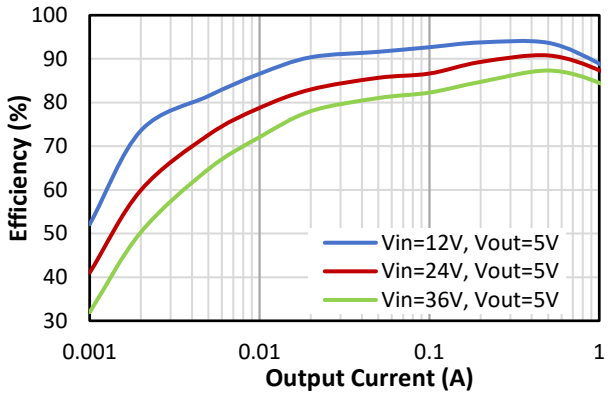


Figure 1. Efficiency Curve

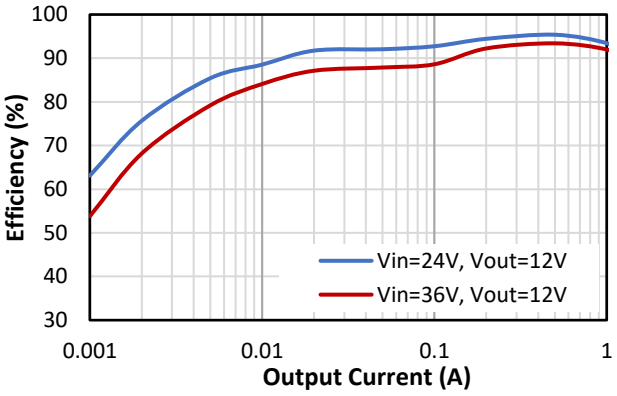


Figure 2. Efficiency Curve, L=22uH

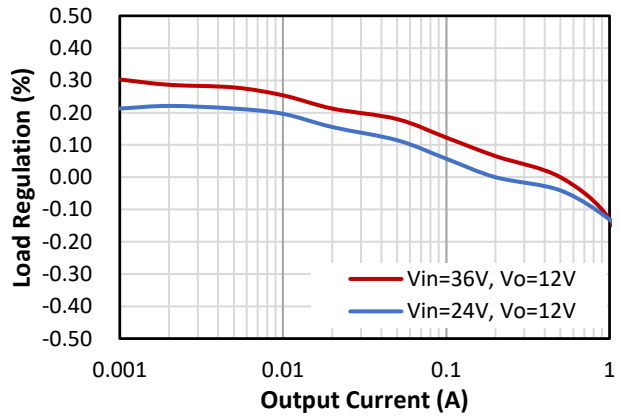


Figure 3. Load Regulation, L=22uH

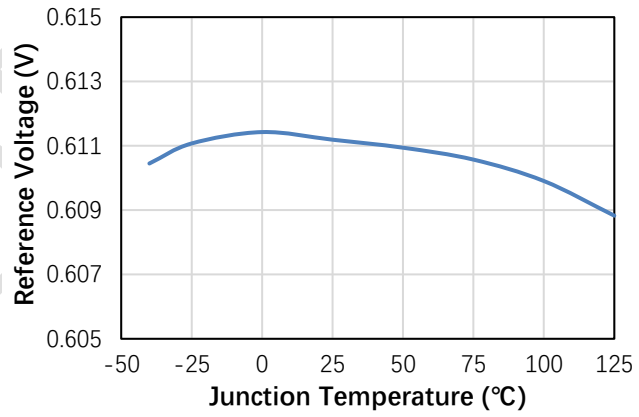


Figure 4. Reference Voltage vs. Junction Temperature

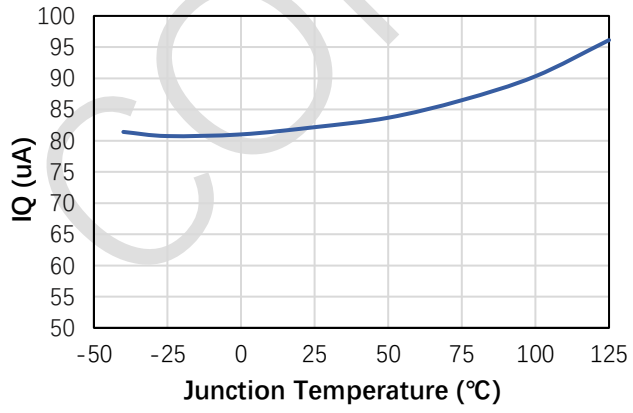


Figure 5. IQ vs Junction Temperature

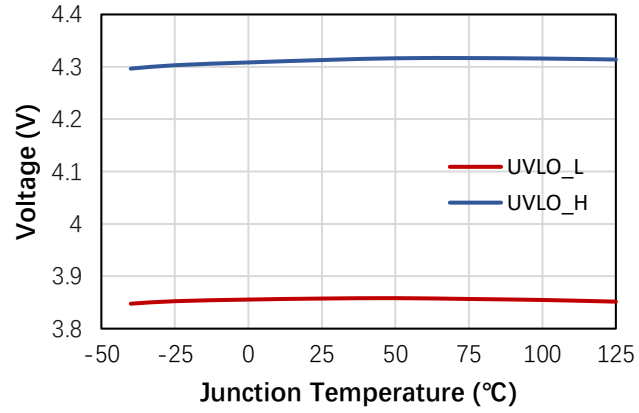


Figure 6. UVLO vs Junction Temperature

9 FUNCTIONAL BLOCK DIAGRAM

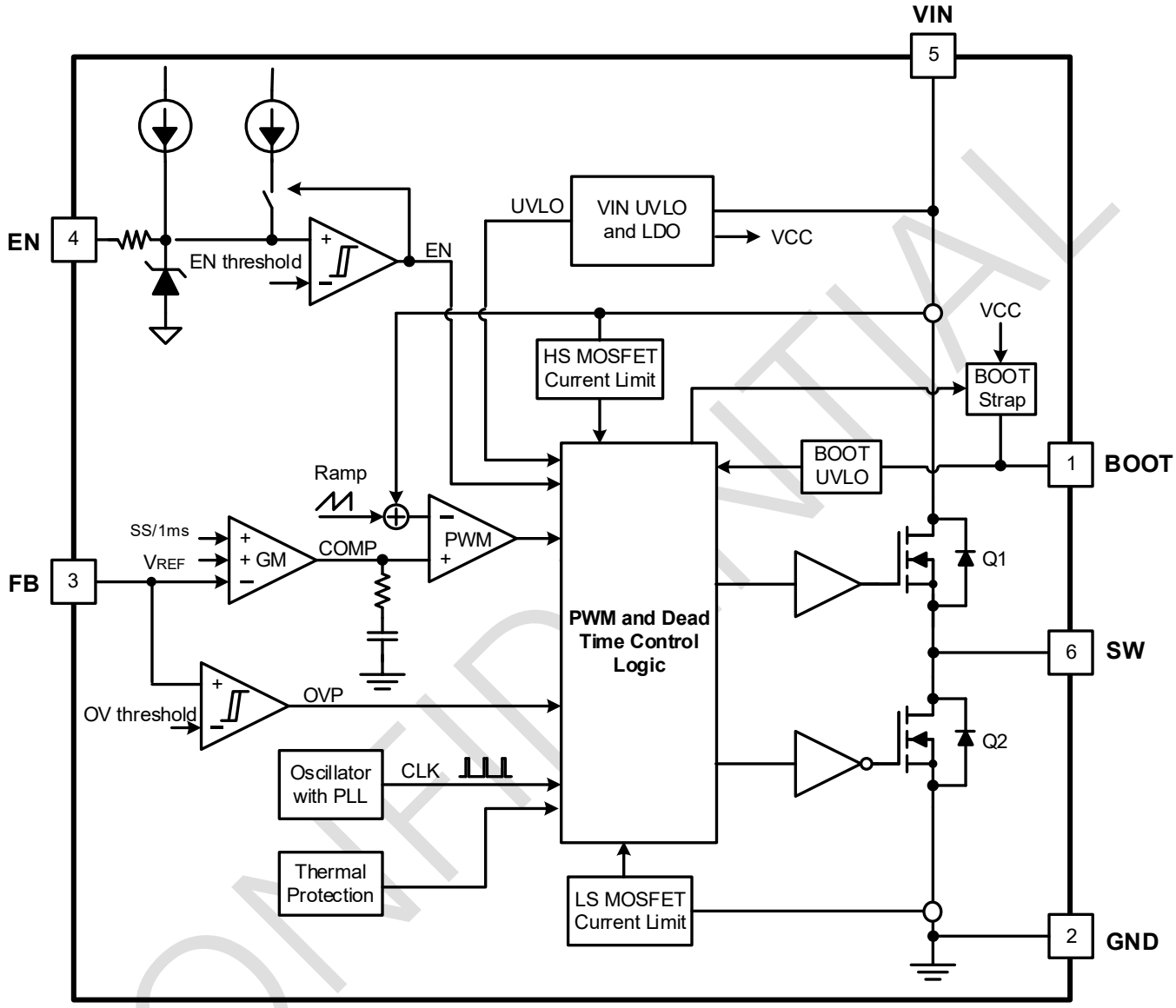


Figure 7. Block Diagram for GBI1412

10 DISCRIPTION

10.1 Overview

The GBI1412 is a 40V, 1A buck converter with an integrated 400 mΩ high-side MOSFET and 200 mΩ low-side MOSFET. With a wide input range from 4.6V to 40V, the device adopts peak current mode and supports a fixed 1MHz switching frequency to minimize off-chip components. The GBI1412 features an internal 1ms soft-start time.

The quiescent current of this device is 80uA in sleep mode and the shutdown current is 1uA. The GBI1412 features an internal 1ms soft-start time. The device has a default input start-up voltage of 4.3V with 450mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device. Connecting EN pin to VIN directly starts up the device automatically.

The device integrates protections, like cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and output short circuit protection and input voltage under-voltage protection. The device also supports monolithic startup with pre-biased output condition.

10.2 Peak Current Mode Control

The GBI1412 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the internal compensation voltage of the internal error amplifier, the high-side MOSFET turns off. When the high-side MOSFET turns off, the inductor current discharges through the low-side MOSFET till the next clock cycle begins.

The integrated error amplifier and the internal compensation builds up the feedback loop to regulates the output voltage to the reference. The error amplifier comparing the voltage of the FB pin with an internal reference voltage of 0.61V. The load current increasement reduces the feedback voltage which is relative to a voltage raise of the error amplifier output till the average inductor current matches the increased load current.

The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

10.3 Pulse Skipping Mode (PSM)

The GBI1412 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. A decrease of the load current leads an increasement in the feedback voltage which yields down the compensation voltage. When the compensation voltage drops to a low clamp threshold, the PSM is

triggered. During the skipping period, the discharge of output capacitor leads the output voltage drop which makes the FB voltage decay. Once the FB voltage drops lower than the reference voltage and the compensation voltage rises above the low clamp threshold, the integrated high-side MOSFET turns on in next clock pulse. After several switching cycles with typical 0.3A peak inductor current, the internal compensation voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This PSM helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. Regarding to improve efficiency further, the quiescent current is 80uA during skipping period with no switching.

10.4 VIN Power

The GBI1412 is designed to operate from an input voltage supply range between 4.6V to 40V, at least 0.1uF and 10uF decoupling ceramic cap are recommended to bypass the supply noise.

10.5 Under Voltage Lockout Threshold and Enable

The EN pin of GBI1412 is a high voltage pin which can be connected to VIN directly to start-up the device. The GBI1412 is enabled when the EN pin voltage higher than the enable threshold of 1.25V and disabled when the EN pin voltage lower than 1.1V. Grace to the internal 1.0uA pull-up current, the device is default enabled when the EN pin floats.

The Under Voltage Lock Out (UVLO) default startup threshold is typical 4.3V with VIN rising and shutdown threshold is 3.85V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin. Connect an external resistor divider (RL and RH) shown in Figure 8 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$\mathrm{RH} = \frac{V_{rise} - 1.14 * V_{fall}}{1.14 * 4.5uA - 1.5uA} \quad (1)$$

$$\mathrm{RL} = \frac{1.25\mathrm{V}}{\frac{V_{rise} - 1.25V}{R_H} + 1.5uA} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

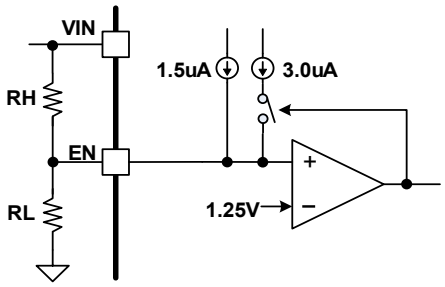


Figure 8. System UVLO by EN divider

10.6 Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off.

The floating supply (BOOT to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs.

10.7 Output Voltage

The GBI1412 regulates the internal reference voltage at 0.61V.

The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the value is higher, the regulator will be more noise sensitive. RFB_BOT in the range of 10kΩ to 100kΩ is recommended for most application.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{0.61V} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

10.8 Overcurrent and Short Circuit Protection

The GBI1412 adopts the peak current mode control. In the overcurrent momentum, the output voltage is yield down by heavy load and the error amplifier drives the compensation voltage high to increase the switching current. As the error amplifier output increases, it will be clamped internally, and the high-side current is clamped by a maximum peak current threshold. The peak current threshold is constant over the full duty cycle range.

When the output overcurrent or short circuit occurs, the device will trigger a cycle-by-cycle peak current clamping and frequency foldback by skipping pulse. This will lead more time for the inductor current to ramp down. Furthermore, a lower switching frequency contributes on lower switching loss, avoids overheating and other potential damages.

10.9 Overvoltage Protection

The GBI1412 implements the overvoltage protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. When the FB pin voltage reaches the rising OVP threshold which is typically 109% of V_{REF}, the high-side MOSFET will be turned off immediately which make the device under OVP. When the FB pin voltage drops below the falling OVP threshold, the high-side MOSFET is turned on and resumed normal operation. The falling OVP threshold is typically 105% of V_{REF}.

10.10 Thermal Shutdown

The GBI1412 features an internal thermal shutdown circuit to protect the device from the damage during excessive heat and power dissipation conditions. The thermal shutdown circuit will be asserted when the junction temperature exceeds typically 170^{0}C. When the junction temperature falls below 140^{0}C, the device restarts with internal soft start phase.

11 APPLICATION INFORMATION

Typical Application

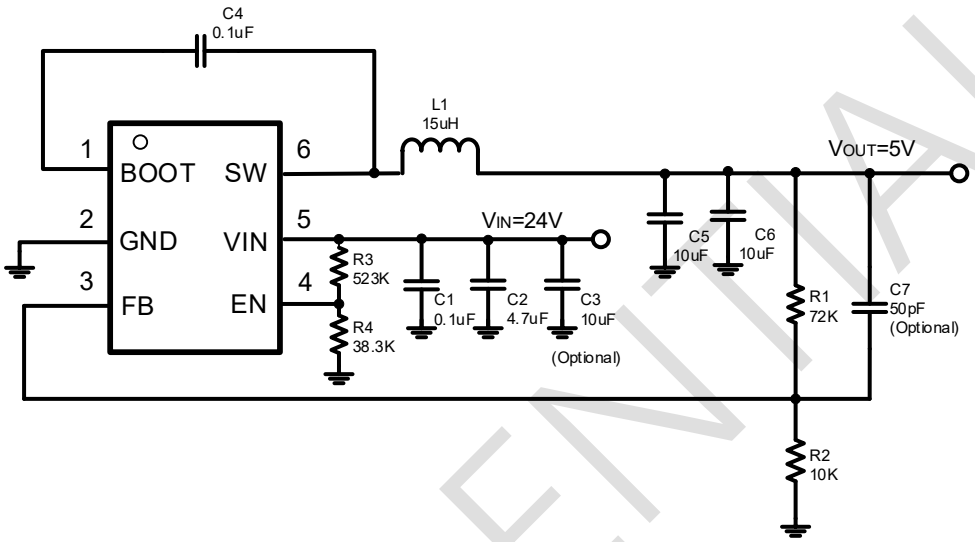


Figure 9. 24V Input, 5V/1A Output

Table 1. Design Parameters

Design Parameters	Example Value
Input Voltage	24V typical, 6~36V
Output Voltage	5V
Output Current	1A
Output voltage ripple (peak to peak)	<50mV
Overshoot/Undershoot range (0.1~0.9A)	<5%
Switching Frequency	1MHz

11.1 Set Output Voltage

The GBI1412 output voltage can be easily set up using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 9. Use Equation (4) to calculate the resistor divider values.

$$R1 = \frac{(V_{OUT} - 0.61) \times R2}{0.61} \quad (4)$$

In this design example the Vout is 5V. Set the resistor R2 value to be approximately 10k.

$$R1 = \frac{(V_{OUT} - 0.61) \times R2}{0.61} = \frac{(5 - 0.61) \times 10k\Omega}{0.61} = 72\ k\Omega$$

Slightly increasing or decreasing R1 to a closest available resistance, the 72kΩ is selected.

11.2 Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A X7R ceramic capacitor 4.7uF to 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin. These capacitors must be rated for 50V.

For this design, one 4.7uF X7R capacitors and one 0.1uF capacitor rated 50V is recommended.

The input voltage ripple can be calculated by using Equation (5) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{1A}{4.7uF \times 1000k} \times \frac{5V}{24V} \times \left(1 - \frac{5V}{24V}\right) = 35mV \quad (5)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

11.3 Inductor Selection

The performance of inductor affects the power supply' s steady state operation, transient behavior, loop stability, and buck converter efficiency. The critical parameters of inductor is the inductance, the DC resistance (DCR), the saturation current and the RMS current.

Use following equation to the minimum inductance:

$$L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (6)$$

Where

- V_{OUT} is output voltage
- K_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.3 is recommended here
- V_{INMAX} is the maximum input voltage

- f_{SW} is the converter switching frequency
- I_{OUT} is the output current

In this design example:

$$L > L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} = \frac{5V \times (40V - 5V)}{40V \times 0.3 \times 1A \times 1MHz} = 14.6\,uH$$

15uH is selected in the design example. Generally, the Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

11.4 Output Capacitor

The output capacitor must be chosen carefully with the reason that this capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. Generally, choose a low-ESR output capacitor like a ceramic capacitor from X5R or X7R family to get small output voltage ripple.

From the required output voltage ripple (<5mV), use the Equation 7 to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} > \frac{\Delta I_{LPP}}{8 \times V_{OUT\_Ripple} \times f_{SW}} = \frac{K_{IND} \times I_{OUT}}{8 \times V_{OUT\_Ripple} \times f_{SW}} \quad (7)$$

The allowed maximum ESR of the output capacitor is calculated by the equation 8.

$$R_{ESR} < \frac{V_{OUT\_Ripple}}{k_{IND} \times I_{OUT}} \quad (8)$$

Where

- V_{OUT_Ripple} is output voltage ripple caused by charging and discharging of the output capacitor.
- k_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.3 is recommended here
- I_{OUT} is the maximum output current
- f_{SW} is the converter switching frequency.

In this design, V_{OUT_Ripple} is smaller than 5mV, f_{SW} is 1000kHz, I_{OUT} is 1A and K_{IND} is 0.3:

$$C_{OUT} > \frac{0.3 \times 1A}{8 \times 5mV \times 1000k} = 7.5\,uF$$

$$R_{ESR} < \frac{5mV}{0.3 \times 1A} = 16.7m\Omega$$

Therefore, two X7R capacitors of 10uF with 25V DC rating and 3.9mΩ ESR are selected.

11.5 Bootstrap Capacitor

For proper operation of the device, a 0.1uF ceramic capacitor of X5R or X7R must be placed between the SW pin to the BOOT pin. The DC rating of this capacitor is must be 10V or higher voltage level.

11.6 Typical BOM Recommendation

Table 2 lists the recommended BOM for typical applications. Considering the capacitor’s degrading under DC bias, it is recommended to leave enough margin on the voltage rating to ensure adequate effective capacitance. If for achieving better load transient performance, larger values of output capacitors are recommended. For more help need, please contact the Gosemicon supporter.

Table 2. Typical BOM Recommendation

V_{OUT}	L	C_{OUT}	R_1	R_2	C_1
3.3V	10uH	2x10uF	45k	10k	0.1uF
5V	15uH	2x10uF	72k	10k	0.1uF
12V	22uH	2x10uF(≥25V)	187k	10k	0.1uF

11.7 Application Curves

Figure 10 through Figure 25 apply to the circuit of Figure 9. V_{IN} = 24 V, T_A = 25°C unless otherwise specified

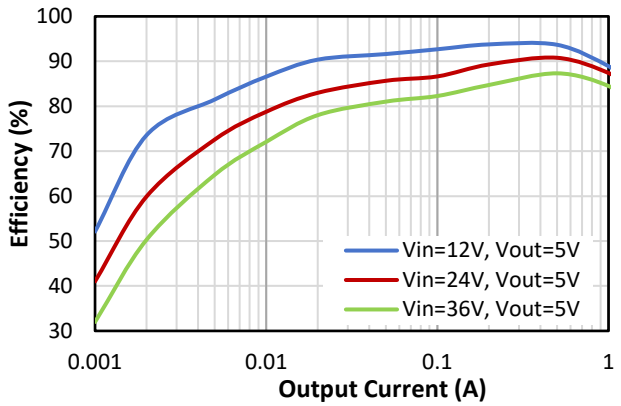


Figure 10. Power Efficiency

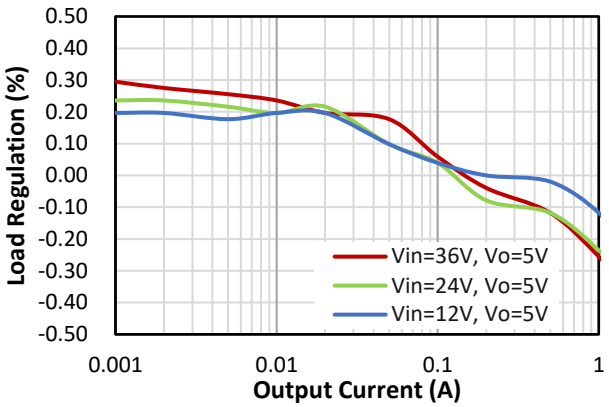


Figure 11. V_{OUT} Vs. Load Regulation

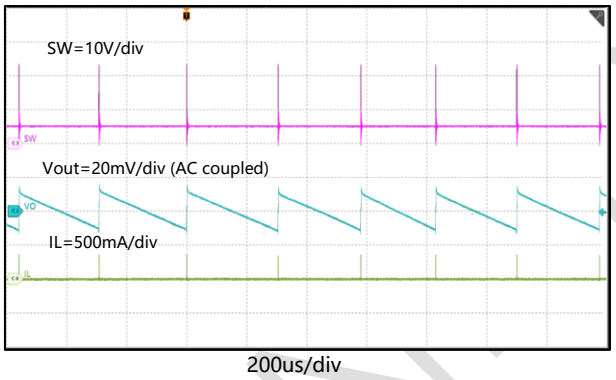


Figure 12. Output Voltage Ripple, I_{OUT}=1mA

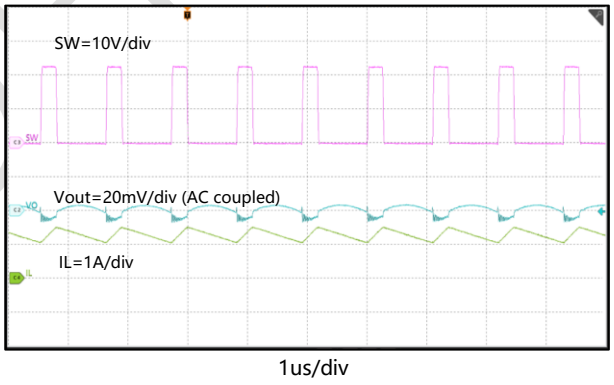


Figure 13. Output Voltage Ripple, I_{OUT}=1A

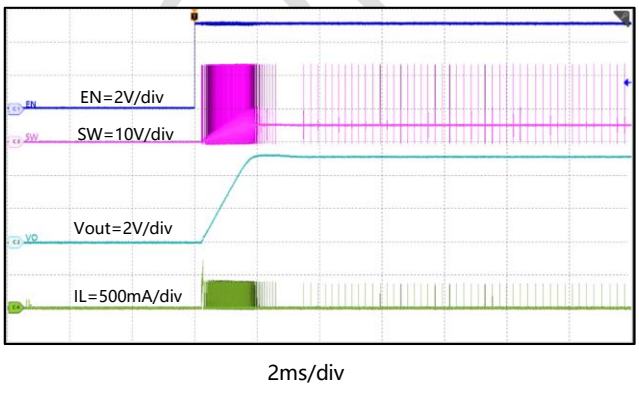


Figure 14. Start-Up with EN, I_{OUT}=1mA

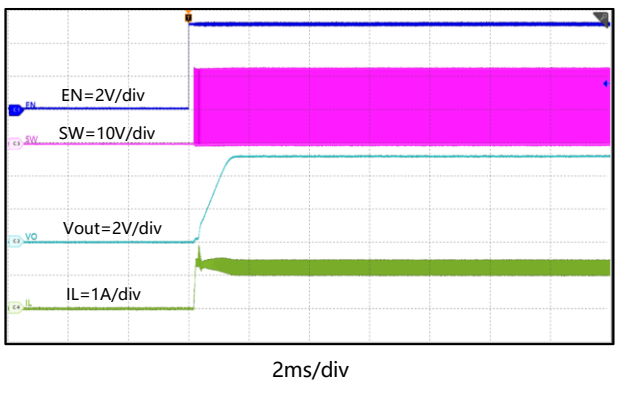
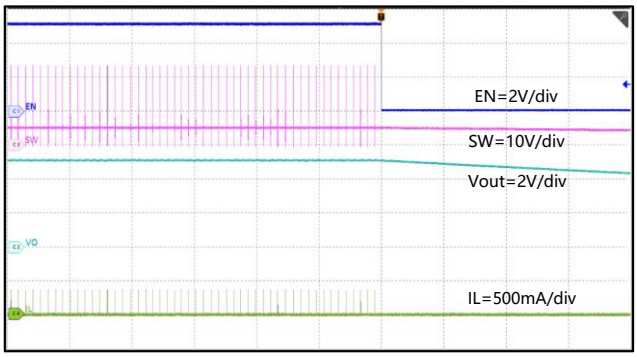
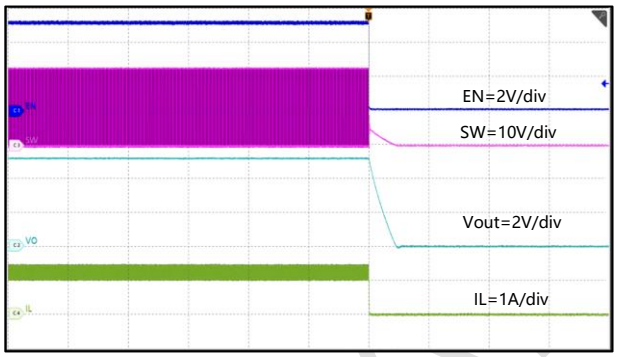


Figure 15. Start-Up with EN, I_{OUT}=1A



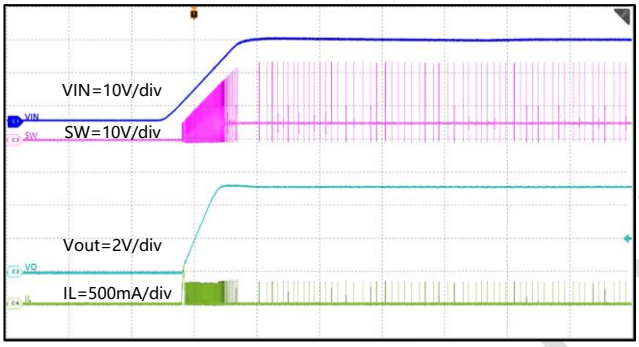
2ms/div

Figure 16. Shut-down with EN, I_{OUT}=1mA



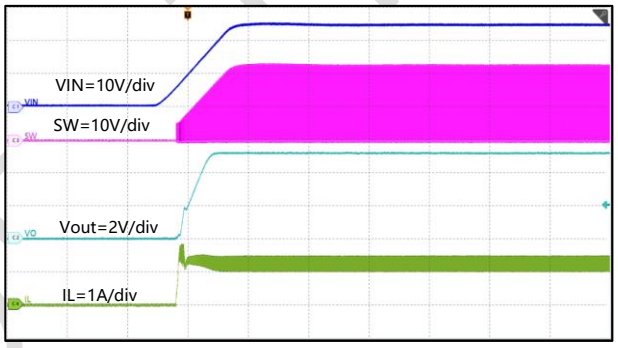
200us/div

Figure 17. Shut-down with EN, I_{OUT}=1A



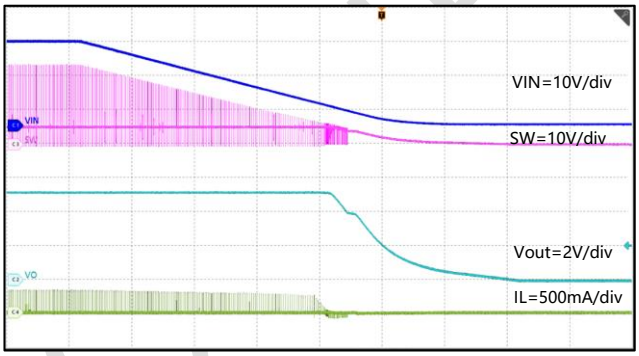
2ms/div

Figure 18. Start-Up with VIN rising, I_{OUT}=1mA



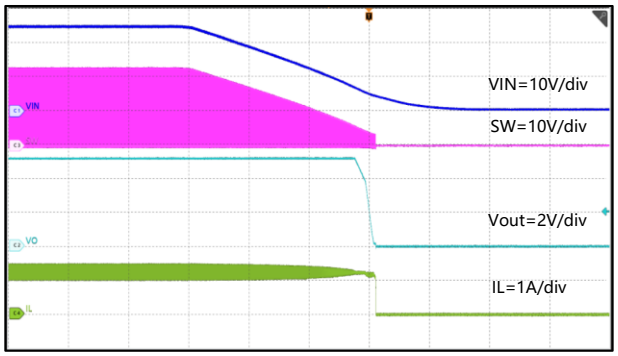
2ms/div

Figure 19. Start-Up with VIN Rising, I_{OUT}=1A



10ms/div

Figure 20. Shut-Down with VIN falling, I_{OUT}=1mA



10ms/div

Figure 21. Shut-Down with VIN falling, I_{OUT}=1A

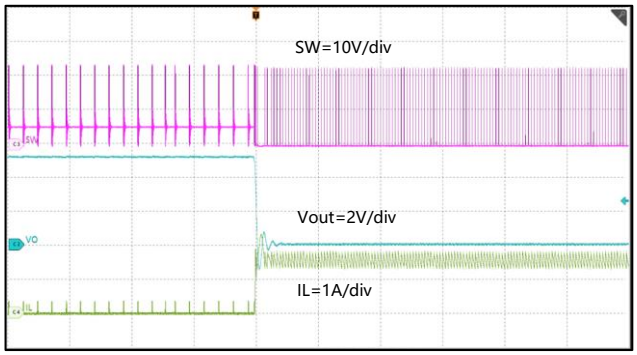


Figure 22. 1A Operation to HardShort, I_{OUT}=0A

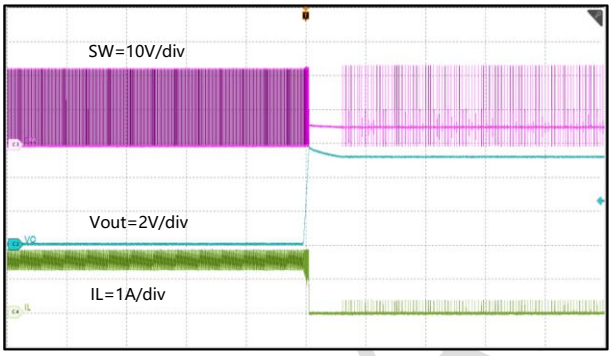


Figure 23. HardShort Recovery, I_{OUT}=0A

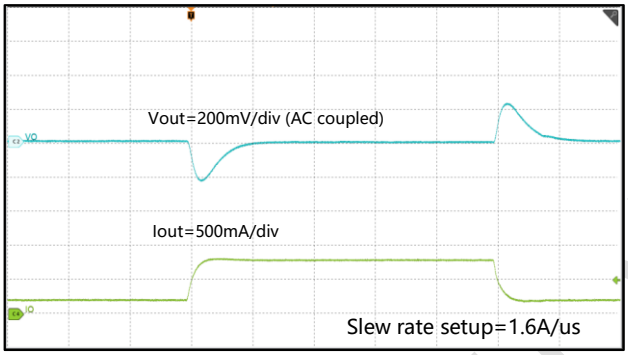


Figure 24. Transient Response 0.2A-0.8A

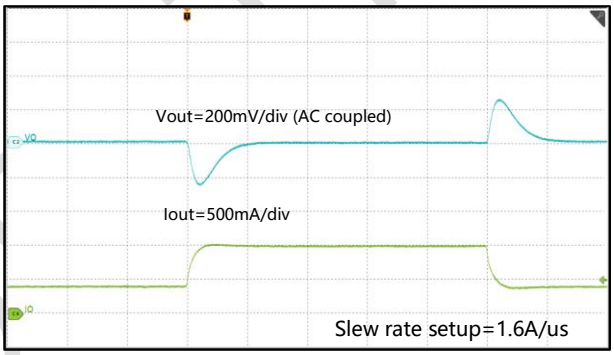


Figure 25. Transient Response 0.4A-1A

12 Layout Guideline and Layout Example

Layout is critical for proper operation. Please follow the layout guidelines.

1. The power ground is very critical. The power trace should take lowest impedance as possible and the ground area should be sufficient to optimize thermal, 8mil max thermal via recommended.
2. Place the bypass input capacitor with low ESR as close as possible to the VIN pin and GND. The bypassing loop from VIN terminal to the GND should be as short as possible.
3. The inductor should be located as close as possible to the SW pin for reducing magnetic and electrostatic noise.
4. The feedback resistor divider should be placed close to the FB pin.
5. The ground connected to the input capacitors and output capacitors should be tied to the system ground plane in only one spot to minimize conducted noise to the system ground plane.

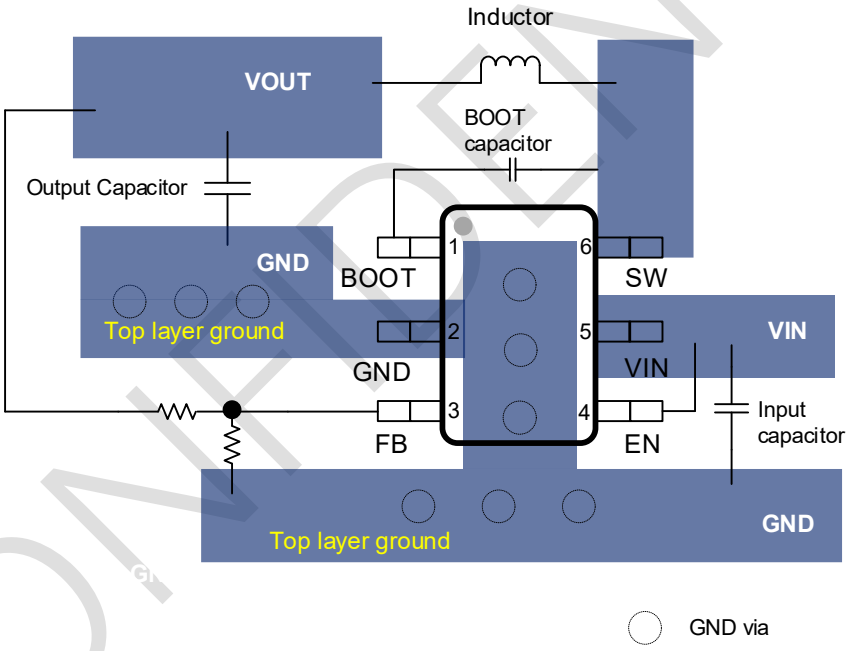
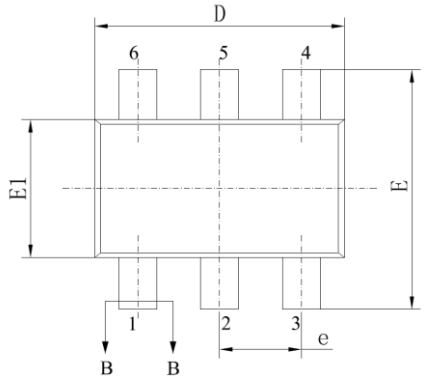
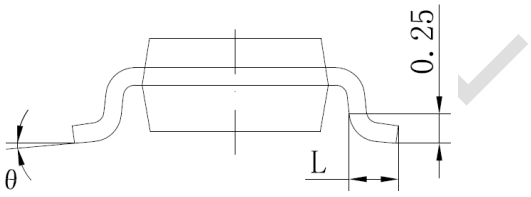
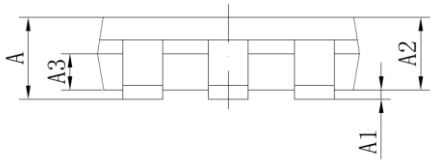


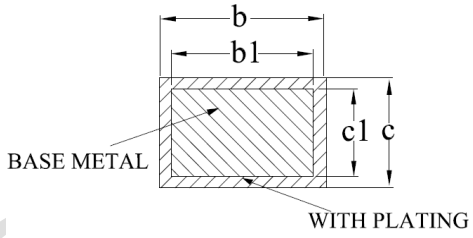
Figure 26. Layout Example

PACKAGE INFORMATION









SECTION B-B

Symbol	Millimeter		
	Min	Nor	Max
A	-	-	0.95
A1	0	-	0.10
A2	0.75	0.80	0.85
A3	0.35	0.40	0.45
b	0.38	-	0.46
b1	0.37	0.40	0.43
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
L	0.30	0.40	0.50
θ	0	-	8°