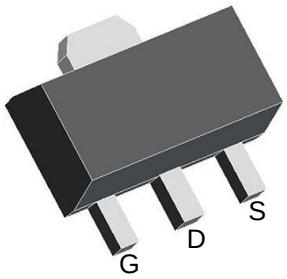
Description：

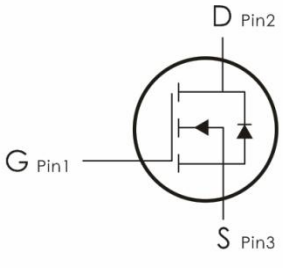
This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.



Features：

1) V_{DS}=60V,I_D=15A,$R_{DS(ON)}$<30m Ω @V_{GS}=10V（Typ：21m Ω）
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra low $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.
6) MSL3



Package Marking and Ordering Information：

Part NO.	Marking	Package	Packing
DOW15N06	15N06	SOT-89	1000 pcs/Reel

Absolute Maximum Ratings： (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1]	15	A
	Continuous Drain Current-T_C=100℃[1]	10.5	
I_{DM}	Pulsed Drain Current[2]	60	
E_{AS}	Single pulse avalanche energy[3]	30	mJ
P_D	Power Dissipation	18	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\Theta JC}$	Thermal Resistance,Junction to Case	7	℃/W

Electrical Characteristics: (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=60V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1.2	1.5	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=10V,I_D=10A	---	21	30	mΩ
		V_{GS}=4.5V,I_D=5A	---	28	40	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz	---	1030	---	pF
C_{oss}	Output Capacitance		---	63	--	
C_{rss}	Reverse Transfer Capacitance		---	52	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=40V, I_D=20A, R_{ENG}=3Ω ,V_{GS}=10V	---	8.4	---	ns
t_r	Rise Time		---	4.2	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	22	---	ns
t_f	Fall Time		---	4.2	---	ns
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=40V, I_D=20A	---	22	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	6.3	---	nC
Drain-Source Diode Characteristics						
I_S	Continuous Drain Current	V_D=V_G=0V	---	---	13.6	A
I_{SM}	Pulsed Drain Current		---	---	54.5	A
Trr	Reverse Recovery Time	I_F=20A,T_J=25℃ dI/dt=100A/us	---	13	---	ns
Qrr	Reverse Recovery Charge		---	0.01	---	nC
V_{SD}	Diode Forward Voltage[3]	V_{GS}=0V, I_{SD}=30A	---	---	1.1	V

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : TJ=25℃,VDD=30V,V_G=10V,L=0.5mH
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics： (T_C=25℃ unless otherwise noted)

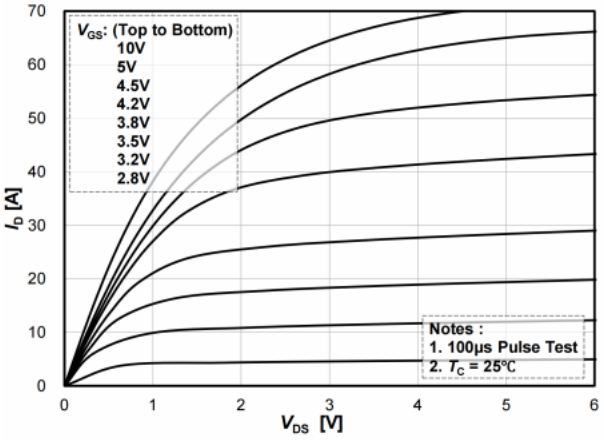


Figure 1. **On-Region Characteristics**

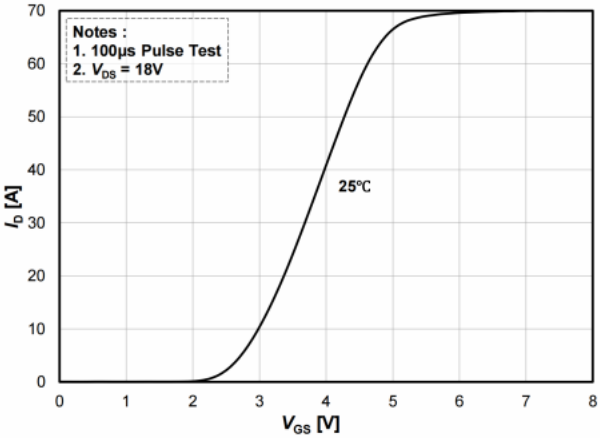


Figure 2. **Transfer Characteristics**

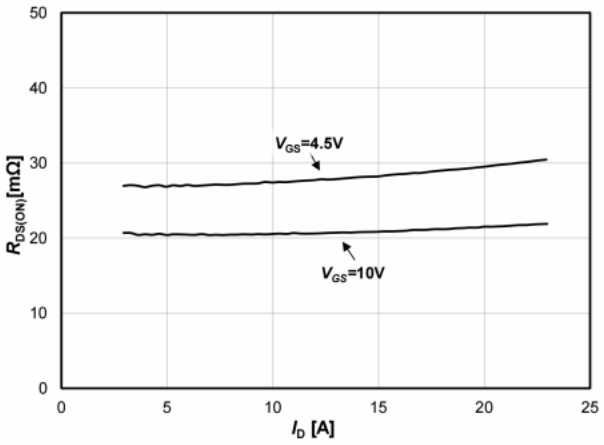


Figure 3. **On Resistance vs. Drain Current**

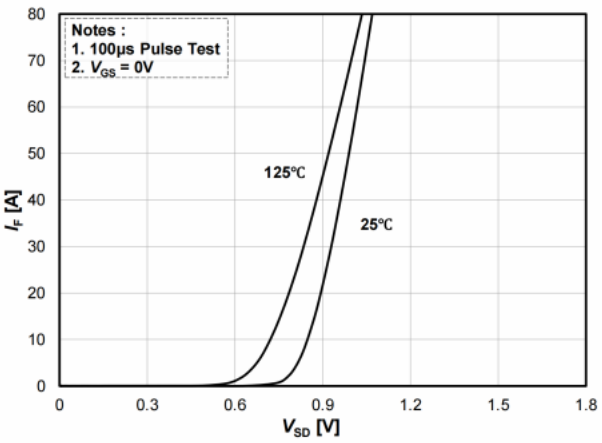


Figure 4. **Diode Forward Voltage vs. Current**

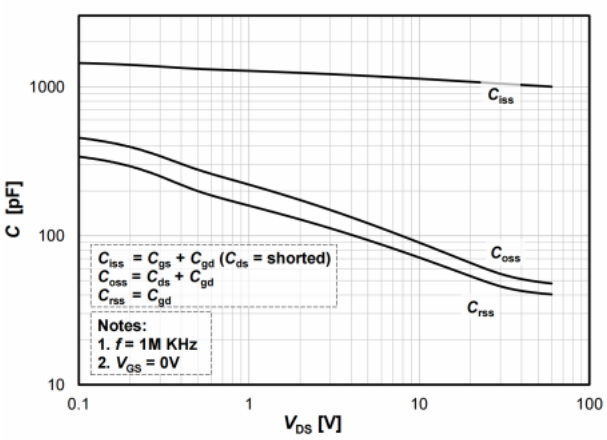


Figure 5. **Capacitance Characteristics**

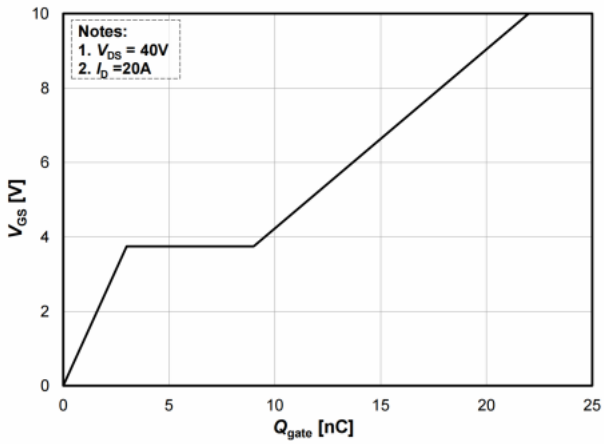


Figure 6. **Gate Charge Characteristics**

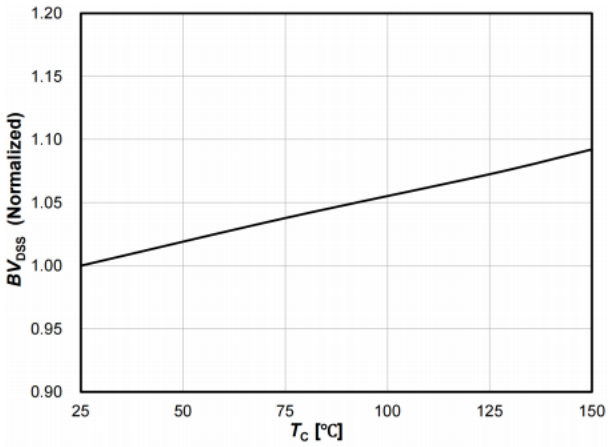


Figure 7. **Normalized BV_{DSS} vs. Temperature**

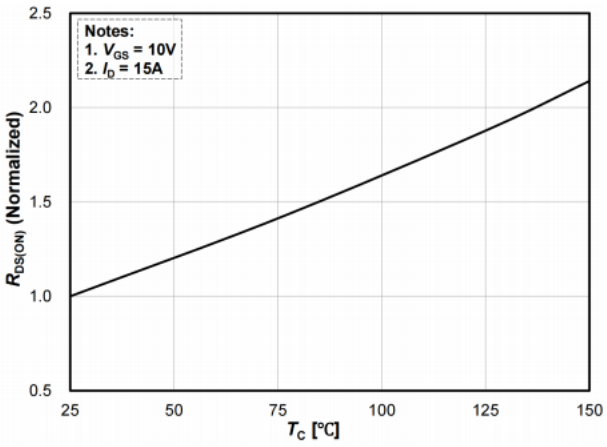


Figure 8. **Normalized On-Resistance Variation vs. Temperature**

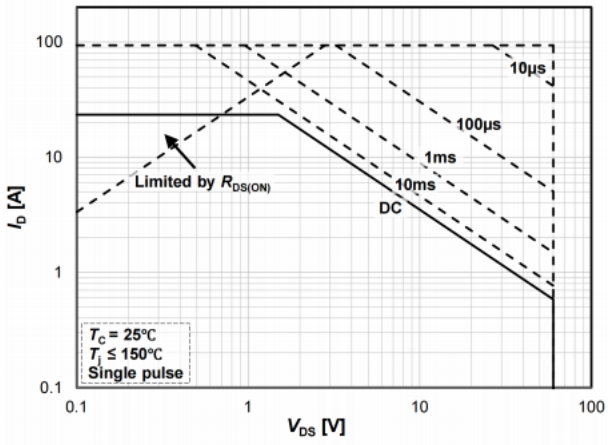


Figure 9. **Safe Operating Area** [3)]

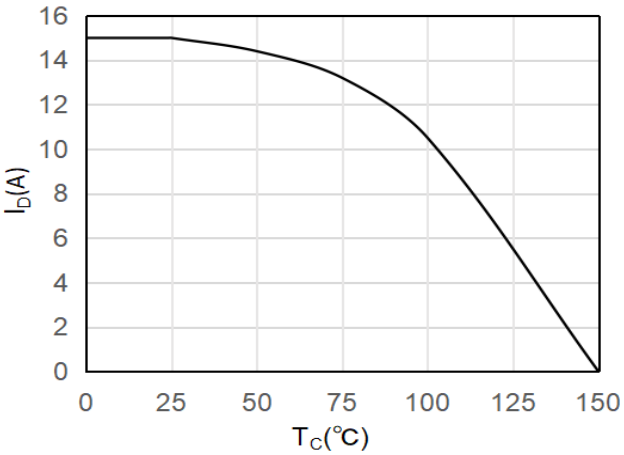


Figure 10. **Drain Current vs. Temperature**

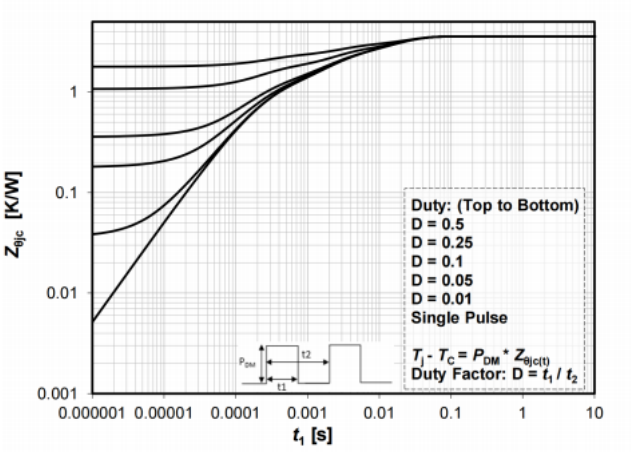
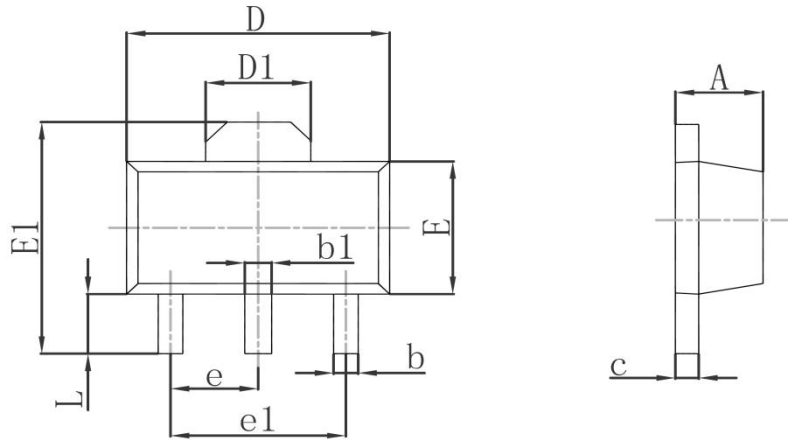


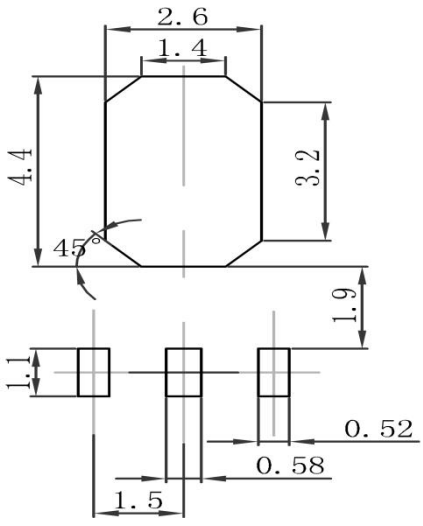
Figure 11. **Transient Thermal Impedance**

SOT-89 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550REF		0.061REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	3.000TYP		0.118TYP	
L	0.900	1.200	0.035	0.047

SOT-89 Suggested Pad Layout



Note:

1.Controlling dimension: in millimeters

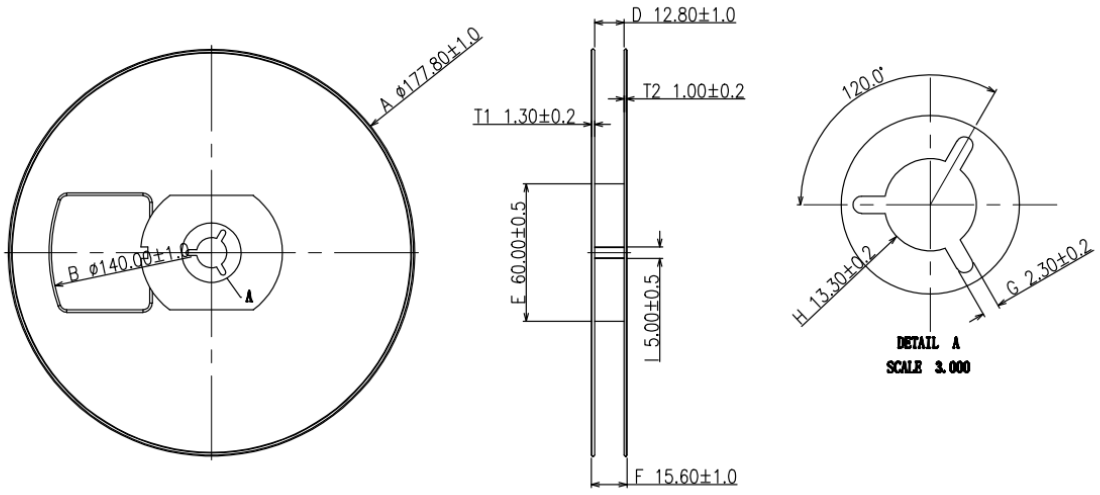
2.General tolerance: ±0.05mm

3.The pad layout is for reference purposes only

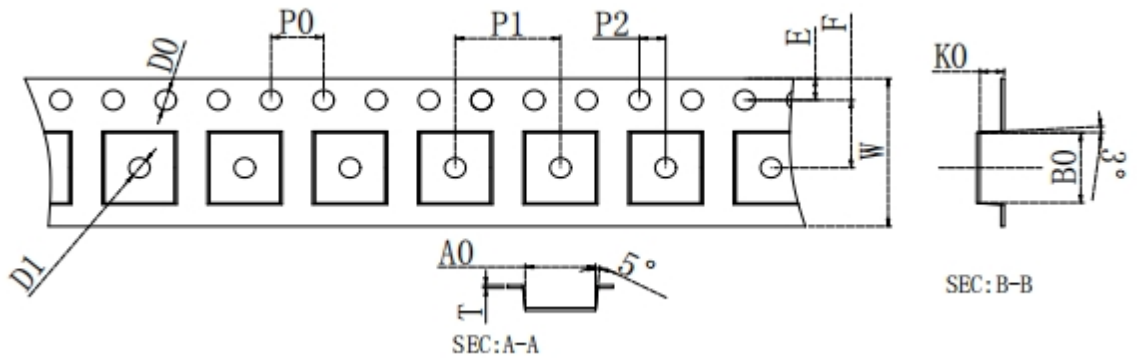
UNIT: mm

Tape & Reel Information

Dimensions in mm



W	12.00±0.10	T	0.22±0.02	D1	1.60±0.10	MM
E	1.75±0.10	F	5.50±0.10	D0	1.60±0.10	PC+PS
P0	4.00±0.10	P1	8.00±0.10	P2	2.00±0.10	SOT89
A0	4.90±0.10	B0	4.50±0.10	K0	1.75±0.10	



Pulling direction

Marking Information：

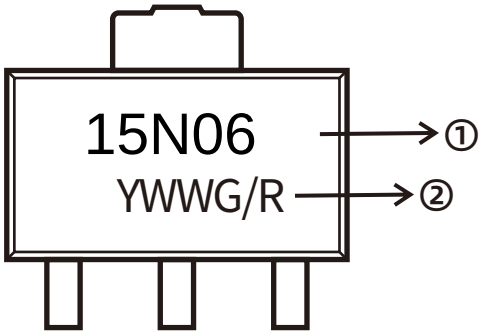
①. Part NO.

②. Date Code(YWWG / R)

Y：Year Code，last digit of the year

WW：Week Code(01-53)

G/R：G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2026-04-29	Release of final version

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