



LPDDR5X Datasheet

RS512M16LP5D1FZB-23BT
245-ball

Revision 1.3

Dec. 5. 2025

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Revision History

Version	Date	Changes
V1.0	2025-7-30	Basic spec and architecture
V1.1	2025-8-19	1) Change product family 2) Change refresh requirement parameters
V1.2	2025-9-10	Revise discrete package dimension
V1.3	2025-12-5	1) Revise product family 2) Revise data rate

Notes This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.

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1. Product Overview

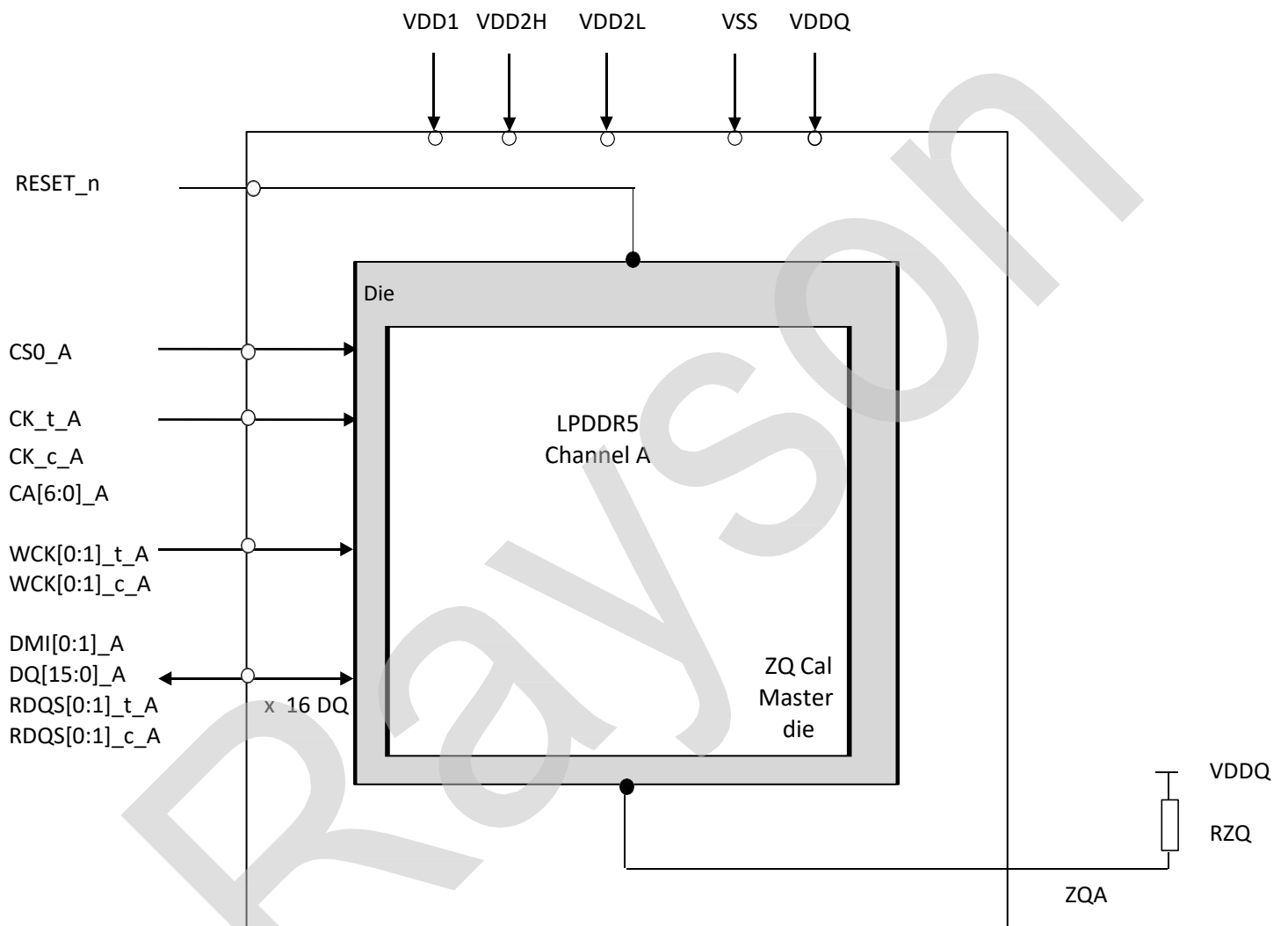
1.1. Feature Overview

- Architecture
 - 17.1 GB/s maximum bandwidth per channel
 - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mbp/s with WCK:CK = 4:1)
 - Selectable CKR (WCK:CK = 2:1 or 4:1)
- LPDDR5X data interface
 - Single x16 channel/die
 - Double-data-rate command/address entry
 - Differential command clocks (CK_t/CK_c) for high-speed operation
 - Differential data clocks (WCK_t/WCK_c)
 - Optional differential read strobe (RDQS_t/ RDQS_c)
 - 16n-bit or 32n-bit prefetch architecture
 - 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
 - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
 - Background ZQ calibration/command-based ZQ calibration
 - Optional link protection (link ECC)
 - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- Ultra-low-voltage core and I/O power supplies
 - V_{DD1} = 1.70–1.95V; 1.8V TYP
 - V_{DD2H} = 1.01–1.12V; 1.05V TYP
 - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.9V TYP
 - V_{DDQ} = 0.5V or 0.45V^L TYP or 0.3V TYP (ODT off only)
- I/O characteristics
 - Interface-LVSTL 0.5/0.3
 - I/O type: Low-swing single-ended, V_{SS} terminated
 - V_{OH}-compensated output drive

- Programmable V_{SS} on-die termination (ODT)
- Non target ODT support
- DVFSQ support
- Low power features
 - Enhanced DVFSQ: Enhanced dynamic voltage frequency scaling core
 - Single-ended CK, single-ended WCK, and single-ended RDQS
 - Data copy
 - Write X
 - $V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}$ (ODT off only): 1.8V/1.05V/ V_{I2H} or 0.9V/0.5V or 0.45V^L/0.3V
- Array configuration
 - 512 Meg x 16 (1 channels x 16 I/O)
- Device configuration
 - 512M16 x 1 die in package
- FBGA “green” package
 - 245-ball FBGA (8.2mm x 12.4mm Seated height: 1.0mm MAX)
- Speed grade, cycle time (t_{WCK})
 - 8533Mb/s
- Operating temperature range
 - -25°C to + 85°C

2. Physical Specifications

2.1. Function Block Diagram



Single-Die, Single-Channel Package, Single-Rank Block Diagram

2.2. Package ballout & Addressing

245-Ball single-Channel Single-Rank Discrete VFBGA

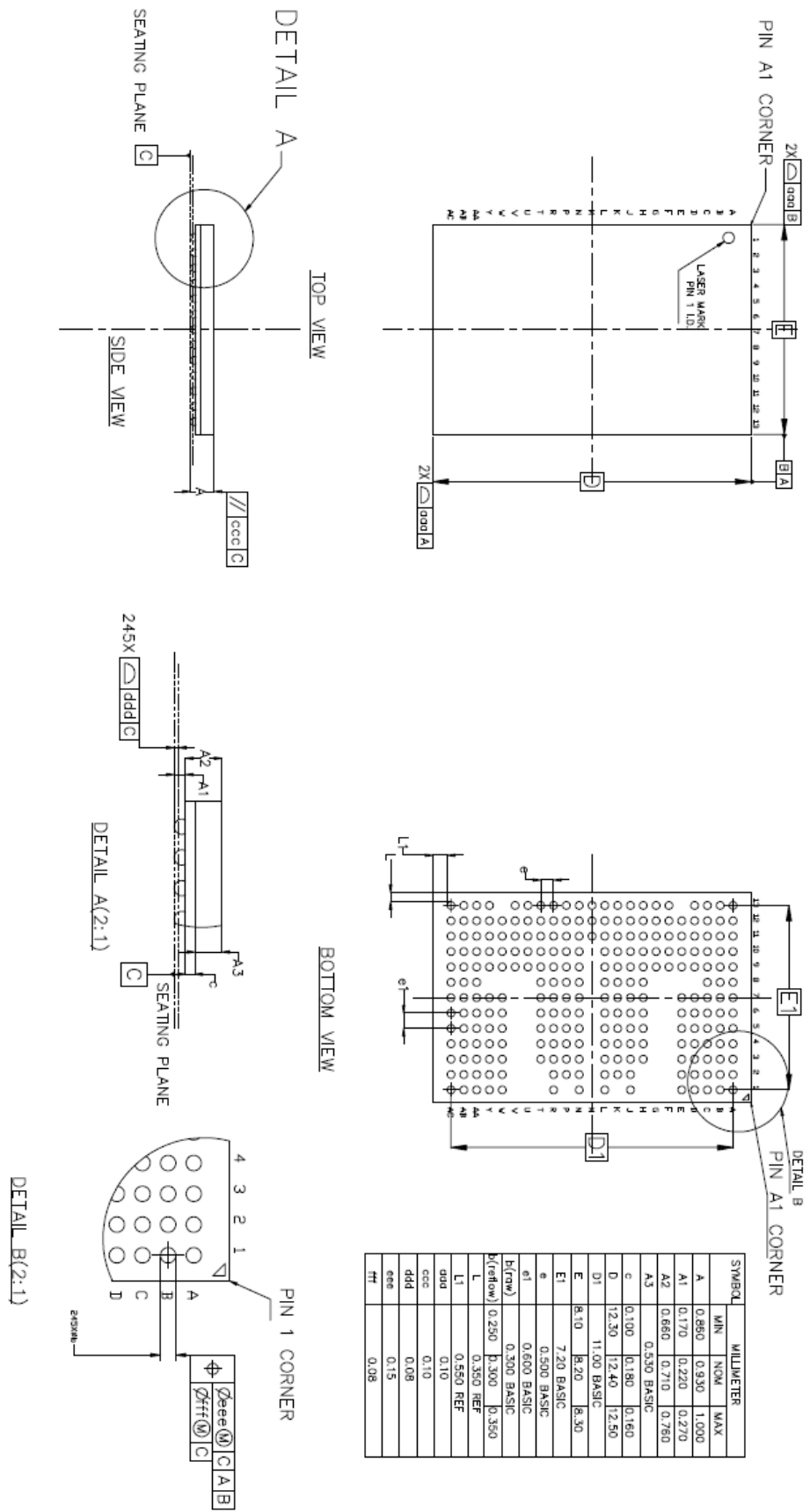
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	VDD1	VDD2L	VDD2H	VSS	VSS	VDD2H	VSS	VDD2H	VSS	NC	NC
B	NC	DQ8_A	VSS	DQ15_A	VSS	RDQS1_C_A	RDQS1_T_A	VSS	CA2_A	CA1_A	VDD2H	VSS	NC
C	DQ10_A	VSS	DQ9_A	VDDQ	DMI1_A	VDDQ	VSS	VSS	VDD2H	VSS	CA6_A	CA4_A	VDD1
D	VSS	DQ12_A	VSS	VDDQ	VSS	WCK1_C_A	WCK1_T_A		CA0_A	CA5_A	VDD2H	VSS	VDD2L
E	DQ13_A	VSS	DQ14_A	VDDQ	DQ11_A	VSS	VDD2L		VDD2H	VSS	CA3_A	VSS	
F									VSS	RFU	VSS	CK_C_A	VSS
G									NC	CS0_A	VSS	CK_T_A	VSS
H			DQ6_A	VSS	DQ5_A	VSS	DQ7_A	VSS	VDDQ	VDDQ	VSS	VSS	VSS
J	VSS	DQ0_A	VSS	DMI0_A	VSS	VDDQ	VDDQ	WCK0_C_A	WCK0_T_A	VSS	VDD2H	VDD2H	ZQ_A
K		VDD2H	VDD2H	VSS	DQ4_A	VSS	DQ3_A	VSS	RDQS0_C_A	RDQS0_T_A	VDDQ	VSS	VDD2L
L	VSS	VSS	VSS	DQ1_A	VSS	DQ2_A	VSS	VDDQ	VSS	VSS	VDD2H	VDD2H	VDD1
M											VSS	VSS	VSS
N	VSS	VSS	VSS	NC	VSS	NC	VSS	VDDQ	VSS	VSS	VDD2H	VDD2H	VDD1
P		VDD2H	VDD2H	VSS	NC	VSS	NC	VSS	NC	NC	VDDQ	VSS	VDD2L
R	VSS	NC	VSS	NC	VSS	VDDQ	VDDQ	NC	NC	VSS	VDD2H	VDD2H	RESET
T			NC	VSS	NC	VSS	NC	VSS	VDDQ	VDDQ	VSS	VSS	VSS
U									NC	NC	VSS	NC	VSS
V									VSS	RFU	VSS	NC	VSS
W	NC	VSS	NC	VDDQ	NC	VSS	VDD2L		VDD2H	VSS	NC	VSS	
Y	VSS	NC	VSS	VDDQ	VSS	NC	NC		NC	NC	VDD2H	VSS	VDD2L
AA	NC	VSS	NC	VDDQ	NC	VDDQ	VSS	VSS	VDD2H	VSS	NC	NC	VDD1
AB	NC	NC	VSS	NC	VSS	NC	NC	VSS	NC	NC	VDD2H	VSS	NC
AC	NC	NC	VDD1	VDD2L	VDD2H	VSS	VSS	VDD2H	VSS	VDD2H	VSS	NC	NC

2.3. Pad Definition

Symbol	Type	Description
CK_t_A CK_c_A	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_A	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] be- come NC pins in a single-rank package.
CA[6:0]_A	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_A WCK[1:0]_c_A	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_A	I/O	Data input/output: Bidirectional databus.
RDQS[1:0]_t_A RDQS[1:0]_c_A	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_A	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2H, VDD2L	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets all channels of the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.
RFU	–	Reserved Future: Not internally connected.

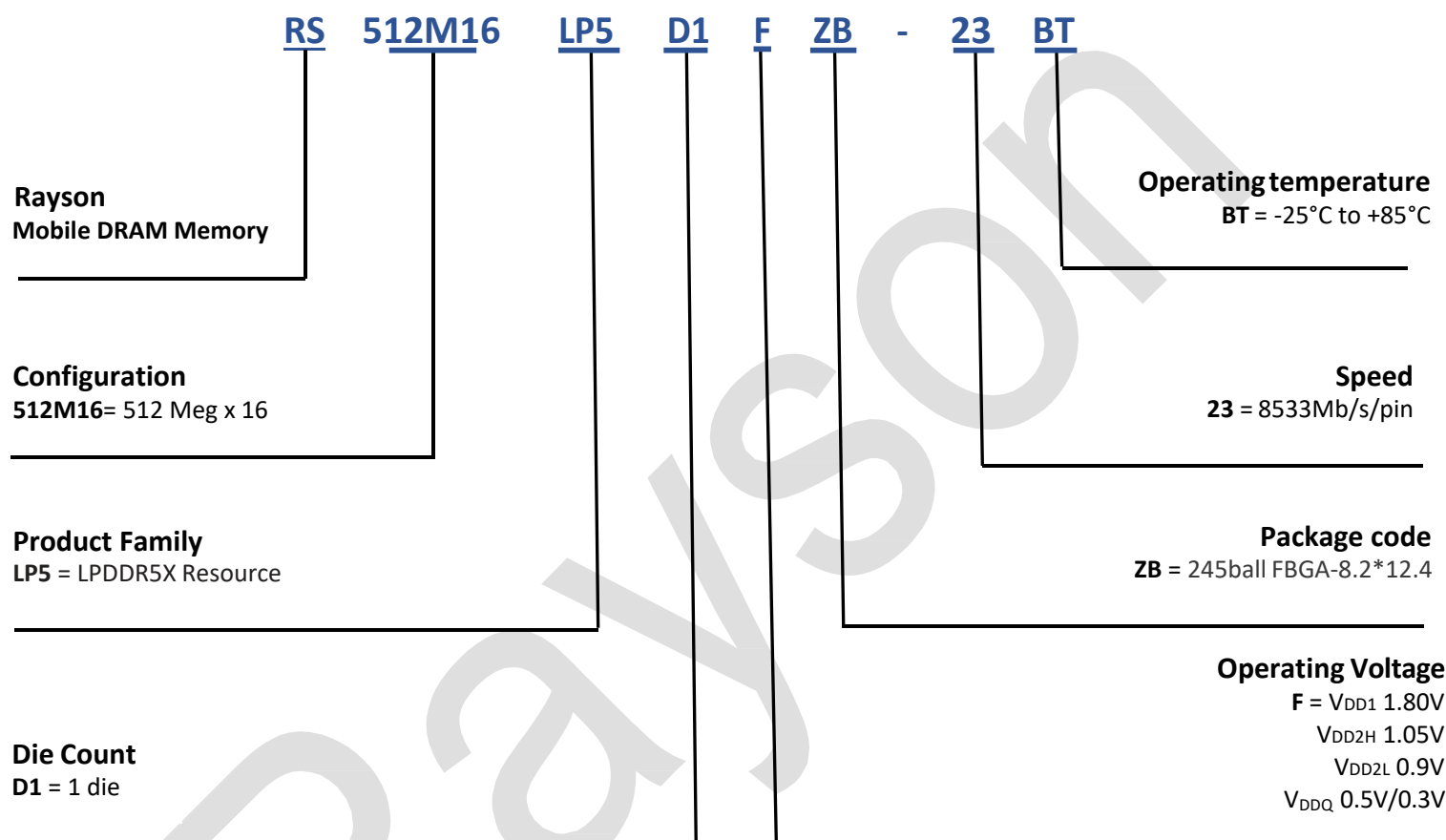
2.4. Discrete Package Dimension

8.2mm X12.4mm



3. Core Specifications

3.1. Part Number Decoding



3.2. Ordering Options

Table 1: Part Number List

Part Number	Total Density	Data Rate	Operating temperature
RS512M16LP5D1FZB-23BT	1GB(8Gb)	8533 Mb/s/pin	-25°C to + 85°C

Table 2: Refresh Requirement Parameters

Parameter	Symbol	8Gb	unit
		BG and 16B Mode	
REFRESH cycle time (all banks)	t_{RFCab}	280	ns
REFRESH cycle time (per bank)	t_{RFCpb}	140	ns
Per bank refresh to per bank refresh time (different bank)	$t_{PBR2PBR}$	90	ns
Per bank refresh to ACTIVATE command time (different bank)	$t_{PBR2ACT}$	7.5	ns

3.3. Die Addressing Table

Configuration		512M16(8Gb/package)	
Die Configuration	Channel A, rank 0	× 16 mode × 1 die	
	Channel B, rank 0	-	
Die Addressing	Bits	8,589,934,592	
	Bank mode	BG mode	16B mode
	Configuration	32Mb × 16 DQ × 4 Banks × 4 BG	32Mb × 16 DQ × 16 Banks
	Number of banks	4	16
	Number of banks groups	4	1
	Array prefetch bits	256	
	Rows per bank	32,768	
	Columns	64	
	Page size (bytes)	2048	
	Native burst length	16	
	Number of I/Os	16	
	Bank address	BA[1:0]	BA[3:0]
	Bank group address	BG[1:0]	-
	Row address	R[14:0]	
	Column address	C[5:0]	
	Burst address	B[3:0]	
	Burst starting address boundar	128-bit	

3.4. Mode Register Contents

MR0		
OP7	Per-pin DFE	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS OP[1] = 0b: Device supports x16 mode OP[2] = 1b: Device supports enhanced WCK always-on mode. OP[3] = 1b: Device supports optimized refresh mode OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior OP[6] = 1b: Device supports Pre Emphasis mode OP[7] = 1b: Device does not support Per Pin DFE
OP6	Pre Emphasis	
OP5	Unified NT ODT behavior mode	
OP4	DMI output behavior mode	
OP3	Optimized refresh mode	
OP2	Enhanced WCK always-on mode	
OP1	Latency Mode	
OP0	NT ODT timing mode	

MR1		
OP7		OP[0] = 0b: Device does not support CS ODT behavior OP OP[1] = 1b: Device supports ARFM
OP6		
OP5		
OP4		
OP3		
OP2		
OP1	ARFM support	
OP0	CS ODT OP support	

MR3		
OP7		OP[4:3] = 00b: BG; 10b: 16B Mode Supported
OP6		
OP5		
OP4	BK/BG Org	
OP3		
OP2		
OP1		
OP0		

MR5		
OP7	Manufacturer ID	1111 1111b : Micron
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR6		
OP7	Revision ID1	1000 1000b
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR8		
OP7	I/O width	OP[7:6] = 00b: x16/channel
OP6		
OP5	Density	OP[5:2] = 0100b: 8Gb
OP4		
OP3		
OP2		
OP1		
OP0		

MR13		
OP7	OP[2]=0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6	
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR19		
OP7		OP[5] = 1b: WCK2DQ Osc FM supported
OP6		
OP5	WCK2DQ Osc FM support	
OP4		
OP3		
OP2		
OP1		
OP0		

MR21			MR22		
OP7	WXS	OP[0] = 1b: WRITE DATA COPY function supported OP[1] = 1b: READ DATA COPY function supported OP[2] = 1b: WRITE X function supported OP[3] = 1b: Device ODTD-CS is supported OP[7] = 1b: Data to be written can be selected with 0 and 1	OP7	RECC	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled
OP6			OP6		
OP5			OP5	WECC	
OP4			OP4		
OP3	ODTD-CSFS		OP3		
OP2	WXFS		OP2		
OP1	RDCFS		OP1		
OP0	WDCFS		OP0		

MR24			MR26		
OP7	DFES	OP[3] = 1b: Device supports Read DCA OP[7] = 1b: Devices supports DFE	OP7		OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported
OP6			OP6	RDQSTFS	
OP5			OP5		
OP4			OP4		
OP3	Read DCA		OP3		
OP2			OP2		
OP1			OP1		
OP0			OP0		

MR27		
OP7	RAAMULT	OP[0] = 1b: RFM is required OP[5:1] = 00101b: 40 OP[7:6]=01b: 4X
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0	RFM	

MR43		
OP7		OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted
OP6	SBEC Rule	
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		

MR57		
OP7	ARFM ³	OP[1:0] = 10b: 2 x RAAIMT OP[3:2] = 00b: 1=Does not support single-bank mode OP[5:4] = 00b: One RAA counter per two banks(1 of 8) OP[7:6] = 00b: default (00101b: 40), 01b:Level A, 10b: Level B, 11b: Level C
OP6		
OP5		
OP4		
OP3		
OP2		
OP1		
OP0		
	RFMSB	
	RAADEC	

- Notes:** 1、 *The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.*
- 2、 *Refer to General LPDDR5 Specifications 1 for mode registers not described here.*
- 3、 *Write link ECC and read link ECC are supported.*

4. IDD Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 1: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade	Unit	Note
		8533 Mb/s		
I_{DD01}	V_{DD1}	3.80	mA	2
I_{DD02H}	V_{DD2H}	53.00		
I_{DD02L}	V_{DD2L}	0.20		
I_{DD0Q}	V_{DDQ}	0.60		
I_{DD2P1}	V_{DD1}	1.50	mA	2
I_{DD2P2H}	V_{DD2H}	3.90		
I_{DD2P2L}	V_{DD2L}	0.20		
I_{DD2PQ}	V_{DDQ}	0.60		
I_{DD2PS1}	V_{DD1}	1.50	mA	2
$I_{DD2PS2H}$	V_{DD2H}	3.90		
$I_{DD2PS2L}$	V_{DD2L}	0.20		
I_{DD2PSQ}	V_{DDQ}	0.60		
I_{DD2N1}	V_{DD1}	1.50	mA	2
I_{DD2N2H}	V_{DD2H}	32.50		
I_{DD2N2L}	V_{DD2L}	0.20		
I_{DD2NQ}	V_{DDQ}	0.60		
I_{DD2NS1}	V_{DD1}	1.50	mA	2
$I_{DD2NS2H}$	V_{DD2H}	32.50		
$I_{DD2NS2L}$	V_{DD2L}	0.20		
I_{DD2NSQ}	V_{DDQ}	0.60		
I_{DD3P1}	V_{DD1}	2.50	mA	2
I_{DD3P2H}	V_{DD2H}	12.50		
I_{DD3P2L}	V_{DD2L}	0.20		
I_{DD3PQ}	V_{DDQ}	0.60		
I_{DD3PS1}	V_{DD1}	2.50	mA	2
$I_{DD3PS2H}$	V_{DD2H}	12.50		
$I_{DD3PS2L}$	V_{DD2L}	0.20		
I_{DD3PSQ}	V_{DDQ}	0.60		

Table 1: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade	Unit	Note
		8533 Mb/s		
I _{DD3N1}	V _{DD1}	2.80	mA	2
I _{DD3N2H}	V _{DD2H}	40.00		
I _{DD3N2L}	V _{DD2L}	0.20		
I _{DD3NQ}	V _{DDQ}	0.60		
I _{DD4R1}	V _{DD1}	20.50	mA	2, 3, 4
I _{DD4R2H}	V _{DD2H}	430.00		
I _{DD4R2L}	V _{DD2L}	0.20		
I _{DD4RQ}	V _{DDQ}	121.00		
I _{DD4RDVFSC1}	V _{DD1}	10.00	mA	3, 4, 6
I _{DD4RDVFSC2H}	V _{DD2H}	32.00		
I _{DD4RDVFSC2L}	V _{DD2L}	115.00		
I _{DD4RDVFSCQ}	V _{DDQ}	74.70		
I _{DD4W1}	V _{DD1}	18.50	mA	2, 3
I _{DD4W2H}	V _{DD2H}	280.00		
I _{DD4W2L}	V _{DD2L}	0.20		
I _{DD4WQ}	V _{DDQ}	0.60		
I _{DD4WDVFSC1}	V _{DD1}	9.00	mA	3, 6
I _{DD4WDVFSC2H}	V _{DD2H}	29.00		
I _{DD4WDVFSC2L}	V _{DD2L}	80.00		
I _{DD4WDVFSCQ}	V _{DDQ}	0.60		
I _{DD51}	V _{DD1}	24.00	mA	2
I _{DD52H}	V _{DD2H}	205.00		
I _{DD52L}	V _{DD2L}	0.20		
I _{DD5Q}	V _{DDQ}	0.60		
I _{DD5ED1}	V _{DD1}	21.00	mA	6
I _{DD5ED2H}	V _{DD2H}	160.00		
I _{DD5ED2L}	V _{DD2L}	26.50		
I _{DD5EDQ}	V _{DDQ}	0.60		
I _{DD5AB1}	V _{DD1}	3.60	mA	2
I _{DD5AB2H}	V _{DD2H}	47.00		
I _{DD5AB2L}	V _{DD2L}	0.20		
I _{DD5ABQ}	V _{DDQ}	0.60		

Table 1: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade	Unit	Note
		8533 Mb/s		
I _{DD5ABED1}	V _{DD1}	3.40	mA	6
I _{DD5ABED2H}	V _{DD2H}	24.00		
I _{DD5ABED2L}	V _{DD2L}	22.00		
I _{DD5ABEDQ}	V _{DDQ}	0.60		
I _{DD5PB1}	V _{DD1}	3.60	mA	2
I _{DD5PB2H}	V _{DD2H}	47.00		
I _{DD5PB2L}	V _{DD2L}	0.20		
I _{DD5PBQ}	V _{DDQ}	0.60		
I _{DD5PBED1}	V _{DD1}	3.40	mA	6
I _{DD5PBED2H}	V _{DD2H}	24.00		
I _{DD5PBED2L}	V _{DD2L}	22.00		
I _{DD5PBEDQ}	V _{DDQ}	0.60		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. Enhanced DVFS and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFS disabled)/0.27–0.37V (DVFSQ enabled); T_C = –25°C to +85°C
6. Enhanced DVFS enabled, DVFSQ enabled, 3200 Mb/s, 16B Mode
7. Notes 1 and 5 apply to entire table.

Table 2: Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
25°C	I _{DD61}	V _{DD1}	0.27	mA
	I _{DD62H}	V _{DD2H}	1.00	
	I _{DD62L}	V _{DD2L}	– (See Note 4)	
	I _{DD6Q}	V _{DDQ}	– (See Note 4)	
85°C	I _{DD61}	V _{DD1}	3.70	
	I _{DD62H}	V _{DD2H}	21.00	
	I _{DD62L}	V _{DD2L}	0.20	
	I _{DD6Q}	V _{DDQ}	0.60	

- Notes: 1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFS and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
4. V_{DD2L} and V_{DDQ} power rail are not used during power-down self refresh.