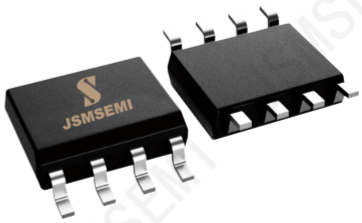
General description

The JSM82C251T is intended for use in applications employing the Controller Area Network(CAN)serial communication physical layer in accordance with the IS0 11898 Standard.The JSM82C251T provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 5Mbps.Designed for operation in harsh environments. The device features cross-wire, overvoltage and loss of ground protection to +40V. Also featured are overtemperature protection as well as -7V to 12V common-mode range,and tolerance to transients +200V. The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial,building automation, and automotive applications.



Applications

- CAN Data Buses
- Industrial Automation
- Building and Climate Control (HVAC)
- Telecommunications and Base Station Control and Status
- CAN Bus Standards Such as CAN open

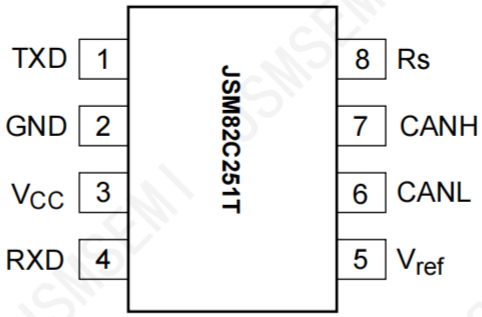
Features and benefits

- Fully compatible with the " ISO 11898-24 V" standard
- Meets or Exceeds ISO 11898
- Slope control to reduce Radio Frequency Interference (RFI)
- Thermally protected
- Short-circuit proof to battery and ground in 24 V powered systems
- Bus-Fault Protection of ±40V
- Bus Pin ESD Protection Exceeds 16kV HBM
- Low-current Standby mode
- An unpowered node does not disturb the bus lines
- At least 120 nodes can be connected
- Signaling Rates up to 5Mbps
- Low-Current Standby Mode: 400μA Typical
- High immunity against electromagnetic interference.
- Glitch-Free Power-Up and Power-Down CAN Bus industrial, building automation, and automotive Protection for Hot-Plugging

Ordeing Infomation

Ordernumber	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
JSM82C251T	SOP-8	JSM82C251T	-40 to 125°C	3	T&R,2500	Rohs

Pinning information



Pin configuration

Pin		Type	Description
Name	No.		
TXD	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), driver input
GND	2	GND	Ground connection
Vcc	3	Supply	Transceiver 5V supply Voltage
RXD	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
V_{ref}	5	O	Vcc /2 reference output pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
Rs	8	I	Mode select pin: strong pulldown to GND = high-speed mode, strong pull up to Vcc = low-power mode, 10kΩ to 100kΩ pulldown to GND = slope control mode

Functional description

The JSM82C251T is intended for use in applications employing the Controller Area Network(CAN)serial communication physical layer in accordance with the IS0 11898 Standard.The JSM82C251T provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 5Mbps.Designed for operation in harsh environments. The device features cross-wire,overvoltage and loss of ground protection to +40V.Also featured are overtemperature protection as well as -7V to 12V common-mode range,and tolerance to transients o+200V. The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial,building automation, and automotive applications.

Rs, pin 8,selects one of three different modes of operation:high-speed,slope control,or low-power mode. The high-speed mode of operation is selected by connecting pin 8 to ground,allowing the transmitter output transistors to switch as fast as possible with no limitation on the rise and fall slope.The rise and fall slope can be adjusted by connecting a resistor to ground at pin 8; the slope is proportional to the pin's output current. Slope control with an external resistor value of 10kΩ gives about 15V/us slew rate; 100kΩ gives about 10V/us slew rate.

If a high logic level is applied to the Rs pin 8, the device enters a low-current standby mode where the driver is switched off and the receiver remains active.The local protocol controller returns the device to the normal mode when it transmits to the bus.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			Min	Max	Unit
Supply Voltage,Vcc			-0.3	7	V
Voltage at any bus terminal (CANH or CANL)			-40	40	V
Transient voltage per ISO 7637, pulse 1,2,3a,3b		CANH,CANL	-200	200	V
Input voltage, V_I (D,Rs, or R)			-0.3	Vcc+0.5	V
Receiver output current, IO			-11	11	mA
Electrical fast transient/burst	IEC 6100-4-4,Classificiation	CANH,CANL	-3	3	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditionsis not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All Voltage Values, except differential I/O bus Voltages, are with respect to network ground terminal.

ESD Ratings

			Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM)	CANH, CANL and GND	±16000	V
		All pins	±4000	
	Charged-device model (CDM)		±1000	

Recommended Operating Conditions

PARAMETER		Min	NOM	Max	Unit
Supply Voltage,Vcc		4.5		5.5	V
Voltage at any bus terminal (common mode)V_I or V_{IC}		-7		12	V
High-level input Voltage,V_{IH}	D input	0.7Vcc			V
Low-level input Voltage,V_{IL}	D input			0.3Vcc	V
Differential input Voltage,V_{ID}		-6		6	V
Input Voltage to Rs,$V_{I(Rs)}$		0		Vcc	V
Input Voltage at Rs for standby,$V_{I(Rs)}$		0.75Vcc		Vcc	V
Wave-shaping resistance, Rs		0		100	kΩ
High-level output current, I_{OH}	Driver	-50			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			50	mA
	Receiver			8	
Operating free-air temperature, T_A		-40		125	°C
Junction temperature, T_J				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

Thermal Information

Symbol	Parameter	Conditions	Typ	Unit
Rth(j-a)	Thermal resistance from junction to ambient	In free air	160	K/W

Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter			Test Conditions	Min	Typ	Max	Unit
Icc	Supply current	Standby	Rs at Vcc, D at Vcc		400	600	μA
		Dominant	D at 0V, 60Ω load, Rs at 0V		1	2	mA
		Recessive	D at Vcc, no load, Rs at 0V		1	2	

Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter			Test Conditions		Min	Typ(1)	Max	Unit
V_{OH}	Bus output Voltage	Dominant	D= 0V,Rs=0V,T ≥ -40°C	CANH,Figure 1,2	3.5		Vcc	V
				CANL,Figure 1,2	0.5		2	
V_{OL}		Recessive	D= 0.7Vcc, Rs=0V,	CANH,Figure 1,2	3	3.5	4	
				CANL,Figure 1,2	3	3.5	4	
$V_{OD(D)}$	Differential output Voltage	Dominant	D=0V, Rs=0V	Figure 1	2.5	3.2	3.5	
			D=0V, Rs=0V, R_{NODE} = 330Ω	Figure 3	2.5	3.2	3.5	V
			D=0V, Rs=0V, R_{NODE} = 165Ω, Vcc≥4.75V	Figure 1,2	2.5	3.2	3.5	
$V_{OD(R)}$		Recessive	D=0.7Vcc	See Figure 1	-120	0	12	mV
			D=0.7Vcc, T ≤ 85°C	No load	-0.5	–0.2	0.05	V
Voc (pp)	Peak-to-peak common-mode output voltage		Figure 9, Rs at 0V			600		mV
I_{IH}	High-level input current		D at 0.7Vcc		-10		10	μA
I_{IL}	Low-level input current		D at 0.3Vcc		-10		15	μA
I_{OS}	Short-circuit output current		Figure 11, V_{CANH} at –7V, CANL Open		-200			mA
			Figure 11, V_{CANH} at 12V, CANL Open				200	
			Figure 11, V_{CANL} at -7V, CANH Open		-200			
			Figure 11, V_{CANL} at 12V, CANH Open				200	
C_o	Output capacitance		See receiver input capacitance					
I_{OZ}	High-impedance output current		See receiver input current					
$I_{IRs(s)}$	Rs input current for standby		Rs at 0.75Vcc		-10			μA
$I_{IRs(f)}$	Rs input current for full speed operation		Rs at 0V		-450		0	μA

(1) All typical Values are at 25°C and with a 5V supply.

Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions		Min	Typ(1)	Max	Unit
V_{IT+}	Positive-going input threshold Voltage	Rs at 0V, (See Table 1)			800	900	mV
V_{IT-}	Negative-going input threshold Voltage			500	700		
V_{hys}	Hysteresis Voltage (V_{IT+} –V_{IT-})				100		
V_{OH}	High-level output Voltage	Figure 6, I_O = –4mA		0.8Vcc			V
V_{OL}	Low-level output Voltage	Figure 6, I_O = 4mA				0.2Vcc	
I_I	Bus input current	CANH or CANL at 12V	Other input at 0V, Rs=0V, D=0.7Vcc			600	μA
		CANH or CANL at 12V,Vcc=0V				715	
		CANH or CANL at 12V		-460			
		CANH or CANL at 12V ,Vcc=0V		-340			
C_I	Input capacitance, (CANH or CANL)	Pin-to-ground,V_I = 0.4 sin(4E6πt)+0.5V, D=0.7Vcc			20		pF
C_{ID}	Differential input capacitance	Pin-to-Pin,V_I = 0.4 sin(4E6πt) + 0.5V, D=0.7Vcc			10		pF
R_{ID}	Differential input resistance	D at 0.7Vcc, Rs at 0V		40	70	100	kΩ
R_{IN}	CANH, CANL input resistance	D at 0.7Vcc, Rs at 0V		20	35	50	kΩ
	Receiver noise rejection	See Figure 13					

VREF-Pin Characteristics

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
Vo	Reference output voltage	–5μA < I_O < 5μA	0.45Vcc		0.55Vcc	V
		–50μA < I_O < 50μA	0.4Vcc		0.6Vcc	

Power Dissipation Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Device power dissipation	Vcc = 5V, T_j = 27°C, R_L = 60 Ω, RS at 0V, Input to D a 500kHz 50% duty cycle square wave		97.7		mW
		Vcc = 5.5V, T_j = 27°C, R_L = 60 Ω, RS at 0V, Input to D a 500kHz 50% duty cycle square wave		14.2		
T_{SD}	Thermal shutdown junction temperature			165		°C

Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation delay time, low-to-high-level output	Figure 4, Rs at 0V		55	85	ns
		Figure 4, Rs with 10 kΩ to ground		80	125	
		Figure 4, Rs with 100 kΩ to ground		110	160	
t_{PHL}	Propagation delay time, high-to-low-level output	Figure 4, Rs at 0V		80	120	
		Figure 4, Rs with 10 kΩ to ground		130	180	
		Figure 4, Rs with 100 kΩ to ground		170	240	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	Figure 4, Rs at 0V		25	50	
		Figure 4, Rs with 10 kΩ to ground		50	100	
		Figure 4, Rs with 100 kΩ to ground		60	120	
t_r	Differential output signal rise time	Figure 4, Rs at 0V	25	50	100	
t_f	Differential output signal fall time		30	40	70	
t_r	Differential output signal rise time	Figure 4, Rs with 10 kΩ to ground	40	70	150	
t_f	Differential output signal fall time		45	60	100	
t_r	Differential output signal rise time	Figure 4, Rs with 100 kΩ to ground	60	100	200	
t_f	Differential output signal fall time		70	90	140	
t_{en}	Enable time from standby to dominant	Figure 8			0.5	μs

Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
$t_{(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	Rs at 0V	Figure 10		90	130	ns
		Rs with 10kΩ to ground			135	205	
		Rs with 100kΩ to ground			180	260	
$t_{(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	Rs at 0V			120	140	
		Rs with 10kΩ to ground			180	215	
		Rs with 100kΩ to ground			240	280	
$t_{(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	Rs at 0V,Vcc from 4.5V to 5.1V			105	145	

Switching Characteristics: Receiver

Over recommended operating conditions(unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation delay time, low-to-high-level output	Figure 6		35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	
$t_{sk(p)}$	IPulse skew (|tpHL - tpLH |)				10	
t_r	Output signal rise time				1.5	
t_f	Output signal fall time				1.5	
$t_{p(sb)}$	Propagation delay time in standby	Figure 12, Rs at Vcc		500	1500	

Parameter Measurement Information

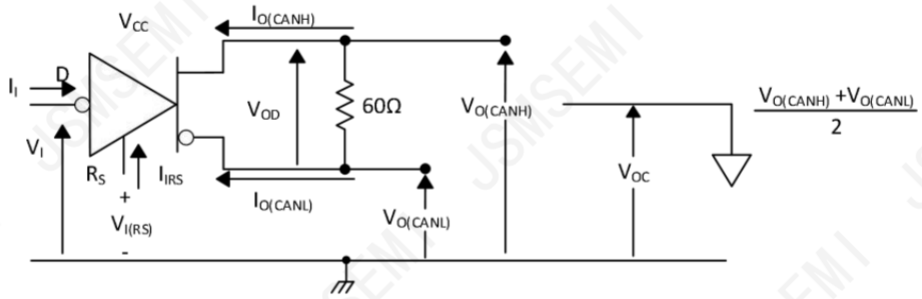


Figure1. Driver Voltage, Current, and Test Definition

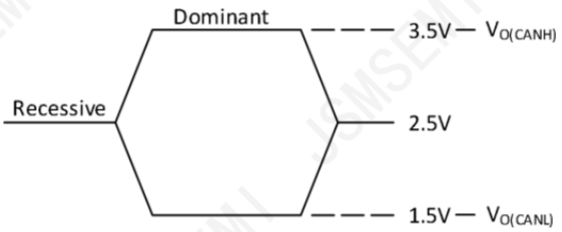


Figure2. Bus Logic State Voltage Definitions

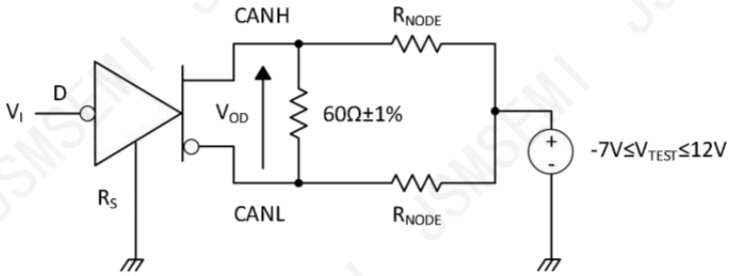
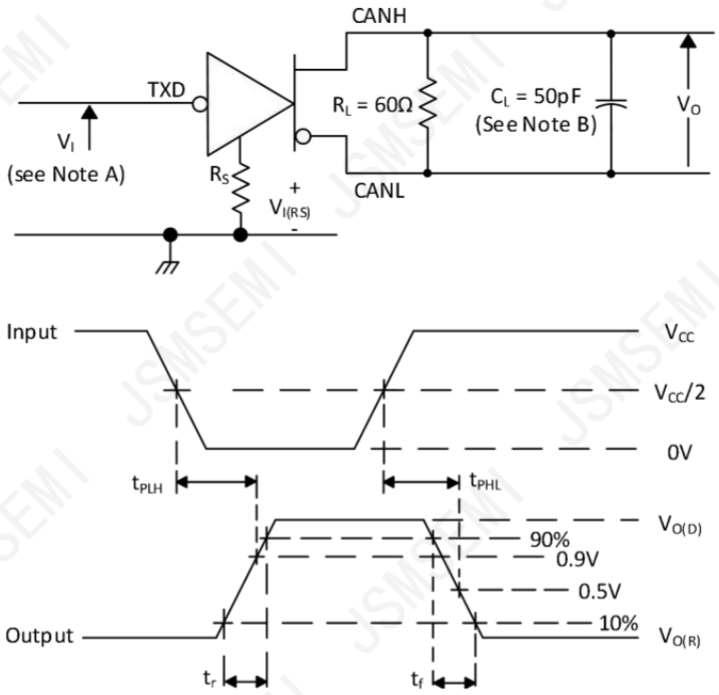


Figure3. Driver OD



A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤125kHz, 50% duty cycle, t_r≤ 6ns, t_f≤ 6ns, Z_O= 50 Ω.
B. C_L includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

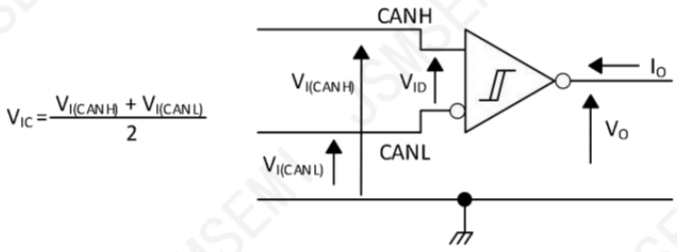
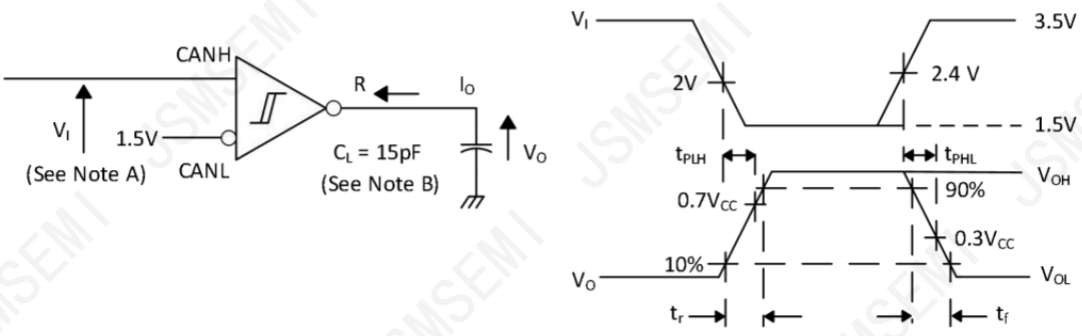


Figure 5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, ZO = 50 Ω.
B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

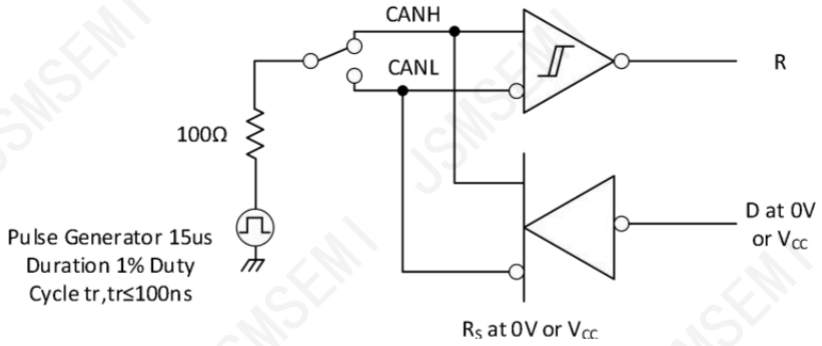


Figure 7.Test Circuit, Transient Overvoltage Test

Table 1. Receiver Characteristics Over Common Mode With $V_{(Rs)}$=1.2V

V_{CANH}	V_{CANL}	DIFFERENTIAL INPUT	OUTPUT	
V_{IC}	V_{ID}	$\|V_{ID}\|$	R	
12V	11.1V	900mV	L	V_{OL}
-6.1V	-7V	900mV	L	
-1V	-7V	6V	L	
12V	6V	6V	L	
-6.5V	-7V	500mV	H	V_{OH}
12V	11.5V	500mV	H	
-7V	-1V	6V	H	
6V	12V	6V	H	
open	open	X	H	

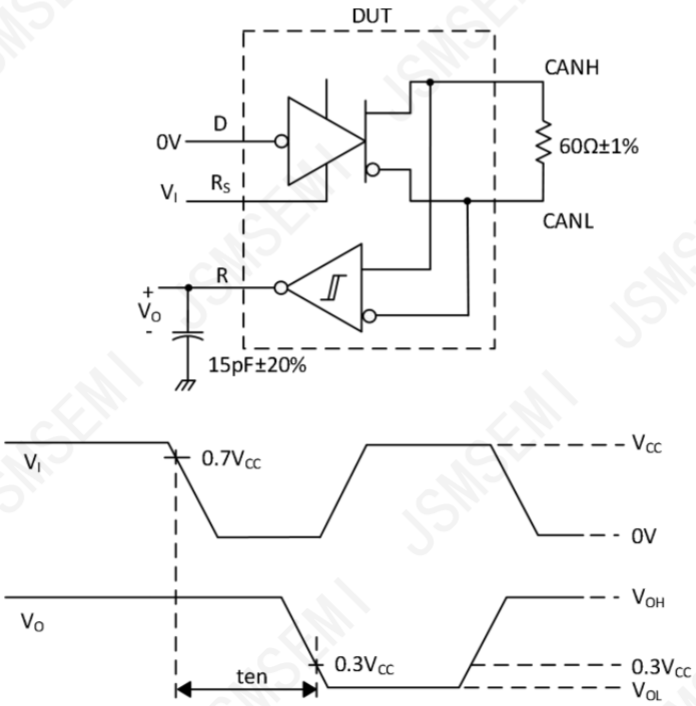
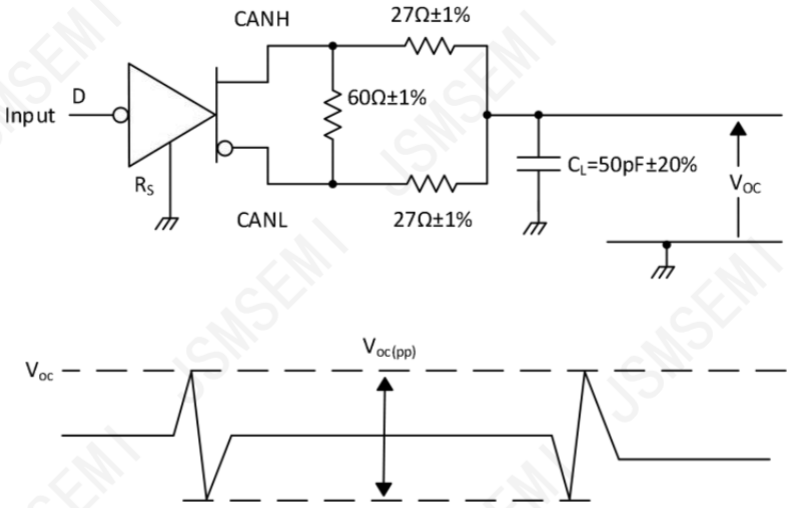


Figure 8. Ten Test Circuit and Voltage Waveforms



The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50%duty cycle, tr ≤ 6ns , tf ≤ 6ns, ZO = 50 Ω.

Figure9. Peak-to-Peak Common Mode Output Voltage

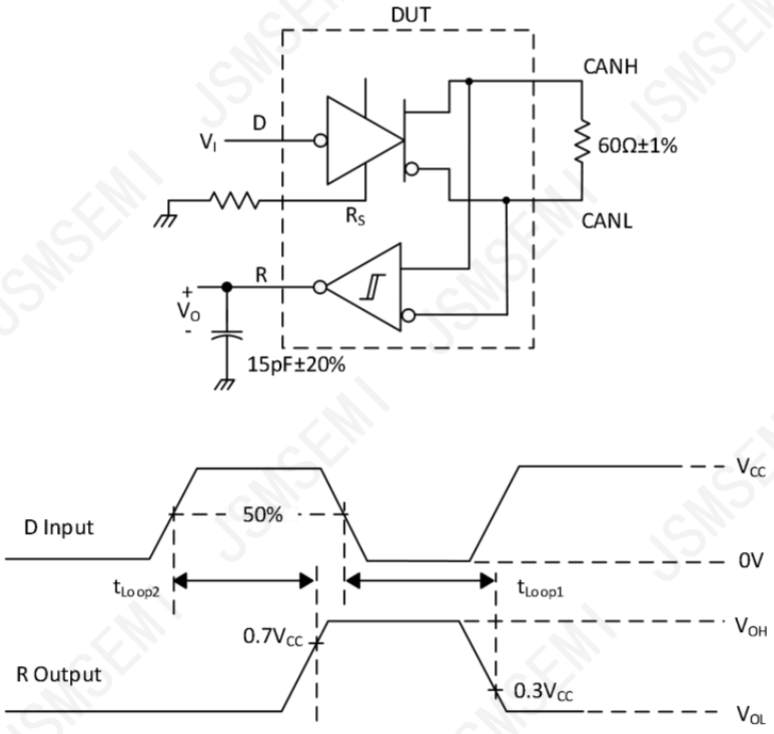


Figure 10. T_{LOOP} Test Circuit and Voltage Waveforms

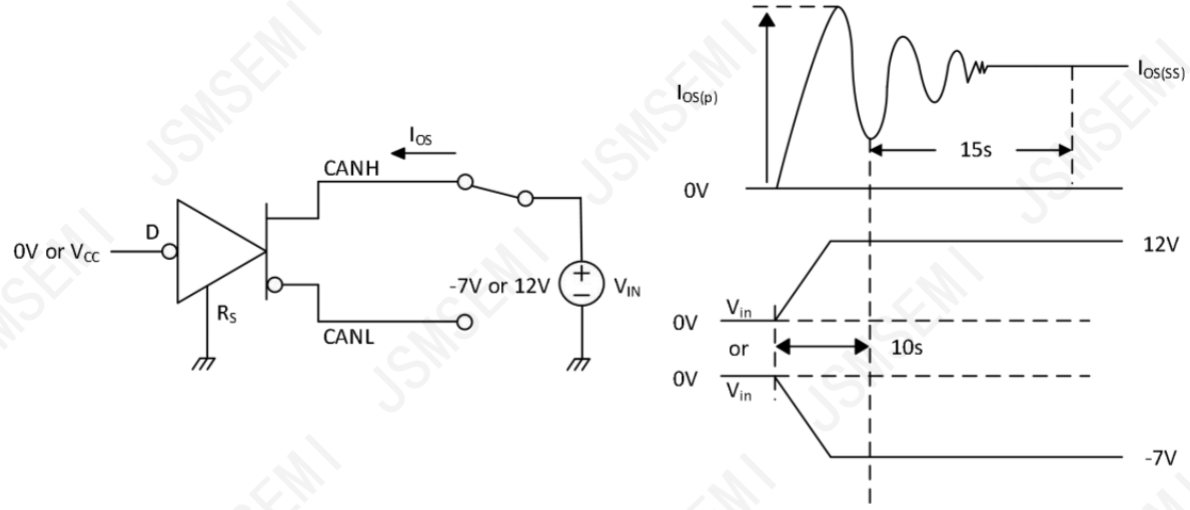
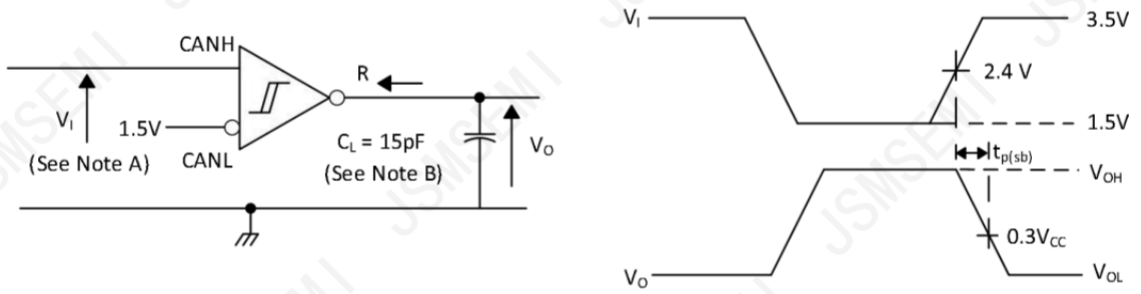
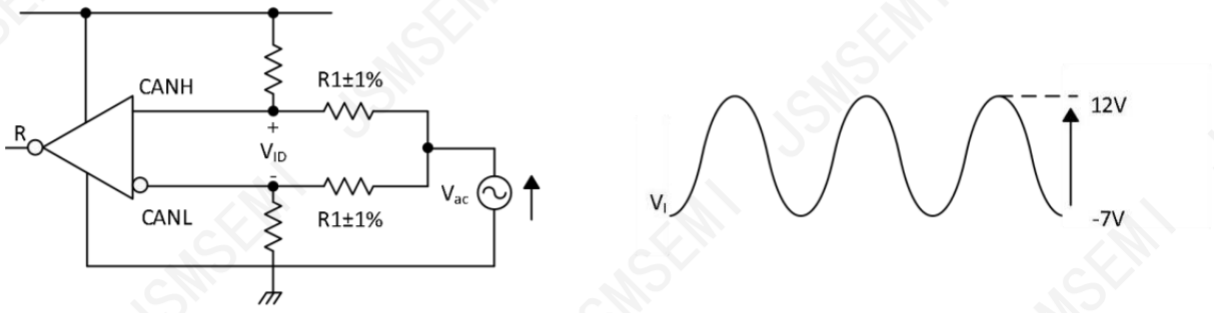


Figure 11. Driver Short-Circuit Test



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, ZO = 50 Ω.
C. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 12. Receiver Propagation Delay in Standby Test Circuit and Waveform



VID	R1	R2
500mV	50	450
900mV	50	227

A. All input pulses are supplied by a generator having the following characteristics: f_{IN} < 1.5 MHz, T_A = 25°C, Vcc = 5V.
B. The receiver output should not change state during application of the common-mode input waveform.

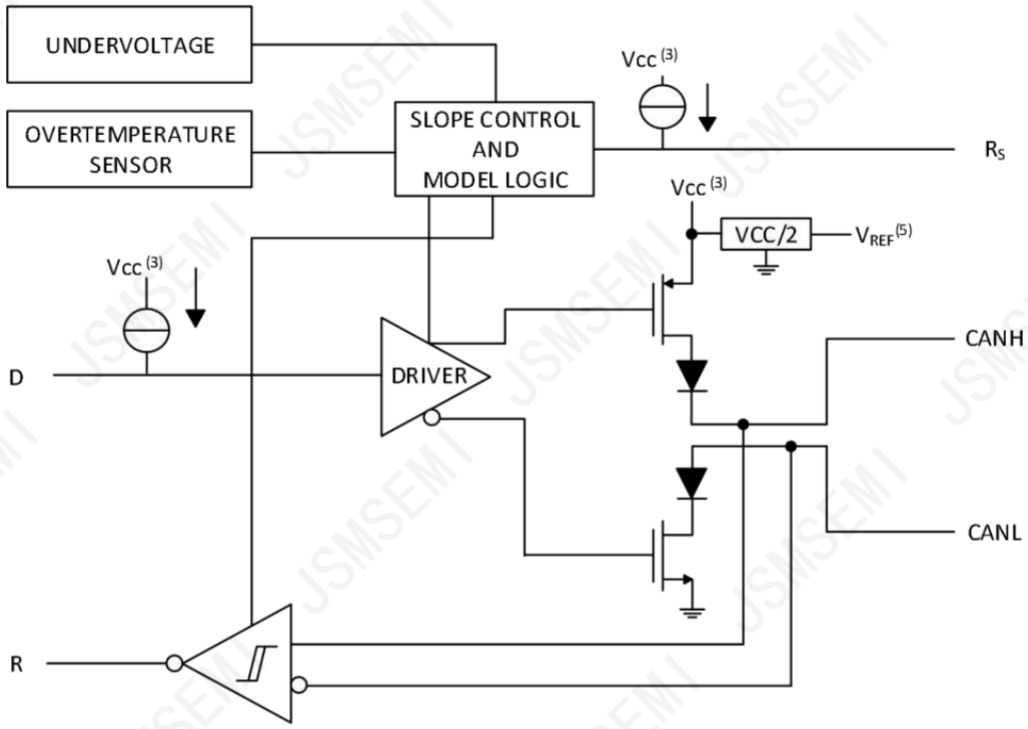
Figure 13. Common-Mode Input Voltage Rejection Test

Detailed Description

Overview

The JSM82C251T CAN bus transceiver is compatible with the ISO 11898-2 High Speed CAN (Controller Area Network)physical layer standard. It is design to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 5Mbps.

Functional Block Diagram



Feature Description

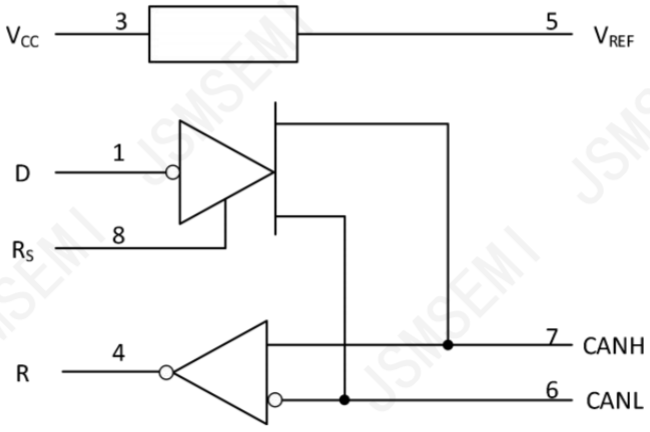


Figure 14. Function Diagram (Positive Logic)

Mode Control

RS, Pin 8, selects one of three possible modes of operation: high-speed, slope control, or low-power mode.

High-Speed Mode

The high-speed mode of operation can be selected by setting RS (Pin 8) low. High-speed allows the output to switch as fast as possible with no internal limitations on the output rise and fall slopes. The CAN bus driver and receiver are fully operational and the CAN communication is bi-directional. The driver is translating a digital input on D to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on R.

Slope Control Mode

The rise and fall slope of the JSM82C251T driver output can be adjusted by connecting a resistor from Rs (Pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 15 . The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ~15V/ µs slew rate, and up to 100 kΩ to achieve a ~10.0V/µs slew rate.

Low-Power Mode

If a high-level input (>0.75Vcc) is applied to RS (Pin 8), the circuit enters a low-current, listen only standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the R output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the RS pin low to return to slope control mode or high-speed mode.

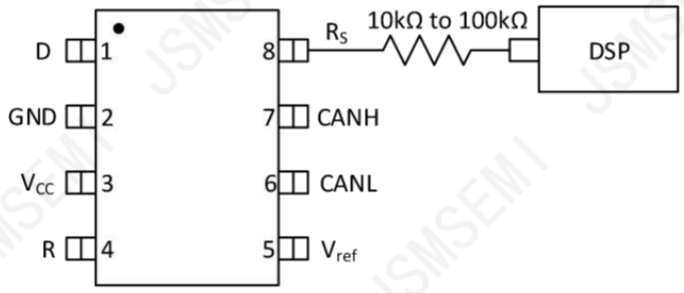


Figure 15. Function Diagram (Positive Logic)

Thermal Shutdown

The JSM82C251T has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 165°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an JSM82C251T is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

Device Functional Modes

Table 2. Driver

Inputs	Voltage at R_S,V_{RS}	Outputs		Bus State
D		CANH	CANL	
L	V_{RS}<1.2V	H	L	Dominant
H	V_{RS}<1.2V	Z	Z	Recessive
OPEN	X	Z	Z	Recessive
X	V_{RS}>0.75Vcc	Z	Z	Recessive
X	OPEN	Z	Z	Recessive

Table 3. Receiver

Differential Inputs [VID = V(CANH) - V(CANL)]	Bus State
V_{ID}≥0.9V	L
0.5V<V_{ID}<0.9V	?
V_{ID}≤0.5V	H
OPEN	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

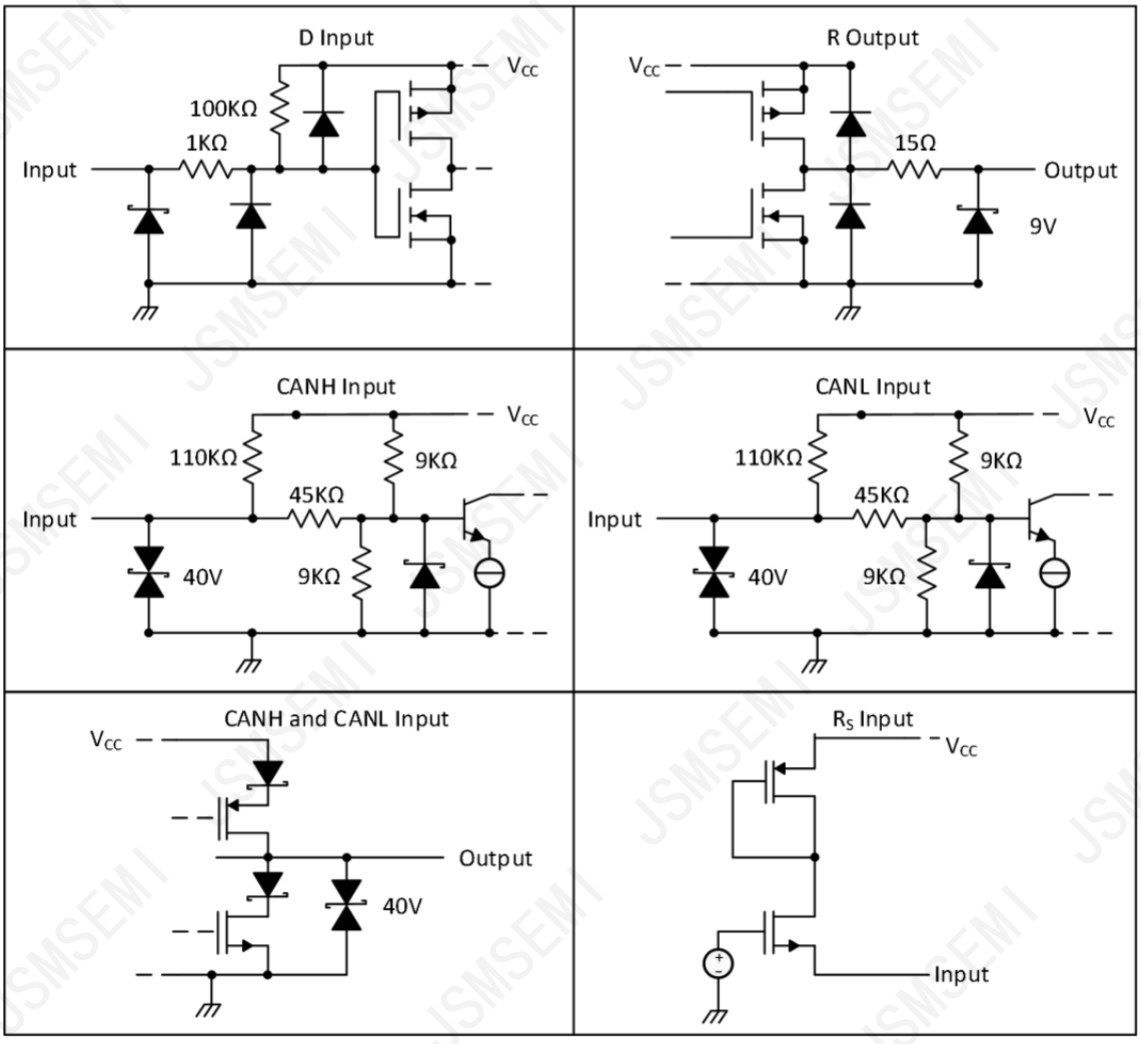


Figure 16. Equivalent Input and Output Schematic Diagrams

Application and Implementation

Application Information

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to Vcc/2 via the high-resistance internal resistors RIN and RID of the receiver, corresponding to a logic high on the D and R pins. See Figure 17 and Figure 18 .

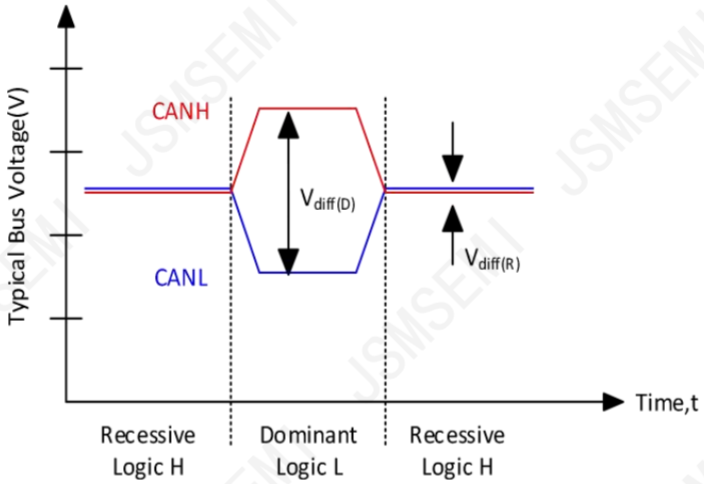


Figure 17. CAN Bus States(Physical Bit Representation)

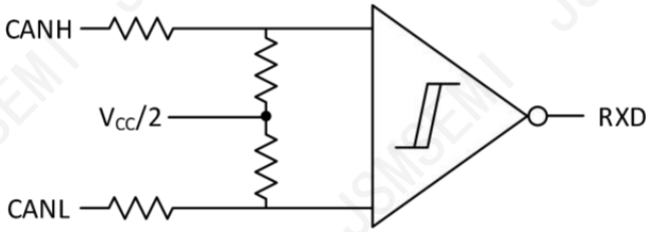


Figure 18. Simplified Recessive Common Mode Bias and Receiver

The JSM82C251T CAN transceiver is typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120Ω characteristic impedance twisted pair cable with termination on both ends of the bus.

The basics of bus arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this sample is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system must also be accounted for with adjustments in signaling rate and stub and bus length. Table 4 lists the maximum signaling rates achieved with the JSM82C251T in high-speed mode with several bus lengths of category-5, shielded twisted-pair cable.

Bus Length(m)	Sinaling Rtae(kbps)
30	1000
100	500
250	250
500	125
1000	62.5

Table 4 Maximum Signaling Rates for Various Cable Lengths

Application Information(continued)

The ISO 11898 standard specifies a maximum bus length of 40 meters and maximum stub length of 0.3 meters with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes on a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A bus with a large number of nodes requires a transceiver with high input impedance such as the JSM82C251T.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120Ω characteristic impedance (Zo). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the ISO 11898 standard, should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the –2V to 7V common-mode range of tolerable ground noise specified in the standard, helps to ensure data integrity. The JSM82C251T extends data integrity beyond that of the standard with an extended –7V to 12V range of common-mode operation.

Typical Application

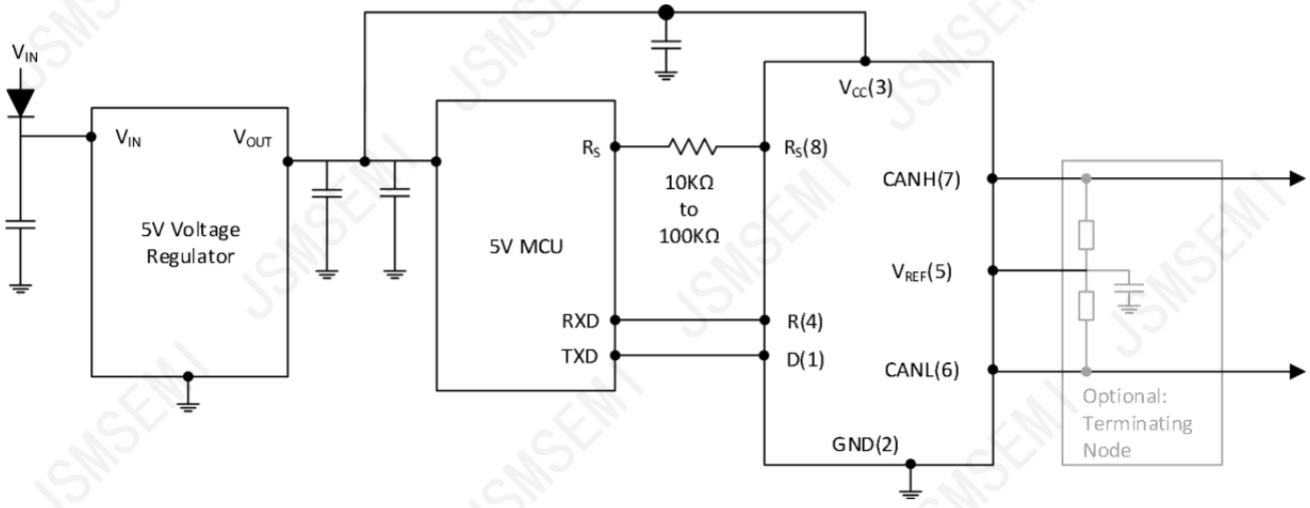


Figure 19. Typical Application Schematic

Design Requirements

Bus Loading, Length, and Number of Nodes

The ISO11898 Standard specifies up to 1Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus.

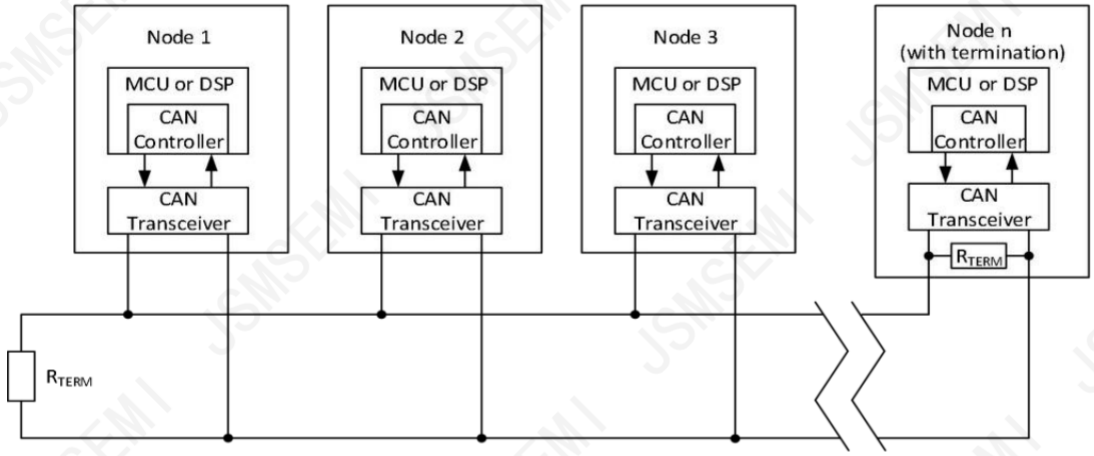


Figure 20. Typical CAN Bus

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as th e JSM82C251T CAN transceiver. ISO11898-2 specifies the driver differential output with a 60Ω load(two 120Ω termi nation resistors in parallel) and the differential output must be greater than 1.5V. TheJSM82C251T devices are speci fied to meet the 1.5V requirement with a 60Ω load, and additionally specified with a differential output voltage minimu m of 1.2V across a common mode range of –2V to 7V via a 330Ω coupling network.

This network represents the bus loading of 120 JSM82C251T transceivers based on their minimum differential input resistance of 40kΩ . Therefore, the JSM82C251T supports up to 120 transceivers on a single bus segment with mar gin to the 1.2V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings,net work imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus l ength may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and dat a rate trade offs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additionalstandards th at have been built on the original ISO 11898 CAN standard.

Detailed Design Procedure

CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (ZO). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node,but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 20). Split termination utilizes two 60Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Typical Application(continued)

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the CAN transceiver's current limit.

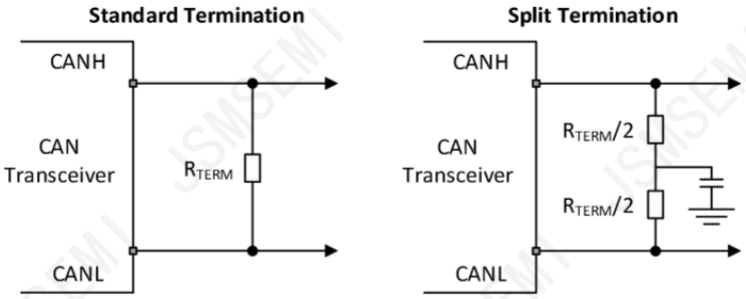


Figure 21. CAN Termination

Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (D pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs(CANH and CANL) to its output pin.

This loop delay will increase as the slope of the driver output is slowed during slope control mode. This increased loop delay means that there is a trade off between the total bus length able to be used and the driver's output slope used via the slope control pin of the device. For example, the loop delay for a 10kΩ resistor from the RS pin to ground is 100ns, and the loop delay for a 100kΩ resistor is 500ns. Therefore, if we use the following rule-of-thumb that the propagation delay of typical twisted pair bus cable is 5ns/m, we can calculate an approximate cable length trade-off between normal high-speed mode and slope control mode with a 100kΩ resistor. Using typical values, the loop delay For a recessive to dominant bit with RS tied directly to ground is 60ns, and with a 100kΩ resistor is 440ns. At 5ns/m of propagation delay, which you have to count in both directions the difference is 38 meters (440–60)/(2×5).

Another option to improving the electromagnetic emissions of the device besides slowing down the edge rates of the driver in slope control mode is using quality shielded bus cabling.

Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close as possible to the Vcc supply pins as possible.

Layout

Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use Vcc and ground planes to provide low inductance. Note: high frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or Varistor solution) and bus filter capacitors C8 and C9 are shown in .

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 22 shows split termination. This is where the termination is split into two resistors, R7 and R8, with the center or split tap of the termination connected to ground Via capacitor C7. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends. See the application section for information on power ratings needed for the termination resistor(s).

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (Vcc).

Use at least two Vias for Vcc and ground connections of bypass capacitors and protection devices to minimize trace and Via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4. Since the internal pull up and pull down biasing of the device is weak for floating pins, an external 1k to 10k ohm pull-up or down resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open drain host processor is used to drive the D pin of the device an external pull-up resistor between 1k and 10k ohms should be used to drive the recessive input state of the device (R1).

Pin 8: is shown assuming the mode pin, Rs, will be used. If the device will only be used in normal mode or slope control mode, R3 is not needed and the pads of C4 could be used for the pull down resistor to GND.

Pin 5 in is shown for the JSM82C251T and JSM82C251T devices which have a Vref output Voltage reference. If used, this pin should be tied to the common mode point of the split termination. If this feature is not used, the pin can be left floating.

Layout Example

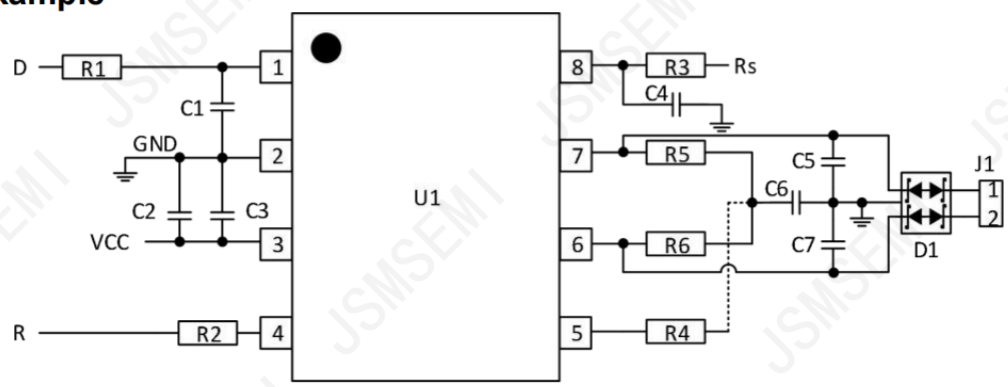
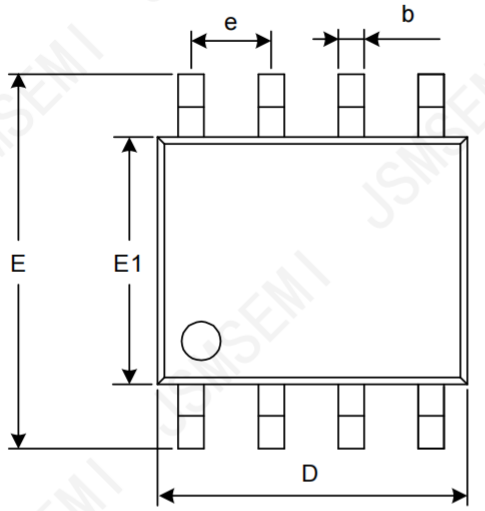
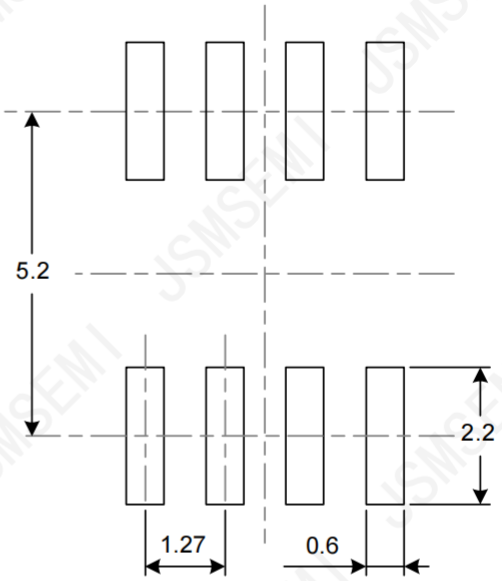


Figure 22. Layout Example Recommendation

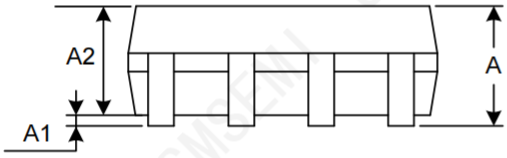
Package Information

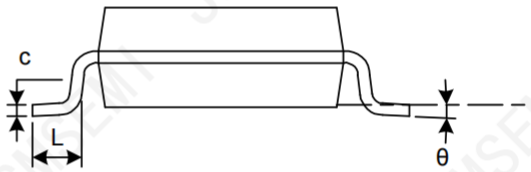
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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