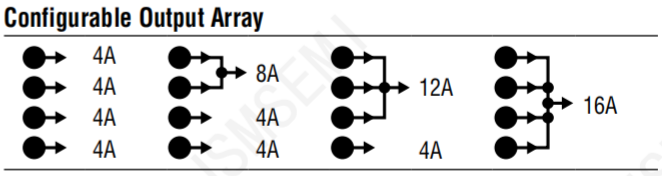
DESCRIPTION

The LTM4644 is a quad DC/DC step-down Module (micromodule) regulator with 4A per output. Outputs can be paralleled in an array for up to 16A capabil-ity. Included in the package are the switching controllers, power FETs,inductors and support components. Operating over an input voltage range of 4V to 16V or 2.4V to 16V with an external bias supply, the LTM4644 supports an output voltage range of 0.6V to 5.5V. Its high efficiency design delivers 4A continuous (5A peak) output current per channel. Only bulk input and output capacitors are needed.

APPLICATIONS

- Multirail Point of Load Regulation
- FPGAs, DSPs and ASICs Applications



FEATURES

- Quad Output Step-Down Module Regulator with 4A per Output
- Wide Input Voltage Range: 4V to 16V
  * 2.4V to 16V with External Bias
- 0.6V to 5.5V Output Voltage
- 4A DC, 5A Peak Output Current Each Channel
- Up to 5.5W Power Dissipation (T_A = 60°C, 200 LFM, No Heat Sink)
- ±1.5%Total Output Voltage Regulation
- Current Mode Control, Fast Transient Response
- Parallelable for Higher Output Current
- Output Voltage Tracking
- Internal Temperature Sensing Diode Output
- External Frequency Synchronization
- Overvoltage, Current and Temperature Protection
- 9mm × 15mm × 5.01mm BGA Package

TYPICAL APPLICATION

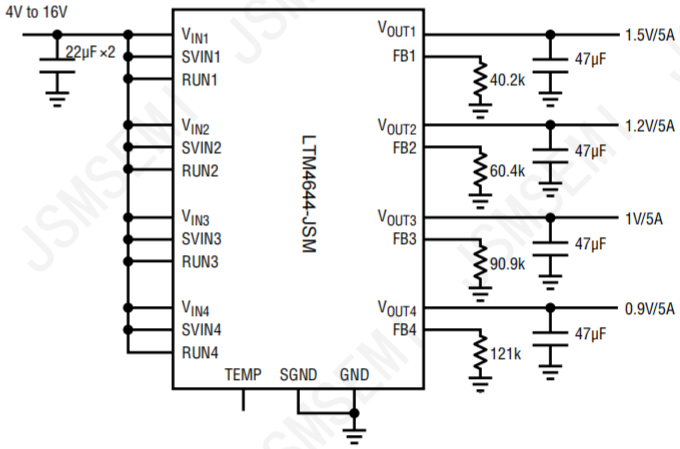
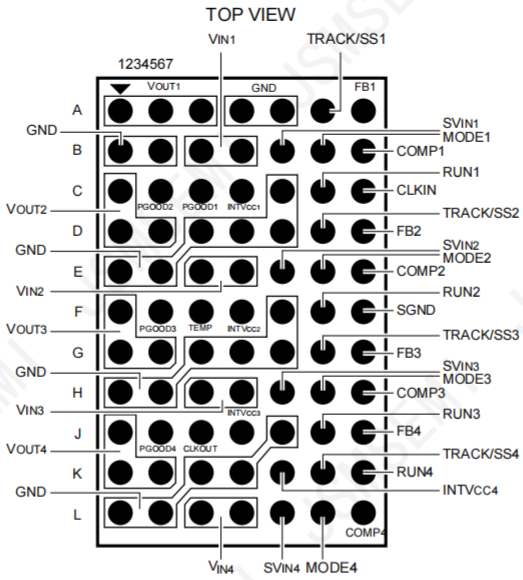


Figure 1. 4V to 16V Input, Quad 0.9V, 1V, 1.2V and 1.5V Output DC/DC µModule Regulator*

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
LTM4644EY#PBF-JSM	BGA-77	JSM4644Y	-40 to 125°C	3	Tray&170	Rohs
LTM4644IY#PBF-JSM	BGA-77	JSM4644Y	-40 to 125°C	3	Tray&170	Rohs
LTM4644MPY#PBF-JSM	BGA-77	JSM4644Y	-55 to 125°C	3	Tray&170	Rohs

PIN CONFIGURATION



BGA PACKAGE
77-LEAD (9mm × 15mm × 5.
01mm)

PIN FUNCTIONS

V_{OUT1} (A1, A2, A3), V_{OUT2} (C1, D1, D2), V_{OUT3} (F1, G1, G2), V_{OUT4} (J1, K1, K2): Power Output Pins of Each Switching Mode Regulator Channel. Apply output load between these pins and GND pins.

GND (A4-A5, B1-B2, C5, D3-D5, E1-E2, F5, G3-G5, H1-H2, J5, K3-K4, L1-L2): Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

V_{IN1} (B3, B4), V_{IN2} (E3, E4), V_{IN3} (H3, H4), V_{IN4} (L3, L4): Power input pins connect to the drain of the internal top MOSFET for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of VIN pins and GND pins.

PGOOD1, PGOOD2, PGOOD3, PGOOD4 (C3, C2, F2, J2): Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10 % of the internal 0.6V reference.

CLKOUT (J3): Output Clock Signal for PolyPhase Opera-tion of the Module. The phase of CLKOUT with respect to CLKIN is set to180°.CLKOUT's peak-to-peak amplitude is INTVCC to GND.CLKOUT is only active when RUN4 is enabled.

$INTV_{CC1}$, $INTV_{CC2}$, $INTV_{CC3}$, $INTV_{CC4}$ (C4, F4, J4, K5): Internal 3.4V Regulator Output of Each Switching Mode Regulator Channel. The internal power drivers and con- trol circuits are powered from this voltage. Each pin is internally decoupled to GND with 1μF low ESR ceramic capacitor already.

SV_{IN1}, SV_{IN2}, SV_{IN}, SV_{IN4} (B5, E5, H5, L5): Signal V_{IN}. Filtered input voltage to the internal3.3V regulator for the control circuitry of each Switching mode Regulator Channel. Tie this pin to the V_{IN} pin respectively in most applications. Connect SV_{IN} to an external voltage supply of at least 4V which must also be greater than V_{OUT}.

TRACK/SS1, TRACK/SS2, TRACK/SS3, TRACK/SS4 (A6, D6, G6, K6): Output Tracking and Soft-Start Pin of Each Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a volt - age below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to match the TRACK voltage.

Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2.5μA pull-up current from INTVCC on this pin, so putting a capacitor here provides soft-start function.

MODE1, MODE2, MODE3, MODE4 (B6, E6, H6, L6): Operation Mode Select for Each Switching Mode Regulator Channel. Tie this pin to INTVCC to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous current mode operation at light loads. Do not leave floating.

RUN1, RUN2, RUN3, RUN4 (C6, F6, J6, K7): RunControl Input of Each Switching Mode Regulator Channel. Enable regulator operation by tying the specific RUN pin above 1.2V. Pulling it below1.1V shuts down the respective regulator channel. Do not leave floating.

FB1, FB2, FB3, FB4 (A7, D7, G7, J7): The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, in LTM4644, this pin is connected to VOUT of each channel with a 60.4k Ω precision resistor. Different output voltages can be programmed with an additional resistor between the FB and GND pins for the LTM4644, and two resistors between the VOUT.In PolyPhase operation,tying the FB pins together allows for parallel operation.

COMP1, COMP2, COMP3, COMP4 (B7, E7, H7, L7): Cur-rent Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The internal current comparator threshold is proportional to this voltage.Tie the COMP pins together for parallel opera-tion.

CLKIN (C7): External Synchronization Input to Phase Detector of the Module. This pin is internally terminated to SGND with 20kΩ. The phase-locked loop will force the channel1turn-on signal to be synchronized with the rising edge of the CLKIN signal. Channel 2,channel 3 and channel 4 will also be synchronized with the rising edgeof the CLKIN signal with a pre-determined phase shift.

SGND (F7): Signal Ground Connection.SGND is connected to GND internally through single point. Use a separated SGND ground copper area for the ground of the feedback resistor and other components connected to signal pins. A second connection between the PGND plane and SGND planeis recommended on the backside of the PCB under-neath the module.

TEMP (F3): Onboard Temperature Diode for Monitoring the VBE Junction Voltage Change with Temperature.

Absolute Maximum Ratings

Symbol	Definition		MIN.	MAX.	Units
V_{IN}, SV_{IN}	Input Voltage(Per Channel)		-0.3	18	V
V_{OUT}	Output Voltage(Per Channel)		-0.3	6	V
RUN	Operating control input voltage(Per Channel)		-0.3	18	V
$INTV_{CC}$	VINTVCC Linear Regulator Voltage(Per Channel)		-0.3	5	V
	PGOOD,MODE,TRACK/ SS,FB Voltage(Per Channel)		-0.3	5	V
	CLKOUT,CLKIN Voltage(Per Channel)		-0.3	5	V
T_S	Storage Temperature		-65	150	°C
T_A	Operating Temperature	E&I	-40	125	°C
		MP	-55	125	
T_J	Junction Temperature		-	150	°C
T_L	Lead Temperature (Soldering, 10s)		-	260	°C

ELECTRICAL CHARACTERISTICS

temperature range, otherwise specifications are at T_A = 25°C . V_{IN} = 12V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel						
V_{IN}, SV_{IN}	Input DC Voltage	$SV_{IN} = V_{IN}$	4		16	V
$V_{OUT(RANGE)}$	Output Voltage Range		0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic, MODE = $INTV_{CC}$,V_{IN} = 4V to 16V, I_{OUT} = 0A to 4A $R_{FB(BOT)}$ = 40.2k	1.477	1.50	1.523	V
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	1.1	1.2	1.3	V
$I_{Q(SVIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$ V_{IN} = 12V, V_{OUT} = 1.5V, MODE = GND Shutdown, RUN = 0, V_{IN} = 12V			16 7 30	mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 4A		0.62		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)	0		4	A
ΔV_{OUT} (Line)/V_{OUT}	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 4V to 16V, I_{OUT} = 0A		0.05	0.15	%/V
ΔV_{OUT} (Load)/V_{OUT}	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 4A		0.5	1	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V		10		mV
$\Delta V_{OUT(START)}$ (1)	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V		10		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, No Load, TRACK/SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 1.5V		2.5		ms
ΔV_{OUTLS} (1)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V		160		mV
t_{SETTLE} (1)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V		40		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V	5	5.5		A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V, –40°C to 125°C	0.592	0.60	0.608	V V
R_{FBHI} (2)	Resistor Between V_{OUT} and FB Pins		60.05	60.40	60.75	kΩ
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V		2.5	4	µA
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout	V_{IN} Falling VIN Hysteresis	2.4	3.0	3.5 500	V mV
$t_{ON(MIN)}$	Minimum On-Time			40		ns
$t_{OFF(MIN)}$	Minimum Off-Time			70		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive	 –13 7	 –10 10	 –7 13	 % %
I_{PGOOD}	PGOOD Leakage			0.02	5	µA
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 1mA,VIN = 5V		0.02	0.1	V
V_{INTVCC}	Internal V_{CC} Voltage	SV_{IN} = 4V to 16V	3.2	3.4	3.6	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA		0.5		%
f_{OSC}	Oscillator Frequency			1		MHz
CLKIN	CLKIN Threshold			0.7		V

Note (1) refers to system board test parameters, and note (2) refers to design guarantee parameters：

- In DCM mode, the output voltage ripple increases. It is recommended to configure it for CCM mode;
- For input and output capacitor selection, ceramic capacitors are recommended. Using only ordinary tantalum capacitors may result in excessive voltage ripple or instability. In the typical application recommended ceramic capacitor configuration, additional tantalum capacitors can be added;

● Each VIN input capacitor is a 22μF ceramic capacitor. An additional large-capacity electrolytic capacitor or tantalum capacitor can also be added to improve the transient characteristics of the input power supply. Adding an additional 100nF input capacitor can filter high-frequency noise; no additional RC filter circuit is needed from SVIN to PVIN. For applications requiring high low-temperature performance or output ripple, the number of output ceramic capacitors needs to be increased. Two 47 μF ceramic capacitors are recommended per output channel. Adding an additional 100nF output capacitor can filter high-frequency noise.

● During PCB design, it is recommended to reserve a capacitor reference (CFF) between the VOUT and VFB pins. Small capacitors of 20pF to 100pF can be added as needed to improve output voltage ripple and load dynamic response.

● PCB design should follow these principles: Use copper plating for high-current paths VIN, VOUT, and GND, and maximize their area.

● Add as many vias as possible when PCB layers are connected. Place input and output capacitors close to the power module. The ground of FB resistors, SS capacitors, etc., must be connected to SGND, and then SGND should be connected to the GND plane at a single point. Place a complete ground plane layer below the components.

TYPICAL PERFORMANCE CHARACTERISTICS(Per Channel)

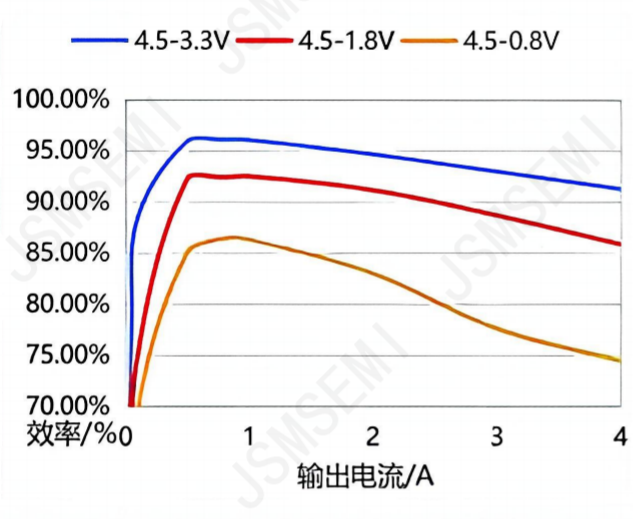


Figure 2. Efficiency curves for converting 4.5V input to 3.3V, 1.8V, and 0.8V

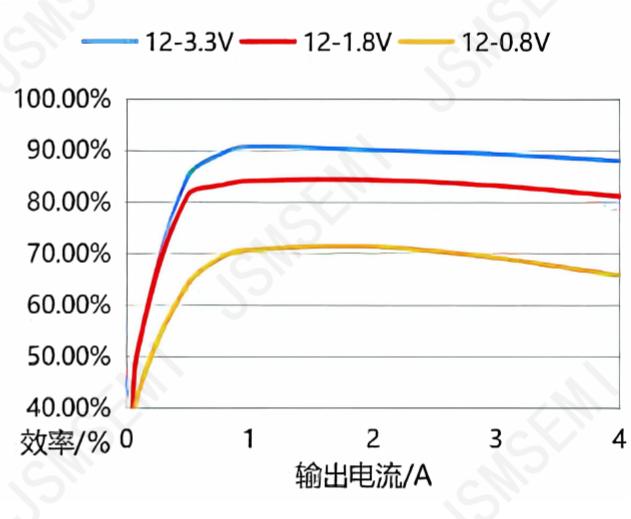


Figure 3.12V input to 3.3V, 1.8V, 0.8V efficiency curves

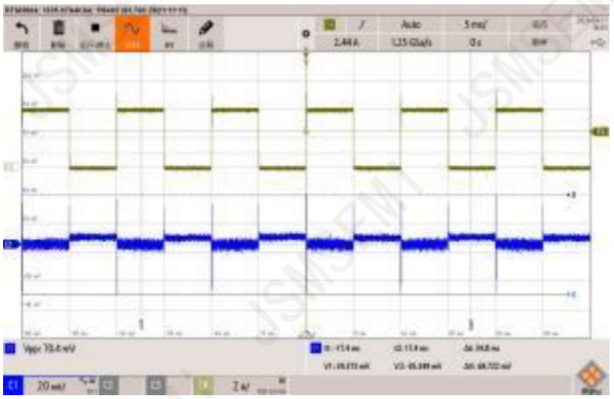


Figure 4. 5V to 1.2V, C_{OUT}=47uF × 2 ceramic capacitor, CCM I_{LOAD}=0A to 4A to 0A, output transient response

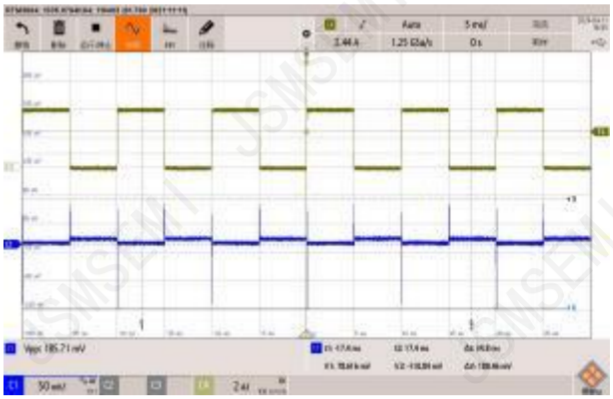


Figure 5. 5V to 3.3V, C_{OUT}=47uF × 2 ceramic capacitor, CCM I_{LOAD}=0A to 4A to 0A, output transient response

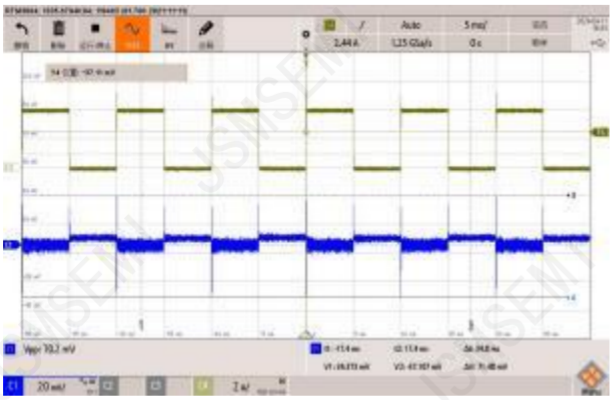


Figure 6. 12V to 1.2V, C_{OUT}=47uF × 2 ceramic capacitor, CCM I_{LOAD}=0A to 4A to 0A, output transient response

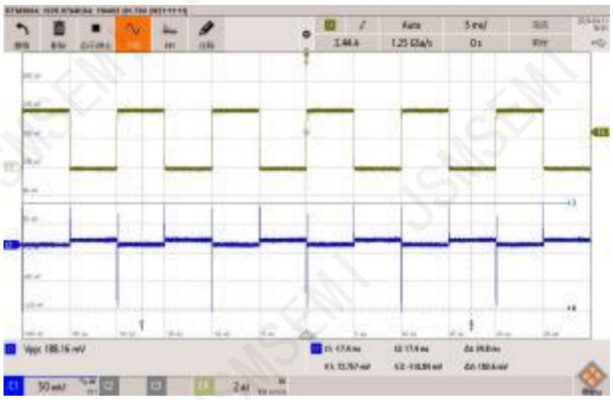


Figure 7. 12V to 3.3V, C_{OUT}=47uF × 2 ceramic capacitor, CCM I_{LOAD}=0A to 4A to 0A, output transient response

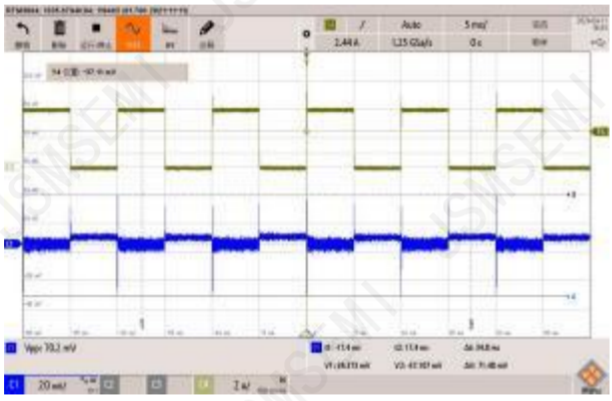


Figure 8. 16V to 12V, C_{OUT}=47uF × 2 ceramic capacitor, CCMI_{LOAD}=0A to 4A to 0A, output transient response

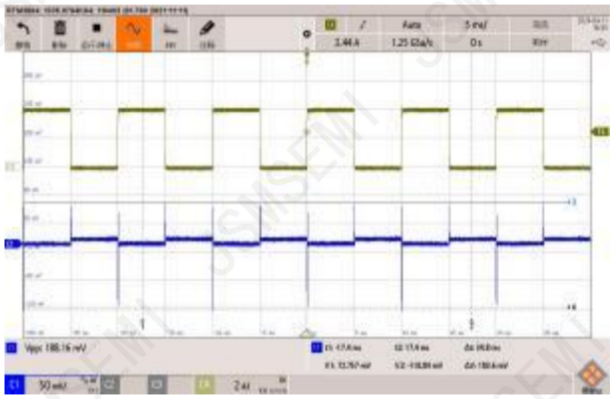


Figure 9. 16V to 3.3V, C_{OUT}=47uF × 2 ceramic capacitor, CCMI_{LOAD}=0A to 4A to 0A, output transient response

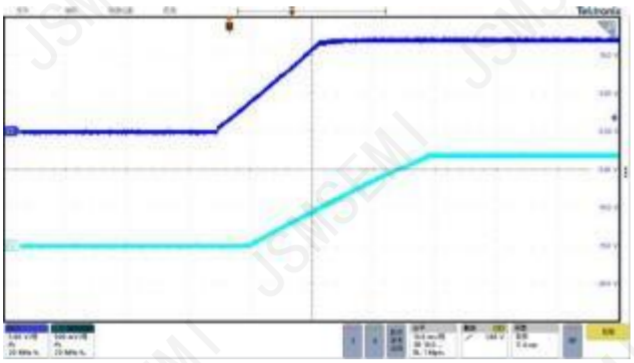


Figure 10. 12V to 1.2V, I_{LOAD}=0A, startup waveform
C1: Vin waveform, C2: V_{OUT} waveform

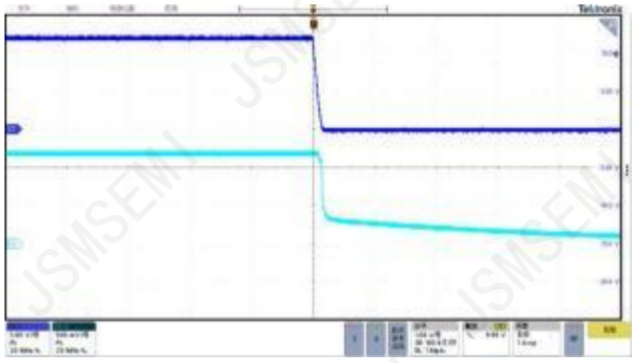


Figure 11. 12V to 1.2V, I_{LOAD}=0A,turn off waveform
C1: Vin waveform, C2: V_{OUT} waveform

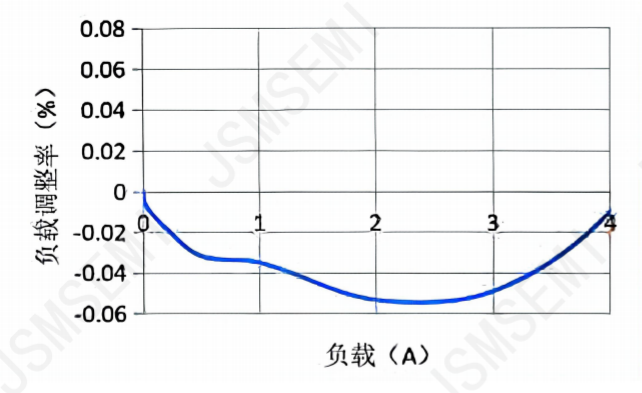


Figure 12. Vin=12V, VOUT=1.2V,
CMM ILOAD=0A to 4A, Line Regulation

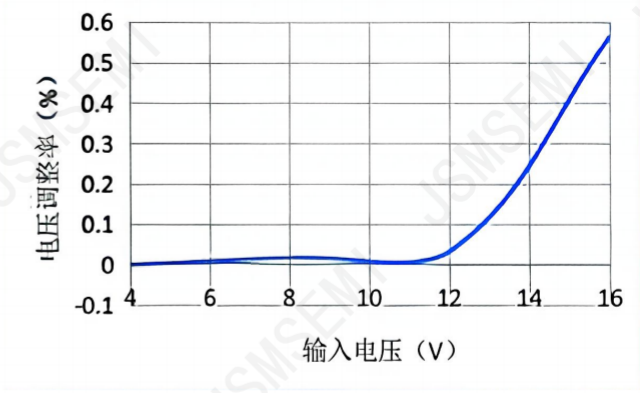


Figure 13. Vin=4V to 16V, VOUT=1.2V
CMM ILOAD=0A, Voltage Regulation

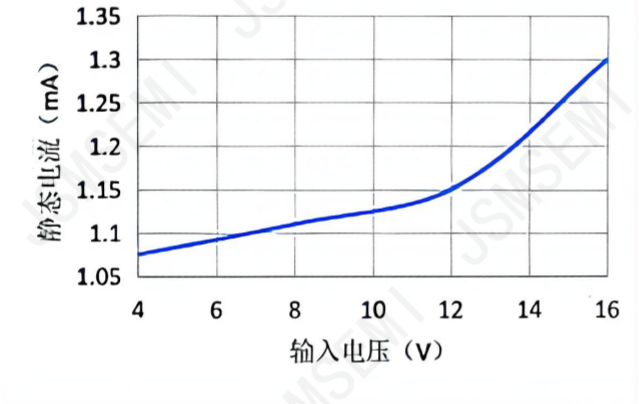


Figure 14. VRUN=2V, VOUT=1.2V, DCM ILOAD=0A,
Static Current Varies with Input Voltage

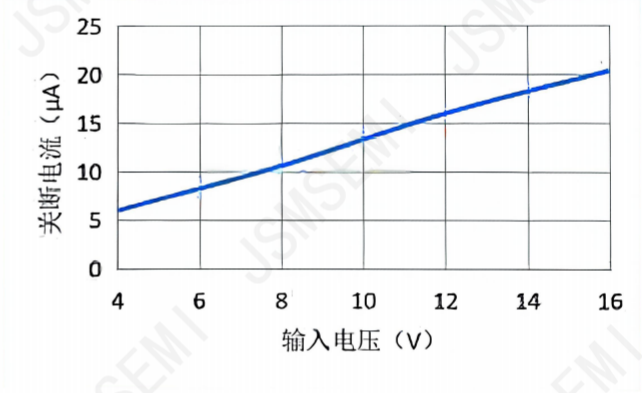


Figure 15. VRUN=0V
Turn Off Current Varies with Input Voltage

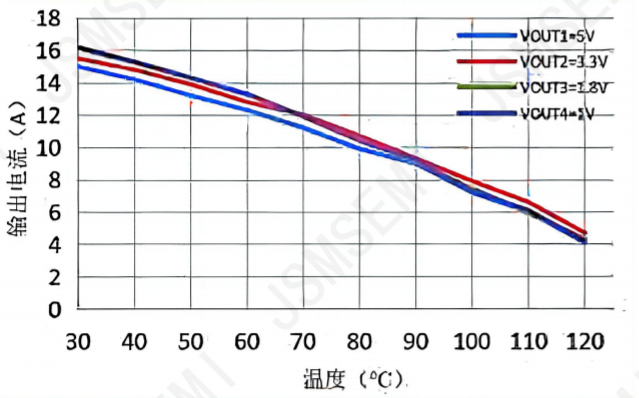


Figure 16. Vin=12V, Derating Curve
(Four Parallel Circuits)

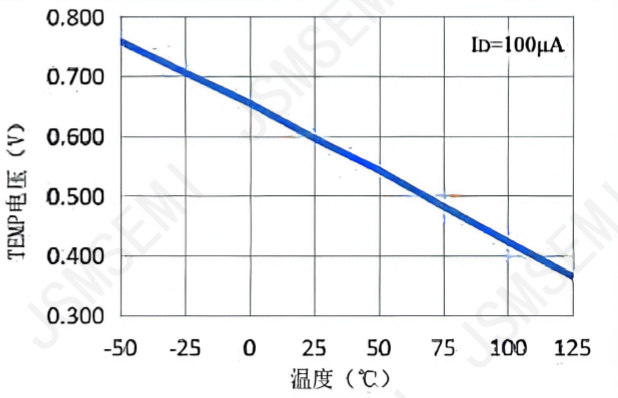


Figure 17. TEMP curve (Itemp=100uA)

BLOCK DIAGRAM

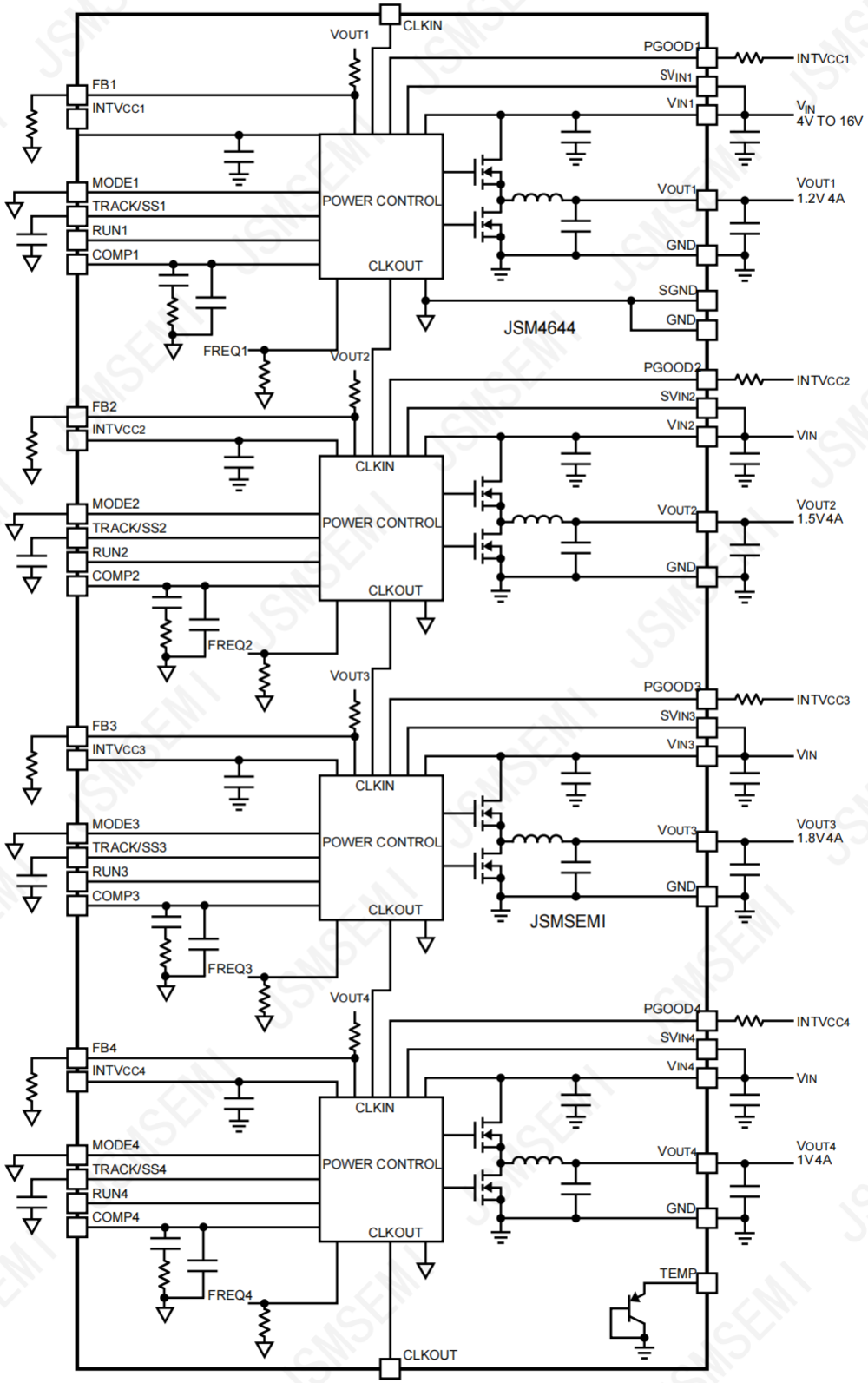


Figure 18. Functional Block Diagram

DECOUPLING REQUIREMENTS (per Channel)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4V to 16V, V_{OUT} = 1.5V)	I_{OUT} = 4A	4.7	10		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4V to 16V, V_{OUT} = 1.5V)	I_{OUT} = 4A	22	47		µF

OPERATION

The LTM4644 is a quad output standalone non-isolated switch mode DC/DC power supply. It has four separate regulator channels with each of them capable of delivering up to 4A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable from 0.6V to 5.5V via a single external resistor over 4V to 16V input voltage range. With an external bias voltage, this module can operate from an input voltage as low as 2.4V.

The LTM4644 integrates four separate constantfre quency contr olled on-time valley current mode regulators, power MOSFETs,inductors,and other supporting discrete com-ponents. The typical switching frequency is set to 1MHz. For switching noise-sensitive applications, the DC/DC Module regulator can be externally synchronized to a clock from 700kHz to1.3MHz.

With current mode control and internal feedback loop compensation,the LTM4644 module has sufficient stabil -ity margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides the flexibility of paralleling any of the separate regulator channels with accurate cur -rent sharing. With a built-in clock interleaving between each two regulator channels, the LTM4644 could easily employ a 2+2,3+1 or 4 channels parallel operation which is more than flexible in a multirail POL application like FPGA. Furthermore, the LTM4644 has CLKIN and CLK-OUT pins for frequency synchronization or polyphasing multiple devices which allow up to 8 phases cascaded to run simultaneously.

Current mode control also provides cycle-by-cycle fast current monitoring. Foldback current limiting is provided in an overcurrent condition to reduce the inductor valley current to approximately 40% of the original value when VFB drops.An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exitsa ±10% window around the regulation point. Except before the TRACK pin rises to 0.6V.

Continuous conduction mode(CCM) operation is forced during OV and UV conditions except duringstart-up when the TRACK pin is ramping up to 0.6V.Pulling the RUN pin below1.1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load cur-rents, discontinuous conduction mode(DCM) operation can be enabled to achieve higher efficiency compared to continuous conduction mode(CCM)by setting the MODE pin to SGND.The TRACK/SS pin is used for power supply tracking and soft-startprogramming.

A temperature diode is included inside the module to moni-tor the temperature of the module.

APPLICATIONS INFORMATION

VIN to VOUT Step-Down Ratios

There are restrictions in the maximum VIN and VOUT step-down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of each regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$D_{MAX} = 1 - t_{OFF(MIN)} \bullet f_{SW}$$

where $t_{OFF(MIN)}$ is the minimum off-time, 70ns typical for LTM4644,and f_{SW} is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is the minimum on-time, 40ns typical for LTM4644. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram,a 60.4k internal feedback resistor connects each regulator channel from VOUT pin to FB pin. Adding a resistor RFB(BOT) from FB pin to GND programs the output voltage:

$$R_{FB(BOT)} = \frac{60.4k}{\frac{V_{OUT}}{0.6} - 1}$$

Table 1. VFB Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
$R_{FB(BOT)}$ (k)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For parallel operation of N channels, use the following equation can be used to solve for $R_{FB(BOT)}$. Tie the VOUT and the FB and COMP pins together for each paralleled output with a single resistor to GND as determined by:

$$R_{FB(BOT)} = \frac{\left(\frac{60.4k}{N}\right)}{\left(\frac{V_{OUT}}{0.6} - 1\right)}$$

Input Decoupling Capacitors

The LTM4644 module should be connected to a low ac-impedance DC source.For each regulator channel,a 10 µF input ceramic capacitor is recommended for RMS ripple current decoupling. A bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads,traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capaci-tor or polymer capacitor.Without considering theinductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where η% is the estimated efficiency of the powermodule. I_{OUT} is the estimated maximum output current, D is the duty cycle of the switch,D=VOUT / VIN

Output Decoupling Capacitors

With an optimized high frequency,high band width design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achievelow output voltage ripple and very good transient response.Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. High frequency noise can be filtered out with magnetic beads, and low-frequency ripple can be filtered by LC filters. Multiphase operation will reduce effective output ripple as a function of the number of phases. But the output capacitance will be more a function of stability and transient response,Attention should be paid to the DC voltage drop introduced by the impedance of the filtering circuit. It is recommended to use at least two 47uF ceramic capacitors as output capacitors.

Discontinuous Conduction Mode (DCM)

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous con-duction mode(DCM) should be used by connecting the MODE pin to SGND. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode,In this mode, the output ripple will increase. It is recommended to use CCM mode.

Force Continuous Conduction Mode (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous conduction mode operation should be used.

Forced continuous opera-tion can be enabled by tying the MODE pin to INTVCC. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse.During start-up,forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4644 's output voltage is in regulation. This mode has the lowest output voltage ripple.

Operating Frequency

The operating frequency of the LTM4644 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency.The default operating frequency is internally set to 1MHz. In most ap-plications,no additional frequency adjusting is required.

If any operating frequency other than 1MHz is requiredby application, the DC/DC Module regulator can be externally synchronized to a clock from 700kHz to 1.3MHz.

Frequency Synchronization and Clock In

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±30% around the 1MHz set frequency. A pulse detection circuit is used to detect a clock on the CLKIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns. The clock high level must be above 2V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled.

Multichannel Parallel Operation

For loads that demand more than 4A of output current, the LTM4644 multiple regulator channels can be easily paralleled to provide more output current without increas-ing input and output voltage ripples. The LTM4644 has preset built-in phase shift between each two of the four regulator channels which is suitable to employ a 2+2,3+1 or 4 channels parallel operation. Table 2 gives the phase difference between regulator channels.

Table 2. Phase Difference Between Regulator Channels

CHANNEL	CH1	CH2	CH3	CH4
Phase Difference	180°	90°	180°	

Figure 19 shows a 2+2 and a 4-channels parallel concept schematic for clock phasing.

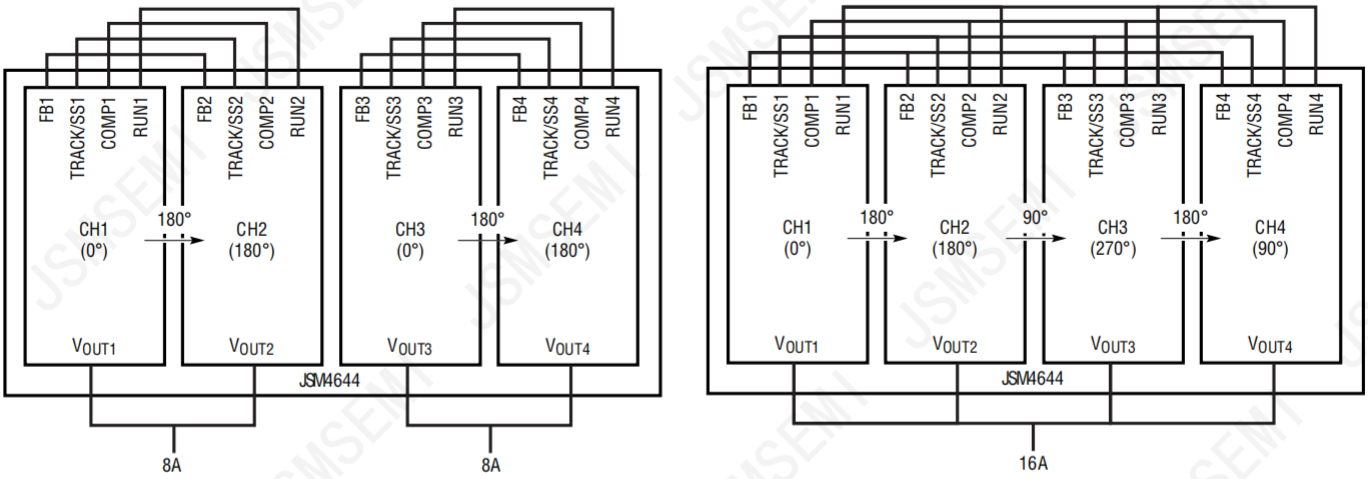


Figure 19. 2+2 and 4 Channels Parallel Concept Schematic

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors.The RMS input ripple current is reduced by,and the effective ripple frequency is multiplied by,the number of phases used(assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4644 device is an inherently current mode con-trolled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie the RUN, TRACK/SS, FB and COMP pins of each paralleling channel together.

Input RMS Ripple Current Cancellation

Figure 20 shows a graph is displayed representing the RMS ripple current reduction as afunction of the number of interleaved phases.

Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start of each regulator channel or track it to a different power supply,The external power supply voltage is divided and connected to this pin through a resistor .A capacitoron the TRACK/SS pin will program the ramp rate of the output voltage ,.An internal 2.5μA current source will charge up the external soft-start capacitor towards the $INTV_{CC}$ voltage.When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage ,When the voltage of this pin is higher than 0.6V, soft start is completed. The total soft-start time can be calculated as: (C_{SS} is an external capacitor for this pin)

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{2.5\mu A}$$

where C_{SS} is the capacitance on the TRACK/SS pin. Cur-rent foldback and forced continuous mode are disabled during the soft-start process,When N channels are connected in parallel, the TRACK/SS of all parallel channels are connected together, and the soft start capacitor is charged at the same time. The "2.5 μA" in the formula becomes "N × 2.5μA"..

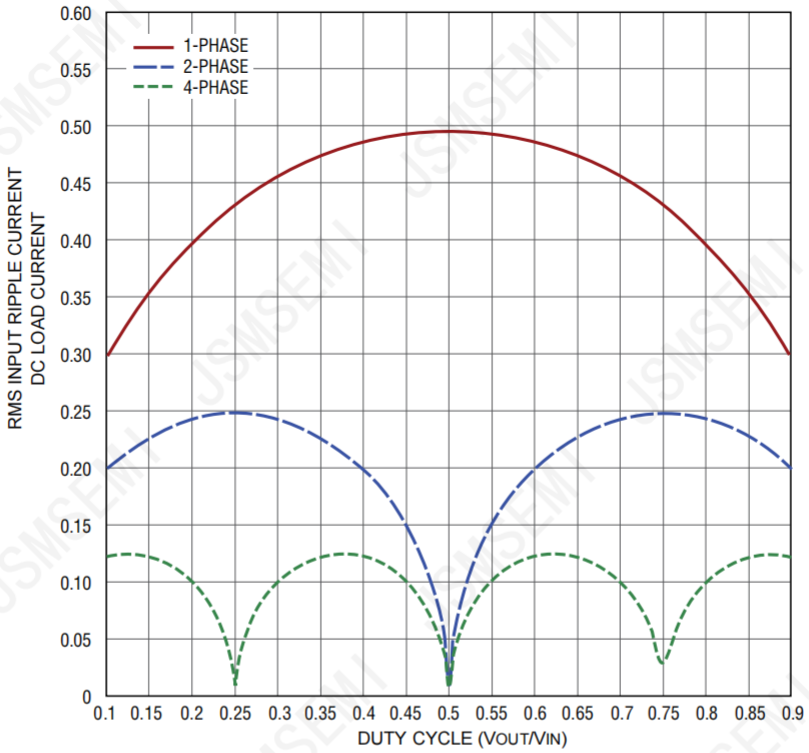


Figure 20. Normalized RMS Ripple Current for Single Phase or Polyphase Applications

Output voltage tracking can also be programmed externally using the TRACK/SS pin of each regulator channel. The output can be tracked up and down with another regula-tor. Figure 21 and Figure 22 show an example waveform and schematic of a ratiometric tracking where the slave regulator's(VOUT2, VOUT3 and VOUT4) output slew rate is proportional to the master's (VOUT1).

Since the slave regulator's TRACK/SS is connected to the master's output through a RTR(TOP)/RTR(BOT) resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below0.6V, the slave output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

Where the 60.4k is the integrated top feedback resistor and the RFB(SL) is the external bottom feedback resistor of the LTM4644. The RTR(TOP)/RTR(BOT) is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 22.

Following the upper equation, the master's output slew rate(MR) and the slave's output slew rate(SR) in volts/time is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

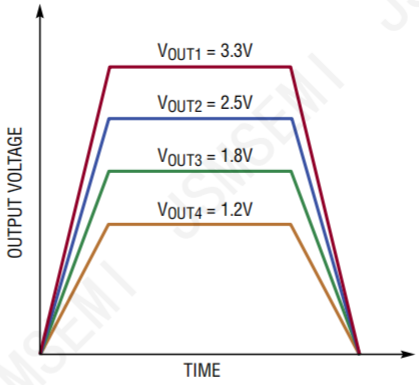


Figure 21. Output Ratiometric Tracking Waveform

Forexample,$V_{OUT(MA)}$=3.3V,MR=3.3V/24ms and $V_{OUT(SL)}$= 1.2V, SR =1.2V/24ms as V_{OUT1} and V_{OUT4} shown in Figure 22. From the equation, we could solve out that $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 13.3k is a good com-bination. Follow the same equation, we can get the same $R_{TR(TOP)}$/$R_{TR(BOT)}$ resistor divider value for V_{OUT2} and V_{OUT3}.

The TRACK pins will have the 2.5μA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The coincident output tracking can be recognized as a special ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 23. From the equation we could easily find out that, in the coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its output voltage divider.

$$\frac{R_{FB(SL)}}{R_{FB(SL)}+60.4k}=\frac{R_{TR(BOT)}}{R_{TR(TOP)}+R_{TR(BOT)}}$$

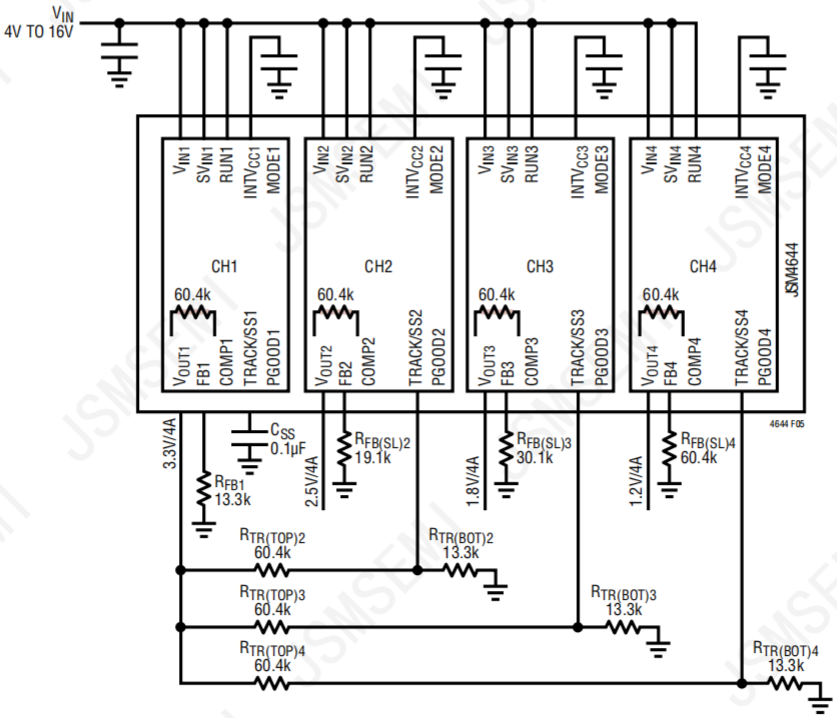


Figure 22. Output Ratiometric Tracking Schematic

For example, $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 60.4k is a good combination for coincident tracking for $V_{OUT(MA)}$= 3.3V and $V_{OUT(SL)}$ = 1.2V application.

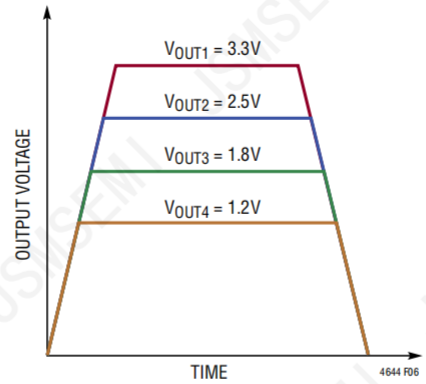


Figure 23. Output Coincident Tracking Waveform

Power Good

The PGOOD pins are open drain pins that can be used to monitor each valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. If the output feedback voltage exceeds its regulation range of ±10%, the internal overvoltage and undervoltage comparator will pull the PGOOD pin output to a low level.

Stability Compensation

The LTM4644 module internal compensation loop of each regulator channel is designed and optimized for low ESR ceramic output capacitors only application. In case of bulk output capacitors is required for output ripples or dynamic transient spike reduction, an additional 20pF to 100pF phase boost capacitoris required between the $V_{OUT}$and FB pins,Optimize output voltage ripple and transient response performance.

RUN Enable

Pulling the RUN pin of each regulator channel to ground forces the regulator into its shutdown state,turning offboth power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.65V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN pin voltage above 1.2V will turn on the entire regulator channel.Pull the RUN pin to ground, enter the off state, and turn off the power MOSFET and most of the control circuits.

Overtemperature Protection

The internal overtem perature protection monitors the junc-tion temperature of the module.If the junction temperature reaches appro ximately 160°C,both power switches will be turned off until the temperature drops about 15°C cooler,Restore normal working condition.

Low Input Application

The LTM4644 module has a separate SV_{IN} pin for each regulator channel which makes it compatible with opera-tion from aninput voltage aslow as 2.4V. The SV_{IN} pin is the signal input of the regulator control circuitry while the V_{IN} pin is the power input which directly connected to the drain of the top MOSFET. In most application with input voltage ranges from 4V to 16V, connect the SV_{IN}pin directly to the V_{IN} pin of each regulator channel. An optional filter, consisting of a resistor(1Ω to 10Ω) be-tween SV_{IN} and V_{IN} ground, can be placed for additional noiseimmunity.This filter is not necessary in most cases if good PCB layout practices are followed.In a low input voltage(2.4V to 4V) application, or to reduce power dissipation by the internal bias LDO,connect SV_{IN} to an external voltage higher than 4V with a 0.1μF local bypass capacitor. Please note, SV_{IN} voltage cannot go below V_{OUT} voltage.

Temperature Monitoring

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode voltage can be understood in the equation:

$$V_D = nV_T \ln\left(\frac{I_D}{I_S}\right)$$

where V_T is the thermal voltage (kT/q), and n, the ideality factor, is 1 for the diode connected PNP transistor being used in the LTM4644. I_S is expressed by the typical empirical equation:

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right)$$

where I_0 is a process and geometry dependent current,(I_0 is typically around 20k orders of magnitude larger than $I_S$at room temperature) and V_{G0} is the band gap voltage of 1.2V extrapolated to absolute zero or –273°C.

If we take the I_S equation and substitute into the V_D equa-tion, then we get:

$$V_D = V_{G0} - \left(\frac{kT}{q}\right)\ln\left(\frac{I_0}{I_D}\right),\ V_T = \frac{kT}{q}$$

The expression shows that the diode voltage decreases (linearly if I_0 were constant) with increasing temperature and constant diode current. Figure 23 shows a plot of $V_D$vs Temperature over the operating temperature range of the LTM4644.

If we take this equation and differentiateit with respect to temperature T, then:

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T}$$

This dV_D/dT term is the temperature coefficient equal to about –2mV/K or –2mV/°C. The equationis simplified for the first order derivation.

Solving for T, $T = -(V_{G0} - V_D)/(dV_D/dT)$ provides the temperature.

1st Example: Figure 24 for 27°C, or 300K thediodevoltage is 0.598V, thus, 300K = –(1200mV – 598mV)/–2.0 mV/K)

2nd Example: Figure 7 for 75°C, or 350K the diode voltage is 0.50V, thus, 350K = –(1200mV – 500mV)/–2.0mV/K)

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting 273 from it.

A typical forward voltage is given in the electrical charac-teristics section of the data sheet, and Figure 24 is the plot of this forward voltage. Measure this forward voltage at 27°C to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor.

Connect a resistor between TEMP and V_{IN} to set the cur-rent to 100µA.

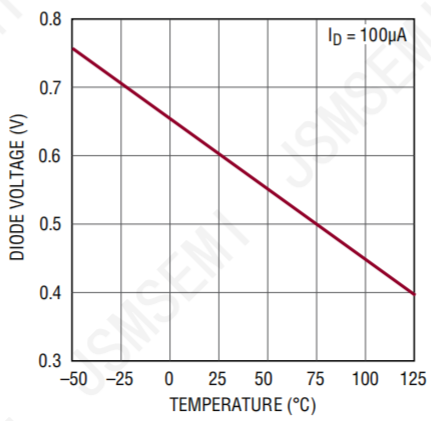


Figure 24. Diode Voltage V_D vs Temperature T(°C)

Power Derating

The internal junction temperature can be monitored by injecting approximately 100μA of current into the TEMP pin and observing the temperature change of the VTEMP voltage. During long-term steady-state operation, it is recommended that the internal temperature not exceed 125°C; during short-term peak power output, the case temperature should ideally not exceed 125°C.

The derating curve takes into account the increase in power losses with varying ambient temperature. While allowing the ambient temperature to rise, the junction temperature is maintained near 125°C by reducing the output current or power. As the ambient temperature rises, reducing the output current will reduce the module's internal losses. Subtracting the operating ambient temperature from the detected junction temperature of 125°C will determine the permissible module temperature rise. The following chart provides a partial reference derating curve for the LTM4644:

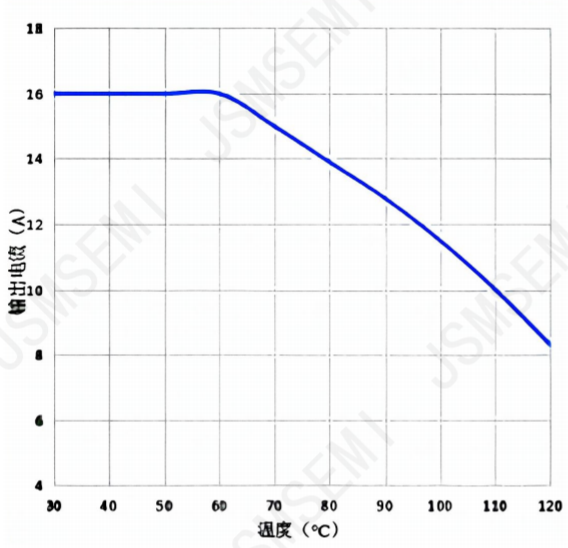


Figure 25. Four-channel Parallel Connection, CCM, 5V~1V Output Reference Derating Curve

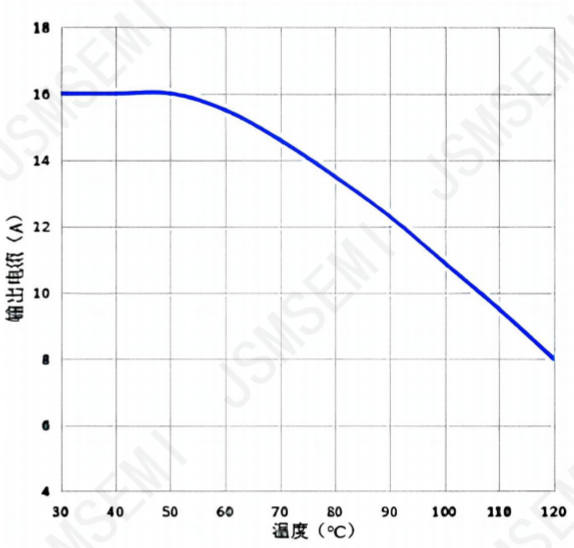


Figure 26. Four-channel Parallel Connection, CCM, 5V~1.5V Output Reference Derating Curve

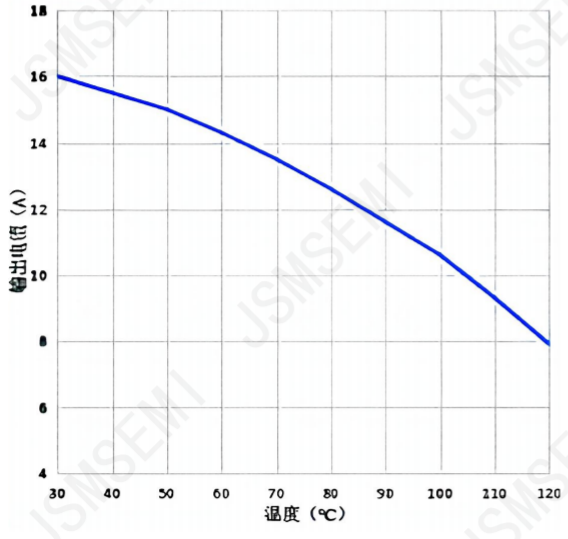


Figure 27. Four-channel Parallel Connection, CCM, 5V~3.3V Output Reference Derating Curve

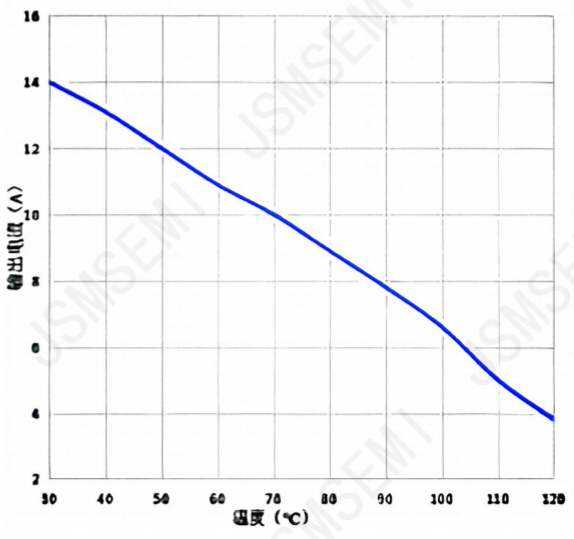


Figure 28. Four-channel Parallel Connection, CCM, 12V~5V Output Reference Derating Curve

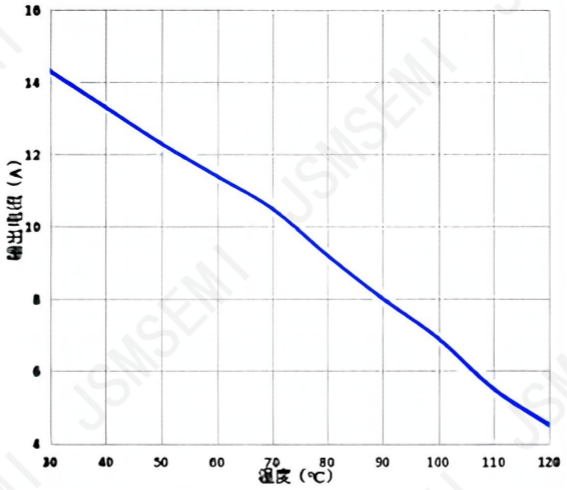


Figure 29. Four-channel Parallel Connection, CCM, 12V~3.3V Output Reference Derating Curve

TYPICAL APPLICATIONS

For the typical LTM4644 application circuit, external component selection is primarily determined by the input voltage, output voltage, and maximum load current.

Considerations

(1) The LTM4644 modules do not provide galvanic isolation from VIN to VOUT. There is no internal fuse. If required,a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

(2) In cases where a large output capacitor is required to reduce dynamic transient spikes, an additional 20pF to 100pF feedforward capacitor is needed between the VOUT and FB pins. It is recommended to add one 20pF feedforward capacitor to each output.

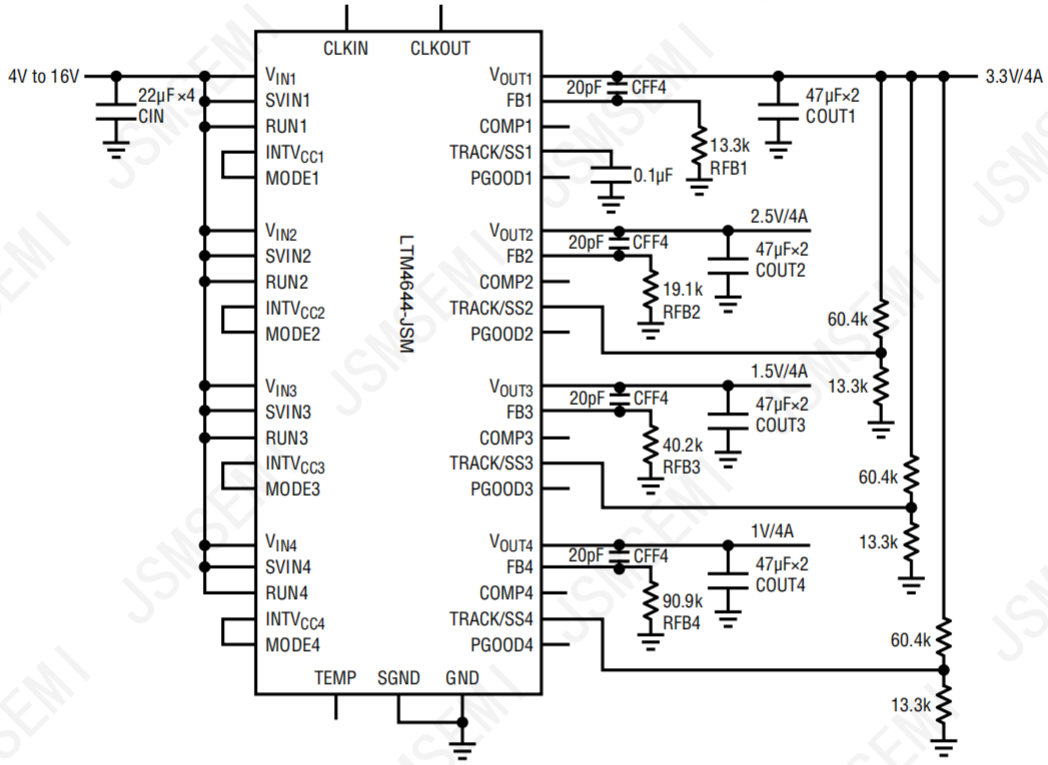


Figure 30. 4V to 16V Input, Quad 1.2V, 1.5V, 2.5V and 3.3V Output with Tracking

VIN	VOUT	CIN	COUT(Per Channel)	RFB	CFF	CCOMP
5V	0.6V	22uF×4	47uF×2	N.C	20pF	N/A
12V	0.6V		47uF×2	N.C	20pF	N/A
5V	1.0V		47uF×2	90.9kΩ	20pF	N/A
12V	1.0V		47uF×2	90.9kΩ	20pF	N/A
5V	1.2V		47uF×2	60.4kΩ	20pF	N/A
12V	1.2V		47uF×2	60.4kΩ	20pF	N/A
5V	1.5V		47uF×2	40.2kΩ	20pF	N/A
12V	1.5V		47uF×2	40.2kΩ	20pF	N/A
5V	1.8V		47uF×2	30.2kΩ	20pF	N/A
12V	1.8V		47uF×2	30.2kΩ	20pF	N/A
5V	2.5V		47uF×2	19.1kΩ	20pF	N/A
12V	2.5V		47uF×2	19.1kΩ	20pF	N/A
5V	3.3V		47uF×2	13.3kΩ	20pF	N/A
12V	3.3V		47uF×2	13.3kΩ	20pF	N/A
12V	5.0V		47uF×2	8.25kΩ	20pF	N/A

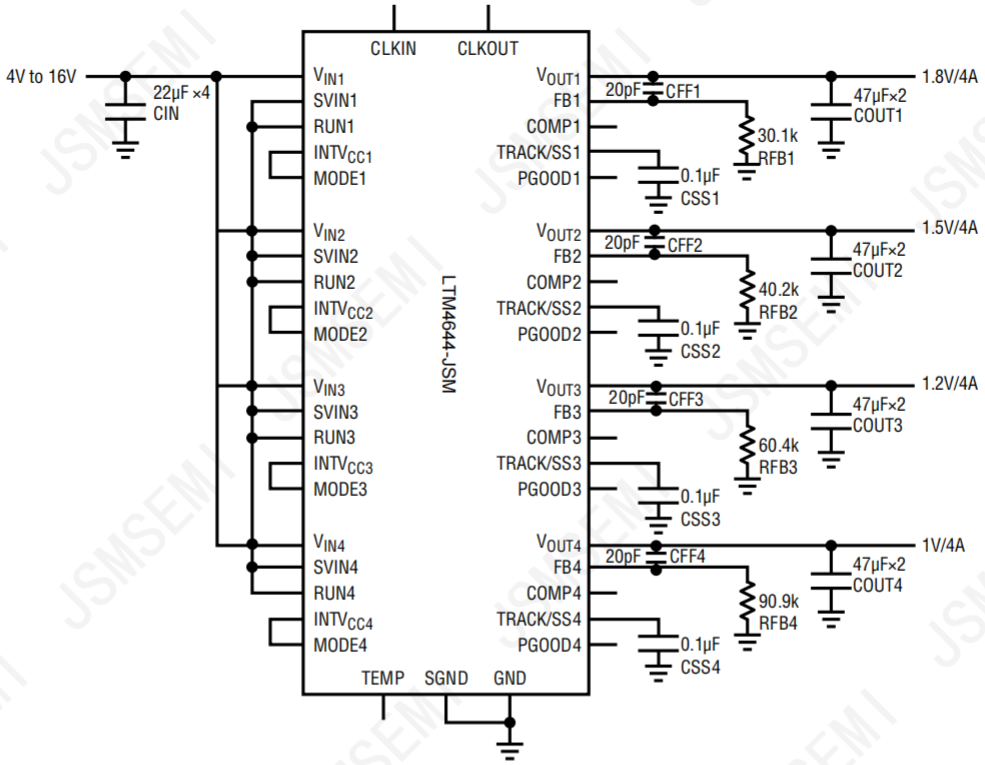


Figure 31. 4V to 16V Input, Quad 1V, 1.2V, 1.5V, 1.8V Output

VIN	VOUT	CIN	COUT(Per Channel)	RFB	CFF	CCOMP
5V	0.6V	22uF×4	47uF×2	N.C	20pF	N/A
12V	0.6V		47uF×2	N.C	20pF	N/A
5V	1.0V		47uF×2	90.9kΩ	20pF	N/A
12V	1.0V		47uF×2	90.9kΩ	20pF	N/A
5V	1.2V		47uF×2	60.4kΩ	20pF	N/A
12V	1.2V		47uF×2	60.4kΩ	20pF	N/A
5V	1.5V		47uF×2	40.2kΩ	20pF	N/A
12V	1.5V		47uF×2	40.2kΩ	20pF	N/A
5V	1.8V		47uF×2	30.2kΩ	20pF	N/A
12V	1.8V		47uF×2	30.2kΩ	20pF	N/A
5V	2.5V		47uF×2	19.1kΩ	20pF	N/A
12V	2.5V		47uF×2	19.1kΩ	20pF	N/A
5V	3.3V		47uF×2	13.3kΩ	20pF	N/A
12V	3.3V		47uF×2	13.3kΩ	20pF	N/A
12V	5.0V		47uF×2	8.25kΩ	20pF	N/A

Notes:
1. The CIN capacitors are 22uF x 4 ceramic capacitors. The soft-start capacitor CSS is typically 100nF;
2. In practical applications, other combinations of ceramic capacitors with different capacitance values can be used for the input and output capacitors, but it is recommended that the total amount not be lower than the recommended value in the table, and it can be increased;
3. "N/A" indicates that it is not installed by default, but it is recommended to reserve the reference number when designing the PCB for debugging.

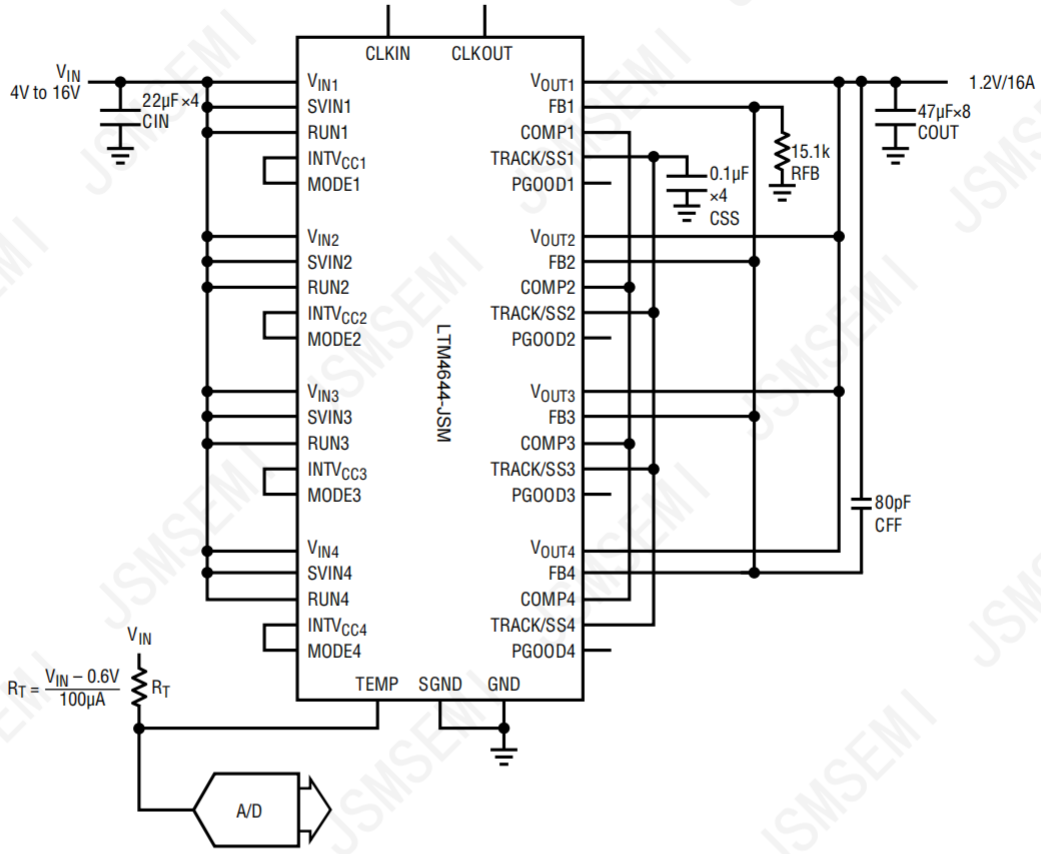


Figure 32. 4V to 16V Input, 4-Phase, 1.2V at 16A Design with Temperature Monitoring

VIN	VOUT	CIN	COUT(Per Channel)	RFB	CFF	CCOMP
5V	0.6V	22uF×4	47uF×8	N.C	80pF	N/A
12V	0.6V		47uF×8	N.C	80pF	N/A
5V	1.0V		47uF×8	22.7kΩ	80pF	N/A
12V	1.0V		47uF×8	22.7kΩ	80pF	N/A
5V	1.2V		47uF×8	15.1kΩ	80pF	N/A
12V	1.2V		47uF×8	15.1kΩ	80pF	N/A
5V	1.5V		47uF×8	10kΩ	80pF	N/A
12V	1.5V		47uF×8	10kΩ	80pF	N/A
5V	1.8V		47uF×8	7.6kΩ	80pF	N/A
12V	1.8V		47uF×8	7.6kΩ	80pF	N/A
5V	2.5V		47uF×8	4.8kΩ	80pF	N/A
12V	2.5V		47uF×8	4.8kΩ	80pF	N/A
5V	3.3V		47uF×8	3.3kΩ	80pF	N/A
12V	3.3V		47uF×8	3.3kΩ	80pF	N/A
12V	5.0V		47uF×8	2.1kΩ	80pF	N/A

Notes:

1. The CIN capacitors are 22uF x 4 ceramic capacitors. The soft-start capacitor CSS is typically 100nF x 4 ;
2. In practical applications, other combinations of ceramic capacitors with different capacitance values can be used for the input and output capacitors, but it is recommended that the total amount not be lower than the recommended value in the table, and it can be increased;
3. "N/A" indicates that it is not installed by default, but it is recommended to reserve the reference number when designing the PCB for debugging.

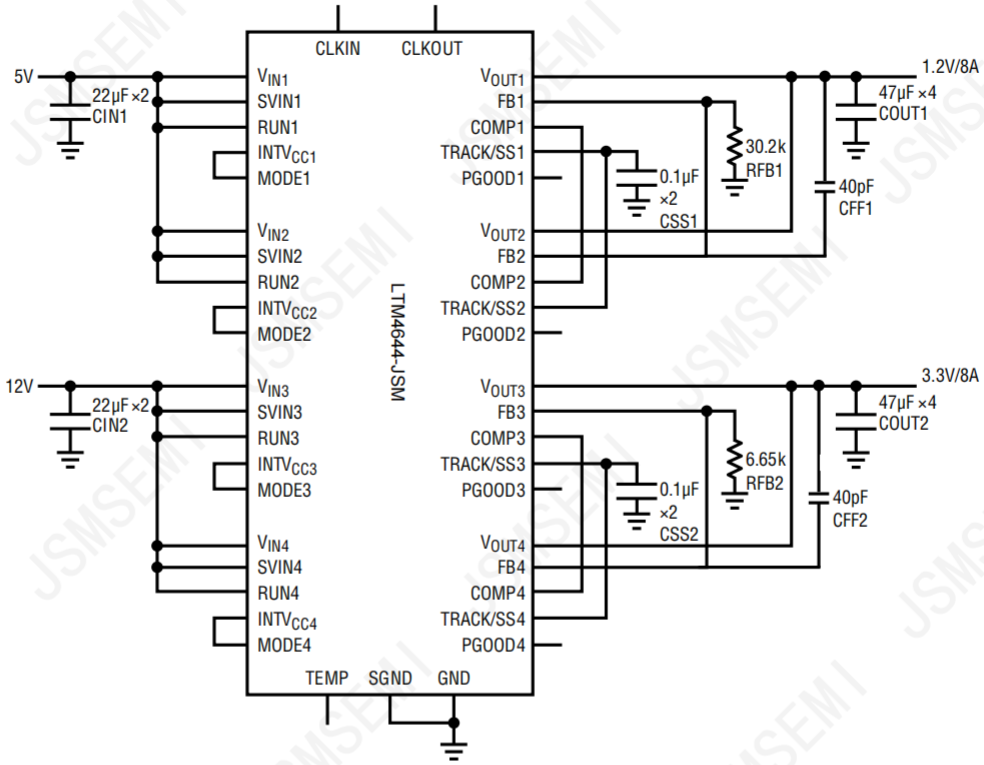


Figure 33. 12V and 5V Two Separate Input Rails, 1.2V at 8A and 3.3V at 8A Output

VIN	VOUT	CIN(Per Channel)	COUT(Per Channel)	RFB	CFF	CCOMP
5V	0.6V	22uF×2	47uF×4	N.C	40pF	N/A
12V	0.6V	22uF×2	47uF×4	N.C	40pF	N/A
5V	1.0V	22uF×2	47uF×4	45.5kΩ	40pF	N/A
12V	1.0V	22uF×2	47uF×4	45.5kΩ	40pF	N/A
5V	1.2V	22uF×2	47uF×4	30.2kΩ	40pF	N/A
12V	1.2V	22uF×2	47uF×4	30.2kΩ	40pF	N/A
5V	1.5V	22uF×2	47uF×4	20.1kΩ	40pF	N/A
12V	1.5V	22uF×2	47uF×4	20.1kΩ	40pF	N/A
5V	1.8V	22uF×2	47uF×4	15.1kΩ	40pF	N/A
12V	1.8V	22uF×2	47uF×4	15.1kΩ	40pF	N/A
5V	2.5V	22uF×2	47uF×4	9.6kΩ	40pF	N/A
12V	2.5V	22uF×2	47uF×4	9.6kΩ	40pF	N/A
5V	3.3V	22uF×2	47uF×4	6.65kΩ	40pF	N/A
12V	3.3V	22uF×2	47uF×4	6.65kΩ	40pF	N/A
12V	5.0V	22uF×2	47uF×4	4.1kΩ	40pF	N/A

Notes:

1. The CIN capacitors are 22uF x 2 ceramic capacitors. The soft-start capacitor CSS is typically 100nF x 2;
2. In practical applications, other combinations of ceramic capacitors with different capacitance values can be used for the input and output capacitors, but it is recommended that the total amount not be lower than the recommended value in the table, and it can be increased;
3. "N/A" indicates that it is not installed by default, but it is recommended to reserve the reference number when designing the PCB for debugging.

Layout Checklist/Example

The high integration of LTM4644 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout consid-erations are still necessary.

•Use large PCB copper areas for high current paths, including V_{IN1} to V_{IN4},GND,V_{OUT1} to V_{OUT4}.It helps to minimize the PCB conduction loss and thermal stress.

•Place high frequency ceramic input and output capaci-tors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.

•Place a dedicated power ground layer underneath the unit.

•To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

•Do not put via directly on the pad, unless they are capped or plated over.

•Use a separated SGND ground copper area for com-ponents connected to signal pins. Connect the SGND to GND underneath the unit,The connection point should be away from the ground terminal of the input capacitor.

•When used in parallel, the input and output capacitors should be evenly distributed across each channel and placed close to the power input and output pins of each channel.

•For high-temperature derating, it is recommended to evaluate the internal temperature of the LTM4644 via the TEMP pin to ensure it does not exceed 125°C. Excessive temperature may trigger over-temperature protection or current limiting protection due to increased on-resistance of the power transistor.

•If a jumper resistor or ferrite bead is used between V_{OUT} and the downstream load, it should be placed after the large-capacity output capacitor of the LTM4644 to ensure that the LTM4644 always has a low-impedance connection to the large-capacity output capacitor.

•The maximum withstand voltage of the PGOOD pin is $INTV_{CC}$. Do not pull it up to a power rail exceeding 3.6V. Usually, pulling it up to the $INTV_{CC}$ pin is sufficient.

•For parallel modules,tie the V_{OUT},V_{FB},and COMP pins together.Use an internal layer to closely connect these pins together.The TRACK/SS pins must not be left floating to avoid excessive inrush current during startup. A 100nF soft-start capacitor (single-channel) is generally recommended.

•Bring out test points on the signal pins for monitoring. Figure 34 gives a good example of the recommended layout.

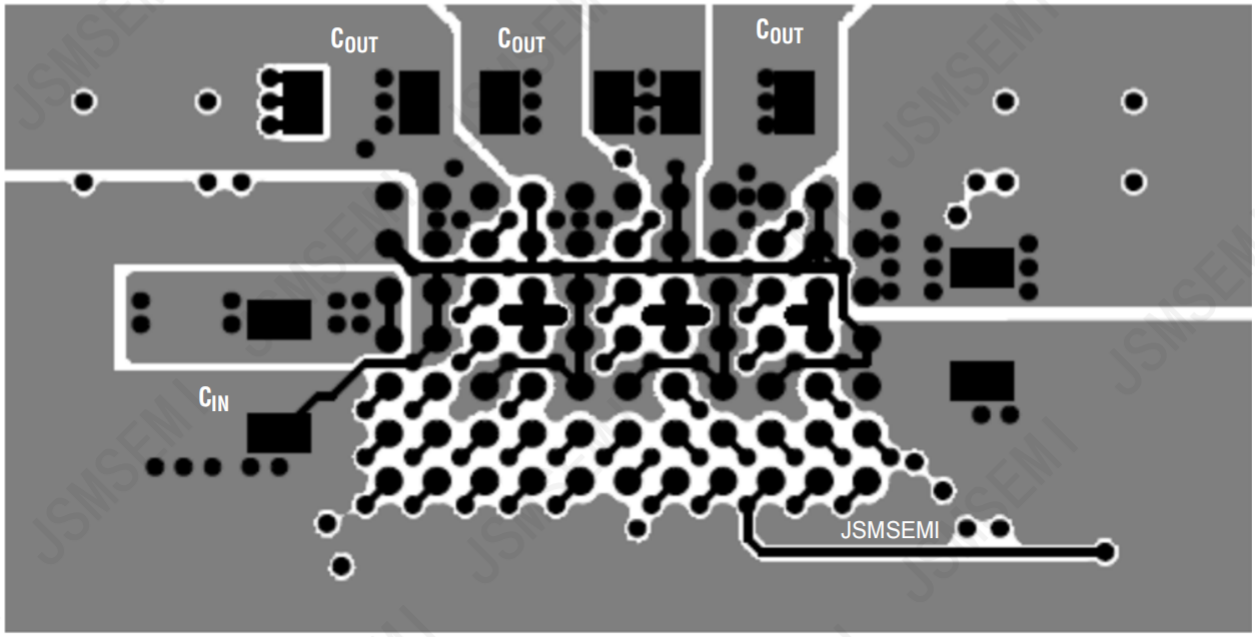
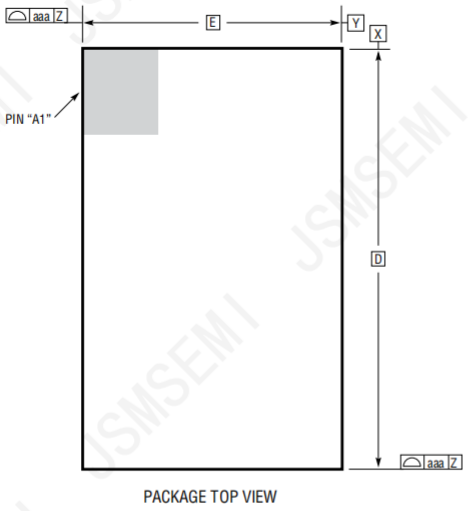


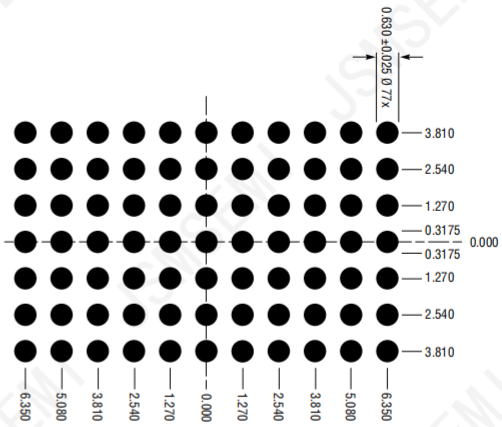
Figure 34. Recommended PCB Layout

Package Information

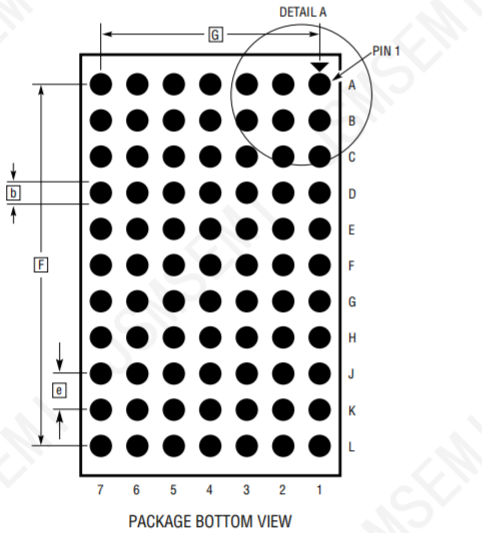
BGA-77(9mmx15mmx5.01mm)



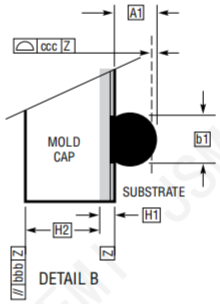
PACKAGE TOP VIEW

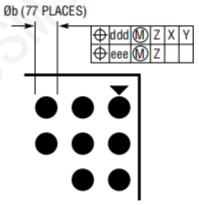


RECOMMENDED LAND PATTERN (Unit: mm)

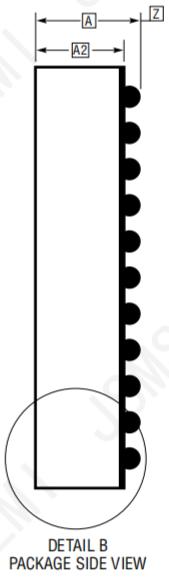


PACKAGE BOTTOM VIEW





DETAIL A



DETAIL B
PACKAGE SIDE VIEW

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D	15.00			
E	9.00			
e	1.27			
F	12.70			
G	7.62			
H1	0.36	0.41	0.46	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 77				

Revision History

Rev.	Change	Date
V1.0	Initial version	7/21/2022

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