OptiMOS™ 7 25 V – Optimized for soft- and hard-switching topologies

About this document

Scope and purpose

This application note is a comprehensive introduction to the concept of this new OptiMOS™ 7 trench power MOSFET 25 V technology and the benefits that it offers in applications.

Intended audience

The intended audiences for this document are design engineers, technicians, students, and developers of electronic systems.

OptiMOS™ family

Infineon's OptiMOS™ power MOSFETs provide best-in-class performance with increase in efficiency, power density, and cost-effectiveness. With ultra low $R_{DS(on)}$ as well as low charge for high switching frequency, they are ideally suited for applications such as:

- Intermediate bus conversion - Artificial intelligence and high-performance computing
- Industrial power supplies
- Server
- Telecom
- Information and communication technologies

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1 Introduction and motivation: OptiMOS™ 7 25 V – Application optimized

Infineon has recently introduced the latest OptiMOS™ 7 technology with the first 15 V trench power MOSFET in the industry. The OptiMOS™ 7 family is now expanding again with the introduction of the two OptiMOS™ 7 power MOSFET 25 V “application-optimized” technology variants for soft- and hard-switching topologies.

Advanced power trench MOSFET concepts have become extremely sophisticated in recent years. In certain aspects, silicon reaches its limits defined by physics, which opens the door to wide bandgap semiconductors based on GaN and SiC. However, the silicon-material system still offers many possibilities for specific optimization, especially for breakdown voltages smaller than 40 V, where silicon stays highly competitive with respect to costs, and performance.

Silicon power MOSFETs are extensively utilized in various applications, particularly within different converter topologies. These topologies can be broadly categorized into two main groups: hard-switching and soft-switching converters. For optimal performance in the application, the optimization of a MOSFET technology needs to be done according to this classification, based on a set of relevant key-characteristics. Therefore, it becomes increasingly difficult to design “general purpose” silicon power trench MOSFET technology without compromising other performance aspects like ruggedness or ease of use. The following sections elaborate in detail the approach in providing two application optimized flavors of OptiMOS™ 7 power MOSFET 25 V.

1.1 What are the challenges in the application?

Artificial Intelligence (AI) is the main driver for an ever-increasing power density improvement of power supplies. In recent years, it has become increasingly evident that the power demand of tensor processing units (TPU) and graphics processing units (GPU) are not following “Moore’s law” anymore and that the demand is increasing at a much faster pace compared to conventional computing (CPU) [1], as illustrated in Figure 1.

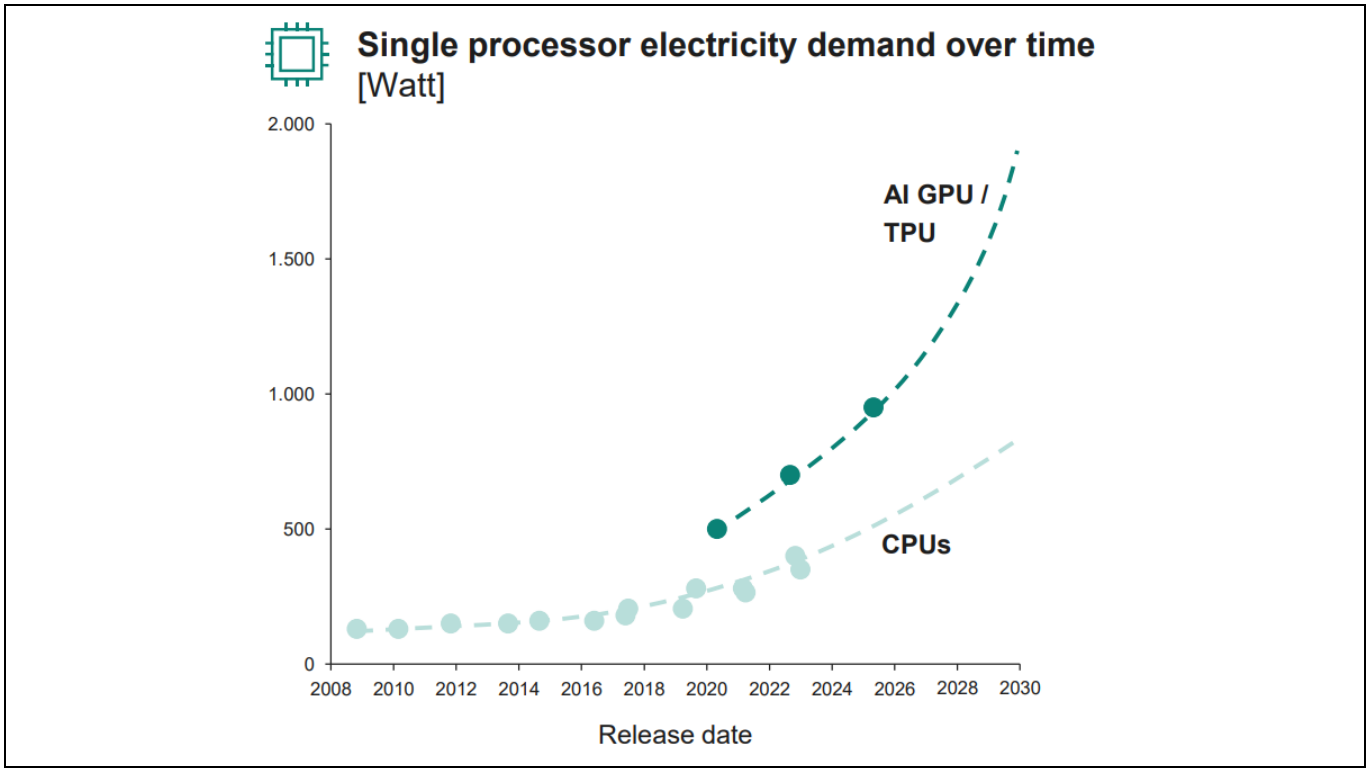


Figure 1 Single processor power demand over time [2]

On the other hand, recent studies show that the efficiency improvement rate of high-performance computers, known as “Koomey's Law”, significantly slowed down in the time range from 2008 to 2023, i.e., energy efficiency doubles now every 2.29 years instead of every 1.57 years as in the period before [3].

Two key challenges arise from this situation:

- The complexity of supplying processing units on a board is increasing, driven by the need to manage thermal performance, transient response, power supply stability, reliability, and limited board space
- The growth of power consumption in datacenters is outpacing the rate of efficiency improvements, as described by Koomey's Law. This means that despite advances in energy-efficient technologies, the overall energy consumption of datacenters is still increasing

US datacenters consumed 4% of the annual electricity generation in 2023, according to an estimate by the Electric Power Research Institute (EPRI). This number is projected to increase to 9% of the domestic load in the coming years. Globally, the concentration of demand is also evident, with data centers projected to make up almost one-third of Ireland's total electricity demand by 2026 [4].

As datacenter capacity continues to grow, it poses a major challenge for sustainable growth. Each new generation of GPUs and TPUs boost computing performance, but also consumes more power than its predecessor. As a result, the total power demand increases as shipment volume rises [5].

To address these challenges, a holistic view of the energy distribution systems in datacenters is required. New standards and concepts are necessary to overcome fundamental limitations. For example, the 48 V ecosystem is a viable way to further boost system efficiency [6].

As a market leader, Infineon recognizes its responsibility to support sustainable growth of datacenter capacity by improving system efficiency in all aspects. This includes proposing new topologies and offering highly reliable discrete MOSFETs and module solutions [7].

The new application optimized OptiMOS™ 7 power MOSFET 25 V family provides specifically optimized discrete power MOSFET solutions to address the needs in hard- and soft-switching converter topologies, not only in AI and high-performance computing but also in industrial, server, storage, and telecom applications.

1.2 OptiMOS™ 7 25 V – “Application Optimized” - Push silicon power trench MOSFET technology to the limits

MOSFET technology innovation needs to go hand-in-hand with package innovation to form a “Dream Team”. Therefore, the first section elaborates on the role of the Source-Down package, followed by a description of the approach providing two application optimized flavors of OptiMOS™ 7 25 V.

1.2.1 Source-Down package

High-performance packages play a key role to push silicon power trench MOSFET technology to the limits. Infineon’s Source-Down (SD) packages mark a milestone in power MOSFET development in terms of package parasitics, thermal management, PCB routing flexibility, chip to package area, and reliability. For more information on the Source-Down package, see the dedicated application note [12].

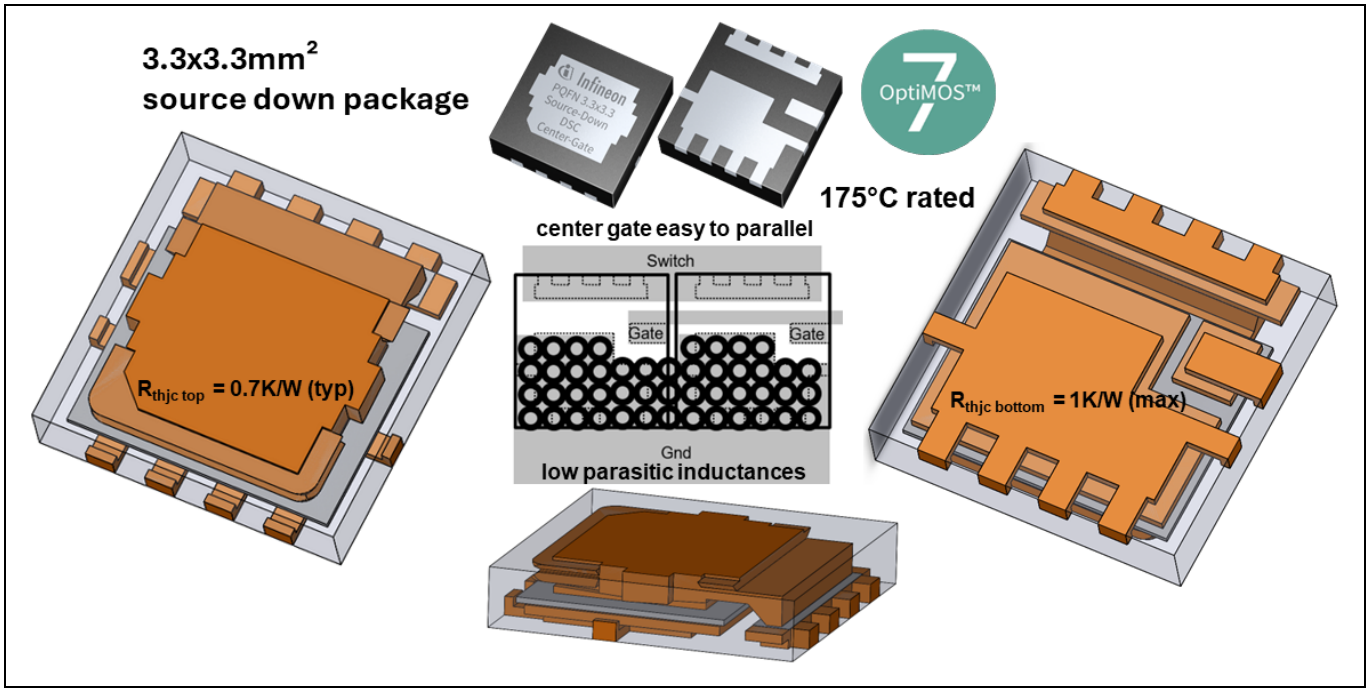


Figure 2 **OptiMOS™ 7 in 3.3 x 3.3 mm² SD DSC package: highlighted features – temperature rating, thermal performance, and possibilities for PCB-routing**

The OptiMOS™ 7 products are available in the 3.3 x 3.3 mm² SD packages. Figure 2 shows the Dual-Side-Cooled (DSC) variant with key features. Thermal management plays a pivotal role when it comes to power density increase.

Figure 3 clearly shows the improvement of the maximum power dissipation of OptiMOS™ 5 compared to OptiMOS™ 7 as a function of the case temperature. Since the introduction of the OptiMOS™ 5 25 V in the 3.3 x 3.3 mm² SD package in 2020, Infineon has continued to further improve process control of packaging [13].

An exceptionally low value of 1 K/W is guaranteed as a maximum value for the thermal resistance junction to the case bottom and 0.7 K/W thermal resistance junction to the case top. The OptiMOS™ 7 product family is rated 175°C for the maximum junction temperature, paving the way for ultra-high system reliability in high power density designs, for example, in systems where immersive cooling thermally directly connects to the MOSFET package and where access for maintenance is limited and expensive [14].

Figure 3 illustrates the positive impact on the maximum power dissipation due to the improved thermal specification of OptiMOS™ 7 in combination with a maximum junction temperature rating of T_{jmax}= 175°C.

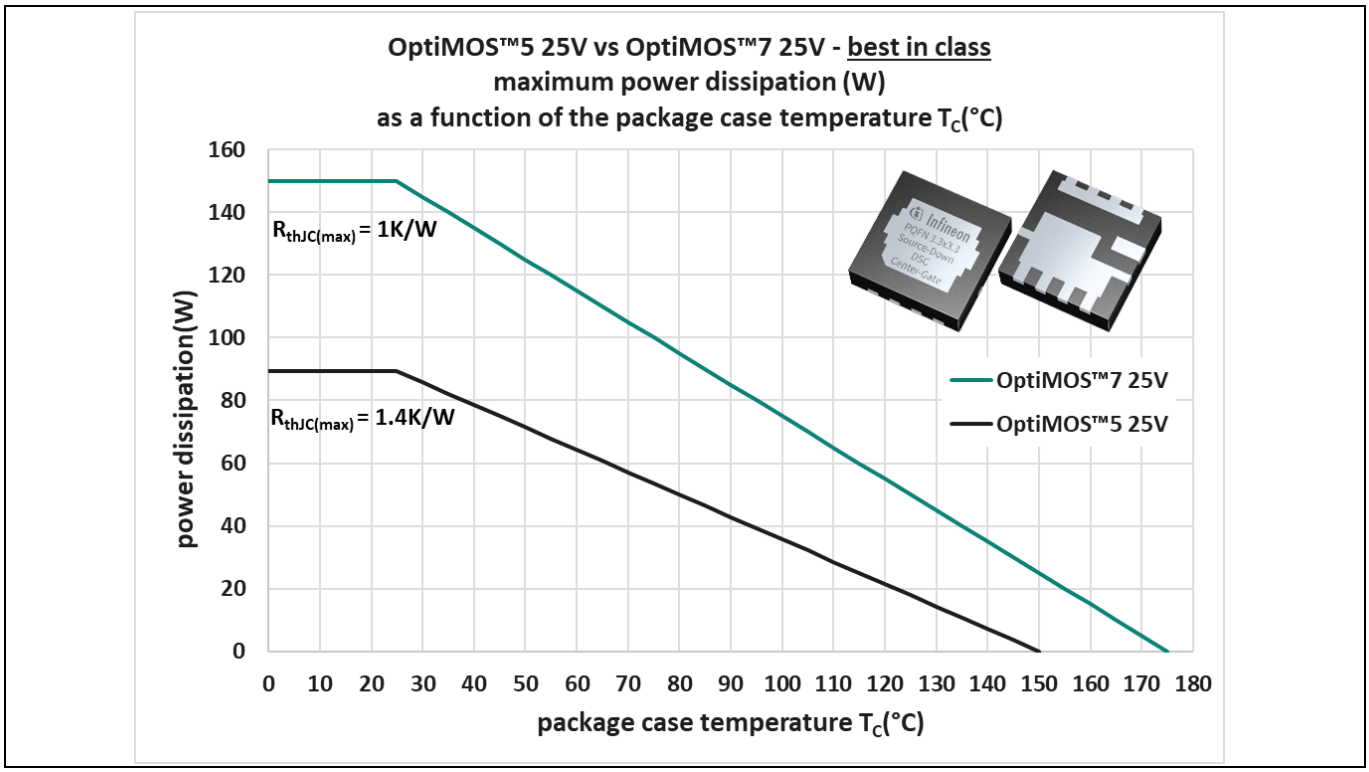


Figure 3 **Maximum power dissipation capability of OptiMOS™ 7 significantly improved compared to OptiMOS™ 6**

The pad arrangement of the package supports the shortest interconnects to the PCB to reduce loop inductances and, in consequence, voltage overshoots. The center-gate feature of the package enables easy paralleling of devices [13].

Figure 4 compares 3.3 x 3.3 mm² PQFN package variants with respect to parasitic inductances for best-in-class chip size. The parasitic inductance L_D+L_S of the SD packages (middle, right) is significantly lower, being half of that of the Drain-Down (DD) package (left). In combination with a good PCB design, fast transient switching can be achieved, pushing silicon technology to new limits [8].

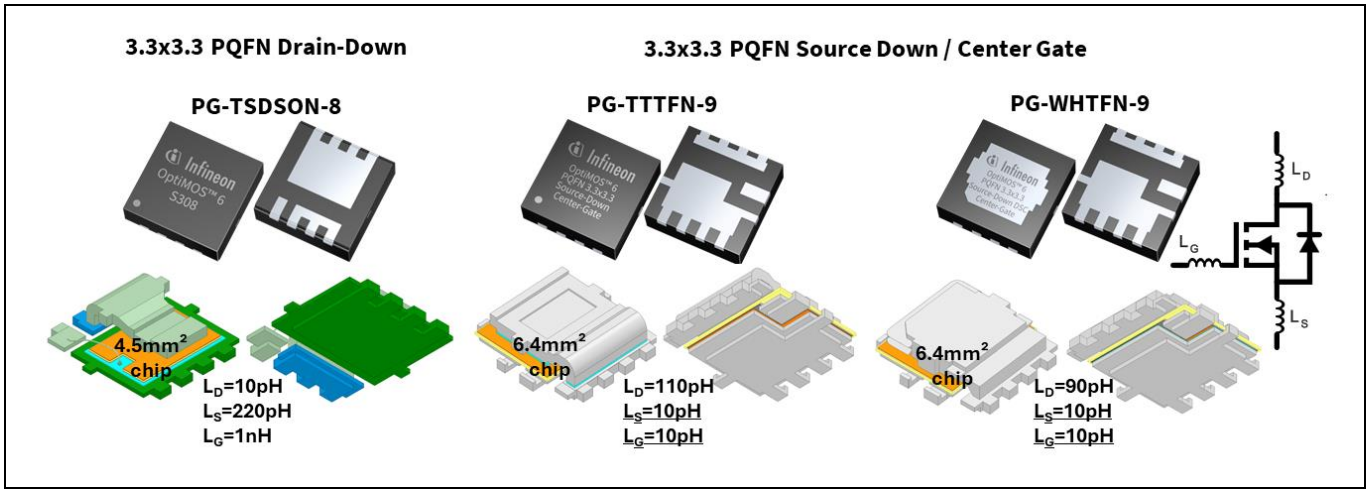


Figure 4 **3.3 x 3.3 mm² PQFN packages: the SD variant has significantly lower parasitic inductances compared to the DD package for best-in-class chip size**

The DSC SD package variant on the very right in Figure 4 has a thicker drain clip than the Bottom-Side-Cooled (BSC) SD package, reducing both parasitic drain inductance and package resistance to even lower values. For SD packages, the parasitic source L_S and gate inductance L_G are negligibly small due to the source pad orientation of the chip inside the package [9][12].

The absence of a common source inductance in the gate driver loop can be challenging in terms of induced turn-on (Section 2.1) [10]. On the other hand, very low gate inductance L_G helps to establish a strong connection to the driver for better gate potential control of the MOSFET. The role of the package parasitics in switching performance will be elaborated in more detail in Section 2.1.2.

1.2.2 OptiMOS™ 7 25 V hard- and soft-switching optimized

As mentioned in the previous section, the SD-package opens the door to fast transient switching due to ultra-low inductive package parasitics. At the same time, the highly reduced package resistance helps to fully leverage a low $R_{DS(ON)}$ of a MOSFET technology on a product level.

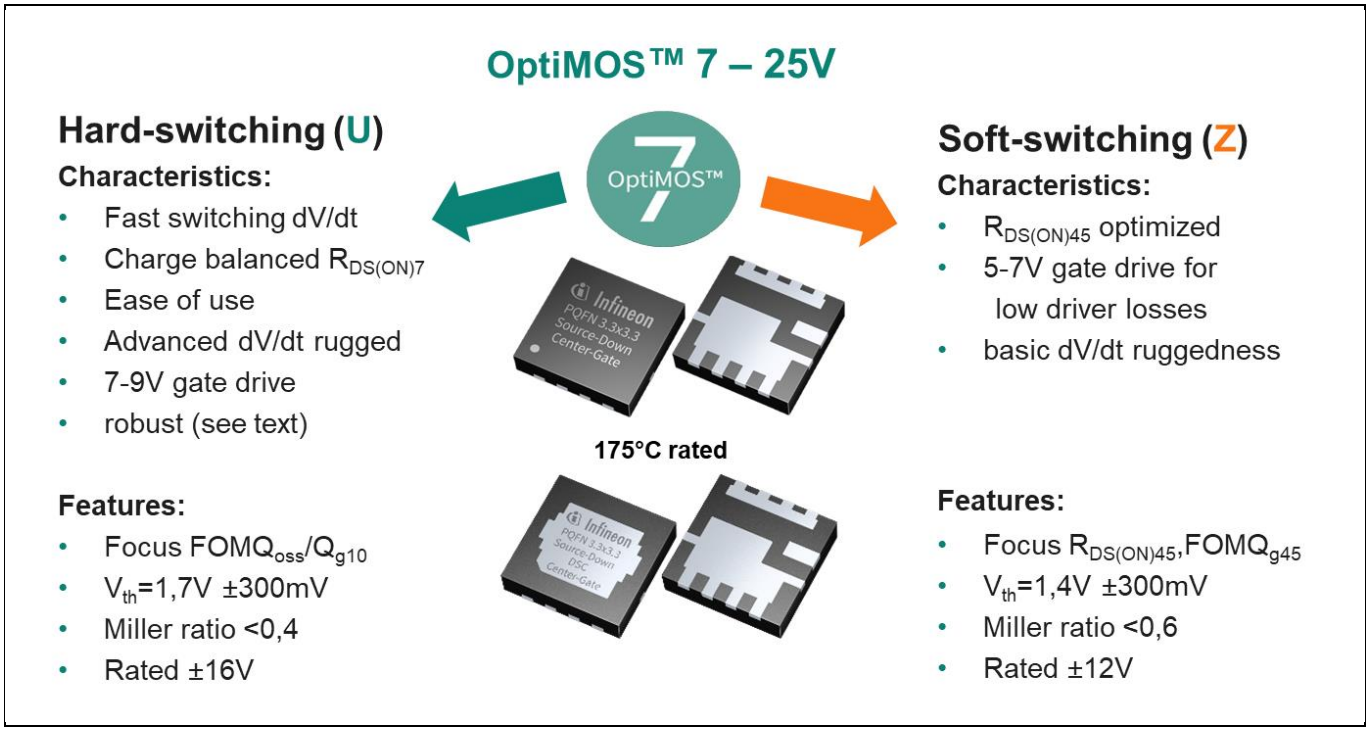


Figure 5 OptiMOS™ 7 25 V "application optimized": key characteristics and features

The design of "general purpose" silicon power trench MOSFETs becomes increasingly more challenging: to realize an ultra-low $R_{DS(ON)}$ at low gate voltages without compromising robustness and hard-commutation response. On a high level, converter topologies can be divided into two groups: hard- and soft-switching.

For optimal performance in the application, the optimization of a MOSFET technology needs to be done according to this classification, based on a set of relevant key-characteristics (Figure 5):

Hard-switching optimized technology (HSW)

- Advanced induced turn-on ruggedness: immunity against gate voltage ringing and fast rising voltage transients dV_{DS}/dt between drain and source

- Low part-to-part variation to optimize design margins and to minimize deadtime, with precise and clean switching
- $R_{DS(ON)10}$ improvement well balanced to the input and output capacitances to optimize $FOMQ_{oss}$ and $FOMQ_{g10}$
- Ringing and overshoot contained by an optimized internal snubber, with C_{oss} curve shape and R_{oss}[11]
- ±16 V extended gate voltage rating to allow gate voltage overdrive for fast charge and discharge of the gate capacitance to reduce the switching time and overlap losses
- Repetitive avalanche[1]: rugged cell design allows a countable number of repetitive avalanche events if pulse energy does not exceed a few µJ

Soft-switching optimized technology (SSW)

- Lowest $R_{DS(ON)45}$ to reduce conduction losses rendering gate voltage overdrive obsolete
- 5–7 V gate drive reduces charges, enables high frequency operation and improve gate oxide reliability
- Basic induced turn-on ruggedness: immunity against moderate voltage transients dV_{DS}/dt between drain and source
- ±12 V gate voltage rating in favor of best $R_{DS(ON)45}$ for an environment of a clean and smooth gate signal
- Repetitive avalanche[1]: basic robustness, with reduced margin compared to the hard-switching optimized technology in favor to optimize $R_{DS(ON)45}$

[1] It is not recommended to operate modern silicon trench MOSFETs under repetitive avalanche conditions. Repetitive avalanche operation leads to a drift of electrical characteristics and have the potential to impact on the lifetime.

2 OptiMOS™ 7 hard-switching optimized

Figure 6 shows two prominent examples for hard switching topologies:

- The synchronous buck converter (Figure 6 left) is a simple, universal, and generic test platform to fully assess the quality of a MOSFET technology for hard-switching (Q_{HS}) and commutation (Q_{LS})
- For the isolated converter (Figure 6 right) the MOSFETs on the secondary side can be treated in analogy to the low-side MOSFET Q_{LS} used in the synchronous buck converter on the left

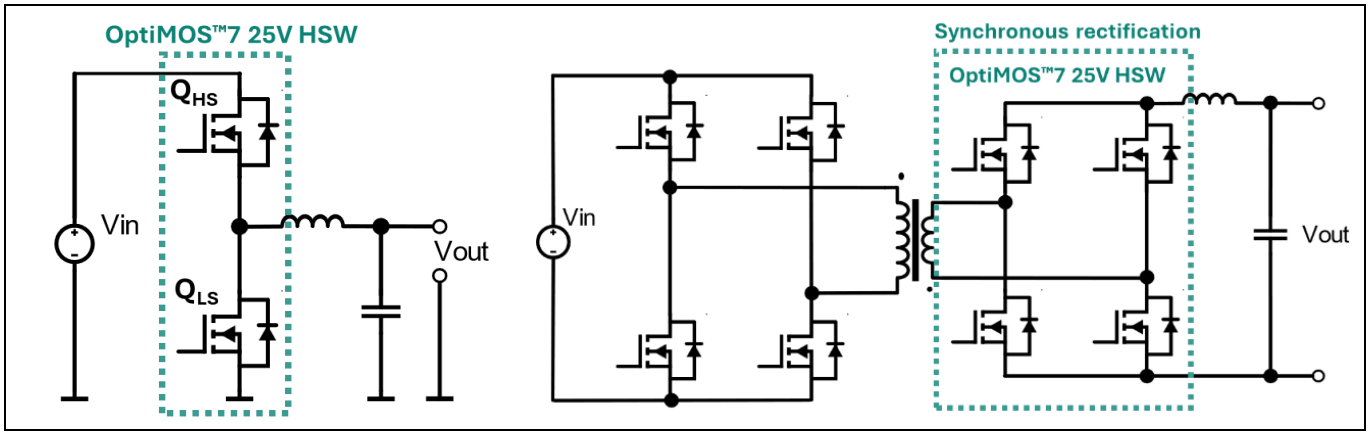


Figure 6 Two representative examples for hard switching topologies: synchronous buck converter (left) and an isolated DCDC converter with full bridge synchronous rectification (right)

The low package parasitic inductance of the SD package enables fast transient switching, beneficial to reduce overlap losses in hard switching topologies (Figure 7). To fully leverage these advantages a hard switching optimized MOSFET technology must have the right qualities to sustain fast voltage and current transients. Hence, ruggedness and ease of use are of highest priority.

Ease of use means a balanced design of the internal snubber to contain voltage overshoot and ringing, combined with a low part to part variation in volume production, to reliably avoid induced turn on, dynamic avalanche and fails in the field due to a countable number of repetitive avalanche events[1] [11].

A low part-to-part variation is the key to enable the shortest deadtimes and to optimize safety margins for the best performance. The subsequent sections will elaborate the features of OptiMOS™ 7 hard-switching optimized in more detail.

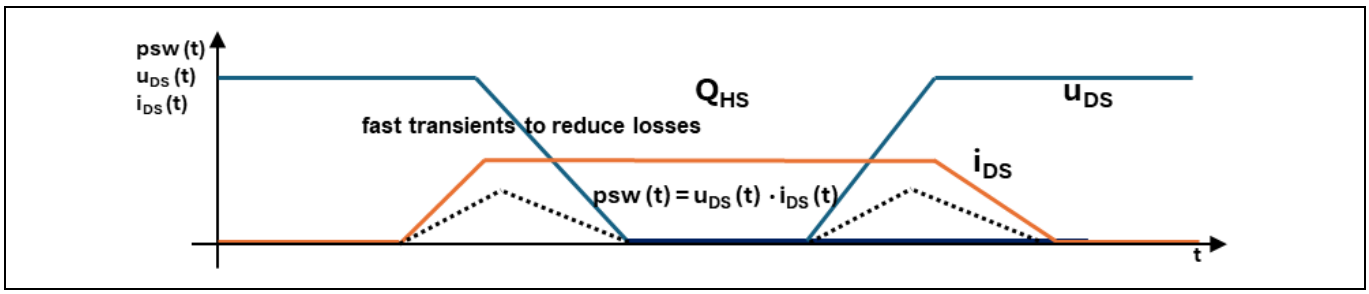


Figure 7 Illustration of the turning on/off process for a MOSFET in hard-switching configuration, e.g. the high side MOSFET in a synchronous buck converter

[1] It is not recommended to operate modern silicon trench MOSFETs under repetitive avalanche conditions. Repetitive avalanche operation leads to a drift of electrical characteristics and have the potential to impact on the lifetime.

Figure 7 shows that the transient overlap between the current and the voltage of the MOSFET should be as short as possible.

2.1 Induced turn on ruggedness

2.1.1 MOSFET basics: gate capacitances, Miller ratio, and threshold voltage

In a half-bridge configuration of MOSFETs the low- and high-side MOSFET should never be turned ON at the same time (Figure 6). By introducing a deadtime between the intermittently switching low-side MOSFET Q_{LS} and high-side MOSFET Q_{HS}, a so-called cross conduction can be avoided.
Ideally the high-side MOSFET Q_{HS} should switch as fast as possible to reduce so called overlap losses (Figure 7). On the other hand, turning on the high side MOSFET Q_{HS} fast leads to a fast voltage transient across the low side MOSFET Q_{LS}. The parasitic capacitances in the MOSFET-chip need to be considered in this case (Figure 8).

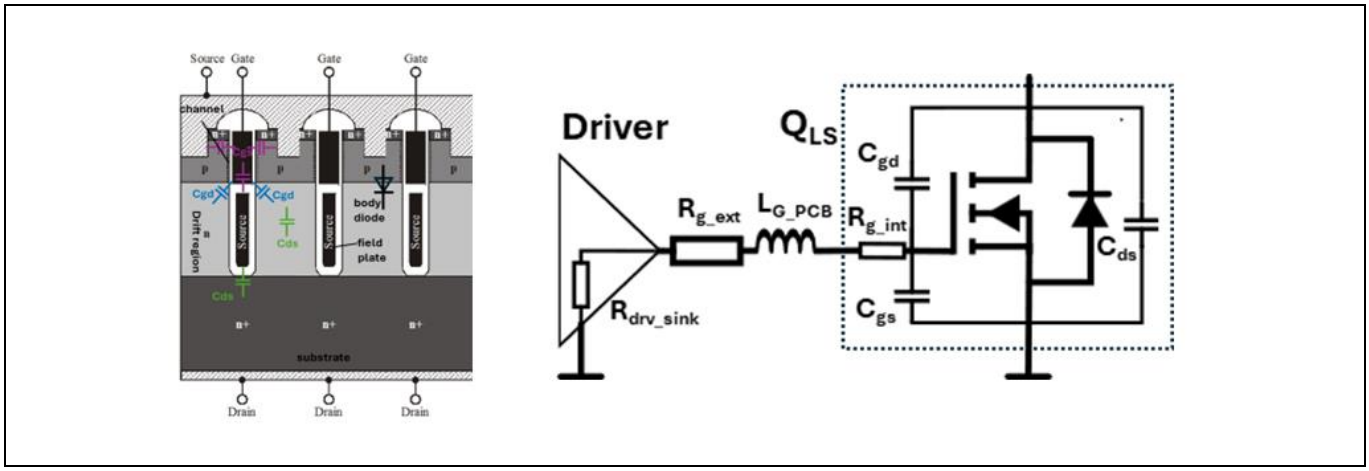


Figure 8 Left: Cross-section of a trench power MOSFET including the capacitive couplings that are present in every single MOSFET cell; Right: corresponding equivalent circuit of the MOSFET used as a low-side switch, connected to the gate driver during turn-off

The capacitance between the gate and the part of the drift region on the drain potential is the so-called Miller capacitance C_{gd}. This capacitance shows a strong dependence of the drain-source voltage, because the dielectric of this capacitor consists basically of the space charge region of the body diode. C_{gs} is defined by the overlap of the gate with the channel and field-plate on source potential (Figure 8 left).

The Miller capacitance couples the gate- to the drain-potential. Due to this capacitive coupling, fast-rising voltage transients dV_{DS}/dt pull the gate potential up. On the other hand, the gate-source capacitance C_{gs} gives support to pin the gate on source potential. The charge ratio between $Q_{gd}/Q_{gs,}$ known as the “Miller Ratio” gives an indication of the coupling strength of the drain potential to the gate.

If the gate-source potential exceeds the threshold voltage a drain current I_D starts to flow in the MOSFET (Figure 10). This effect is then called “induced turn on”, “shot-through” or “cross-conduction”. Induced turn on can be problematic with respect to several different aspects. Even spurious cross-conduction can cause EMI problems and affect reliability due to hot carrier stress, also if no clear impact on the efficiency can be seen.

The MOSFET driver controls the voltage applied between the external gate and source pin of the MOSFET (Figure 8 right). The impedance of the driver to MOSFET connection reduces the control strength of the driver on the gate local gate potential in the MOSFET cell (Figure 8 left). This impedance consists of the internal gate

resistor of the MOSFET $R_{g,int}$, an optional external gate resistor $R_{g,ext}$, the internal resistor of the gate driver Rdrv, sink and the parasitic inductance of the PCB connection LG_PCB including also the parasitics of the packages. The role of the package parasitics will by analyzed in section 2.1.2.

The parasitics in the gate loop, i.e., in the driver to MOSFET connection, limit the controllability of the local gate potential on a MOSFET-cell level (Figure 8 left). In conclusion, in case of ultrafast raising drain-source voltage transients dV_{DS}/dt the driver can only support to a certain extent to keep the gate on source potential. To mitigate this limitation, the MOSFET cell concept design should be inherently rugged against induced turn on.

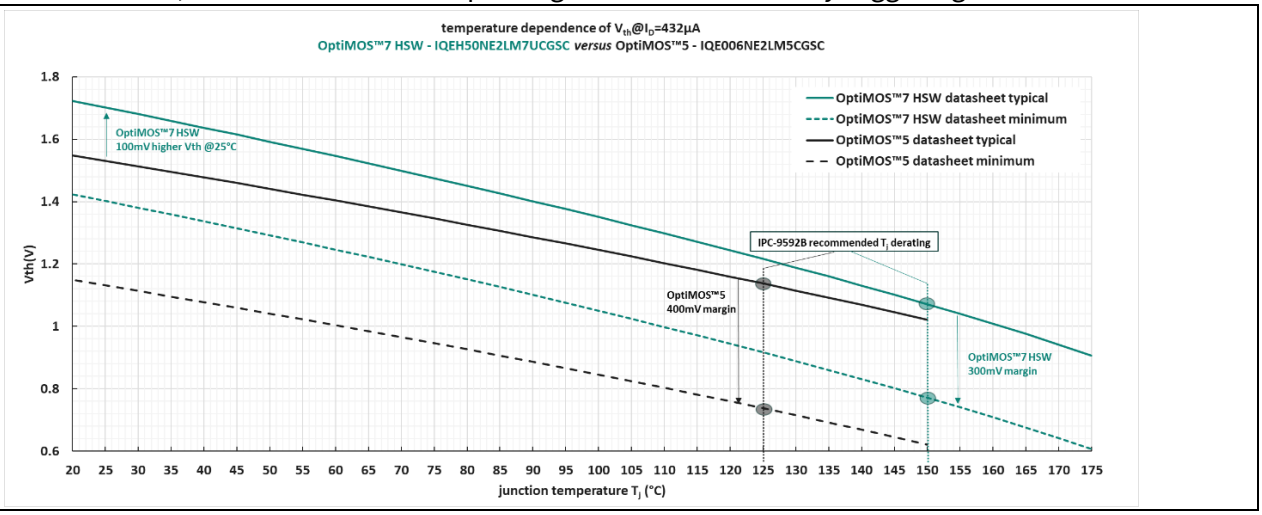


Figure 9 OptiMOS™ 7 HSW provides an improved threshold voltage margin compared to OptiMOS™ 5

Figure 9 shows that the circles mark the maximum recommended junction temperature. In combination with the excellent Miller ratio, OptiMOS™ 7 HSW achieves an “advanced induced turn on ruggedness” also at high operation temperatures.

OptiMOS™ 7 hard-switching optimized was designed with the intention to provide advanced induced turn on ruggedness over the full operation temperature range considering volume production margins (Figure 9):

- ±300 mV threshold voltage V_{th} margin, achieved by improved production process control
- 100 mV higher threshold voltage V_{th} compared to OptiMOS™ 5
- Miller ratio $Q_{gd}/Q_{gs(th)}$ = 0.52 @25°C and $Q_{gd}/Q_{gs(th)min}$ = 0.93 @150°C

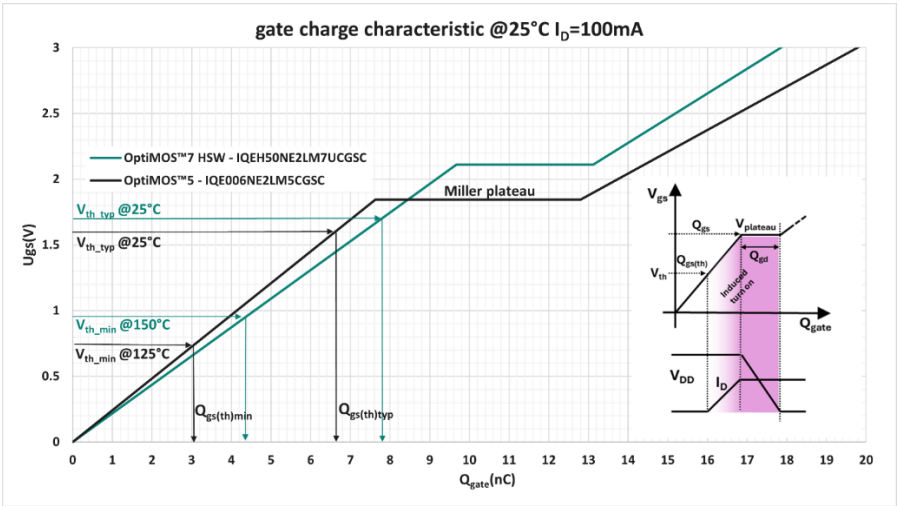


Figure 10 Gate charge characteristic $Q_{gate}(V_{th})$ as a function of the gate voltage

Figure 10 shows that a gate charge $Q_{gs(th)}$ is required that threshold voltage V_{th} is reached, the colored area in the inset on the right marks when a drain current ID starts to flow. OptiMOS™ 7 HSW was designed with a higher $Q_{gs(th)}$ over the full temperature operation range compared to OptiMOS™ 5 and with a reduced Q_{gd}, visible in the shorter miller plateau.

The threshold voltage V_{th} decreases with increasing junction temperature T_j (Figure 9). To provide best reliability, a temperature derating of 25°C with respect to the maximum junction temperature T_j is recommended referring to an industrial standard like IPC-9592B, i.e., 150°C for OptiMOS™ 7 HSW and 125°C for OptiMOS™ 5. By improving the threshold voltage margin to ±300 mV and by increasing the typical threshold voltage level by 100 mV, the minimum threshold voltage of OptiMOS™ 7 HSW at 150°C is still higher than that of OptiMOS™ 5 at 125°C.

Figure 10 compares the gate charge characteristic as a function of the gate voltage $Q_{gate(Vth)}$: OptiMOS™ 7 was designed with a higher $Q_{gs(th)}$ over the full temperature operation range compared to OptiMOS™ 5 and with a reduced Q_{gd}, visible in the shorter miller plateau. With an excellent Miller ratio OptiMOS™ 7 HSW achieves an “advanced induced turn on ruggedness” also at high operation temperatures.

The next section will elaborate on the role of the package parasitics in conjunction with induced-turn-on ruggedness.

2.1.2 Role of package parasitics for induced turn on – the basics

As already mentioned in Section 1.2.1, the SD-package exhibits exceptionally low package parasitics (Figure 4). Three aspects can be considered in this context:

- Ultra low parasitic inductance L_D+L_S - enabling fast transient switching, reducing switching losses
- Chip gate pad connected directly to PCB: parasitic package inductance L_G becomes practically 0
- Chip source pad connected directly to PCB: parasitic package inductance L_S becomes practically 0

It is important to notice for point 1 and 2, that a good PCB design becomes crucial to leverage the full advantage of OptiMOS™ 7 HSW in the SD-package. All high-frequency loops should be kept as short as possible. Differential returns for current paths to cancel the magnetic fields and reduce parasitic PCB inductance should be used to reduce overshoots and to improve the connection between driver and MOSFET.

The third point in the list requires a deeper investigation. The lack of a common source inductance L_{CSI} in the gate driver loop can be problematic in terms of induced turn on.

Figure 11 shows a model of the low side switch Q_{LS} in a synchronous buck converter considering MOSFET and package parasitics (Figure 6). The common source inductance L_{CSI} consists of L_{S_int} and L_{S_PCB}. The initial condition is defined by the state where the body diode of Q_{LS} is freewheeling the current of the buck inductance (constant current source), i.e., during the deadtime shortly before the turn on of the high side MOSFET Q_{HS}. The driver pulls the external gate connection of the MOSFET Q_{LS} to the ground.

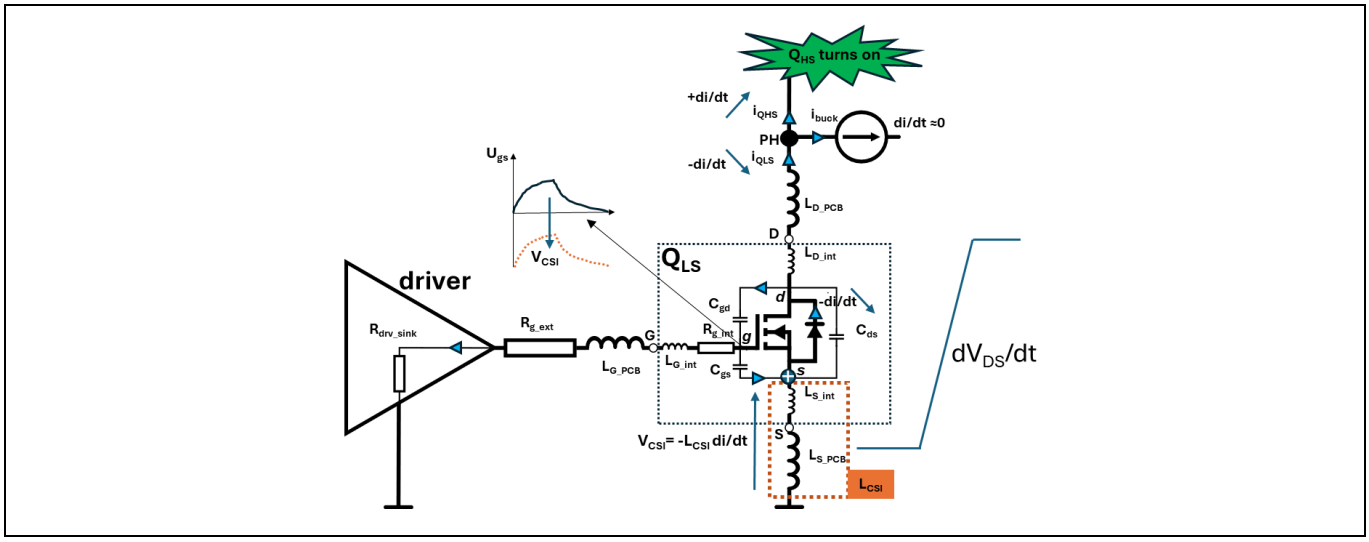


Figure 11 Processes in the low side MOSFET Q_{LS} in a synchronous buck converter when the high side MOSFET Q_{HS} is turning on

When the high side MOSFET Q_{HS} is turned on, the current i_{QLS} commutes from the body diode of the low side MOSFET Q_{LS} to the high side MOSFET Q_{HS}. The voltage across the MOSFET starts to rise at the onset of the body diode reverse recovery (symbolized by the dV_{DS}/dt). At this stage the capacitances C_{gd} and C_{ds} start to get charged, i.e., the drain-source voltage across the low side MOSFET Q_{LS} starts to increase. The capacitive voltage divider with C_{gd} and C_{gs} between drain and source defines how strong the gate-source potential is pulled up.

The current i_{QLS} through the low-side MOSFET Q_{LS} drops during the commutation of the current to the high-side MOSFET Q_{HS}. This current transient induces a voltage on the common source inductance L_{CSI}. In consequence, the source potential is rising. With the gate potential on the ground the gate-source voltage becomes negative. In conclusion, a common source inductance L_{CSI} in the gate driver loop mitigates induced turn on of the low-side MOSFET Q_{LS}.

As mentioned in the first paragraph of the section, differential returns for current paths help to establish a strong connection between MOSFET and gate driver to compensate for the effect of a low common source inductance L_{CSI}.

On top of that, OptiMOS™ 7 hard switching optimized was designed to be inherently rugged to provide advanced induced turn on ruggedness (Section 2.1.1). In combination with the high performance SD package OptiMOS™ 7 HSW is the perfect fit in applications with high dV/dt and short deadtimes to enable high switching frequency.

2.1.3 OptiMOS™ 7 hard-switching optimized: Advanced induced turn on ruggedness

The synchronous buck converter is a very useful generic testplatform to illustrate advanced induced turn-on ruggedness (Figure 6). Figure 12 shows the switching waveforms U_{ds} and U_{gs} (left) and the efficiency with the device temperature (right) of the low side MOSFET Q_{LS}.

By changing the gate resistor R_g of the low side MOSFET Q_{LS} two extreme corner cases of the damping for the gate-driver loop can be studied: over- (R_g=2Ω) and under-damping (R_g=0Ω) [8]. Both cases can be critical, because the level of the gate signal could lead to an additional voltage bias during the high side MOSFET Q_{HS} turns on.

OptiMOS™ 7 hard switching optimized illustrates implessively that no induced turn-on is visible for the overdamping case, where the gate signal does not reach the zero line cleanly: the efficiency is even slightly higher compared to the overdamped case due to reduced body-diode conduction time and device temperature at full load is 2°C lower compared to the underdamped case with R_g=0 Ω.

The advanced induced turn-on ruggedness of OptiMOS™ 7 HSW optimized enables minimum deadtime settings reducing body-diode losses and improving power density.

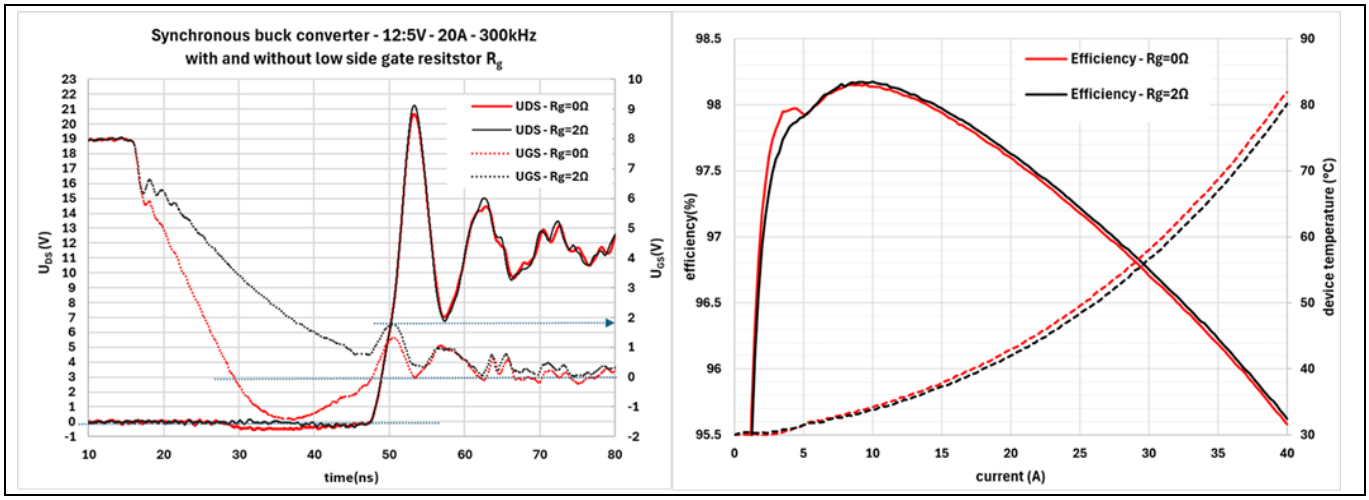


Figure 12 **Synchronous buck converter 12 V to 5 V – 300 kHz: Gate-Source U_{gs} and Drain-Source U_{ds} switching waveforms (left); efficiency and device temperature (right)**

2.2 Performance benchmarking: Isolated full-bridge/full-bridge converter

OptiMOS™ 7 power MOSFET 25 V HSW was benchmarked in an insulated full-bridge to full-bridge (FB-FB) topology, with a typical commercially available so called “quarter brick” (57.9 mm x 36.8 mm).

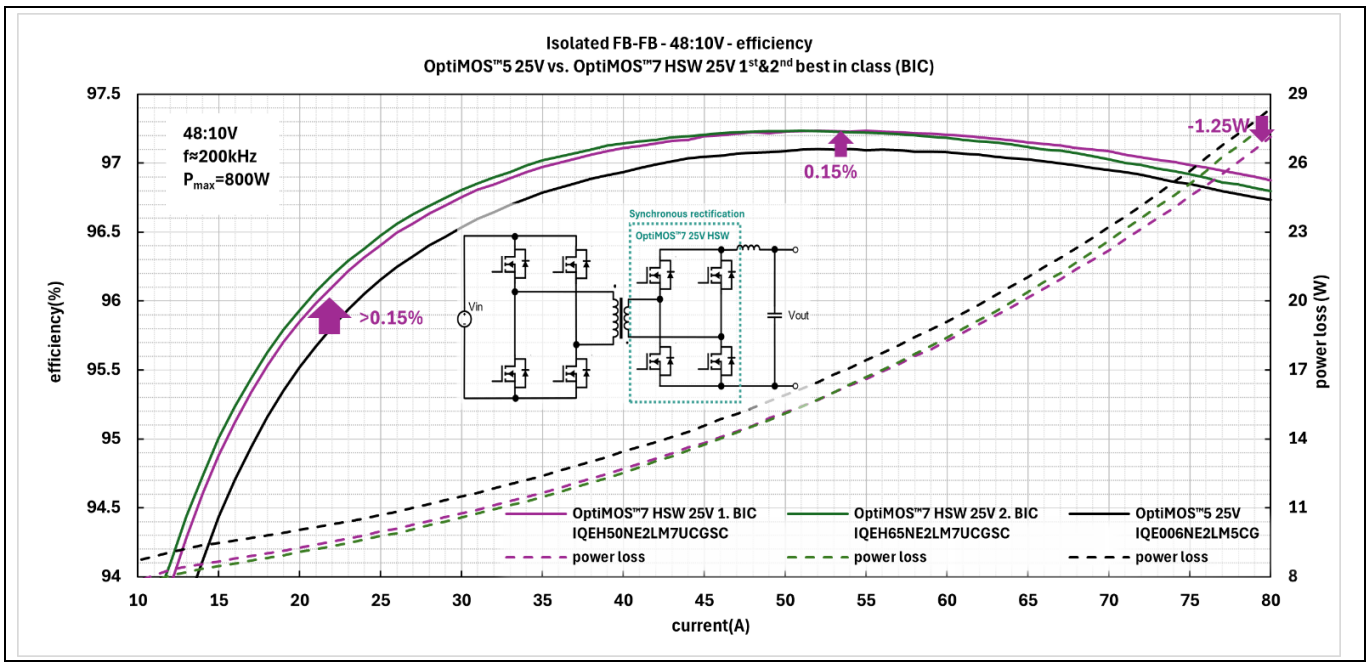


Figure 13 **Insulated FB-FB converter 48:10 V @200 kHz switching frequency: OptiMOS™ 7 HSW 1st and 2nd BIC show an efficiency improvement over the full load range compared to OptiMOS™5 25 V**

Figure 13 shows that the second BIC variant shows a slightly higher efficiency due to lower Q_{oss}, whereas the first BIC shows higher full load efficiency due to the low $R_{DS(ON)}$.

The secondary side consists of 12 MOSFETs, i.e., three parallel MOSFETs for every individual cell in the FB. The operation frequency is around 200 kHz with a conversion rate of 48:10 V and a gate driving voltage of 9 V. The coldplate of the converter was removed during testing. The board was plugged in on a hostboard to connect the supply and the electronic load. 3 m/s forced convection was applied towards the long side of the converter board to achieve steady state conditions; the board was heated up for 10 minutes. The current was then decreased in 1 A steps to 0 A.

Compared to OptiMOS™ 5 25 V the efficiency in the range medium to full load can be improved by 0.15% for the OptiMOS™ 7 25 V HSW best in class (BIC) due to the improved $R_{DS(ON)10}$. A significant improvement of the efficiency by >0.15% at low load can be seen mainly as a result of an improved $FOMQ_{oss10}$ and $FOMQ_g$. The advanced induced turn on ruggedness could on top help to reduce the deadtime to a minimum and to further improve the efficiency (Section 2.1.3).

OptiMOS™ 7 25 V HSW 2nd BIC shows a slightly better performance at low load due to lower Q_g and Q_{oss10}, and a lower full load efficiency due to higher $R_{DS(ON)}$ compared to OptiMOS™ 7 25 V HSW BIC. Nevertheless, the efficiency is significantly better than the OptiMOS™ 5 25 V over the full load range.

The overall power losses for the OptiMOS™ 7 25 V HSW 1st BIC are 1.25 W lower compared to OptiMOS™ 5 25 V at full load. With 12 MOSFETs this corresponds to 100 mW lower power losses per domain. Reduced losses in the MOSFET are beneficial to mitigate thermal runaway, i.e., a vicious cycle between $R_{DS(ON)}$ increase with temperature and temperature increase due to $R_{DS(ON)}$ increase causing higher conduction losses. This is very important in high power density designs.

Figure 14 shows the thermal image of the converter: the temperature of the synchronous rectifier is 5°C lower for OptiMOS™ 7 25 V HSW BIC compared to OptiMOS™ 5 25 V.

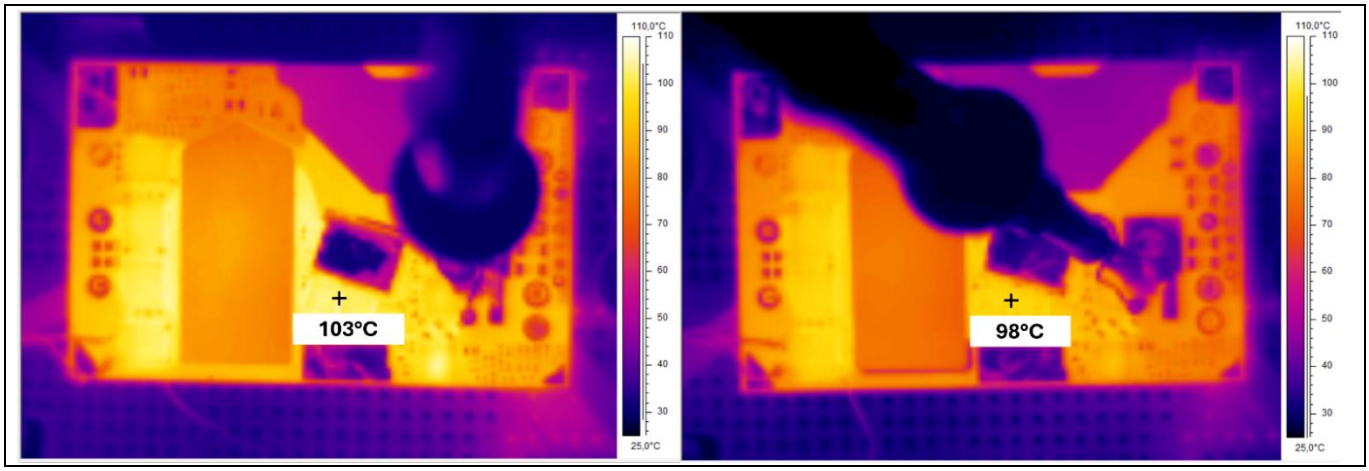


Figure 14 Thermal image of the insulated FB-FB converter quarter-brick: the cross marks the temperature of the synchronous rectifier: 103°C for OptiMOS™ 5 25 V and 98°C for OptiMOS™ 7 25 V HSW 1st BIC

3 OptiMOS™ 7 soft-switching optimized

Voltage and current transients are more relaxed in soft switching application. Less stringent requirements on robustness and ease of use open more degree of freedom to optimize specifically for the best performance without compromises and to focus on $R_{DS(ON)}$ and gate charge reduction. The very low contribution of the package resistance to the MOSFET on resistance enables full leverage of a very low ohmic technology.

3.1 $R_{DS(ON)}$ characteristic and gate charges

OptiMOS™ 7 SSW optimized was developed with the intention to provide low $R_{DS(ON)}$ already at low gate driving voltages to reduce gate driver losses to enable high frequency operation.

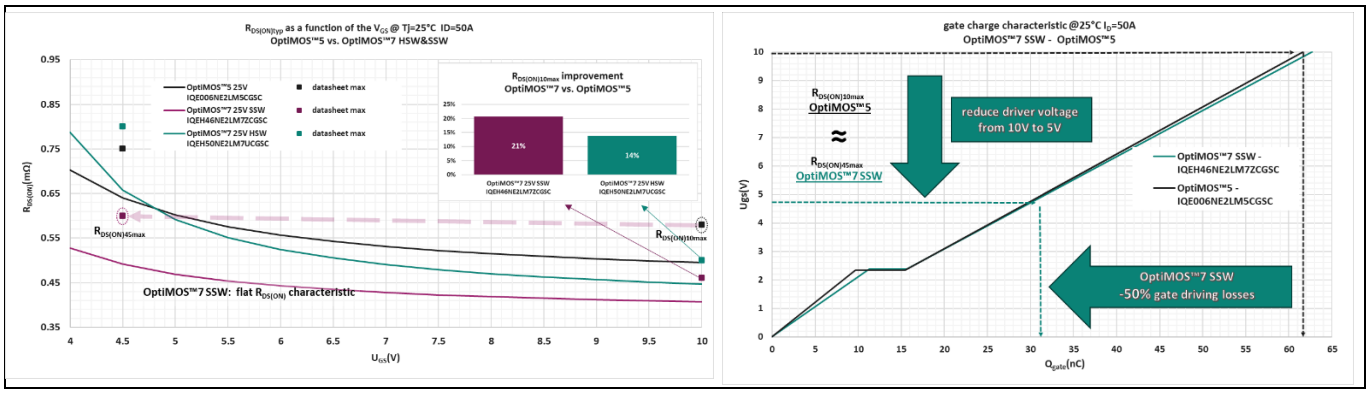


Figure 15 $R_{DS(ON)}$(VGS) characteristic of OptiMOS™ 7 SSW is very flat

Figure 15 shows the $R_{DS(ON)45max}$ of OptiMOS™ 7 SSW is comparable to the $R_{DS(ON)10max}$ of OptiMOS™ 5. The $R_{DS(ON)10max}$ is significantly better for OptiMOS™ 7 SSW/HSW compared to OptiMOS™ 5 (inset).

Figure 15 shows the very flat $R_{DS(ON)}$ characteristic of OptiMOS™ 7 SSW due to a reduced threshold voltage V_{th_typ}= 1.4 V and due to the thinner gate oxide. Whereas, the $R_{DS(ON)}$ characteristics of OptiMOS™ 7 hard-switching optimized (HSW) and OptiMOS™ 5 are significantly steeper for gate-source voltages U_{GS} smaller than 5 V. $R_{DS(ON)10max}$ levels are significantely better for both OptiMOS™ 7 flavors compared to OptiMOS™ 5 (inset).

$R_{DS(ON)45max}$ of OptiMOS™ 7 soft-switching optimized (SSW) is on a same level as the $R_{DS(ON)10max}$ of OptiMOS™ 5, while the gate driving losses are reduced by 50%.

3.2 Performance benchmarking: Hybrid Switched Capacitor (HSC)

A 500 W Hybrid-Switched Capacitor (HSC) reference board from Infineon was selected to perform a benchmarking between OptiMOS™ 5 and OptiMOS™ 7 SSW (Figure 16). The specialty of this topology is that with a Multi-Tapped-Autotransformer (MTA) enables continuous energy flow from input to output to maximize power density [15].

The operation frequency is 390 kHz with a conversion ratio of 8:1. The benchmarking was performed with a nominal input voltage of 48 V, resulting in an output voltage of 6 V unregulated. Forced convection was applied on the board from the side with 3 m/s without applying a headspreader or coldplate on top.

Apart of the device under test all other components on the board remained the same as on the original reference board. The driver voltage is 6 V. The MOSFETs operate in zero voltage switching (ZVS) so that in conclusion the losses in the semiconductor switches are mainly related to conduction losses.

Figure 17 shows a model-based loss breakdown for the platform in Figure 16 at 480 A [15]. It is important to notice that the losses in the multitaped auto-transformer (MTA) contribute nearly 2/3 to the overall losses. A redesign of the board for higher output power would make the impact of OptiMOS™ 7 SSW more evident.

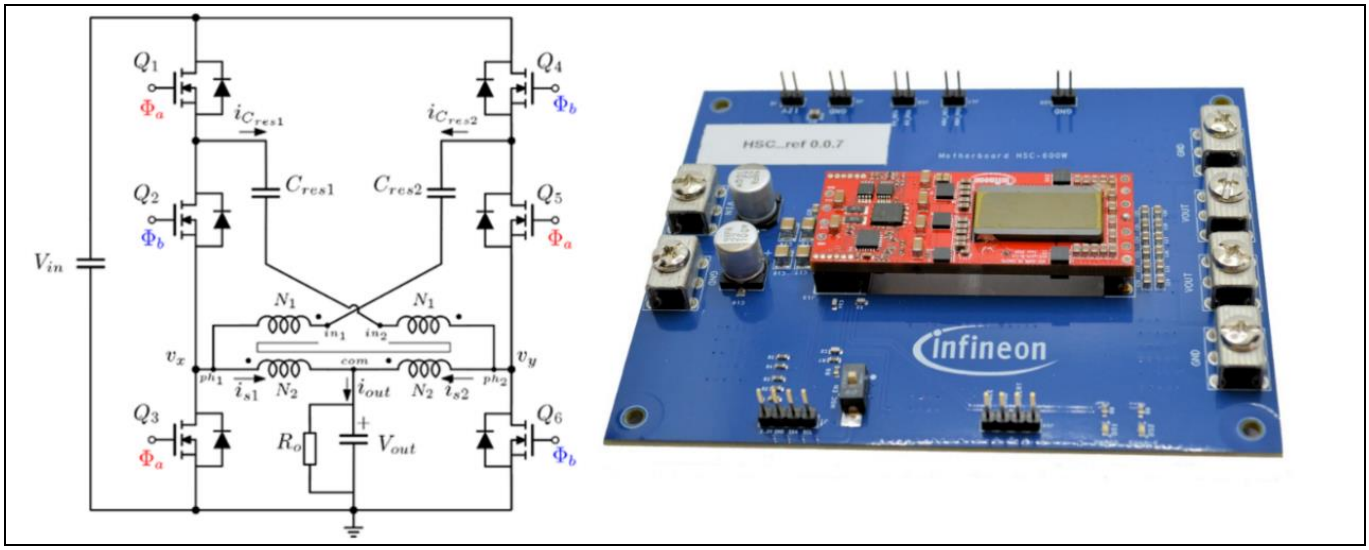


Figure 16 500 W Hybrid Switched Capacitor (HSC) reference board from Infineon: REF_500W_HSC_6V

Figure 18 shows the experimental data of the efficiency and the power losses comparing OptiMOS™ 5 and OptiMOS™ 7 SSW without considering gate driving losses. For the same driving voltage the gate charges are identical between the groups as explained in section 3.1.

The board was running for 10 minutes at 80 A to achieve steady state conditions: the maximum board temperature ranged between 105°C and 110°C for both groups, i.e., mainly dominated by the losses in the PCB and in the MTA. The current was then stepped down by 1 A every 30 seconds to zero. An efficiency improvement at full load of 0.17% was observed. The overall power losses were reduced by 700 mW or 175 mW per domain. With an RMS current of 28 A per MOSFET an $R_{DS(ON)}$ improvement of 220 µΩ at a junction temperature of approximately 120°C can be estimated. The advantage of a lower $R_{DS(ON)}$ can be fully leveraged in converter designs with extreme power densities with high output currents.

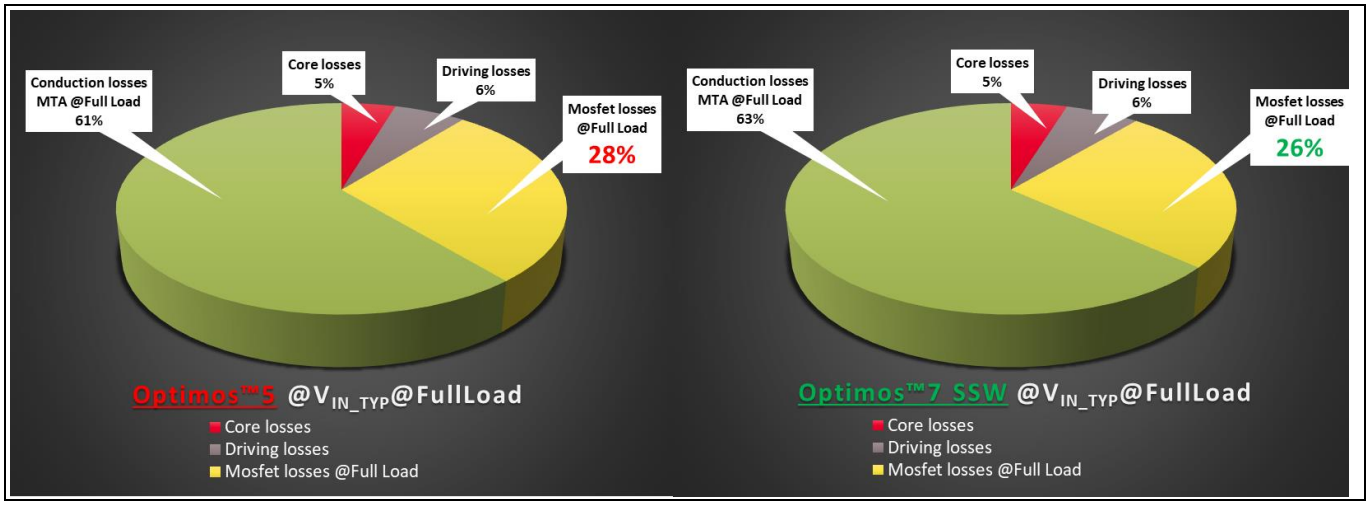


Figure 17 Loss breakdown for the reference board REF_500W_HSC_6V operated at 480 W output power, i.e., 480 W output power

Figure 17 illustrates that OptiMOS™ 5 (left) shows 2% higher losses compared to OptiMOS™ 7 SSW (right).

Figure 19 compares the drain-source voltage U_{DS} on the synchronous rectifier between OptiMOS™ 5 and OptiMOS™ 7 SSW. The magnetization current was not touched in the setup, i.e., the slightly different Q_{oss} between the two groups has no visible impact on the curve shape and timing.

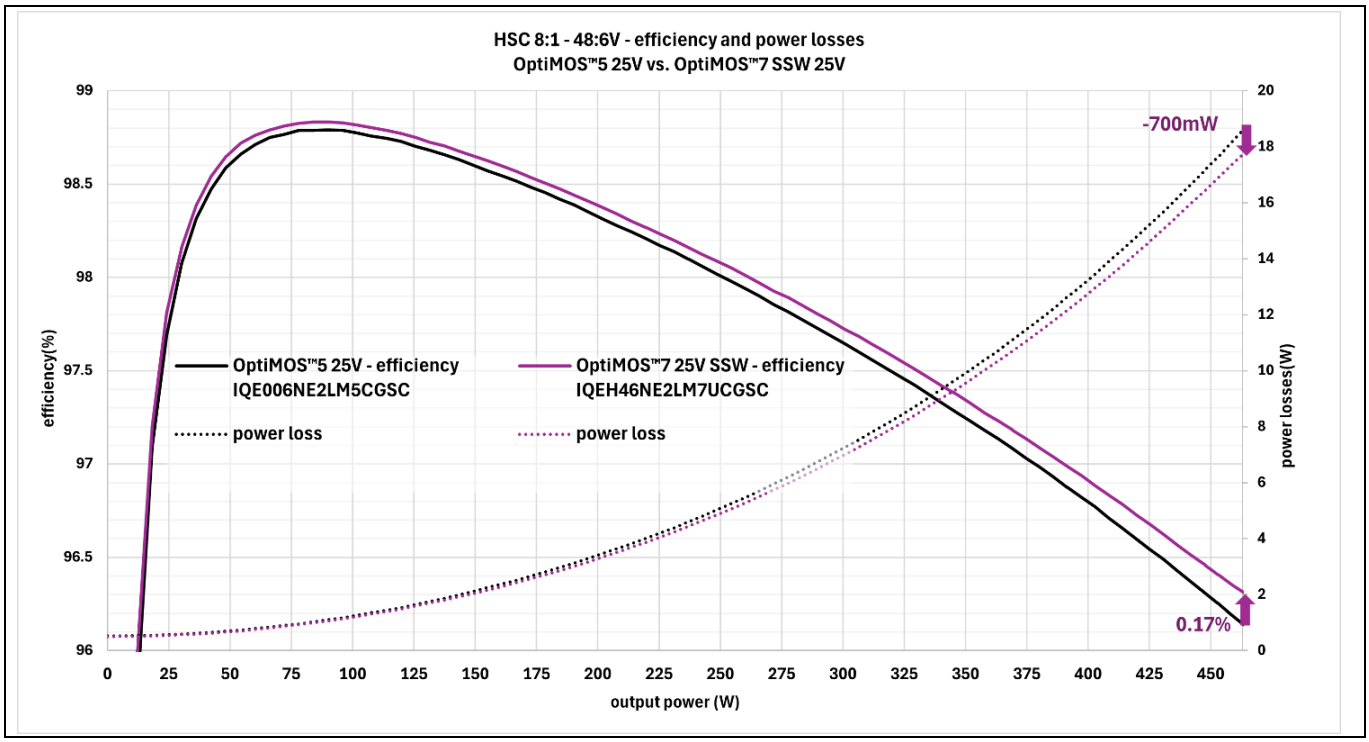


Figure 18 OptiMOS™ 7 SSW shows an efficiency improvement of 0.17% at full load compared to OptiMOS™ 5. The overall power losses were reduced by 0.7 W at full load

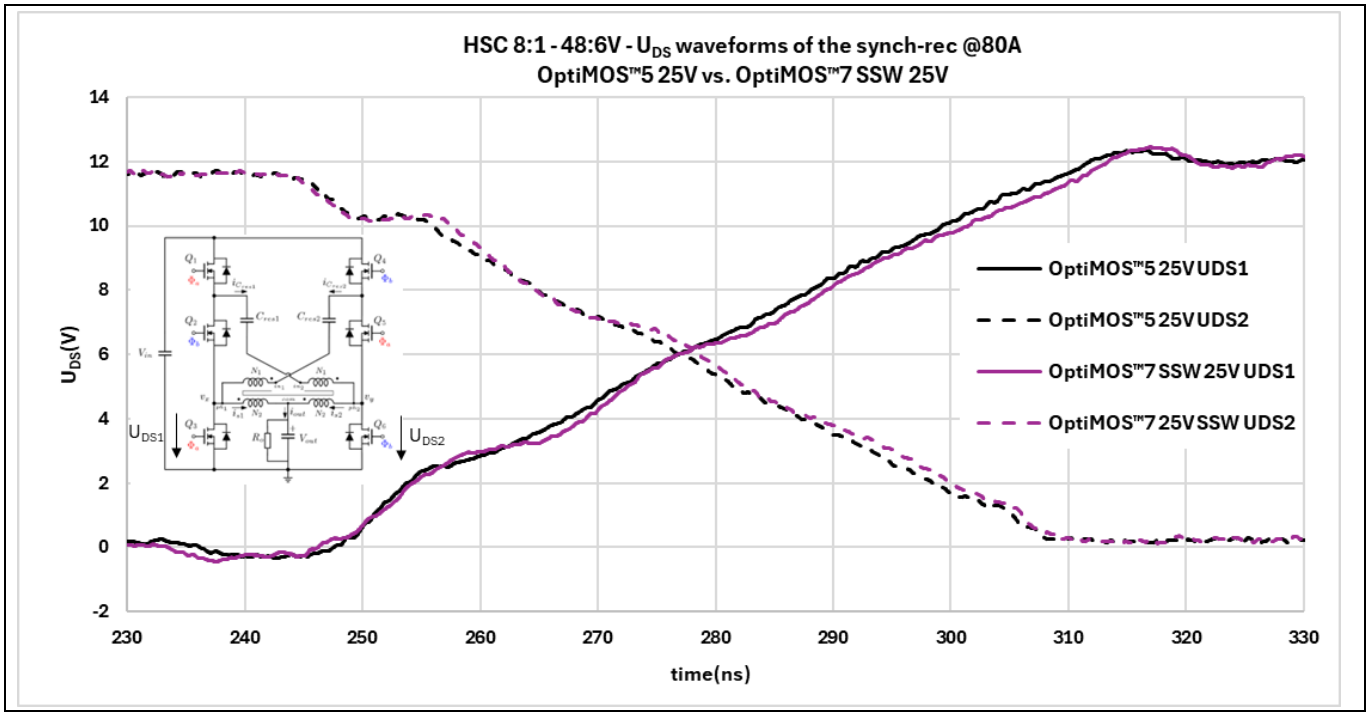


Figure 19 **The drain-source voltage U_{DS} of the synchronous rectifier for the test board depicted in Figure 16: Comparing OptiMOS™ 5 and OptiMOS™ 7 SSW at 80 A waveforms are practically identical**

4 Portfolio and comparison

Table 1 provides a side-by-side comparison between Infineon's latest silicon trench MOSFET technology, OptiMOS™ 7 25 V, and its predecessor, OptiMOS™ 5 25 V.

The first column of the table refers to the salescode of the respective products. Two different package variants are available: a bottom-side cooled variant (BSC), as well as a dual-side cooled variant (DCS). The DSC variant can be identified by ending "SC" in the salescode, whereas the "CG" referes to the center gate feature of the Source-Down MOSFET package (Figure 20). Table 1 shows only best-in-class devices. Additional portfolio products are available as well.

Table 1 Datasheet comparison: OptiMOS™ 7 25 V application optimized versus OptiMOS™ 5 25 V

3.3 x 3.3 mm² PQFN SD BSC **3.3 x 3.3 mm² PQFN SD DSC**	**V_{gs} (V)**	**$V_{th\ typ}$ (V)**	**[1] $R_{DS(on)45max}$ (mΩ)**	**[2] $R_{DS(on)10max}$ (mΩ)**	**Miller ratio Q_{gd}/Q_{gs}**	**[3] $FOMQ_{oss}$ (nC·mΩ)**	**[4] $FOMQ_{g45}$/ [5] $FOMQ_{g10}$ (nC·mΩ)**
OptiMOS™ 7 25 V – hard-switching optimized (U)							
IQEH54NE2LM7UCG IQEH50NE2LM7UCGSC	±16	1.7	0.84 0.8	0.54 0.5	0.3	20 18	[4]22 / [5]30 [4]21 / [5]28
OptiMOS™ 7 25 V – soft-switching optimized (Z)							
IQEH50NE2LM7ZCG IQEH46NE2LM7ZCGSC	±12	1.4	0.64 0.6	0.5 0.46	0.4	26 24	[4]18/ [5]31 [4]17/ [5]29
OptiMOS™ 5 25 V – reference							
IQE006NE2LM5CG IQE006NE2LM5CGSC	±16	1.6	0.75	0.58	0.61	24	22 / 36

The letter "U" refers to the hardswitching variant, whereas the letter "Z" refers to the soft switching optimized version of OptiMOS™ 7 25 V. Featured characteristics for the respective technology variant are highlighted in the respective color.

[1] @V_{gs} = 4.5 V
[2] @V_{gs} = 10 V
[3] $RDS_{(on)10,max}$ · $Q_{oss,typ}$
[4] $RDS_{(on)45,max}$ · $Q_{g4.5,typ}$
[5] $RDS_{(on)10,max}$ · $Q_{g10,typ}$

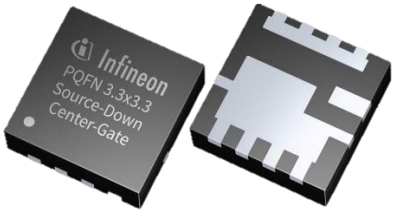
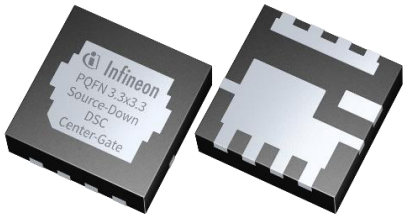
 PG-TTTFN-9 Bottom-side cooled (BSC)	3.3 x 3.3 mm² PQFN Source-Down Center gate *“CG” salescode identifier*	 PG-WHTFN-9 Dual-side cooled (DSC) “SC” *salescode identifier*

Figure 20 OptiMOS™ 7 25 V package variants: bottom side cooled (left) and dual side cooled (right)

The key feature of the Source-Down package concept is the orientation of the active side of the silicon chip toward the bottom side of the component as described elsewhere in more detail [9].

5 Summary

The OptiMOS™ 7 25 V application optimized is a new silicon trench MOSFET technology from Infineon that offers improved performance and efficiency in power conversion applications. The technology is available in two variants: hard-switching optimized (HSW) and soft-switching optimized (SSW).

The HSW variant features advanced induced turn-on ruggedness, low part-to-part variation, and optimized $FOMQ_{oss}$ and $FOMQ_{g}$, making it suitable for high-frequency operation.

The SSW variant is optimized for low conduction losses and high-frequency operation, with a very flat $R_{DS(ON)}$ characteristic and reduced gate driving losses. Benchmarking results show that the OptiMOS™ 7 25 V HSW and SSW variants outperform the OptiMOS™ 5 25 V in terms of efficiency and power losses.

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