LPDDR4X Datasheet

BWCGBX32N2A-64G-X

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Revision History

Version	Date	Description
1.0	2024/09	First Release
2.0	2024/10	Added specific values for IDD parameters
3.0	2025/03	1. Split original datasheet into two files 2. Updated device configuration 3. Added IDD6Q value

Table of Contents

1. Introduction

1.1 Product Information

Part ID	Capacity	Size	Package
BWCGBX32N2A-64G-X	64Gb	10*15mm	FBGA200

Table.1 Product Information

1.2 Part Number Chart

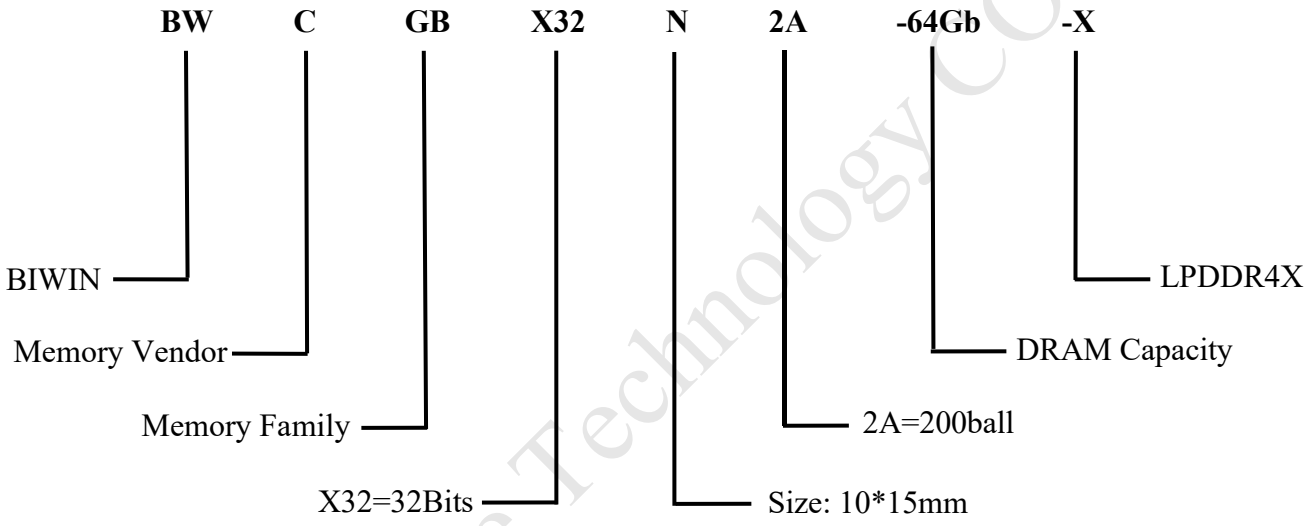


Figure 1 Part Number Chart

1.3 Features

- Ultra-low-voltage core and I/O power supplies
  - VDD1 = 1.70–1.95V; 1.80V NOM
  - VDD2 = 1.06–1.17V; 1.10V NOM
  - VDDQ = 0.57–0.65V; 0.60V NOM or VDDQ = 1.06–1.17V; 1.10V NOM
- Frequency range
  2133–10 MHz (data rate range: 4266–20 Mb/s/pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Differential data strobe supported
- Programmable preamble and postamble for both read and write operation
- 32-bit burst length Fixed or OTF supported and enabled by MRS, and 16-bit default burst length is supported
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.5 GB/s per die
- On-chip temperature sensor to control self refresh rate
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable VSS (ODT) termination
- Array configuration
  2Gig x 32 (2 channels x 16 I/O)
- Device configuration
  1G16 x 4 die in package
- FBGA “green” package
  200-ball FBGA (10mm*15mm)
  seated height 0.95mm (MAX)
- Speed grade, cycle time
  468ps@RL=36/40
- Operating temperature range
  -25°C to +85°C

Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
2133	4266	36/40	18/34

1.4 Device Configuration

Item	Description	2G32 (64Gb/package)
Die Organization	Channel A, rank 0	x16 mode × 1 die
	Channel B, rank 0	x16 mode × 1 die
	Channel A, rank 1	x16 mode × 1 die
	Channel B, rank 1	x16 mode × 1 die
Die Addressing	Density per die	16Gb
	Bits	17,179,869,184
	Configuration	128Mb × 16 DQ × 8 Banks
	Number of channels	2
	Number of banks	8
	Array prefetch bits	256
	Rows per bank	131,072
	Columns	64
	Page size (bytes)	2048
	Channel density(bits per channel)	17,179,869,184
	Total density(bits per die)	17,179,869,184
	Bank address	BA[2:0]
	Row address	R[16:0]
	Column address	C[9:0]
	Burst starting address boundary	64-bit

Table.2 Device Configuration

1.5 Refresh Requirement Parameters

Parameter	Symbol	16Gb Die	Unit
REFRESH cycle time (all banks)	t_{RFCab}	380	ns
REFRESH cycle time (per bank)	t_{RFCpb}	190	ns
Per bank refresh to per bank refresh time (different bank)	$t_{PBR2PBR}$	90	ns

Table.3 Refresh Requirement Parameters

Note: This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.

1.6 Functional Block Diagram

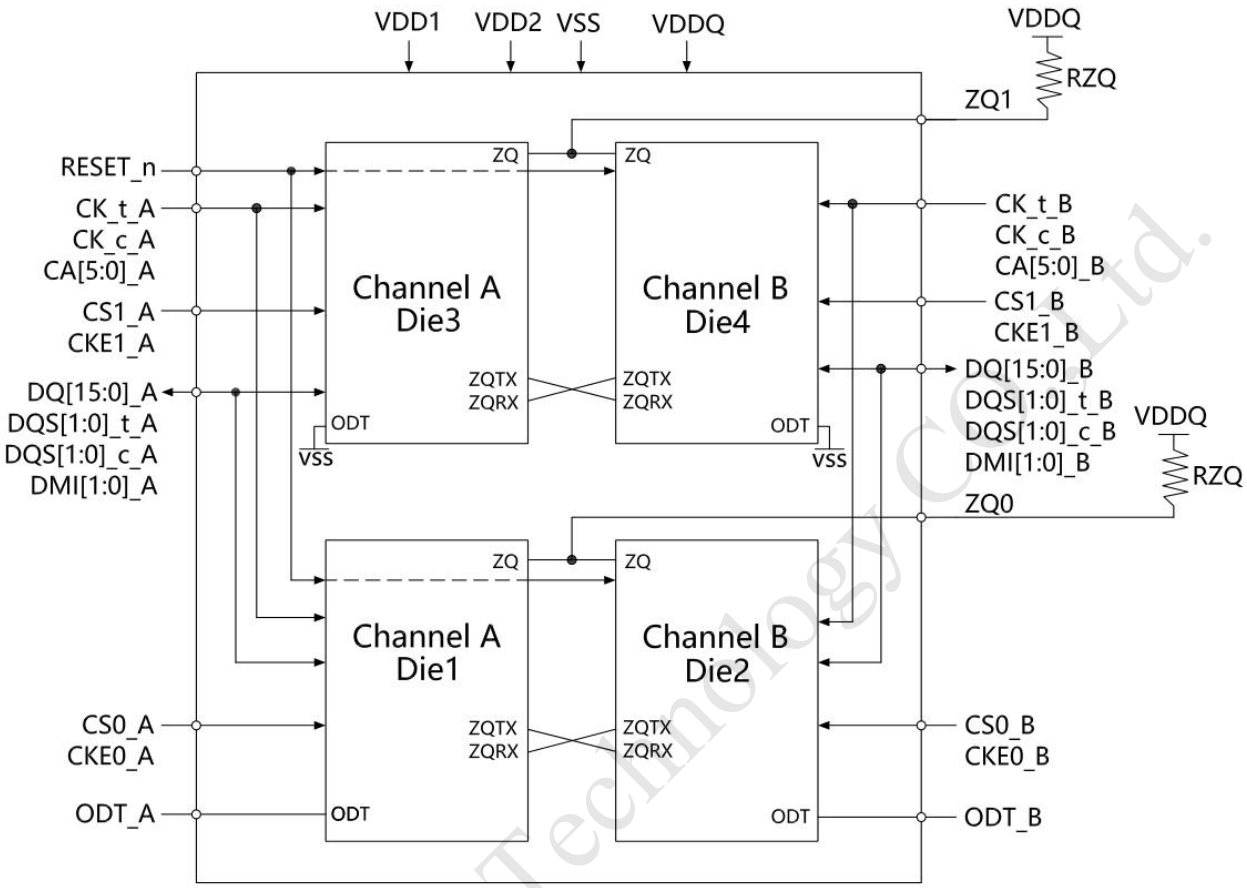
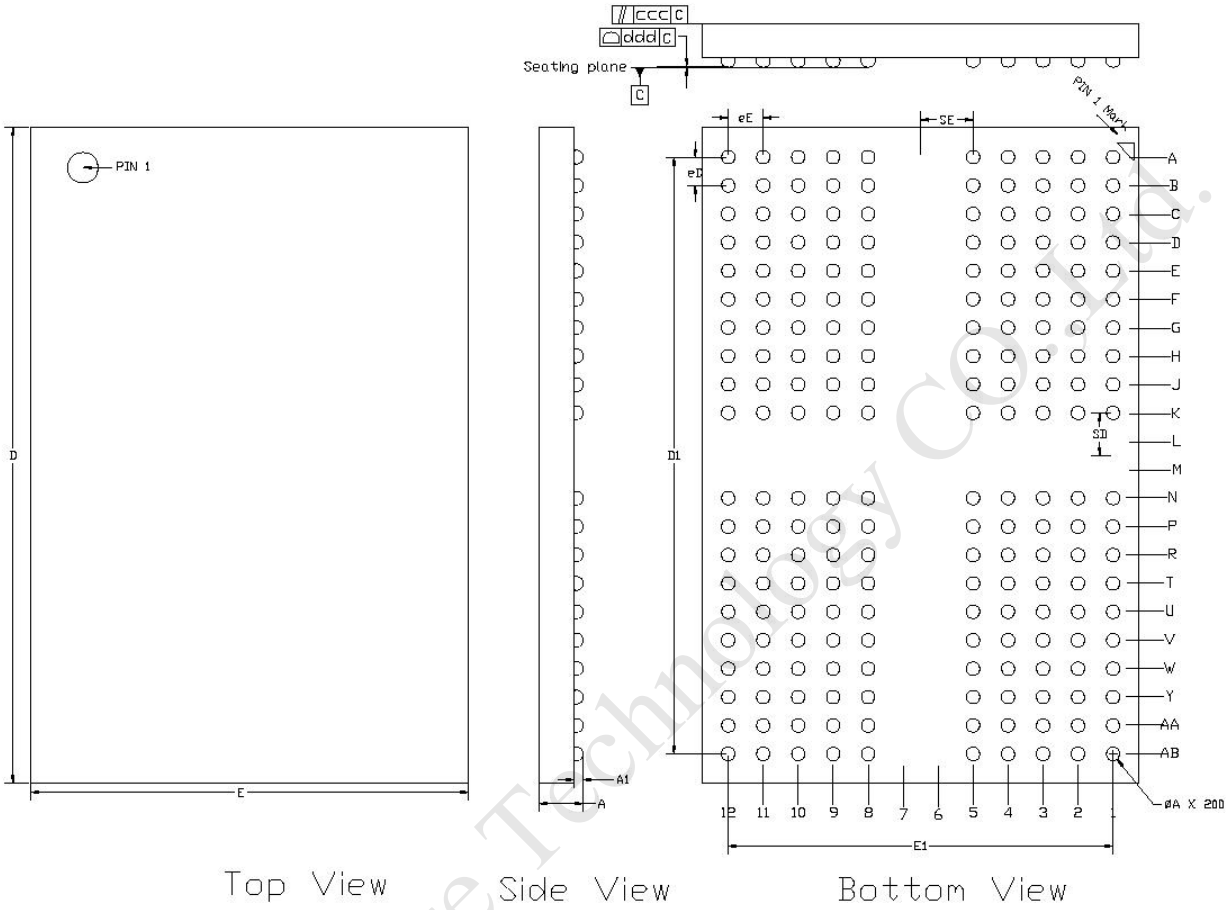


Figure.2 Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram

1.7 Package Dimensions



ITEM	Symble	Unit:mm		
		MIN	NORM	MAX
BODY SIZE	D	14.90	15.00	15.10
	E	9.90	10.00	10.10
TOTAL THICKNESS	A	0.75	0.85	0.95
STAND OFF	A1	0.18	0.21	0.24
EDGE BALL (CENTER TO CENTER)	D1	13.65		
	E1	8.80		
BALL PITCH	eD	0.65		
	eE	0.80		
even number of balls (eE/2,eD/2) odd number of balls (0)	SE	1.20		
	SD	0.975		
BALL COUNT	n	200		
BALL WIDTH (after reflow)	ΦA	0.29	0.32	0.35
BALL TO OUTLINE	d1	0.575	0.675	0.775
	e1	0.500	0.600	0.700
Mold package warpage	ccc			0.08
COPLANARITY	ddd			0.08

Notice:
1.Ball diameter: 0.3mm(Raw)
2."●"---bumping ball location
3.In the diagram,there are 200 ball locations in all.

Figure.3 Package Dimensions (10mm*15mm*0.95mm max)

1.8 Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	NC	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1_A	DM0_A	DQ6_A	VSS			VSS	DQ14_A	DM1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T_A	VSS	VDDQ			VDDQ	VSS	DQS1_T_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_C_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_T_A	CK_C_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE0_B			CK_T_B	CK_C_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_C_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_C_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_T_B	VSS	VDDQ			VDDQ	VSS	DQS1_T_B	VSS	VDDQ
Y	VSS	DQ1_B	DM0_B	DQ6_B	VSS			VSS	DQ14_B	DM1_B	DQ9_B	VSS
AA	NC	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	NC
AB	NC	NC	VSS	VDD2	VSS			VSS	VDD2	VSS	NC	NC

Figure.4 200-Ball Dual-Channel Single-Rank Discrete FBGA

1.9 PIN Description

Symbol	Type	Description
CK_t_[A:B] CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CS0_[A:B] CS1_[A:B]	Input	**Chip select:** Each rank in each channel has its own CS signals.
CA[5:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
CKE0_[A:B] CKE1_[A:B]	Input	**Clock enable**: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0]_t_[A:B] DQS[1:0]_c_[A:B]	I/O	**Data strobe**: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data duringa READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel has its own DQS_t and DQS_c strobes.
DMI[1:0]_[A:B]	I/O	**Data Mask/Data Bus Inversion**: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
VSS	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets all channels of the die.
NC	-	**No connect:** Not internally connected.
RFU	-	**RFU:** Reserved for future use on larger capacity configurations.

Table.4 LPDDR Ball Descriptions

Note: ZQ1, CKE1, CS1 balls are reserved for 2-rank package. For 1-rank package those balls are RFU.

1.10 Mode Register Definition

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0						**RFM support**	**Latency mode**	**REF**
	OP[0] = 1b: Only modified refresh mode supported							
	OP[1] = 0b: Device supports normal latency							
	OP[2] = 0b: Device supports TRR							
MR3						**PPRP[2]**		
	OP[2] = 0b: PPR protection disabled (default) 1b: PPR protection enabled							
MR5	**Manufacturer ID**							
	0001 0011b							
MR6	**Revision ID1**							
	-							
MR8	**I/O width**		**Density**					
	OP[7:6] = 00b: x16/channel		OP[5:2] = 0110B:16Gb single channel die					
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR24	**TRR Mode**				**Unlimited MAC**	**MAC value**		
	OP[3:0] = 1000b: Unlimited MAC							
	OP[7] = 0b: Disable (default) 1b: Reserved							
MR26	**PPR resources[3]**							
	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0
	0b: PPR resource is not available 1b: PPR resource is available							

Table.5 Mode Register Contents

Notes:

1. The contents of mode registers described here reflect information specific to each die in these packages.
2. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry (MR3 OP[2] =1b).
3. Before using PPR function, confirm the availability of PPR resource by reading MR25.

2. I_{DD} Parameters

2.1 I_{DD} Specification

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: tCK = tCK (MIN); tRC = tRC (MIN); CKE is HIGH; CS is LOW between valid commands;CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD01}	V_{DD1}	-
	I_{DD02}	V_{DD2}	
	I_{DD0Q}	V_{DDQ}	2
Idle power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2P1}	V_{DD1}	-
	I_{DD2P2}	V_{DD2}	
	I_{DD2PQ}	V_{DDQ}	2
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	-
	I_{DD2PS2}	V_{DD2}	
	I_{DD2PSQ}	V_{DDQ}	2
Idle non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	-
	I_{DD2N2}	V_{DD2}	
	I_{DD2NQ}	V_{DDQ}	2
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	-
	I_{DD2NS2}	V_{DD2}	
	I_{DD2NSQ}	V_{DDQ}	2
Active power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	-
	I_{DD3P2}	V_{DD2}	
	I_{DD3PQ}	V_{DDQ}	2
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3PS1}	V_{DD1}	-
	I_{DD3PS2}	V_{DD2}	
	I_{DD3PSQ}	V_{DDQ}	3
Active non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	-
	I_{DD3N2}	V_{DD2}	
	I_{DD3NQ}	V_{DDQ}	3
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	-
	I_{DD3NS2}	V_{DD2}	
	I_{DD3NSQ}	V_{DDQ}	3

Parameter/Condition	Symbol	Power Supply	Note
Operating burst READ current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL =RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	-
	I_{DD4R2}	V_{DD2}	
	I_{DD4RQ}	V_{DDQ}	4
Operating burst WRITE current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4W1}	V_{DD1}	-
	I_{DD4W2}	V_{DD2}	
	I_{DD4WQ}	V_{DDQ}	3
All-bank REFRESH burst current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tRFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD51}	V_{DD1}	-
	I_{DD52}	V_{DD2}	
	I_{DD5Q}	V_{DDQ}	3
All-bank REFRESH average current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	-
	I_{DD5AB2}	V_{DD2}	
	I_{DD5ABQ}	V_{DDQ}	3
Per-bank REFRESH average current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	-
	I_{DD5PB2}	V_{DD2}	
	I_{DD5PBQ}	V_{DDQ}	3
Power-down self refresh current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	I_{DD61}	V_{DD1}	5, 6
	I_{DD62}	V_{DD2}	5, 6
	I_{DD6Q}	V_{DDQ}	3, 5, 6

Table.6 IDD Specification

Notes:
1. ODT disabled MR11 op[6:4] = 000b
2. I_{DD} current specifications are tested after the device is properly initialized.
3. Measured currents are the summation of V_{DDQ} and V_{DD2}.
4. Guaranteed by design with output load = 5pF and RON = 40 ohm.
5. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the elevated temperature range.
6. This is the general definition that applies to full-array self refresh.
7. For all I_{DD} measurements, $V_{IHCKE} = 0.8 \times V_{DD2}$; $V_{ILCKE} = 0.2 \times V_{DD2}$.
8. LPDDR4: V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V
9. LPDDR4X: V_{DD2}= 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V

2.2 I_{DD} Parameters for Single Die

V_{DD1} = 1.70–1.95V; V_{DD2} = 1.06–1.17V; V_{DDQ} = 0.57–0.65V;
T_C= +85°C

Symbol	Supply	Speed Grade 4266Mb/s	Unit	Note
IDD01	VDD1	2.93	mA	-
IDD02	VDD2	32.37		
IDD0Q	VDDQ	0.12		
IDD2P1	VDD1	0.43	mA	-
IDD2P2	VDD2	1.22		
IDD2PQ	VDDQ	0.12		
IDD2PS1	VDD1	0.43	mA	-
IDD2PS2	VDD2	1.22		
IDD2PSQ	VDDQ	0.12		
IDD2N1	VDD1	0.43	mA	-
IDD2N2	VDD2	13.89		
IDD2NQ	VDDQ	0.12		
IDD2NS1	VDD1	0.46	mA	-
IDD2NS2	VDD2	10.29		
IDD2NSQ	VDDQ	0.12		
IDD3P1	VDD1	0.43	mA	-
IDD3P2	VDD2	3.04		
IDD3PQ	VDDQ	0.12		
IDD3PS1	VDD1	0.43	mA	-
IDD3PS2	VDD2	3.04		
IDD3PSQ	VDDQ	0.12		
IDD3N1	VDD1	1.03	mA	-
IDD3N2	VDD2	23.25		
IDD3NQ	VDDQ	0.12		
IDD3NS1	VDD1	1.03	mA	-
IDD3NS2	VDD2	20.13		
IDD3NSQ	VDDQ	0.12		
IDD4R1	VDD1	3.65	mA	2, 3
IDD4R2	VDD2	243.81		
IDD4RQ	VDDQ	106.56		
IDD4W1	VDD1	3.60	mA	3
IDD4W2	VDD2	193.41		
IDD4WQ	VDDQ	0.12		

Symbol	Supply	Speed Grade 4266Mb/s	Unit	Note
I_{DD51}	V_{DD1}	18.82	mA	-
I_{DD52}	V_{DD2}	137.01		
I_{DD5Q}	V_{DDQ}	0.12		
I_{DD5AB1}	V_{DD1}	2.33	mA	-
I_{DD5AB2}	V_{DD2}	26.85		
I_{DD5ABQ}	V_{DDQ}	0.12		
I_{DD5PB1}	V_{DD1}	2.30	mA	-
I_{DD5PB2}	V_{DD2}	27.33		
I_{DD5PBQ}	V_{DDQ}	0.12		

Table.7 IDD Parameters

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. I_{DD4RQ} value is reference only. Typical value. $V_{OH} = V_{DDQ}/3$, TC = 25°C.
3. BL = 16, DBI disabled.

2.3 Full-Array Power-Down Self Refresh Current for Single Die

V_{DD1} = 1.70–1.95V; V_{DD2} = 1.06–1.17V; V_{DDQ} = 0.57–0.65V;

Temperature	Supply	Value	Unit
25°C	V_{DD1}	0.43	mA
	V_{DD2}	1.25	
	V_{DDQ}	0.08	
85°C	V_{DD1}	1.51	mA
	V_{DD2}	7.46	
	V_{DDQ}	0.08	

Table.8 Full-Array Current for Singe Die

Note:
I_{DD6} 25°C is the typical value in the distribution with nominal V_{DD} and a reference only value. I_{DD6} 85°C is the maximum I_{DD} guaranteed value considering the worst case conditions of process, temperature, and voltage.

3. MARKING

First Row: Simplified BIWIN Logo

Second Row: Sales Item P/N

Third Row: LOT No. + Serial Number

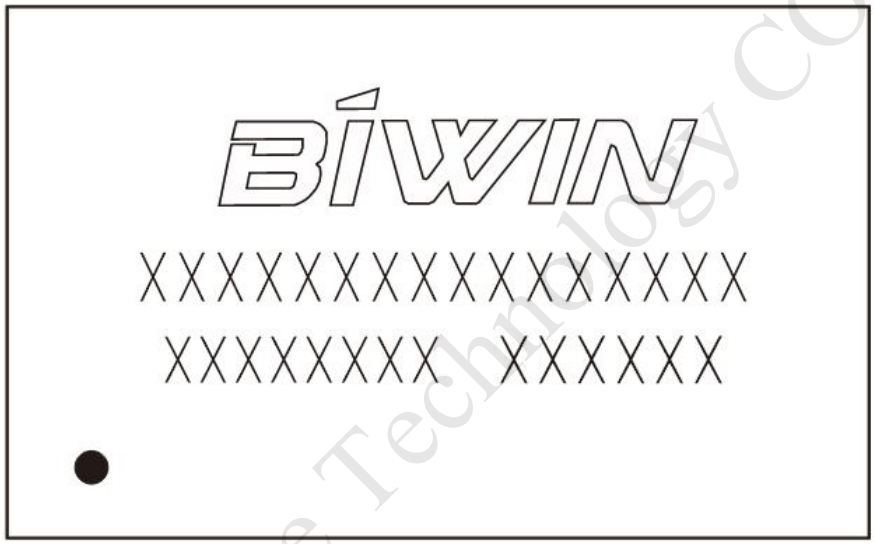


Figure5. Schematic Diagram of Product Marking