LPDDR4X Datasheet

BWCC2X32N2A-16G-X
BWCC2X32N2A-32G-X

Ver.1.0

Dec.2022

Released

DAT-CES-0188-A

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Revision History

Version	Date	Description
1.0	Dec.2022	First Release

1. Features

•Ultra-low-voltage core and I/O power supplies

– V_{DD1} = 1.70–1.95V; 1.80V nominal

– V_{DD2} = 1.06–1.17V; 1.10V nominal

– V_{DDQ} = 0.57–0.65V; 0.60Vnominal
or V_{DDQ} = 1.06–1.17V; 1.10V nominal

•Frequency range

–2133–10 MHz (data rate range: 4266–20 Mb/s/ pin)

•16n prefetch DDR architecture

•8 internal banks per channel for concurrent operation

•Single-data-rate CMD/ADR entry

•Bidirectional/differential data strobe per byte lane

•Programmable READ and WRITE latencies (RL/WL)

•Programmable and on-the-fly burst lengths (BL = 16, 32)

•Directed per-bank refresh for concurrent bank operation and ease of command scheduling

•Up to 8.5 GB/s per die

•On-chip temperature sensor to control self refresh rate

•Partial-array self refresh (PASR)

•Selectable output drive strength (DS)

•Clock-stop capability

•RoHS-compliant, “green” packaging

•Programmable VSS (ODT) termination

Options

• $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.80V/1.10V/0.60V or 1.10V

Array configuration

– 512 Meg × 32 (2 channels × 16 I/O)

– 1 Gig × 32 (2 channels × 16 I/O)

• Device configuration

– 512M16 × 2 die in package

– 512M16 × 4 die in package

• FBGA “green” package

– 200-ball FBGA (10mm x 15mm)

• Speed grade, cycle time

– 468ps@RL=36/40

• Operating temperature range

– –25°C to +85°C

Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
2133	4266	36/40	18/34

Table 1 Key Timing Parameters

2. Product Information

Part ID	Capacity	Size	Package
BWCC2X32N2A-16G-X	16Gb	10mm*15mm*0.9mm	FBGA200
BWCC2X32N2A-32G-X	32Gb	10mm*15mm*0.9mm	FBGA200

Table 2 Product Information

		512M16
Density per die		8Gb
Density per channel		8Gb
Configuration		64Mb × 16DQ× 8 banks
Number of channels (per die)		1
Number of banks (per channel)		8
Array prefetch (bits, per channel)		256
Number of rows (per channel)		65,536
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		8,589,934,592
Total density (bits per die)		8,589,934,592
Bank address		BA[2:0]
×16	**Row address**	R[15:0]
	Column address	C[9:0]
Burst starting address boundary		64bit

Table 3 Die Addressing

Note:Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

		16Gb	32Gb
Die organization in the package	**Channel A, rank 0**	8Gb × 16 mode ×1 die	8Gb × 16 mode ×1 die
	Channel B, rank 0	8Gb × 16 mode ×1 die	8Gb × 16 mode ×1 die
	Channel A, rank 1	-	8Gb × 16 mode ×1 die
	Channel B, rank 1		8Gb × 16 mode ×1 die

Table 4 Die Organization

2.1 MR0, MR[6:5], MR8, MR13, MR24, MR25 Definition

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			Single-ended mode			RFM support	Latency mode	REF
	OP[0] = 1b: Only modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[2] = 0b: Device supports TRR							
MR3						**PPRP**[3]		
	OP[2] = 0b: PPR protection disabled (default) 1b: PPR protection							
MR5	**Manufacturer ID**							
	0001 0011							
MR6	**Revision ID1**							
	-							
MR8	**I/O width**		**Density**					
	OP[7:6] = 00b: x16/channel		OP[5:2] = 0010b: 4Gb single channel die OP[5:2] = 0100b: 8Gb single channel die					
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR24	**TRR mode**				**Unlimited MAC**	**MAC value**		
	OP[3:0] = 1000b: Unlimited MAC OP[7] = 0b: Disable (default)							
MR25	**PPR resources**[4]							
	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0
	0b: PPR resource is not available 1b: PPR resource is available							

Table 5 Mode Register Definition

Notes: 1. The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.

2. Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.

3. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry.(MR3 OP[2]=1b).

4. Before using PPR function, confirm the availability of PPR resource by reading MR25.

2.2 Part Numbering

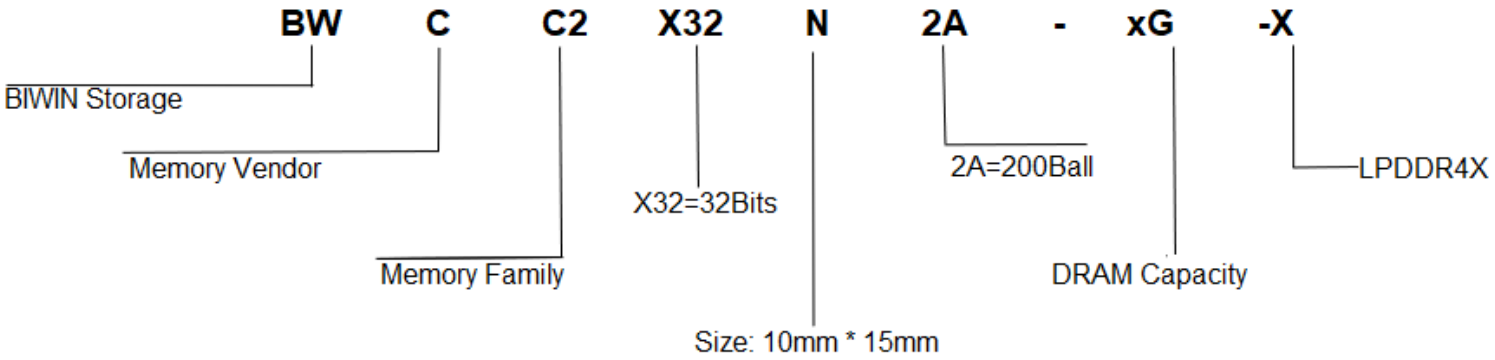


Figure 1 Part Numbering

2.3 Package Block Diagrams

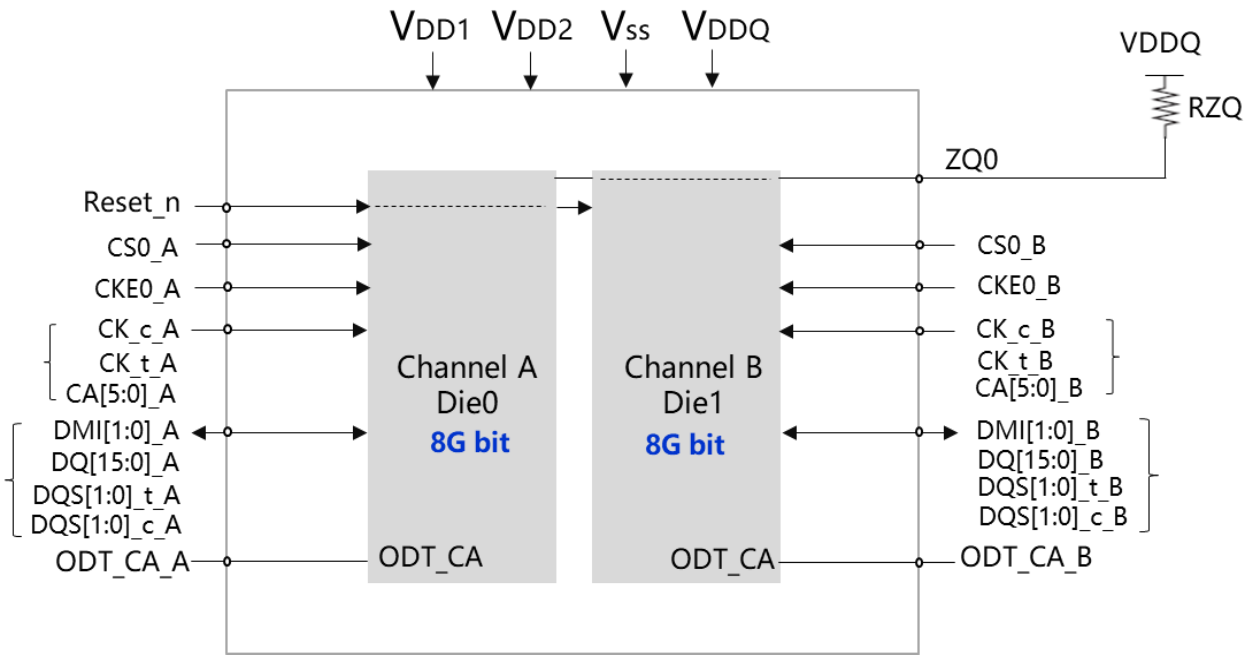


Figure 2-1 Dual-Die, Dual-Channel, Single-Rank Package Block Diagram (2GB x32 I/O)

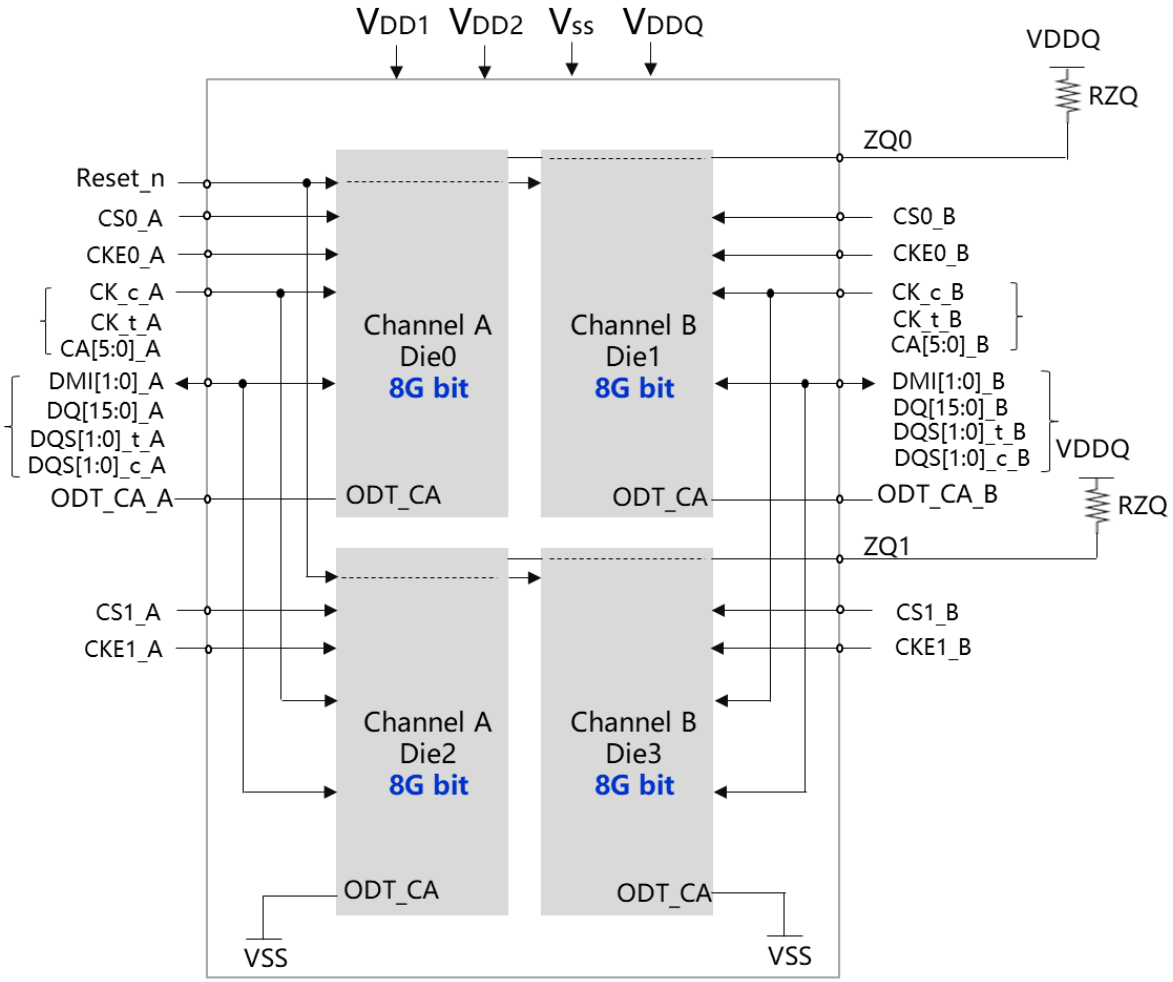
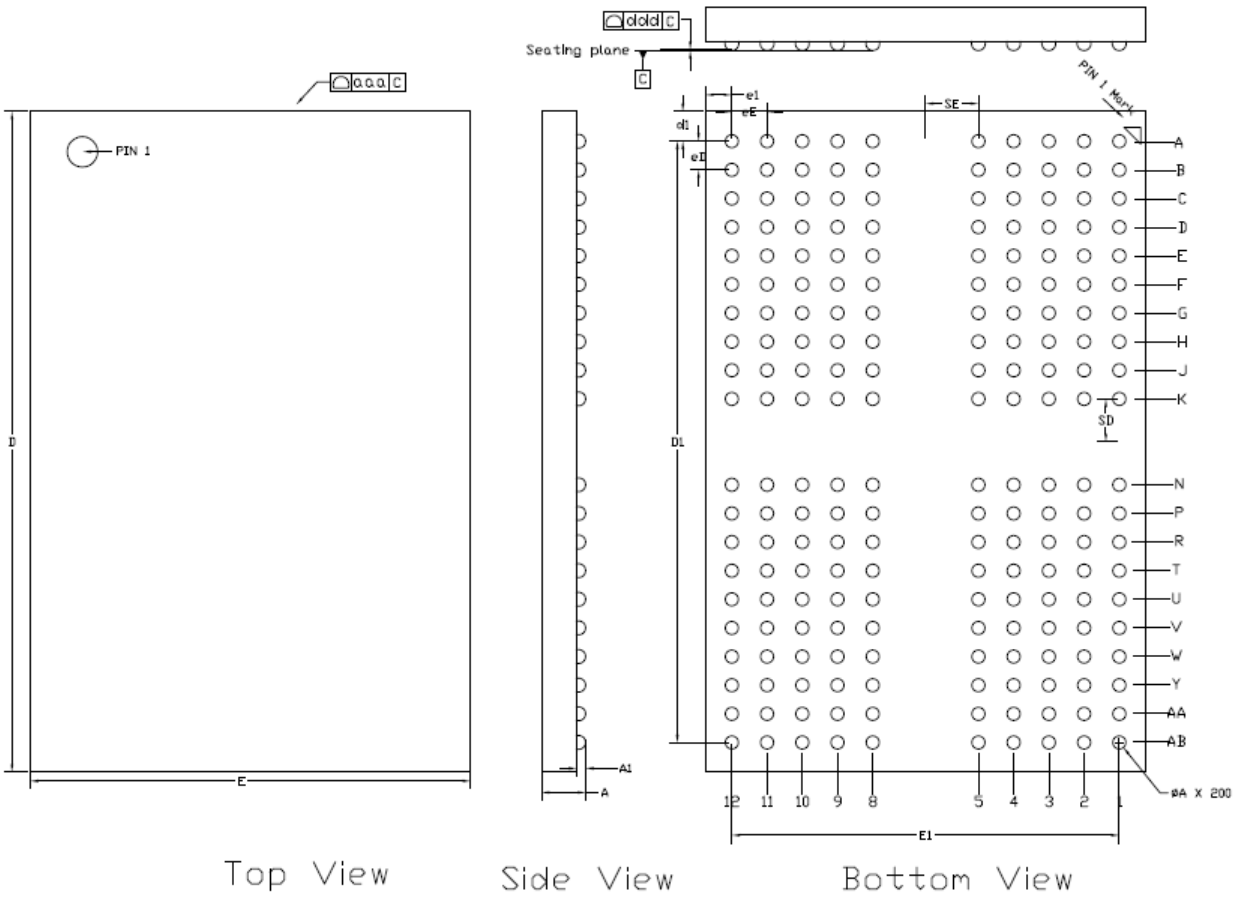
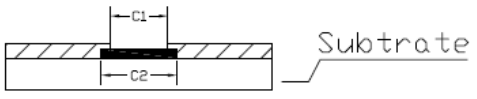


Figure 2-2 Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram (4GB x32 I/O)

2.4 Package Dimension



ITEM	Symble	Unit:mm		
		MIN	NORM	MAM
BODY SIZE	D	14.90	15.00	15.10
	E	9.90	10.00	10.10
TOTAL THICNESS	A	0.80	0.90	1.00
STAND OFF	A1	0.18	0.21	0.24
EDGE BALL (CENTER TO CENTER)	D1	13.65		
	E1	8.80		
BALL PITCH	eD	0.65		
	eE	0.80		
even number of balls (eE/2,eD/2) odd number of balls (0)	SE	1.20		
	SD	0.98		
BALL COUNT	n	200		
BALL WIDTH (after reflow)	ΦA	0.29	0.32	0.35
Solder mask opening	C1	0.27	0.30	0.33
Ball pad diameter	C2	0.33	0.36	0.39
BALL TO OUTLINE	d1	0.57	0.67	0.77
	e1	0.50	0.60	0.70
Mold package warpage	aaa	0.08		
COPLANARITY	ddd	0.08		



200ball Ø0.3mm Dimensions apply to solder balls postreflow on Ø0.3mm SMD ball pads.

Notice:
1.Ball diameter: 0.3mm
2."◗"---bumping ball location
3.In the diagram,there are 200 ball locations in all.

Figure 3 Package Dimension (10mm*15mm*0.9mm)

2.5 Ball Assignment

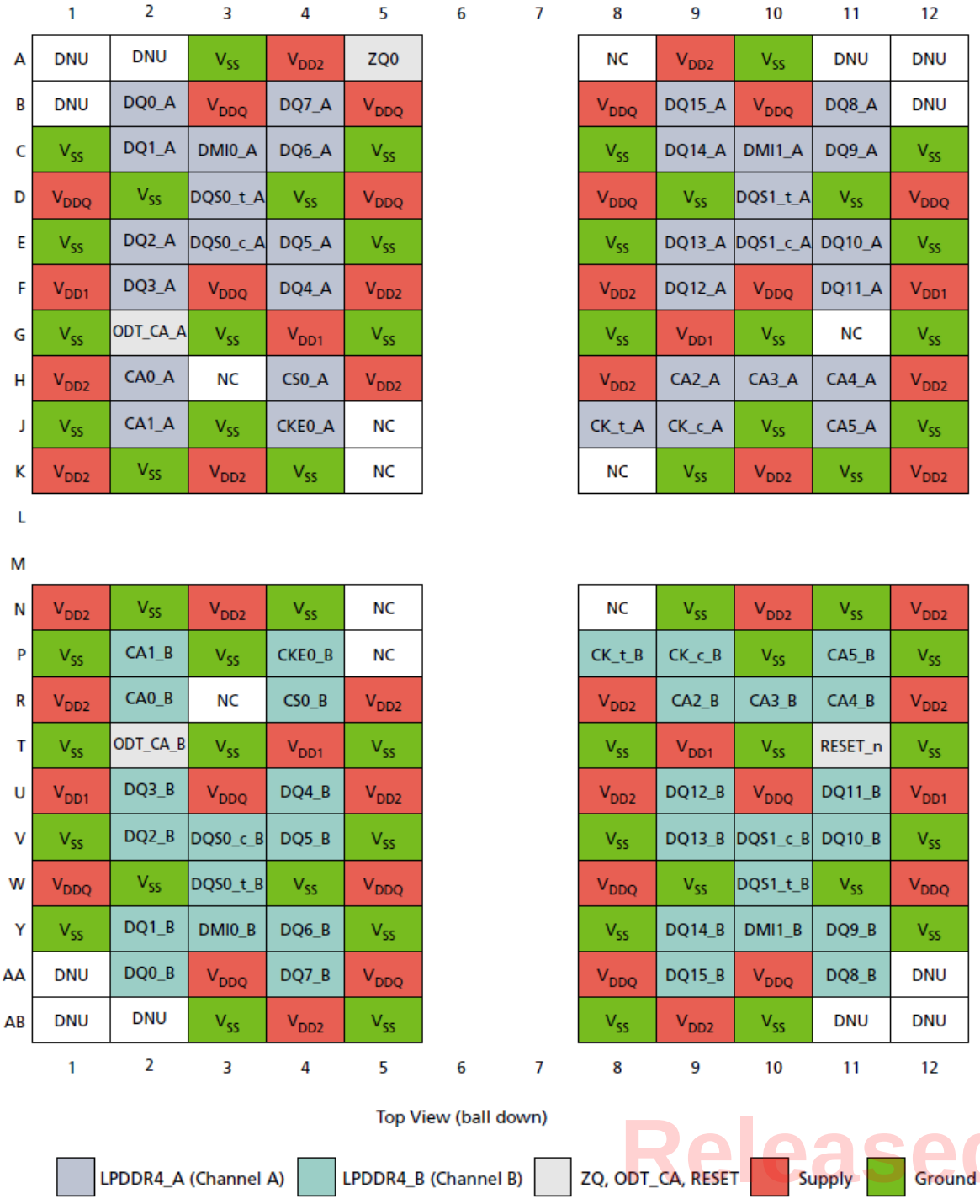


Figure 4-1 Dual-Channel, Single-Rank Discrete FBGA

2.5 Ball Assignment

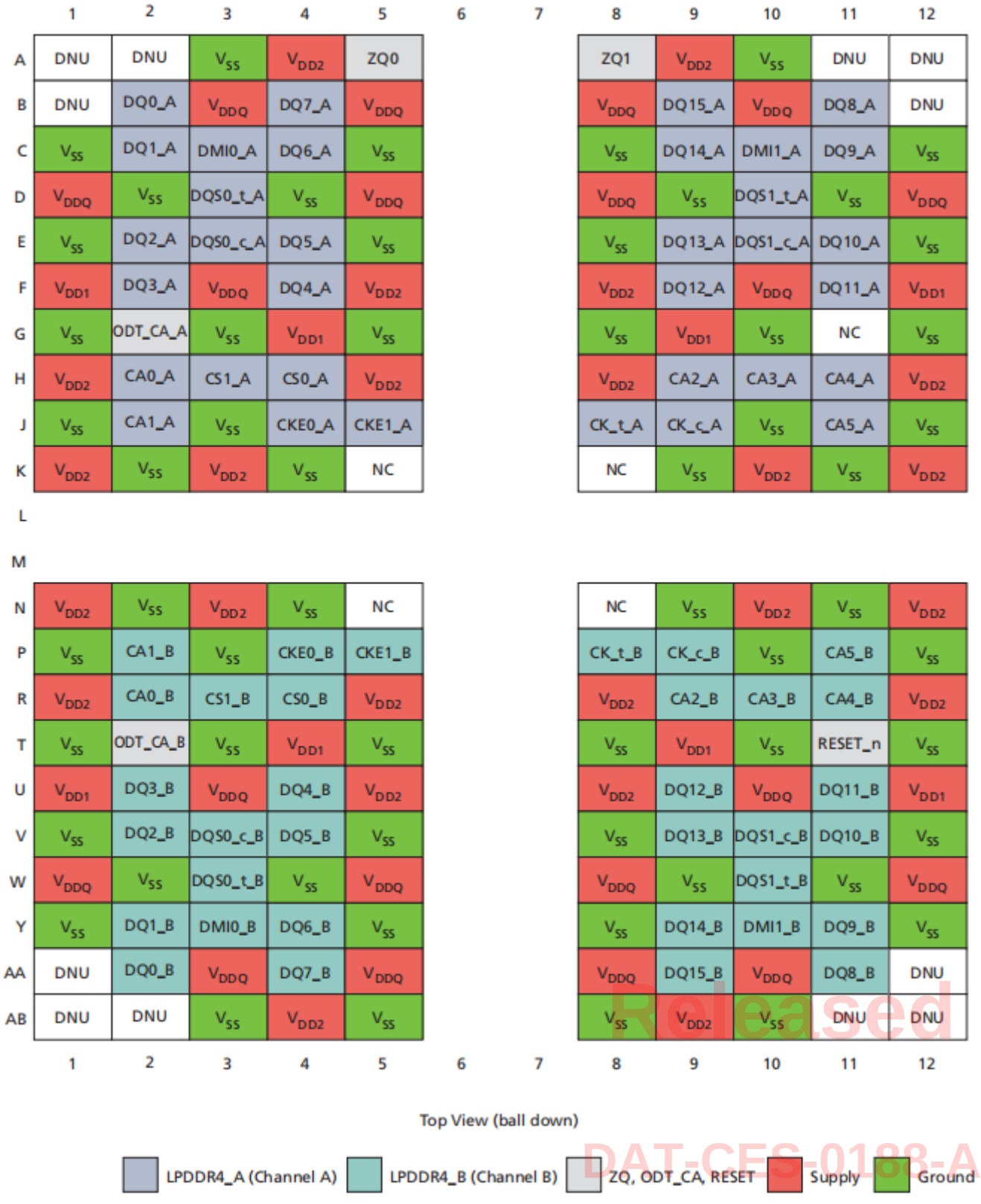


Figure 4-2 Dual-Channel, Dual-Rank Discrete FBGA

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters is referenced to clock. Each channel has its own clock pair.
CKE0_A, CKE1_A, CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B, CS1_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT control: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indi- cate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.

ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.

Table 6 Ball/Pad Description

Note: ZQ1, CKE1_A, CKE1_B, CS1_A, and CS1_B balls are reserved for 2-rank package. For 1-rank package those balls are NC.

2.6 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard temperature range.

Parameter/Condition	Symbol	Power	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin;CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ,ODT disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK = tCKmin;CKE is LOW;CS is LOW;All banks are idle;CA bus inputs are switching;Data bus inputs are stable,ODT disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stop:CK_t =LOW, CK_c =HIGH;CKE is LOW;CS is LOW;All banks are idle;CA bus inputs are sta- ble;Data bus inputs are stable,ODT disabled	IDD2PS	VDD1	
	IDD2PS	VDD2	
	IDD2PS	VDDQ	3
Idle non power-down standby current:tCK = tCKmin;CKE is HIGH; CS is LOW;All banks are idle;CA bus inputs are switching;Data bus inputs are stable,ODT disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Idle non power-down standby current with clock stopped:CK_t=LOW; CK_c=HIGH;CKE is HIGH;CS is LOW;All banks are idle;CA bus inputs are stable;Data bus inputs are	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NS	VDDQ	3
Active power-down standby current:tCK = tCKmin;CKE is LOW;CS is LOW;One bank is active;CA bus inputs are switching;Data bus inputs are stable, ODT disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stop:CK_t=LOW, CK_ c=HIGH;CKE is LOW;CS is LOW;One bank is active;CA bus inputs are stable;Data bus inputs are stable,ODT disabled	IDD3PS	VDD1	
	IDD3PS	VDD2	
	IDD3PS	VDDQ	4
Active non-power-down standby current:tCK = tCKmin;CKE is HIGH;CS is LOW;One bank is active;CA bus inputs are switching; Data bus inputs are stable,ODT disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped:CK_t=LOW, CK_c=HIGH;CKE is HIGH;CS is LOW; One bank is active;CA bus inputs are stable;Data bus inputs	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Operating burst READ current:tCK = tCKmin;CS is LOW between valid commands;One bank is active;BL = 16 or 32; RL = RL(MIN);CA businputs are switching;50% data change each burst	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Operating burst WRITE current:tCK = tCKmin;CS is LOW between valid commands;One bank is active;BL = 16 or 32; WL = WLmin;CA bus inputs are switching;50% data change each burst transfer ODT	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All bank REFRESH Burst current:tCK = tCKmin;CKE is HIGH between valid commands;tRC = tRFCabmin;Burst refresh;CA bus inputs are switching;- Data bus inputs are stable;ODT disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4
All bank REFRESH Average current:tCK = tCKmin;CKE is HIGH between valid commands;tRC = tREFI;CA bus inputs are switching;Data bus inputs are stable;ODT disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5AB	VDDQ	4
Per bank REFRESH Average current:tCK = tCKmin; CKE is HIGH between valid commands;tRC = tREFI/8;CA bus inputs are switching;Data bus inputs are stable;ODT disabled	IDD5PB1	VDD1	
	IDD5PB2	VDD2	
	IDD5PB	VDDQ	4

Parameter/Condition	Symbol	Power	Note
Power Down Self Refresh current (-25 ° C to +85 ° C):CK_t=LOW, CK_ c=HIGH;CKE is LOW;CA bus inputs are stable;Data bus inputs are sta- ble;Maximum 1x Self Refresh	IDD61	VDD1	6,7,8,1
	IDD62	VDD2	6,7,8,1
	IDD6Q	VDDQ	4,6,7,8,
Power Down Self Refresh current (+85 ° C to +105 ° C): CK_t=LOW, CK_c=HIGH;CKE is LOW;CA bus inputs arestable;	IDD6ET1	VDD1	7,8,11
	IDD6ET2	VDD2	7,8,11
	IDD6ET	VDDQ	4,7,8,1

Note:

1. DBI Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 Ω.
6. The 1x Self Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
9. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
10. IDD6 85 °C is guaranteed, IDD6 45 °C is typical of the distribution of the arithmetic mean.
11. IDD6ET is a typical value, is sampled only, and is not tested.
12. Dual Channel devices are specified in dual channel operation (both channels operating together).

Table 7 IDD Specification Parameters and Operating Conditions

2.7 IDD Parameters Single Die

VDD2 =1.06–1.17V, VDDQ = 0.57–0.65V or VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V

Symbol	Supply	4266 Mbps	Unit	Note
I_{DD01}	V_{DD1}	2.46	mA	
I_{DD02}	V_{DD2}	44.47		
I_{DD0Q}	V_{DDQ}	1.20		
I_{DD2P1}	V_{DD1}	0.26	mA	
I_{DD2P2}	V_{DD2}	1.39		
I_{DD2PQ}	V_{DDQ}	1.20		
I_{DD2PS1}	V_{DD1}	0.26	mA	
I_{DD2PS2}	V_{DD2}	1.39		
I_{DD2PSQ}	V_{DDQ}	1.20		
I_{DD2N1}	V_{DD1}	0.26	mA	
I_{DD2N2}	V_{DD2}	21.01		
I_{DD2NQ}	V_{DDQ}	1.20		
I_{DD2NS1}	V_{DD1}	0.26	mA	
I_{DD2NS}	V_{DD2}	15.10		
I_{DD2NSQ}	V_{DDQ}	1.20		
I_{DD3P1}	V_{DD1}	0.29	mA	
I_{DD3P2}	V_{DD2}	5.10		
I_{DD3PQ}	V_{DDQ}	1.20		
I_{DD3PS1}	V_{DD1}	0.29	mA	
I_{DD3PS2}	V_{DD2}	5.10		
I_{DD3PSQ}	V_{DDQ}	1.20		
I_{DD3N1}	V_{DD1}	0.86	mA	
I_{DD3N2}	V_{DD2}	29.08		
I_{DD3NQ}	V_{DDQ}	1.20		
I_{DD3NS1}	V_{DD1}	0.86	mA	
I_{DD3NS2}	V_{DD2}	19.80		
I_{DD3NSQ}	V_{DDQ}	1.20		
I_{DD4W1}	V_{DD1}	2.50	mA	
I_{DD4W2}	V_{DD2}	220.25		
I_{DD4WQ}	V_{DDQ}	1.20		
I_{DD4R1}	V_{DD1}	3.23	mA	
I_{DD4R2}	V_{DD2}	264.86		
I_{DD4RQ}	V_{DDQ}	85.00		

Symbol	Supply	4266 Mbps	Unit	Note
I_{DD51}	V_{DD1}	9.86	mA	
I_{DD52}	V_{DD2}	109.60		
I_{DD5Q}	V_{DDQ}	1.20		
I_{DD5AB1}	V_{DD1}	0.97	mA	
I_{DD5AB2}	V_{DD2}	27.11		
I_{DD5ABQ}	V_{DDQ}	1.20		
I_{DD5PB1}	V_{DD1}	1.08	mA	
I_{DD5PB2}	V_{DD2}	27.61		
I_{DD5PBQ}	V_{DDQ}	1.20		

Table 8 IDD Parameters – Single-Die

Notes:

1. Published IDD values except IDD4RQ are the maximum IDD values considering the worst- case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. IDD4RQ value is reference only. Typical value. VOH = 0.5 × VDDQ; TC = 25°C
4. IDD values reflect dual-channel operation with the same pattern for each channel.

VDD2 =1.06–1.17V, VDDQ = 0.57–0.65V or VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V

Temperatur	Symbol	Supply	Full-Array Self Refresh Current	Unit	Note
25°C	I_{DD61}	V_{DD1}	0.28	mA	
	I_{DD62}	V_{DD2}	1.22		
	I_{DD6Q}	V_{DDQ}	0.10		
85°C	I_{DD61}	V_{DD1}	0.61	mA	
	I_{DD62}	V_{DD2}	4.92		
	I_{DD6Q}	V_{DDQ}	0.10		

Table 9 IDD6 Full-Array Self Refresh Current

Notes:

1. I_{DD6} 25°C is the typical value in the distribution with nominal VDD and a reference only value. IDD6 85°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. I_{DD} values reflect dual-channel operation with the same pattern for each channel.

3. AC Timing

3.1 AC Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate 1600	3200	3733	4267	Unit
Average clock period	^{t}CK(AVG)	Min	1250	625	535	468	ps
		Max	100	100	100	100	ns
Average HIGH pulse width	^{t}CH(AVG)	Min	0.46				^{t}CK(AVG)
		Max	0.54				
Average LOW pulse width	^{t}CL(AVG)	Min	0.46				^{t}CK(AVG)
		Max	0.54				
Absolute clock period	^{t}CK(ABS)	Min	^{t}CK(AVG)min + ^{t}JIT(per)min				ps
Absolute clock HIGH pulse width	^{t}CH(ABS)	Min	0.43				^{t}CK(AVG)
		Max	0.57				
Absolute clock LOW pulse width	^{t}CL(ABS)	Min	0.43				^{t}CK(AVG)
		Max	0.57				
Clock period jitter	^{t}JIT(per)allowed	Min	–70	–40	–34	–30	ps
		Max	70	40	34	30	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	^{t}JIT(cc)allowed	Max	140	80	68	60	ps

Table 10 Clock Timing

Parameter	Symbol	Min/ Max	Data Rate 533	1066	1600	2133	2667	3200	3733	4267	Unit	Notes
DQS output access time from CK_t/CK_c	^{t}DQSCK	Min	1500								ps	1
		Max	3500									
DQS output access time from CK_t/CK_c - voltage variation	^{t}DQSCK_VOLT	Max	7								ps/mV	2
DQS output access time from CK_t/CK_c - temper-ature variation	^{t}DQSCK_TEMP	Max	4								ps/°C	3
CK to DQS rank to rank variation	^{t}DQSCK_rank2rank	Max	1.0								ns	4, 5
DQS_t, DQS_c to DQ skew total, per group, per access (DBIDisabled)	^{t}DQSQ	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	^{t}QH	Min	MIN(^{t}QSH, ^{t}QSL)								ps	6

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Data output valid window time total, per pin (DBI-Disabled)	tQW_total	Min	0.75			0.73		0.70			UI	6, 11
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	Min	MIN(tQSH_DBI, tQSL_DBI)								ps	6
Data output valid window time total, per pin (DBI-Enabled)	tQW_total_DBI	Min	0.75			0.73		0.70			UI	6, 11
DQS_t, DQS_c differential output LOW time (DBI- Disabled)	tQSL	Min	tCL(ABS) - 0.05								tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI-Disabled)	tQSH	Min	tCH(ABS) - 0.05								tCK(AVG)	10, 11
DQS_t, DQS_c differential output LOW time (DBI-Enabled)	tQSL-DBI	Min	tCL(ABS) - 0.045								tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI-Enabled)	tQSH-DBI	Min	tCH(ABS) - 0.045								tCK(AVG)	10, 11
Read preamble	tRPRE	Min	1.8								tCK(AVG)	
Read postamble	tRPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(AVG)	
DQS Low-Z from clock	tLZ(DQS)	Min	(RL × tCK) + tDQSCK(MIN) - (tRPRE(MAX) × tCK) - 200ps								ps	
DQ Low-Z from clock	tLZ(DQ)	Min	(RL × tCK) + tDQSCK(MIN) - 200ps								ps	
DQS High-Z from clock	tHZ(DQS)	Max	(RL × tCK) + tDQSCK(MAX)+(BL/2 × tCK) + (tRPST(MAX) × tCK) - 100ps								ps	
DQ High-Z from clock	tHZ(DQ)	Max	(RL × tCK) + tDQSCK(MAX) + tDQSQ(MAX) + (BL/2 × tCK) - 100ps								ps	

Table 11 Read Output Timing

Notes:

1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.
2. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQand VDD2. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the MAX[ABS(tDQSCK(MIN)@V1 - tDQSCK(MAX)@V2), ABS(tDQSCK(MAX)@V1 - tDQSCK(MIN)@V2)]/ABS(V1 - V2).
3. tDQSCK_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to tDQSCK_rank2rank.
5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.

6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a spec-ified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. ^{t}QSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
10. ^{t}QSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN ^{t}CH(ABS) and ^{t}CL(ABS). When the input clock jitter MIN ^{t}CH(ABS) and ^{t}CL(ABS) is 0.44 or greater than ^{t}CK(AVG), the minimum value of ^{t}QSL will be ^{t}CL(ABS) - 0.04 and ^{t}QSH will be ^{t}CH(ABS) - 0.04.

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Rx timing window total at V_{dIVW} voltage levels	TdIVW_-total	Max	0.22					0.25			UI	1, 2, 3
DQ and DMI input pulse width (at V_{CENT_DQ})	TdIPW	Min	0.45								UI	7
DQ-to-DQS offset	^{t}DQS2DQ	Min	200								ps	6
		Max	800									
DQ-to-DQ offset	^{t}DQDQ	Max	30								ps	7
DQ-to-DQS offset temperature variation	^{t}DQS2DQ_temp	Max	0.6								ps/°C	8
DQ-to-DQS offset voltage variation	^{t}DQS2DQ_volt	Max	33								ps/50mV	9
DQ-to-DQS offset rank to rank variation	^{t}DQS2DQ_rank2rank	Max	200								ps	10, 11
WRITE command to first DQS transition	^{t}DQSS	Min	0.75								^{t}CK(AVG)	
		Max	1.25									
DQS input HIGH-level width	^{t}DQSH	Min	0.4								^{t}CK(AVG)	
DQS input LOW-level width	^{t}DQSL	Min	0.4								^{t}CK(AVG)	
DQS falling edge to CK setup time	^{t}DSS	Min	0.2								^{t}CK(AVG)	
DQS falling edge from CK hold time	^{t}DSH	Min	0.2								^{t}CK(AVG)	
Write postamble	^{t}WPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								^{t}CK(AVG)	
Write preamble	^{t}WPRE	Min	1.8								^{t}CK(AVG)	

Table 12 Write Timing

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx differential DQ-to-DQS jitter total timing window at the VdIVW voltage levels.

3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(DQ)}$ range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the $V_{CENT\_DQ(pin\_mid)}$.
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.
7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. ^{t}DQS2DQ(MAX) delay variation as a function of temperature.
9. ^{t}DQS2DQ(MAX) delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.
10. The same voltage and temperature are applied to ^{t}DQS2DQ_rank2rank.
11. ^{t}DQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
12. UI = ^{t}CK(AVG)(MIN)/2.

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
CKE minimum pulse width (HIGH and LOW pulse width)	^{t}CKE	Min	MAX(7.5ns, 4*n*CK)				ns	1
Delay from valid command to CKE input LOW	^{t}CMDCKE	Min	MAX(1.75ns, 3*n*CK)				ns	1
Valid clock requirement after CKE input LOW	^{t}CKELCK	Min	MAX(5ns,5*n*CK)				ns	1
Valid CS requirement before CKE input LOW	^{t}CSCKE	Min	1.75				ns	
Valid CS requirement after CKE input LOW	^{t}CKELCS	Min	MAX(5ns,5*n*CK)				ns	1
Valid Clock requirement before CKE Input HIGH	^{t}CKCKEH	Min	MAX(1.75ns, 3*n*CK)				ns	1
Exit power-down to next valid command delay	^{t}XP	Min	MAX(7.5ns, 5*n*CK)				ns	1
Valid CS requirement before CKE input HIGH	^{t}CSCKEH	Min	1.75				ns	
Valid CS requirement after CKE input HIGH	^{t}CKEHCS	Min	MAX(7.5ns, 5*n*CK)				ns	1
Valid clock and CS requirement after CKE input LOW after MRW command	^{t}MRWCKEL	Min	MAX(14ns, 10*n*CK)				ns	1
Valid clock and CS requirement after CKE input LOW after ZQCAL START command	^{t}ZQCKE	Min	MAX(1.75ns, 3*n*CK)				ns	1

Table 13 CKE Input Timing

Note:

1. Delay time has to satisfy both analog time(ns) and clock count (*n*CK). For example, ^{t}CMDCKE will not expire until CK has toggled through at least 3 full cycles (3tCK) and 3.75ns has transpired. The case that 3nCK is applied to is shown below

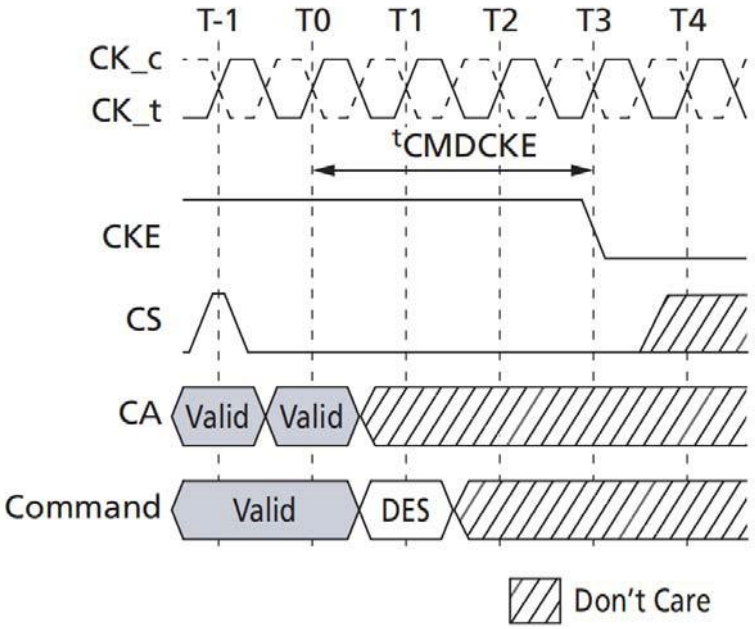


Figure 5 tCMDCKE Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Command/address valid window (referenced from CA V_{IL}/V_{IH} to CK V_{IX})	^{t}CIVW	Min	0.3								^{t}CK(AVG)	1, 2, 3
Address and control input pulse width (referenced to V_{REF})	^{t}CIPW	Min	0.55	0.55	0.55	0.6	0.6	0.6	0.6	0.6	^{t}CK(AVG)	4

Table 14 Command Address Input Timing

Notes: 1. CA Rx mask timing parameters at the pin including voltage and temperature drift.

2. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(CA)}$ range irre-spective of the input signal common mode.
4. CA only minimum input pulse width defined at the V_{CENT_CA}(pin mid).

Parameter	Symbol	Min/ Max	Value	Unit
Clock cycle time	^{t}CKb	Min	18	ns
		Max	100	
DQS output data acess time from CK	^{t}DQSCKb	Min	1.0	ns
		Max	10.0	
DQS edge to output data edge	^{t}DQSQb	Max	1.2	ns

Table 15 Boot Timing Parameters (10–55 MHz)

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
MODE REGISTER WRITE (MRW) command period	^{t}MRW	Min	MAX(10ns, 10nCK)				ns
MODE REGISTER SET command delay	^{t}MRD	Min	MAX(14ns, 10nCK)				ns
MODE REGISTER READ (MRR) com-mand period	^{t}MRR	Min	8				^{t}CK(AVG)
Additional time after ^{t}XP has expired until the MRR command may be issued	^{t}MRRI	Min	^{t}RCD(MIN) + 3nCK				ns
Delay from MRW command to DQS driven out	^{t}SDO	Max	MAX(12nCK, 20ns)				ns

Table 16 Mode Register Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
READ latency (DBI dis-abled)	RL-A	Min	6	10	14	20	24	28	32	36	^{t}CK(AVG)	
READ latency (DBI enabled)	RL-B	Min	6	12	16	22	28	32	36	40	^{t}CK(AVG)	
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	16	18	^{t}CK(AVG)	
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	30	34	^{t}CK(AVG)	
ACTIVATE-to-ACTIVATE command period (same bank)	^{t}RC	Min	^{t}RAS + ^{t}RPab (with all-bank precharge) ^{t}RAS + ^{t}RPpb (with per-bank precharge)								ns	
Minimum self refresh time (entry to exit)	^{t}SR	Min	MAX(15ns, 3nCK)								ns	
Self refresh exit to next valid command delay	^{t}XSR	Min	MAX(^{t}RFCab + 7.5ns, 2nCK)								ns	
CAS-to-CAS delay	^{t}CCD	Min	8								^{t}CK(AVG)	
CAS-to-CAS delay masked write	^{t}CCDMW	Min	32								^{t}CK(AVG)	
Internal READ-to-PRE-CHARGE command delay	^{t}RTP	Min	MAX(7.5ns, 8nCK)								ns	
RAS-to-CAS delay	^{t}RCD	Min	MAX(18ns, 4nCK)								ns	
Row precharge time (sin-gle bank)	^{t}RPpb	Min	MAX(18ns, 3nCK)								ns	
Row precharge time (all banks)	^{t}RPab	Min	MAX(21ns, 3nCK)								ns	

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Row active time	^{t}RAS	Min	MAX(42ns, 3nCK)								ns	
		Max	MIN(9 × ^{t}REFI × Refresh Rate, 70.2)								µs	
Write recoverytime	^{t}WR	Min	MAX(18ns, 4nCK)								ns	
Write-to-read delay	^{t}WTR	Min	MAX(10ns, 8nCK)								ns	
Active bank A to active bank B	^{t}RRD	Min	MAX(10ns, 4nCK)							MAX(7.5ns, 4nCK)	ns	1
Precharge-to-precharge delay	^{t}PPD	Min	4								^{t}CK(AVG)	2
Four-bank activate win-dow	^{t}FAW	Min	40							30	ns	1
Delay from SRE com-mand to CKE input LOW	^{t}ESCKE	Min	MAX(1.75ns, 3nCK)								-	3

Table 17 Core Timing Parameters

Notes:

1. 4267 Mb/s timing value is supported at lower data rates if the device is supporting 4266 Mb/s speed grade.
2. Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
3. Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

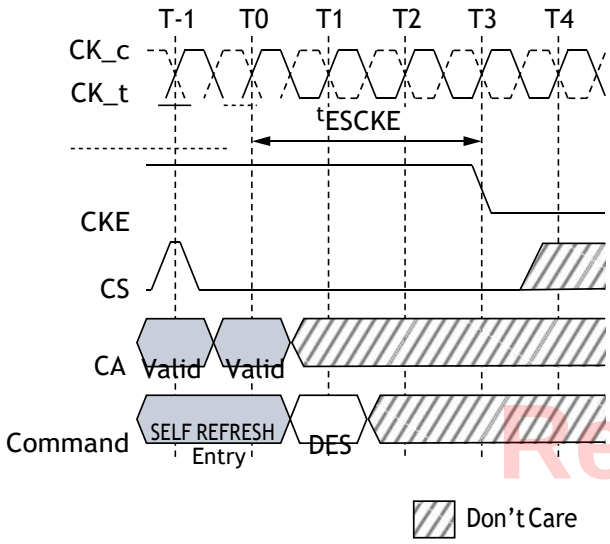


Figure 6: ^{t}ESCKE Timing

4. The refresh rate is determined by the value in MR4 OP[2:0].

Parameter	Symbol	Min/ Max	Data Rate
			533-4267
CA ODT value update time	^{t}ODTUP	Min	RU(20ns/^{t}CK(AVG))

Table 18 CA Bus ODT Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
Valid clock requirement after CKE input LOW	^{t}CKELCK	Min	MAX(5ns, 5*n*CK)				^{t}CK	
Data setup for VREF training mode	^{t}DStrain	Min	2				ns	
Data hold for VREF training mode	^{t}DHtrain	Min	2				ns	
Asynchronous data read	^{t}ADR	Max	20				ns	
CA BUS TRAINING com-mand-to-command delay	^{t}CACD	Min	RU(^{t}ADR/^{t}CK)				^{t}CK	1
Valid strobe requirement before CKE LOW	^{t}DQSCKE	Min	10				ns	
First CA BUS TRAINING command following CKE LOW	^{t}CAENT	Min	250				ns	
V_{REF} step time – multiple steps	^{t}VREFca_LONG	Max	250				ns	
VREF step time – one step	^{t}VREF-ca_SHORT	Max	80				ns	
Valid clock requirement before CS HIGH	^{t}CKPRECS	Min	2^{t}CK + ^{t}XP				-	
Valid clock requirement after CS HIGH	^{t}CKPSTCS	Min	MAX(7.5ns, 5*n*CK)				-	
Minimum delay from CS to DQS tog-gle in command bus training	^{t}CS_VREF	Min	2				^{t}CK	
Minimum delay from CKE HIGH to strobe High-Z	^{t}CKEHDQS	Min	10				ns	
CA bus training CKE HIGH to DQ tri-state	^{t}MRZ	Min	1.5				ns	
ODT turn-on latency from CKE	^{t}CKELODTon	Min	20				ns	
ODT turn-off latency from CKE	^{t}CKEHODToff	Min	20				ns	
Exit command bus training mode to next valid command delay	^{t}XCBT_Short	Min	MAX(200ns, 5*n*CK)				-	2
	^{t}XCBT_Middle	Min	MAX(200ns, 5*n*CK)				-	2
	^{t}XCBT_Long	Min	MAX(250ns, 5*n*CK)				-	2

Table 19 CA Bus Training Parameters

Notes:

1. If ^{t}CACD is violated, the data for samples which violate ^{t}CACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
2. Exit command bus training mode to next valid command delay time depends on value of $V_{REF(CA)}$ setting: MR12 OP[5:0] and $V_{REF(CA)}$ range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in ^{t}FC value mapping table. Additionally exit command bus training mode to next valid command delay time may affect $V_{REF(DQ)}$ setting. Settling time of $V_{REF(DQ)}$ level is same as $V_{REF(CA)}$ level.

Symbol	800–2133 MHz	Unit
^{t}ODTon(MIN)	1.5	ns
^{t}ODTon(MAX)	3.5	ns
^{t}ODToff(MIN)	1.5	ns
^{t}ODToff(MAX)	3.5	ns

Table 20 Asynchronous ODT Turn On and Turn Off Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
DQS output access time from CK_t/CK_c (derated)	^{t}DQSCKd	Max	3600				ps
RAS-to-CAS delay (derated)	^{t}RCDd	Min	^{t}RCD + 1.875				ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	^{t}RCd	Min	^{t}RC + 3.75				ns
Row active time (derated)	^{t}RASd	Min	^{t}RAS + 1.875				ns
Row precharge time (derated)	^{t}RPd	Min	^{t}RP + 1.875				ns
Active bank A to active bank B (derated)	^{t}RRDd	Min	^{t}RRD + 1.875				ns

Table 21 Temperature Derating Parameters

Note:

1. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b.

3.2 CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

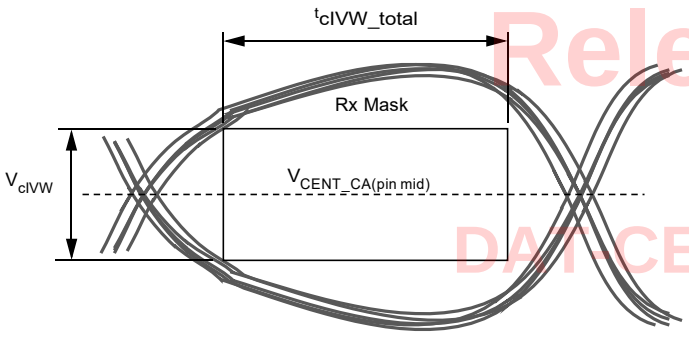


Figure 7 CA Receiver (Rx) Mask

4. CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

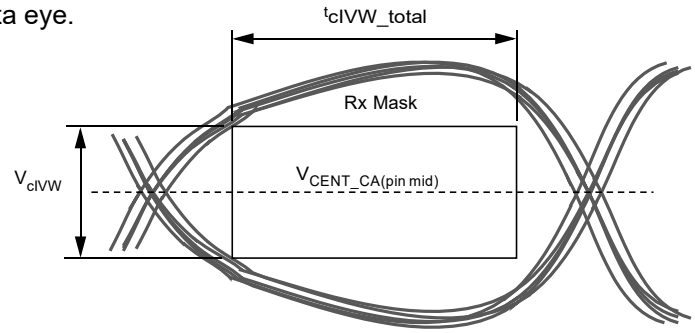


Figure 8 CA Receiver (Rx) Mask

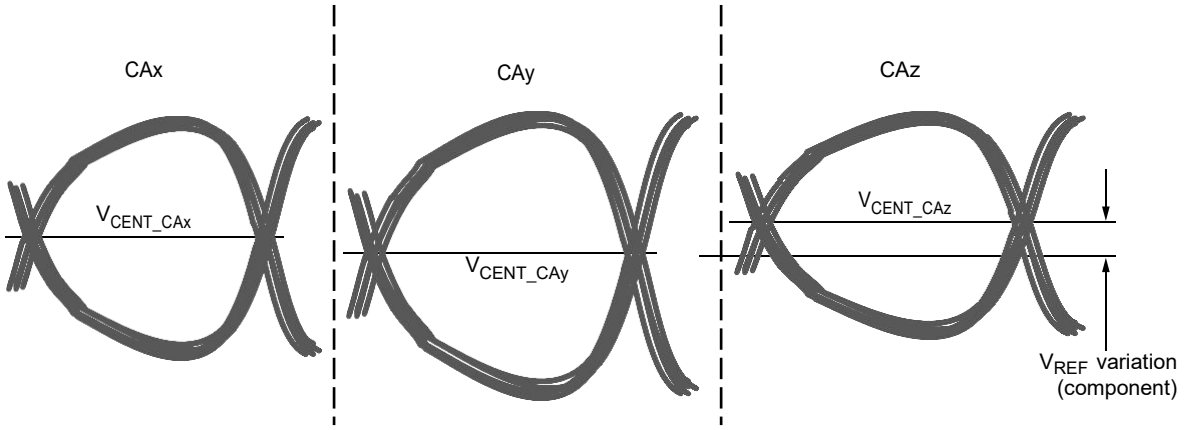
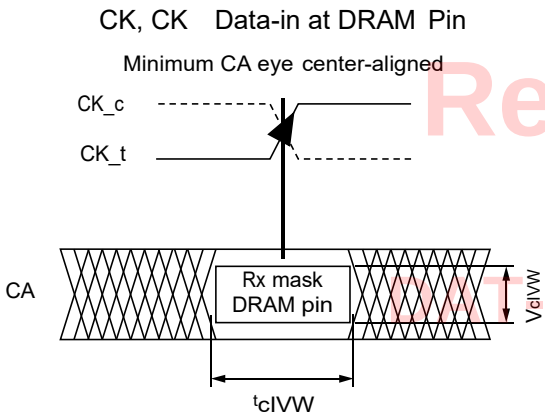


Figure 9 Across Pin $V_{REF\ (CA)}$ Voltage Variation

$V_{CENT\_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{CENT_CA} voltage level and the smallest V_{CENT_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{CENT} level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.



TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Figure 10 CA Timings at the DRAM Pins

Note:

1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around VCENT_CA(pin mid).

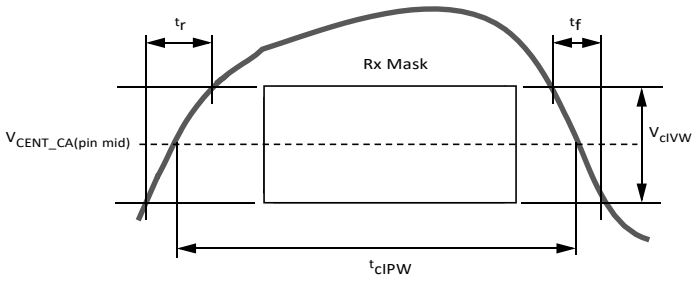


Figure 11CA ^{t}cIPW and SRIN_cIVW Definition (for Each Input Pulse)

Note:

1. SRIN_cIVW = V_{dIVW_total}/(^{t}r or ^{t}f); signal must be monotonic within ^{t}r and ^{t}f range.

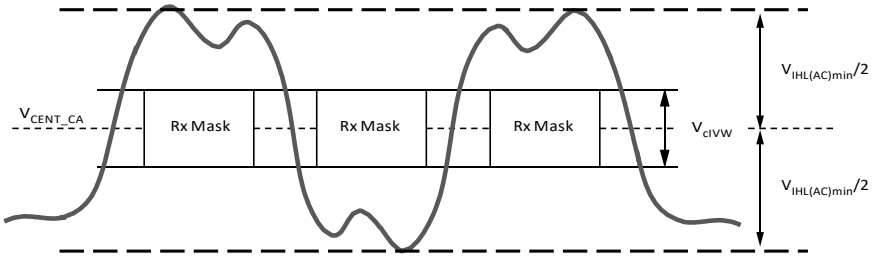


Figure 12 CA V_{IHL_AC}Definition (for Each Input Pulse)

Symbol	Parameter	DQ –1333[7]		DQ – 1600/1867		DQ – 3200/3733		DQ –4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{cIVW}	Rx mask voltage peak-to-peak	–	175	–	175	–	155	–	145	mV	1, 2, 3
$V_{IHL(AC)}$	CA AC input pulse amplitude peak-to-peak	210	–	210	–	190	–	180	–	mV	4, 6
SRIN_-cIVW	Input slew rate over V_{cIVW}	1	7	1	7	1	7	1	7	V/ns	5

Table 22 DRAM CMD/ADR, CS

Notes:

1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx mask voltage V_{cIVW} total(MAX) must be centered around $V_{CENT\_CA(pin\ mid)}$.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(CA)}$ range irrespective of the input signal common mode.
4. CA-only input pulse signal amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT\_CA(pin\ mid)}$, such that $V_{IHL(AC)}$/2 (MIN) must be met both above and below V_{CENT_CA}.
5. Input slew rate over V_{cIVW} mask is centered at $V_{CENT\_CA(pin\ mid)}$.
6. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
7. The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the ^{t}cIVW (ps) = 450ps at or below 1333 operating frequencies.
8. UI = ^{t}CK(AVG)MIN.

5. DQ Tx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask (V_{dIVW_total}, TdIVW_total) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

5.1 DRAM Data Timing

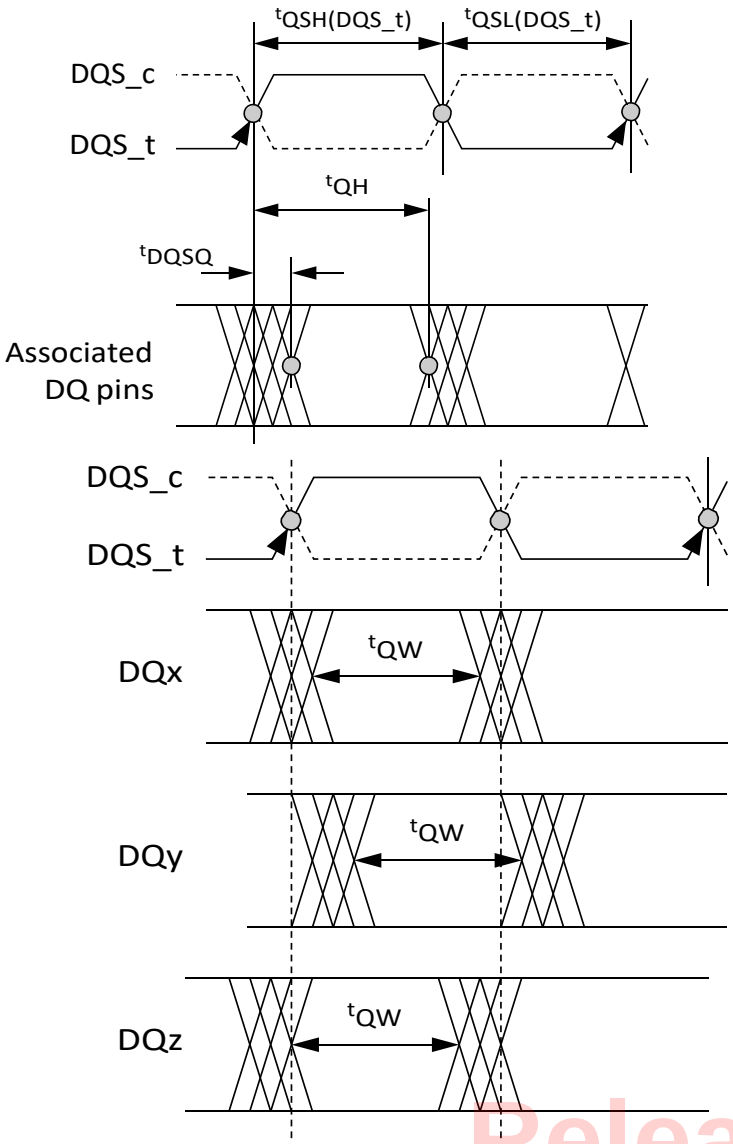


Figure 13 Read Data Timing Definitions – ^{t}QH and ^{t}DQSQ Across DQ Signals per DQS Group

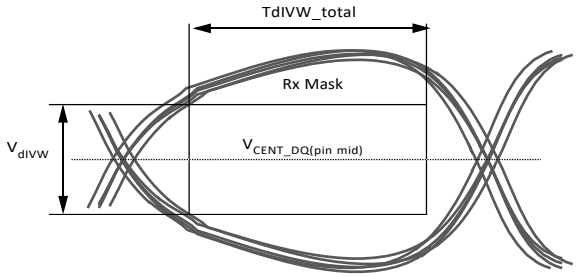


Figure 14 DQ Receiver (Rx) Mask

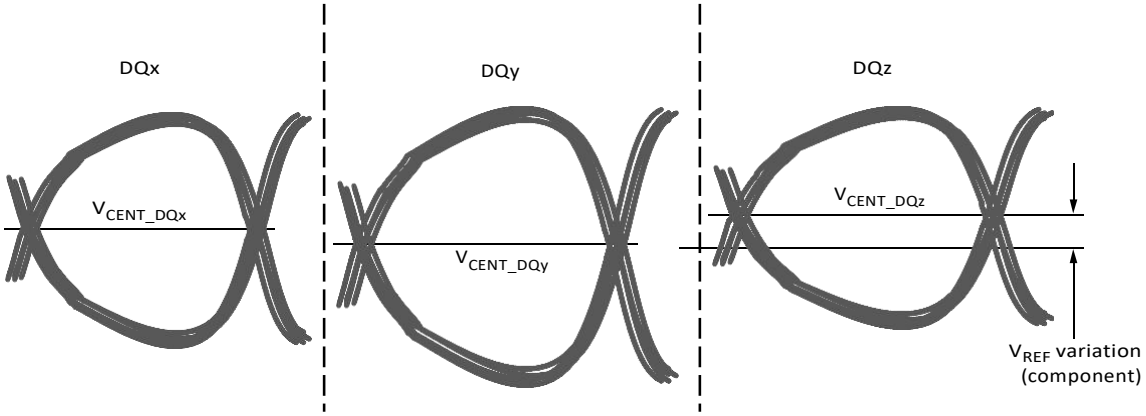


Figure 15 Across Pin V_{REF} DQ Voltage Variation

$V_{CENT\_DQ(pin\_mid)}$ is defined as the midpoint between the largest V_{CENT_DQ} voltage level and the smallest V_{CENT_DQ} voltage level across all DQ pins for a given DRAM component. Each V_{CENT_DQ} is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

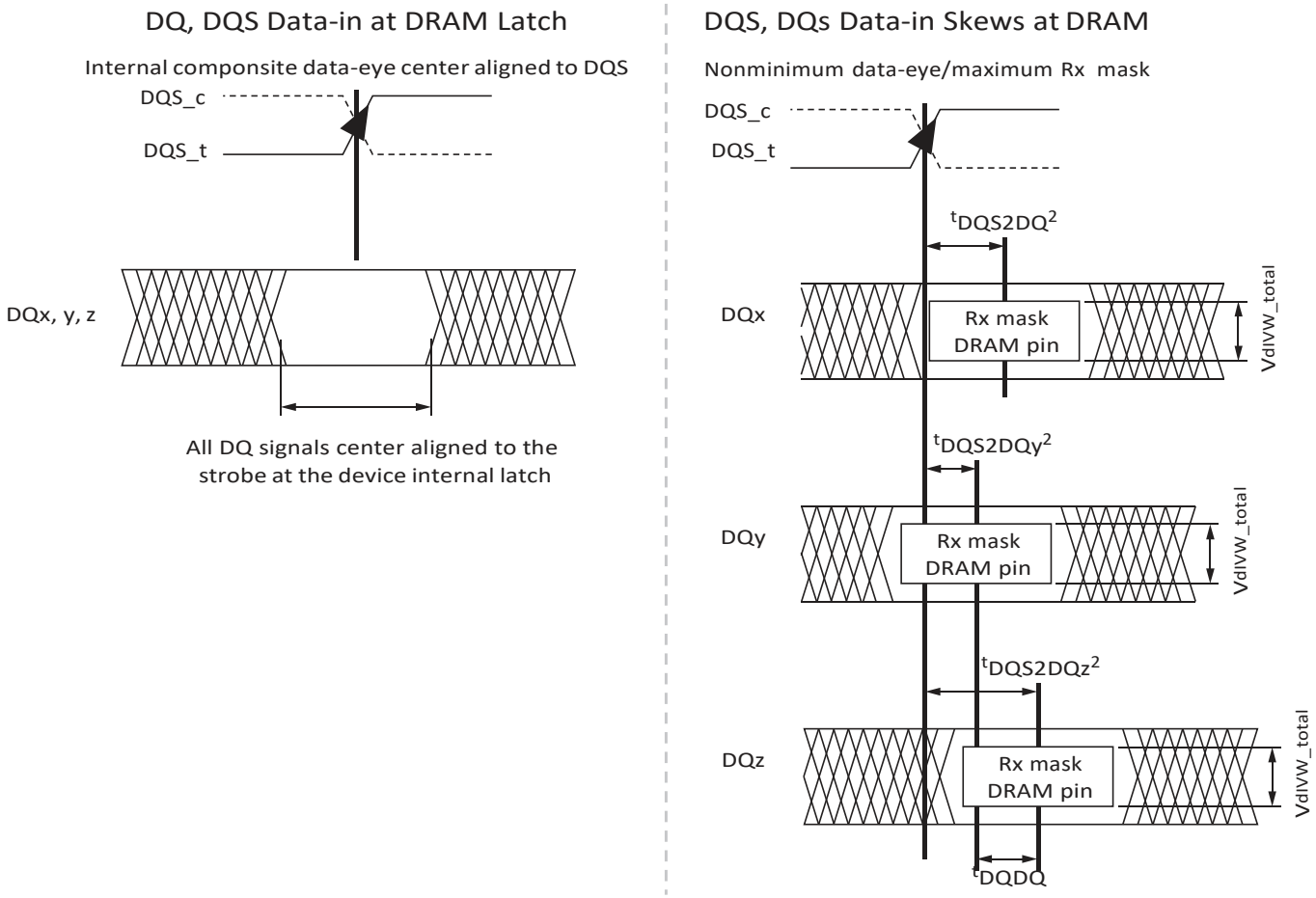


Figure 16 DQ-to-DQS ^{t}DQS2DQ and ^{t}DQDQ

Notes:

1. These timings at the DRAM pins are referenced from the internal latch.
2. tDQS2DQ is measured at the center (midpoint) of the TdIVW window.
3. DQz represents the MAX tDQS2DQ in this example.
4. DQy represents the MIN tDQS2DQ in this example.

All of the timing terms in DQ to DQS_t are measured from the DQS_t/DQS_c to the center (midpoint) of the TdIVW window taken at the V_{dIVW_total} voltage levels centered around $V_{CENT\_DQ(pin\_mid)}$. In figure above, the timings at the pins are referenced with respect to all DQ signals center-aligned to the DRAM internal latch. The data-to-data offset is defined as the difference between the MIN and MAX ^{t}DQS2DQ for a given component.

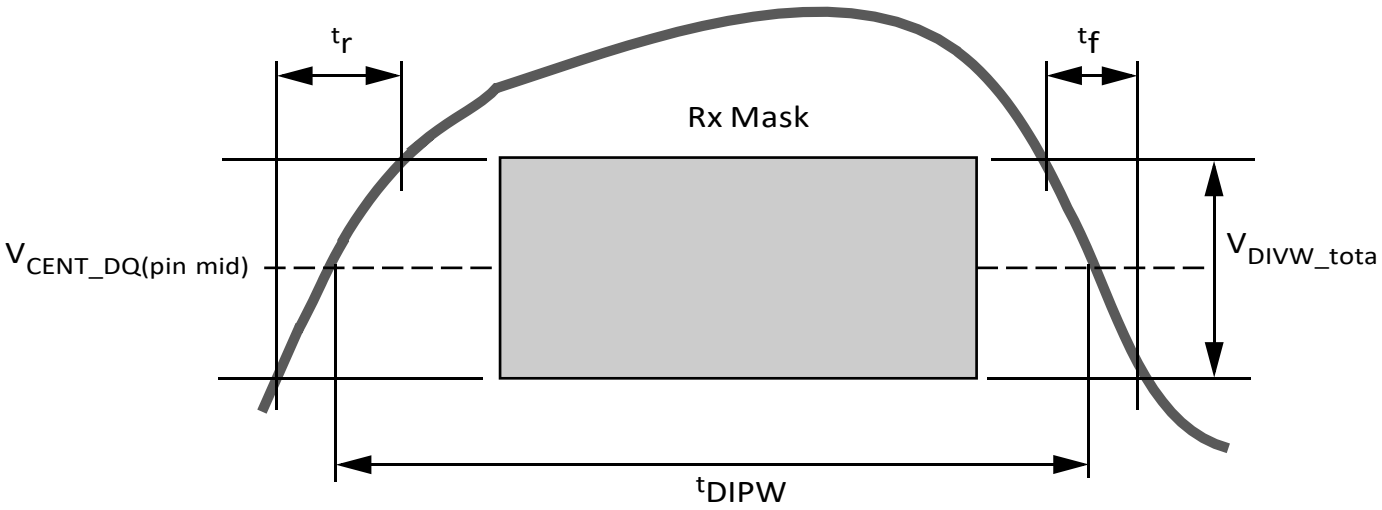
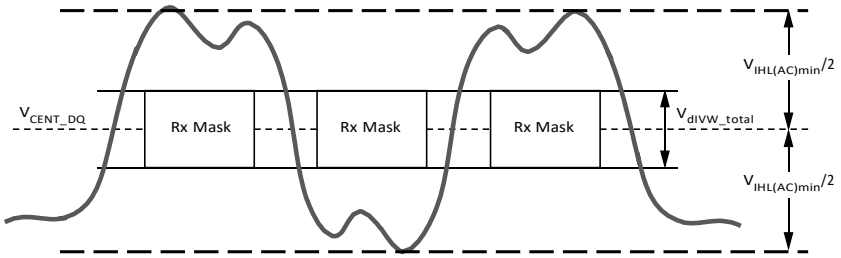


Figure 17 DQ tDIPW and SRIN_dIVW Definition for Each Input Pulse

$$UI = {}^{t}CK(AVG)\,MIN/2$$

Note:

1. SRIN_dIVW = V_{dIVW_total}/(^{t}r or ^{t}f) signal must be monotonic within ^{t}r and ^{t}f range.



Symbol	Parameter	1600/1867		2133/2400		3200/3733		4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{dIVW_total}	Rx mask voltage – peak-to-peak	–	140	–	140	–	140	–	120	mV	1, 2, 3
$V_{IHL(AC)}$	DQ AC input pulse amplitude peak-to-peak	180	–	180	–	180	–	170	–	mV	1, 7
SRIN_dIVW	Input slew rate over V_{dIVW_total}	1	7	1	7	1	7	1	7	V/ns	6

Table 23 DQs In Receive Mode

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx mask voltage VdIVW_total(MAX) must be centered around VCENT_DQ(pin_mid).
3. Defined over the DQ internal VREF range. The Rx mask at the pin must be within the internal VREF DQ range irre-spective of the input signal common mode.
4. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design.

5. DQ-only input pulse amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT\_DQ(pin\_mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_DQ}.
6. Input slew rate over V_{dIVW} mask centered at $V_{CENT\_DQ(pin\_mid)}$.
7. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
8. UI = $^{t}CK(AVG)(MIN)/2$.

6. Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Symbol	Description	Calculation	Notes
$^{t}CK(avg)$ and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit $^{t}CK(avg)$ represents the actual clock average $^{t}CK(avg)$ of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. $^{t}CK(avg)$ can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$t_{CK(avg)} = \left(\sum_{j=1}^{N} t_{CK_j}\right)/N$ Where N = 200	
$^{t}CK(abs)$	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
$^{t}CH(avg)$	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH(avg)} = \left(\sum_{j=1}^{N} t_{CH_j}\right)/(N \times t_{CK(avg)})$	
$^{t}CL(avg)$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left(\sum_{j=1}^{N} t_{CL_j}\right)/(N \times t_{CK(avg)})$	
$^{t}JIT(per)$	The single-period jitter defined as the largest deviation of any signal ^{t}CK from $^{t}CK(avg)$.	$t_{JIT(per)} = \min/\max \text{ of } \{t_{CK_i} - t_{CK(avg)}\}$ Where i = 1 to 200	1
$^{t}JIT(per),act$	The actual clock jitter for a given system.		
$^{t}JIT(per),allowed$	The specified clock period jitter allowance.		
$^{t}JIT(cc)$	The absolute difference in clock periods between two consecutive clock cycles. $^{t}JIT(cc)$ defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = \max \text{ of } \{t_{CK_{i+1}} - t_{CK_i}\}$	1
$^{t}ERR(nper)$	The cumulative error across *n* multiple consecutive cycles from $^{t}CK(avg)$.	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j}\right) - (n \times t_{CK(avg)})$	1
$^{t}ERR(nper),act$	The actual clock jitter over *n* cycles for a given system.		
$^{t}ERR(nper),allowed$	The specified clock jitter allowance over *n* cycles.		
$^{t}ERR(nper),min$	The minimum $^{t}ERR(nper)$.	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	2
$^{t}ERR(nper),max$	The maximum $^{t}ERR(nper)$.	$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$	2
$^{t}JIT(duty)$	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	$t_{JIT(duty),min} = MIN((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$ $t_{JIT(duty),max} = MAX((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$	

Table 24 Definitions and Calculations

Notes:

1. Not subject to production testing.
2. Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

6.1 tCK(abs), tCH(abs), and tCL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg),min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg),min	^{t}CK(avg)

Table 25 ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Notes:

1. ^{t}CK(avg),min is expressed in ps for this table.
2. tJIT(duty),min is a negative value.

7. Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (^{t}JIT(per)) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

7.1 Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support ^{t}nPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks, or ^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

7.2 Cycle Time Derating for Core Timing Parameters

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) and ^{t}ERR(^{t}nPARAM),act exceed ^{t}ERR(^{t}nPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{^{t}\text{PARAM} + {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{^{t}\text{nPARAM}} - {}^{t}\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

7.3 Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (^{t}nPARAM), clock cycle derating should be specified with ^{t}JIT(per).

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) plus (^{t}ERR(^{t}nPARAM),act) exceed the supported cumulative ^{t}ERR(^{t}nPARAM),allowed, derating is required. If the equation below results in a positive value for a core timing parameter (^{t}CORE), the required clock cycle derating will be that posi-tive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{^{t}\text{PARAM} + {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{\text{CK(avg)}\ ^{t}}\right\} - {}^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

7.4 Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (t_{IS}, t_{IH}, t_{ISb}, t_{IHb}) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the $t_{JIT(per)}$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

7.5 Clock Jitter Effects on READ Timing Parameters

t_{RPRE}

When the device is operated with input clock jitter, t_{RPRE} must be derated by the $t_{JIT(per),act,max}$ of the input clock that exceeds $t_{JIT(per),allowed,max}$. Output deratings are relative to the input clock:

$$t_{RPRE(min,derated)} = 0.9 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}}\right)$$

For example, if the measured jitter into a LPDDR4 device has $t_{CK(avg)}$ = 625ps, $t_{JIT(per),act,min}$ = –xx, and $t_{JIT(per),act,max}$ = +xx ps, then $t_{RPRE,min,derated}$ = 0.9 - ($t_{JIT(per),act,max}$ - $t_{JIT(per),allowed,max}$)/$t_{CK(avg)}$ = 0.9 - (xx - xx)/xx = yy $t_{CK(avg)}$.

$t_{LZ(DQ)}$,$t_{HZ(DQ)}$,t_{DQSCK},$t_{LZ(DQS)}$,$t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where:*n*= 0,1; and*m*= 0–15, and specified timings must be met with respect to that clock edge. Therefore, they are not affected by $t_{JIT(per)}$.

t_{QSH},t_{QSL}

These parameters are affected by duty cycle jitter, represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = MIN {($t_{QSH(abs)min}$ - $t_{DQSQmax}$), ($t_{QSL(abs)min}$ - $t_{DQSQmax}$)}. This minimum data valid window must be met at the target frequency regardless of clock jitter.

t_{RPST}

t_{RPST} is affected by duty cycle jitter, represented by $t_{CL(abs)}$. Therefore, $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$. $t_{RPST(abs)min}$ = $t_{CL(abs)min}$ - 0.05 = $t_{QSL(abs)min}$.

7.6 Clock Jitter Effects on WRITE Timing Parameters

t_{DS},t_{DH}

These parameters are measured from a data signal (DMI*n* or DQ*m*, where *n*= 0, 1 and *m*= 0–15) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: *n* = 0,1) crossing. The specification values are not affected by the amount of $t_{JIT(per)}$ applied, because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

t_{DSS},t_{DSH}

These parameters are measured from a data signal (DQS_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per)allowed}$.

t_{DQSS}

t_{DQSS} is measured from a data strobe signal (DQSn_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual $t_{JIT(per),act}$ of the input clock in excess of $t_{JIT(per)allowed}$.

$$t_{DQSS(min,derated)} = 0.75 - \left\{ \frac{t_{JIT(per),act,min} - t_{JIT(per),allowed}}{t_{CK(avg)}}, \text{ min} \right\}$$

$$t_{DQSS(max,derated)} = 1.25 - \left\{ \frac{t_{JIT(per),act,max} -}{t_{JIT(per),allowed, max}} \right\}$$

For example, if the measured jitter into an LPDDR4 device has tCK(avg) = 625ps, tJIT(per),act,min = -xxps, and tJIT(per),act,max = +xx ps, then:

$t_{DQSS,(min,derated)}$ = 0.75 - (-xx + yy)/625 = xxxx $t_{CK(avg)}$

$t_{DQSS,(max,derated)}$ = 1.25 - (xx – yy)/625 = xxxx $t_{CK(avg)}$