# 67. Apple Authentication 3.0 Coprocessor

## 67.1 Overview

Apple Authentication 3.0 Coprocessor (Auth 3.0 CP) is used to authenticate an accessory with devices running iOS 10.0.2 or later. See Accessory Authentication (page 196) for more information.

The Auth 3.0 CP is available in the following versions:

- XDFN, see XDFN Package (page 583).
- WLCSP, see WLCSP Package (page 585).

See Table 94-1 (page 755) for sample part numbers.

The Auth 3.0 CP Export Classification Control Number (ECCN) is EAR99. Both XDFN and WLCSP versions have a moisture sensitivity level (MSL) of 1.

## 67.2 Mechanical

This section provides technical details and tolerances for the Auth 3.0 CP chip.

### 67.2.1 XDFN Package

Figure 67-1 (page 584) shows the Auth 3.0 CP's package's layout, pad locations, and dimensional tolerances.

Figure 67-1 Auth 3.0 CP package (XDFN)

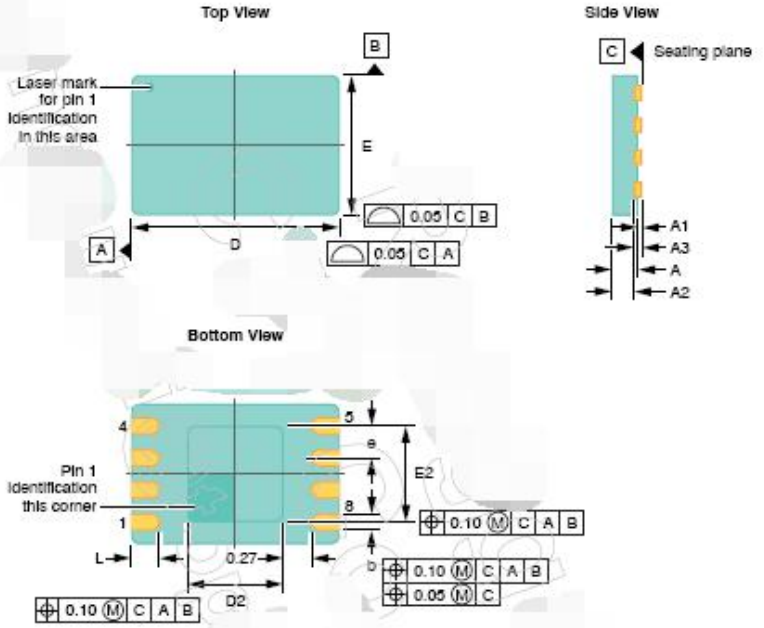



Table 67-1 Auth 3.0 CP dimensions (XDFN)

| Symbol | Minimum | Nominal | Maximum |
|---|---|---|---|
| A | | | 0.40 mm |
| A1 | | | 0.05 mm |
| A2 | | 0.23 mm | 0.28 mm |
| A3 | | 0.127 mm (REF) | |
| b | 0.18 mm | 0.25 mm | 0.30 mm |
| D | | 3.00 mm (BSC) | |
| D2 | 1.56 mm | 1.66 mm | 1.76 mm |
| E | | 2.00 mm (BSC) | |
| E2 | 1.40 mm | 1.50 mm | 1.60 mm |
| L | 0.35 mm | 0.40 mm | 0.45 mm |
| e | | 0.50 mm (BSC) | |

Figure 67-2 (page 585) and Table 67-2 (page 585) show the Auth 3.0 CP's recommended land pattern dimensions. The package includes a central paddle (exposed pad) that may be left not connected or may be connected to Ground.

Figure 67-2 Auth 3.0 CP land pattern dimensions (XDFN)

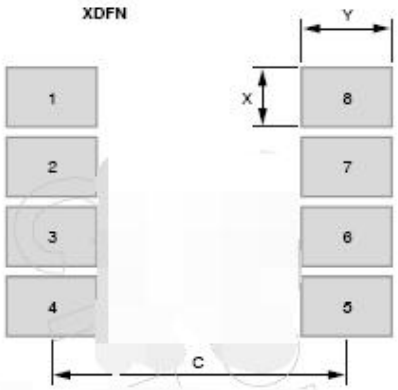



Table 67-2 Auth 3.0 CP land pattern dimensions (XDFN)

| Dimension/Symbol | Value |
|---|---|
| Body | 2 mm x 3 mm |
| Pitch | 0.50 mm |
| Lead Length | 0.45 mm |
| C | 2.90 mm |
| X | 0.30 mm |
| Y | 0.90 mm |

## 67.2.2 WLCSP Package

Figure 67-3 (page 586) shows the Auth 3.0 CP's package's layout, pad locations, and dimensional tolerances.

Figure 67-3 Auth 3.0 CP package (WLCSP)

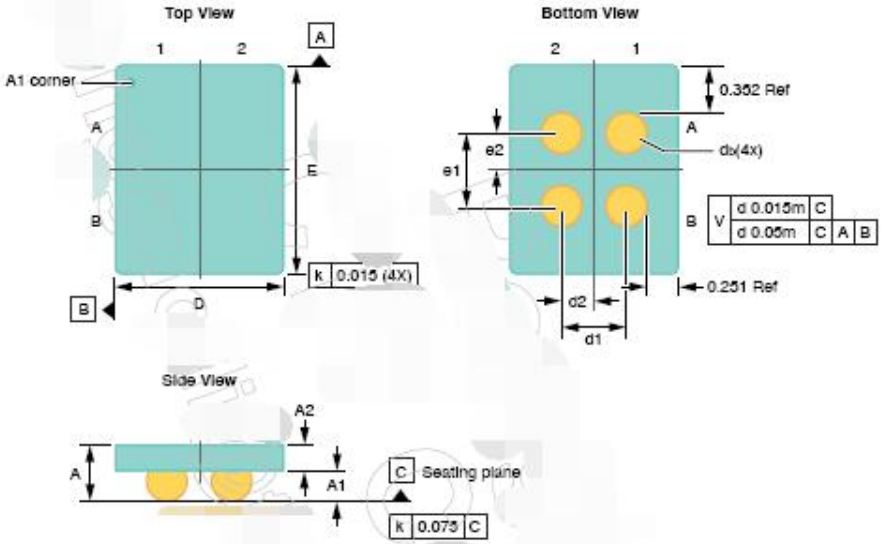



Table 67-3 Auth 3.0 CP dimensions (WLCSP)

| Symbol | Minimum | Nominal | Maximum |
|---|---|---|---|
| A | 0.330 mm | 0.360 mm | 0.390 mm |
| A1 | 0.160 mm | 0.175 mm | 0.190 mm |
| A2 | 0.170 mm | 0.185 mm | 0.200 mm |
| D | 1.122 mm | 1.152 mm | 1.182 mm |
| d1 | 0.400 mm (BSC) | | |
| d2 | 0.200 mm (BSC) | | |
| E | 1.424 mm | 1.454 mm | 1.484 mm |
| e1 | 0.500 mm (BSC) | | |
| e2 | 0.250 mm (BSC) | | |
| b | 0.230 mm | 0.250 mm | 0.270 mm |

The ball shear is 161 g/ball. Apple recommends mounting Auth 3.0 CP on a PCB with 227 µm diameter round pads.

## 67.2.3 Packing

Figure 67-4 (page 587) and Figure 67-5 (page 588) describe how the Auth 3.0 CP is delivered to accessory manufacturing facilities.

Figure 67-4 Auth 3.0 CP packing tape

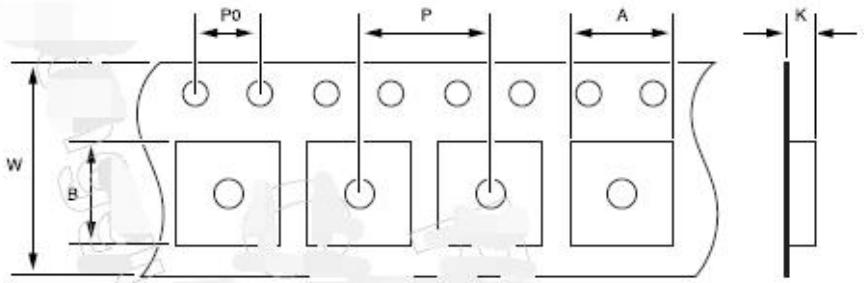



Table 67-4 Auth 3.0 CP packing tape dimensions (XDFN)

| Symbol | Minimum | Nominal | Maximum |
|---|---|---|---|
| P0 | 3.90 mm | 4.00 mm | 4.10 mm |
| P | 3.90 mm | 4.00 mm | 4.10 mm |
| A | 2.15 mm | 2.20 mm | 2.25 mm |
| B | 3.15 mm | 3.20 mm | 3.25 mm |
| K | 0.48 mm | 0.53 mm | 0.58 mm |
| W | 11.90 mm | 12.00 mm | 12.30 mm |

Table 67-5 Auth 3.0 CP packing tape dimensions (WLCSP)

| Symbol | Minimum | Nominal | Maximum |
|---|---|---|---|
| P0 | 3.90 mm | 4.00 mm | 4.10 mm |
| P | 1.95 mm | 2.00 mm | 2.05 mm |
| A | 1.24 mm | 1.29 mm | 1.34 mm |
| B | 1.54 mm | 1.59 mm | 1.64 mm |
| K | 0.44 mm | 0.49 mm | 0.54 mm |
| W | 7.90 mm | 8.00 mm | 8.30 mm |

Figure 67-5 Auth 3.0 CP packing reel (XDFN and WLCSP)

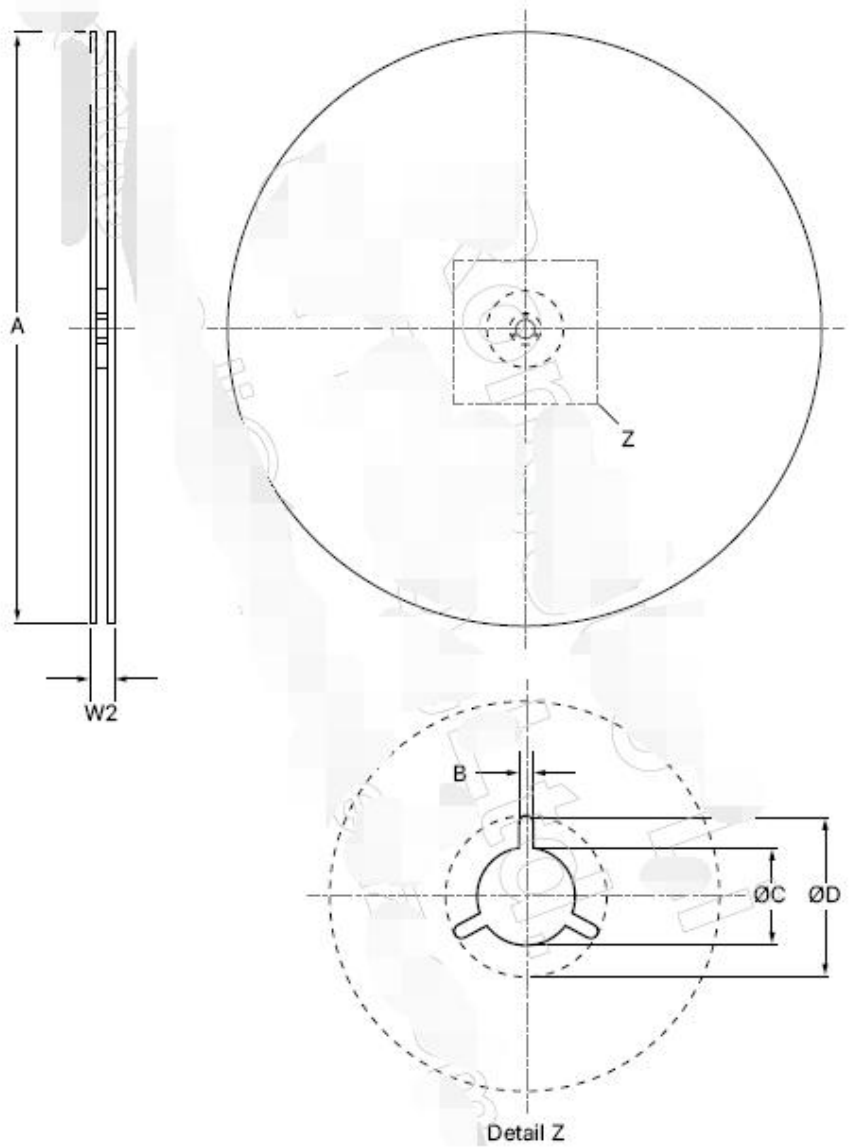


Table 67-6 Auth 3.0 CP packing reel dimensions (XDFN)

| Symbol | Minimum | Nominal | Maximum |
|---|---|---|---|
| A | 328.0 mm | 330.0 mm | 332.0 mm |
| W2 | | | 18.4 mm |
| B | 1.5 mm | 2.0 mm | 2.5 mm |
| ØC | 12.8 mm | 13.0 mm | 13.5 mm |
| ØD | 20.2 mm | | |

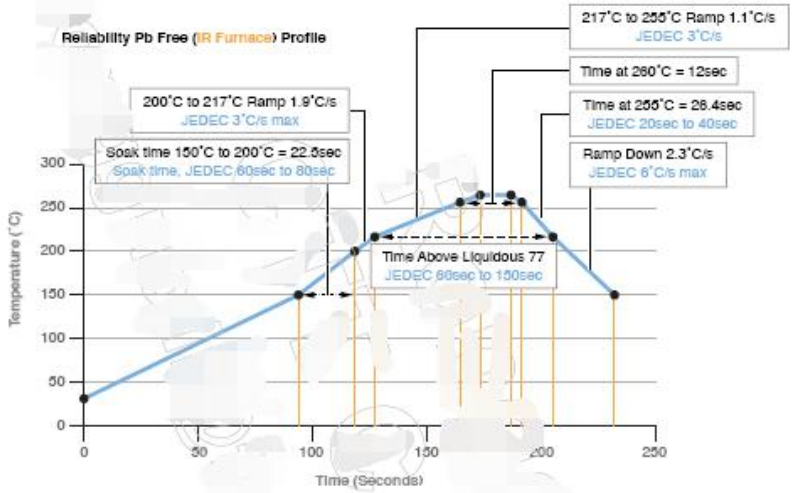
Table 67-7 Auth 3.0 CP packing reel dimensions (WLCSP)

| Symbol | Minimum | Nominal | Maximum |
|---|---|---|---|
| A | 328.0 mm | 330.0 mm | 332.0 mm |
| W2 | | | 14.4 mm |
| B | 1.5 mm | 2.0 mm | 2.5 mm |
| ØC | 12.8 mm | 13.0 mm | 13.5 mm |
| ØD | 20.2 mm | | |

## 67.2.4 Handling

The Auth 3.0 CP package is Pb-free and is designed to withstand a standard reflow profile with a peak reflow temperature below 260 °C. See Figure 67-6 (page 590) for the reflow profile of the Auth 3.0 CP (XDFN and WLCSP).

Figure 67-6 Auth 3.0 CP reflow profile (XDFN and WLCSP)




# 67.3 Pad Assignments

## 67.3.1 XDFN Package

Figure 67-7 Auth 3.0 CP, top view (XDFN)

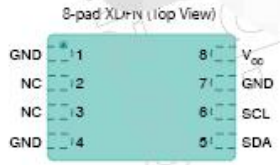



Table 67-8 Auth 3.0 CP signals (XDFN)

| Signal | Pad | I/O | Description |
|---|---|---|---|
| GND | 1 | | Ground |
| NC | 2-3 | | Must not be connected. |

| Signal | Pad | I/O | Description |
|---|---|---|---|
| GND | 4 | | Ground |
| SDA | 5 | I/O | I²C data |
| SCL | 6 | I | I²C clock |
| GND | 7 | I | Ground |
| $V_{CC}$ | 8 | | Supply voltage |

**Note:** Pads 1, 4, and 7 are internally connected to each other. The ground terminal of the bypass capacitor should be as close as possible to any one of these three pads.

## 67.3.2 WLCSP Package

**Figure 67-8** Auth 3.0 CP, top view (WLCSP)

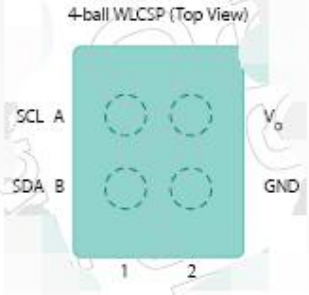



**Table 67-9** Auth 3.0 CP signals (WLCSP

| Signal | Pad | I/O | Description |
|---|---|---|---|
| SCL | 1A | I | I²C clock |
| SDA | 1B | I/O | I²C data |
| $V_{CC}$ | 2A | | Supply voltage |
| GND | 2B | | Ground |

# 67.4 Electrical

This section provides technical details and tolerances for the Auth 3.0 CP chip.

## 67.4.1 Maximum Environmental Conditions

Table 67-10 (page 592) lists the Auth 3.0 CP's absolute maximum electrical and free-air temperature ranges. Stresses to the Auth 3.0 CP beyond the ranges may cause permanent damage. Exposure to either end of any range may affect the Auth 3.0 CP reliability.

**Table 67-10** Auth 3.0 CP maximum electrical and temperature ranges

| Condition | Maximum Range |
|---|---|
| Voltage applied at $V_{CC}$ relative to $V_{SS}$ | -0.3 V to +6.0 V |
| Voltage applied to any pad | -0.3 V to $V_{CC}$ + 0.3 V |
| Storage temperature | -65 to +150 °C |

## 67.4.2 Recommended Operating Conditions

Internal sensors may force the Auth 3.0 CP to its reset state if any of the conditions listed in Table 67-11 (page 592) are exceeded. Attempting to operate the Auth 3.0 CP in this state is not recommended and may lead to the Auth 3.0 CP failure or unreliability.

**Table 67-11** Auth 3.0 CP maximum electrical and temperature ranges

| Condition | Recommended Range |
|---|---|
| Operating free-air temperature | -40 to +85 °C |
| Supply voltage | 1.71 V to 3.6 V |

## 67.4.3 ESD Characteristics

**Table 67-12** ESD characteristics

| Pad | Description | ESD Requirement | Voltage |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | CDM ±1 kV, HBM ±4 kV | +3.6 V |
| SDA | $I^2C$ data | IEC 61000-4-2 ±8 kV Contact Discharge | +8.0 V limited to 150 ms max over lifetime. |
| SCL | $I^2C$ clock | CDM ±1 kV, HBM ±4 kV | +5.5 V |

## 67.4.4 DC Characteristics

Table 67-13 DC characteristics

| Item | Description | Minimum | Typical | Maximum |
|---|---|---|---|---|
| $I_{CHAL}$ | Operating current while computing challenge | - | - | 1.15 mA |
| $I_{SLEEP}$ | Sleep current | - | 100 nA | 2000 nA |
| $V_{OL}$ | Output Voltage Low, $I_{OL}$ = 8 mA | - | - | 0.4 V |
| $V_{OL}$ | Output Voltage Low, $I_{OL}$ < 500 µA | | - | 0.2 V |
| $C_{SDA}$ | Input capacitance of SDA | | 60 pF | - |
| $C_{SCL}$ | Input capacitance of SCL | - | 3 pF | - |
| $V_{CC}$ | Supply voltag | 1.71 V | - | 3.6 V |
| $I_{IH}$ | Input Current ($V_{IH}$ = 0 V, 3.6 V) | -1 µA | | 1 µA |
| $V_{IH}$ | Input Voltage High | 0.7 V × $V_{CC}$ | | 3.9 V |
| $V_{IL}$ | Input Voltage Low | -0.3 V | | 0.3 V × $V_{CC}$ |

## 67.4.5 AC Characteristics

This section is applicable over recommended operating range from $T_A$ = -40° to +85°, $V_{CC}$ = +1.71 V to +3.6 V.

Table 67-14 AC characteristics

| Item | Description | Minimum | Typical | Maximum |
|---|---|---|---|---|
| $t_{WATCHDOG}$ | Watchdog Timeout to drop into sleep | 3.2 s | 4 s | 4.8 s |
| $t_{DIT}$ | Auth 3.0 CP Initialization Time from power applied or wake from sleep | - | - | 1 ms |
| $t_{AUTH}$ | Authentication Time | | | 500 ms |
| $t_{CERT}$ | Certificate Generation | - | - | 10 ms |
| $t_{READ}$ | EEPROM Reads | - | - | 1.5 ms |
| $t_{WRITE}$ | EEPROM Writes | - | - | 20 ms |
| $t_{SN}$ | Serial Number Formatting | - | - | 1 ms |
| $t_{CMD}$ | All Other Commands | - | - | 800 µs |
| $f_{SCK}$ | SCL Clock Frequency | 0 kHz | - | 400 kHz |

| Item | Description | Minimum | Typical | Maximum |
|---|---|---|---|---|
| $t_{HIGH}$ | SCK High Time | 0.6 µs | - | - |
| $t_{LOW}$ | SCK Low Time | 1.2 µs | - | - |
| $t_{SU.STA}$ | Start Setup Time | 0.6 µs | - | - |
| $t_{HD.STA}$ | Start Hold Time | 0.6 µs | - | - |
| $t_{SU.STO}$ | Stop Setup Time | 0.6 µs | - | - |
| $t_{SU.DAT}$ | Data In Setup Time | 100 ns | - | - |
| $t_{HD.DAT}$ | Data In Hold Time | 0 ns | - | - |
| $t_R$ | Input Rise Time from $0.1 \times V_{CC}$ to $0.9 \times V_{CC}$ | - | - | 1 µs |
| $t_F$ | Input Fall Time from $0.9 \times V_{CC}$ to 0.1 times $V_{CC}$ | - | - | 1 µs |
| $t_{AA}$ | Clock Low to Data Out Valid | - | - | 0.9 µs |
| $t_{DH}$ | Data Out Hold Time | 50 ns | - | - |
| $t_{BUF}$ | Time bus must be free before a new transmission can start. | 1.2 µs | - | - |
| $t_I$ | Input Filter Glitch Suppression (SCL,SDA) | - | - | 50 ns |

**Note:** Calculation time measured from the end of the trailing break after command input to the point in time when the Auth 3.0 CP begins transmitting the first bit of the response.

### 67.4.6 Sleep Mode

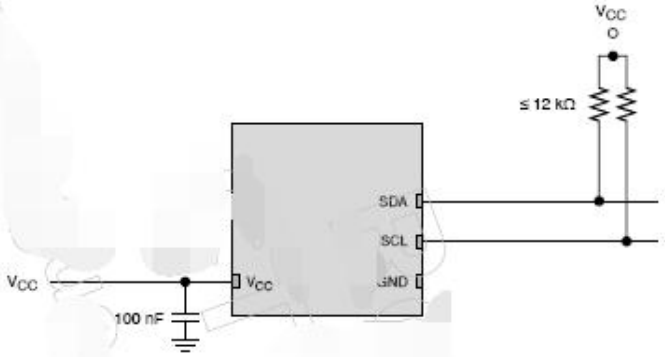
The Auth 3.0 CP conserves power by entering a sleep mode. It enters this mode automatically after the watchdog timer expires ($t_{WATCHDOG}$) or via the sleep register, see Sleep (page 604).

When in sleep mode, the Auth 3.0 CP automatically wakes in response to any $I^2C$ communications sent to its address.

### 67.4.7 Reference Design

Accessories must implement the reference design as shown in Figure 67-9 (page 595).

Figure 67-9 Auth 3.0 CP reference design




## 67.5 I²C Interface

The Auth 3.0 CP acts as a I²C slave and uses a 7-bit slave address, see Addressing (page 596).

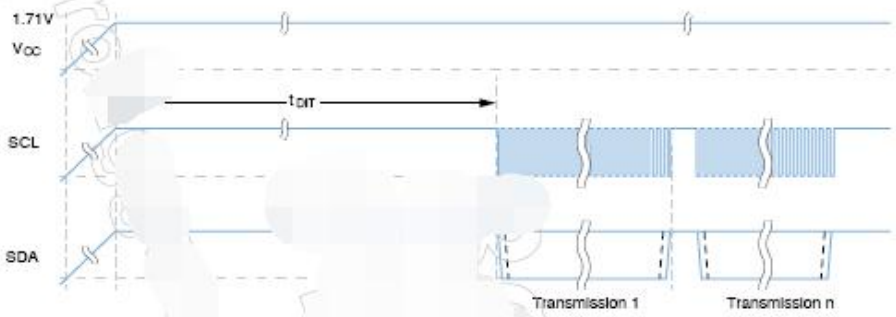
### 67.5.1 Setup

The I²C interface is started either by supplying power to the $V_{CC}$ line or by any transition on the SDA line if the Auth 3.0 CP is in sleep mode, see Sleep Mode (page 594).

The I²C output buffer is cleared on power-up and wake from sleep mode.

The Auth 3.0 CP requires a certain amount of time to read the I²C address when powered up. The first data transmission must start no earlier than $t_{DIT}$, see Table 67-14 (page 593), after the $V_{CC}$ line goes high. See Figure 67-10 (page 596) for an I²C timing diagram.

Figure 67-10 Auth 3.0 CP I²C power up timing




## 67.5.2 Hardware

The I²C Interface operates at 100 kHz (standard mode) or 400 kHz (full speed) and consists of two signals:

- *SDA*: Data
- *SCL*: Clock

Accessories must connect pull-up resistors (12 kΩ maximum) from the same power supply as the Auth 3.0 CP to the SCL and SDA lines of the Auth 3.0 CP.

## 67.5.3 Addressing

The slave address for writing is shown in Figure 67-11 (page 596) and the corresponding read address in Figure 67-12 (page 596).

Figure 67-11 Auth 3.0 CP I²C slave write address

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/nW |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Figure 67-12 Auth 3.0 CP I²C slave read address

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/nW |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

The I²C write address of the Auth 3.0 CP consists of the seven bits [A6:A0] followed by 0 for the R/nW bit. The I²C read address of the Auth 3.0 CP consists of the seven bits [A6:A0] followed by 1 for the R/nW bit. The write and read addresses of the Auth 3.0 CP are `0x20` and `0x21` respectively.

## 67.5.4 I²C Transaction Format

Table 67-15 Auth 3.0 CP read/write transaction data format

| Field | Bytes | Description |
|---|---|---|
| I²C Slave Address + R/W bit | 1 | Must be `0x20` for a write transaction or `0x21` for a read transaction. |
| Register | 1 | See Registers (page 598) |
| Payload | 0-n | Payload data. |

## 67.5.5 Writing to the Auth 3.0 CP

To write data to the Auth 3.0 CP, follow these steps:

1. Send the I²C start sequence.
2. Send the I²C write address of the Auth 3.0 CP.
3. Check for an ACK from the slave; if a NACK is received, wait 500 µs and then loop back to Step 1.
4. Send the register address at which to begin writing.
5. Check for an ACK from the slave; if a NACK is received, wait 500 µs and then loop back to Step 1.
6. Send the data bytes.
7. Send the I²C stop sequence.

The accessory must send a I²C stop sequence after the last data byte of any write to ensure that the Auth 3.0 CP will start the execution of the operation. The behavior of the Auth 3.0 CP is undefined if a I²C start sequence is sent prior to a I²C stop sequence.

## 67.5.6 Reading from the Auth 3.0 CP

To read data from the Auth 3.0 CP, follow these steps:

1. Send the I²C start sequence.
2. Send the I²C write address of the Auth 3.0 CP.
3. Check for an ACK from the slave; if a NACK is received, wait 500 µs and then loop back to Step 1.
4. Send the register address at which to begin reading.
5. Check for an ACK from the slave; if a NACK is received, wait 500 µs and then loop back to Step 1.
6. Send the I²C stop sequence.

7. Send the I²C start sequence.
8. Send the I²C read address of the Auth 3.0 CP.
9. Check for an ACK from the slave; if a NACK is received, wait 500 µs and then loop back to Step 7.
10. Read the data bytes.
11. Send the I²C stop sequence.

If the read buffer on the accessory is limited and cannot read all the desired bytes prior to issuing the I²C stop sequence in Step 11, then the following sequence may be repeated as many times as necessary to retrieve all remaining bytes:

1. Send the I²C start sequence.
2. Send the I²C read address of the Auth 3.0 CP.
3. Check for an ACK from the slave; if a NACK is received, wait 500 µs and then loop back to Step 6.
4. Read the data bytes.
5. Send the I²C stop sequence.

After all bytes in the register have been transmitted to the accessory, the Auth 3.0 CP will return `0x00` in response to all further reads until a new register number is selected.

## 67.5.7 Registers

### 67.5.7.1 Device Version

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Device Version | 0x00 | 0 | uint8 | 0x07 | 1 | Read-only |

Reading from this register will return `0x07`.

### 67.5.7.2 Authentication Revision

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Authentication Revision | 0x01 | 0 | uint8 | 0x01 | 1 | Read-only |

Reading from this register will return `0x01`.

### 67.5.7.3 Authentication Protocol Major Version

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Authentication Protocol Major Version | 0x02 | 0 | uint8 | 0x03 | 1 | Read-only |

Reading from this register will return `0x03`.

### 67.5.7.4 Authentication Protocol Minor Version

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Authentication Protocol Minor Version | 0x03 | 0 | uint8 | 0x00 | 1 | Read-only |

Reading from this register will return `0x00`.

### 67.5.7.5 Device ID

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Device ID | 0x04 | 0 | uint8 | 0x00 0x00 0x03 0x00 | 4 | Read-only |

Reading from this register will return `0x00 0x00 0x03 0x00`.

### 67.5.7.6 Error Code

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Error Code | 0x05 | 0 | uint8 | 0x00 | 1 | Read-only |

**Table 67-16** Error Code register parameters

| Bit | Name | Description |
|---|---|---|
| 7-0 | Error Code | See Table 67-17 (page 599). |

**Table 67-17** `Error Code` values

| Value | Description |
|---|---|
| 0x00 | No error. |
| 0x01 | Reserved |
| 0x02 | Invalid register specified or register is read-only. |
| 0x03-0x04 | Reserved |
| 0x05 | Sequence error, command out of sequence. |
| 0x06 | Internal process error during challenge response generation. |
| 0x07-0xFF | Reserved |

Reading the Error Code register will clear it.

Attempts to access an undefined register may result in an error code of `0x02`.

### 67.5.7.7 Authentication Control and Status

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Authentication Control and Status | 0x10 | 1 | uint8 | 0x00 | 1 | Read/Write |

When read from, the Authentication Control and Status register provides the status of the most recently requested Auth 3.0 CP process, as shown in Figure 67-13 (page 600) and Table 67-18 (page 600). When written to, the Authentication Control and Status register controls the start of the Auth 3.0 CP processes, as shown in Figure 67-14 (page 601) and Table 67-21 (page 601).

**Figure 67-13** Auth 3.0 CP Authentication Control and Status register, read-only bits


**Table 67-18** Authentication Control and Status read-only register parameters

| Bit | Name | Description |
|---|---|---|
| 7 | Error Set | See Table 67-19 (page 600). |
| 6-4 | Procedure Results | See Table 67-20 (page 600). |
| 3-0 | | Reserved |

**Table 67-19** `Error Set` values

| Value | Description |
|---|---|
| 0 | The Error Code register contains a value of zero |
| 1 | The Error Code register contains a non-zero value. Both this bit and the Error Code register contents are cleared after the Error Code register is next read or on the next power-on. |

**Table 67-20** `Procedure Results` values

| Value | Description |
|---|---|
| 0 | Most recent challenge response generation process did not produce valid results or no challenge response generation process has been requested. |
| 1 | Accessory challenge response successfully generated. |
| 2-7 | Reserved |

Figure 67-14 Auth 3.0 CP Authentication Control and Status register, write-only bits

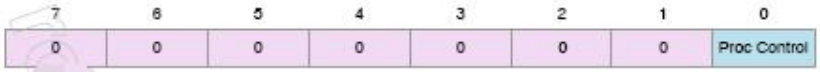



Table 67-21 Authentication Control and Status write-only register parameters

| Bit | Name | Description |
|---|---|---|
| 7-1 | | Reserved |
| 0 | Procedure Control | See Table 67-22 (page 601). |

**Note:** Bits 7-3 must be zero. The data written to the Authentication Control and Status register must be 0x01 to initiate challenge response computation.

Table 67-22 `Procedure Control` values

| Value | Description |
|---|---|
| 0 | No operation. This control does nothing and always reports success (Error Set = 0; Procedure Results = 0). |
| 1 | Start new challenge response generation process |

### 67.5.7.8 Challenge Response Data Length

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Challenge Response Data Length | 0x11 | 1 | uint16 | 0 | 2 | Read-only |

The Challenge Response Data Length register holds the length in bytes of the results of the most recent challenge response generation process. If a completed challenge response is stored in the output buffer of the Auth 3.0 CP, this register will return a value of 64. In all other cases it will return a value of zero.

### 67.5.7.9 Challenge Response Data

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Challenge Response Data | 0x12 | 1 | uint8 | Undefined | 64 | Read-only |

If the Auth 3.0 CP has computed a challenge response, the challenge response itself will be returned in this register. If there is no valid challenge response stored in the Auth 3.0 CP SRAM, the interface will return 0x00 for all bytes.

### 67.5.7.10 Challenge Data Length

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Challenge Data Length | 0x20 | 2 | uint16 | 0 | 2 | Read-only |

The Challenge Data Length register holds the length in bytes of the current challenge stored within the Auth 3.0 CP. If a challenge is valid within the Auth 3.0 CP it will return a value of 32, otherwise, it will return a value of zero on a read.

### 67.5.7.11 Challenge Data

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Challenge Data | 0x21 | 2 | uint8 | Undefined | 32 | Read/Write |

The Challenge Data register holds the current challenge data. If a valid challenge is stored within the Auth 3.0 CP, its value may be read via this register, otherwise reads of this register return all zeros.

This challenge data must be written to the Auth 3.0 CP by the accessory and must always be 32 bytes in length. If any number of bytes other than 32 is sent to the Auth 3.0 CP, the challenge register will be cleared and an error returned.

### 67.5.7.12 Accessory Certificate Data Length

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Accessory Certificate Data Length | 0x30 | 3 | uint16 | 607-609 | 2 | Read-only |

The Accessory Certificate Data Length register holds the length of the X.509 certificate that is stored within the Auth 3.0 CP. The length of a certificate varies between 607 and 609, inclusive.

### 67.5.7.13 Accessory Certificate Data

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Accessory Certificate Data 1 | 0x31 | 3 | uint8 | Certificate | 128 | Read-only |
| Accessory Certificate Data 2 | 0x32 | 3 | uint8 | Certificate | 128 | Read-only |
| Accessory Certificate Data 3 | 0x33 | 3 | uint8 | Certificate | 128 | Read-only |
| Accessory Certificate Data 4 | 0x34 | 3 | uint8 | Certificate | 128 | Read-only |
| Accessory Certificate Data 5 | 0x35 | 3 | uint8 | Certificate | 128 | Read-only |

The Accessory Certificate Data registers hold the binary X.509 certificate that is stored in Auth 3.0 CP. The accessory certificate may be read from the Auth 3.0 CP in 128-byte pages starting at any of Accessory Certificate Data addresses, or it may be read in a continuous stream starting at Accessory Certificate Data 1. The Accessory Certificate Data Length value can be read to determine the exact number of bytes in the Accessory Certificate Data.

The accessory must wait at least $t_{CERT}$ for the Auth 3.0 CP to create the certificate from the stored elements whenever it is requested. This means that if any register within block 3 is selected via a zero length write, the subsequent read operation must not be issued for $t_{CERT}$, even if the only intention is to read the length register.

### 67.5.7.14 Self-Test Status

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Self-Test Status | 0x40 | 4 | uint8 | 0x00 | 1 | Read-only |

The Self-Test Status register reports the results of the X.509 certificate and private key tests, as shown in Figure 67-15 (page 603) and Table 67-23 (page 603).

Figure 67-15 Auth 3.0 CP Self-Test Status register


Table 67-23 Self-Test Status register parameters

| Bit | Name | Description |
|---|---|---|
| 7 | X.509 Certificate | See Table 67-24 (page 603). |
| 6 | Private key | See Table 67-24 (page 603). |
| 5-0 | | Reserved |

Table 67-24 Self-Test Status values

| Value | Description |
|---|---|
| 0 | Error |
| 1 | Pass |

**Note:** The X.509 and private key tests only verify that these elements are present in flash memory; no authentication is performed.

### 67.5.7.15 Device Certificate Serial Number

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Device Certificate Serial Number | 0x4E | 4 | uint8 | Certificate | 32 | Read-only |

The Device Certificate Serial Number register returns the certificate serial number as an ASCII string. Each byte in the serial number stored within the device will be returned as two ASCII characters in the range of 0-9, A-F.

### 67.5.7.16 Sleep

| Name | Address | Block | Type | Power-Up Value | Bytes | Access |
|---|---|---|---|---|---|---|
| Sleep | 0x60 | 1 | uint8 | Undefined | 1 | Write-only |

Writing 0xEE to this register will force the Auth 3.0 CP to sleep.