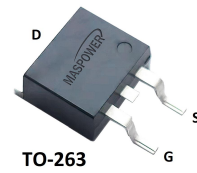


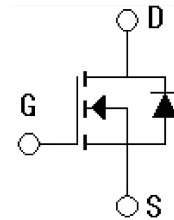
Features

- High density cell design for ultra low $R_{ds(on)}$
- Special process technology for high ESD capability
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Applications

- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible Power Supply (UPS)



Absolute Ratings ($T_c=25^\circ\text{C}$)

Parameter	Symbol		Value	Unit
Drain-Source Voltage	V _{DSS}		70	V
Transient Gate-Source Voltage	V _{GSM}		±30	V
Continuous Gate-Source Voltage	V _{GSS}		±20	V
Drain Current-continuous	I _D	T _C =25℃	210	A
		T _C =100℃	150	A
Drain Current-pulse (note 1)	I _{DM}		840	A
Single pulse avalanche energy (note 2)	E _{AS}		2200	mJ
Avalanche Current(note 1)	I _{AR}		120	A
Peak Diode Recovery dv/dt(note 3)	dv/dt		20	V/ns
Power Dissipation	P _D	T _C =25℃	274	W
		T _C =100℃	109	W
Operating and Storage Temperature Range	T _J , T _{STG}		-55~+150	℃
Maximum Lead Temperature for Soldering Purposes	T _L		300	℃

Electrical Characteristics($T_{CASE}=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Tests conditions	Min	Typ	Max	Unit
Drain-Source Voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	70	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=70\text{V}, V_{GS}=0\text{V}$	-	-	1	μA

Gate body leakage current	I _{GSS}	V _{DS} =0V,V _{GS} =±20V	-	-	±200	nA
On-Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V,I _D =40A (note 4)	-	3	4	mΩ
Forward Transconductance	G _{FS}	V _{DS} =5V,I _D =10A (note 4)	100	165	-	S
Dynamic Characteristics						
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	11000	-	pF
Output capacitance	C _{oss}		-	914	-	pF
Reverse transfer capacitance	C _{rss}		-	695	-	pF
Switching-Characteristics						
Turn-On delay time	t _{d(on)}	V _{DD} =30V,I _D =2A, R _L =15Ω, R _{GEN} =2.5Ω V _{GS} =10V (note 4)	-	23	-	ns
Turn-On rise time	t _r		-	190	-	ns
Turn-Off delay time	t _{d(Off)}		-	130	-	ns
Turn-Off rise time	t _f		-	120	-	ns
Total Gate Charge	Q _g	V _{DS} =25V,I _D =30A, V _{GS} =10V (note 4,5)	-	250	-	nC
Gate-Source charge	Q _{gs}		-	48	-	nC
Gate-Drain charge	Q _{gd}		-	98	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (note 4)	V _{SD}	V _{GS} =0V,I _S =40A	-		1.2	V
Reverse recovery time	t _{rr}	T _J =25℃,I _F =10A dI _F /dt=100A/μs (note 4)		48		ns
Reverse recovery charge	Q _{rr}			78		nC

Thermal Characteristics

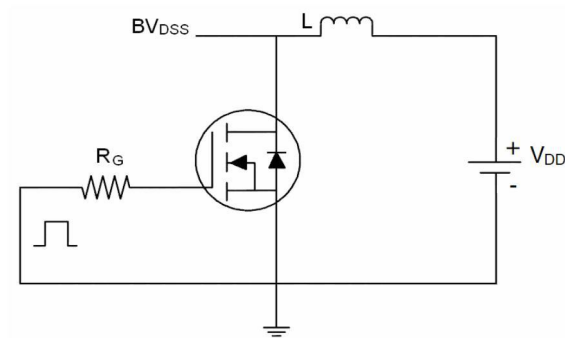
Parameter	Symbol	Value	Unit
Thermal Resistance, junction to Case, Max	$R_{th(j-C)}$	0.455	$^\circ C/W$
Thermal Resistance, junction to Ambient, Max	$R_{th(j-A)}$	52	$^\circ C/W$

Notes:

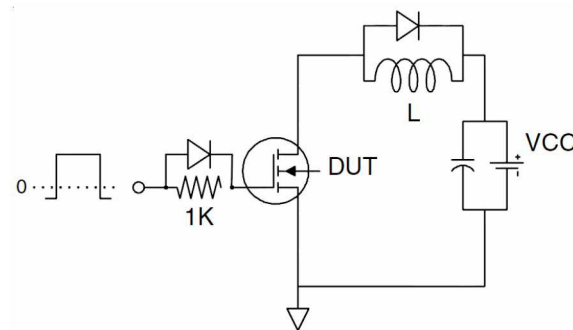
1. Pulse width limited by maximum junction temperature.
2. E_{AS} condition: $T_J=25^\circ C, V_{DD} = 37.5V, V_{GE} = 10V, L = 0.22mH, R_g = 25\Omega, I_{AS} = 100A$
3. $I_{SD} \leq 210A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS},$ Starting $T_J=25^\circ C$
4. Pulse Test: Pulse Width $\leq 400\mu s,$ Duty Cycle $\leq 2\%$.
5. Essentially independent of operating temperature.

Test Circuit

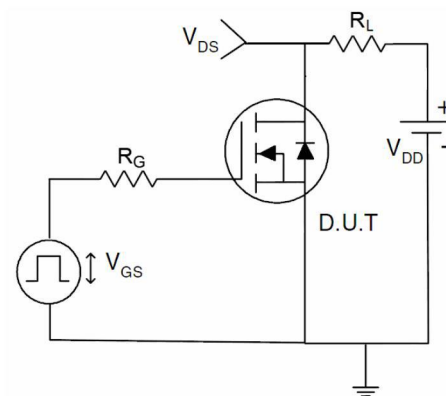
1) E_{AS} Test Circuit



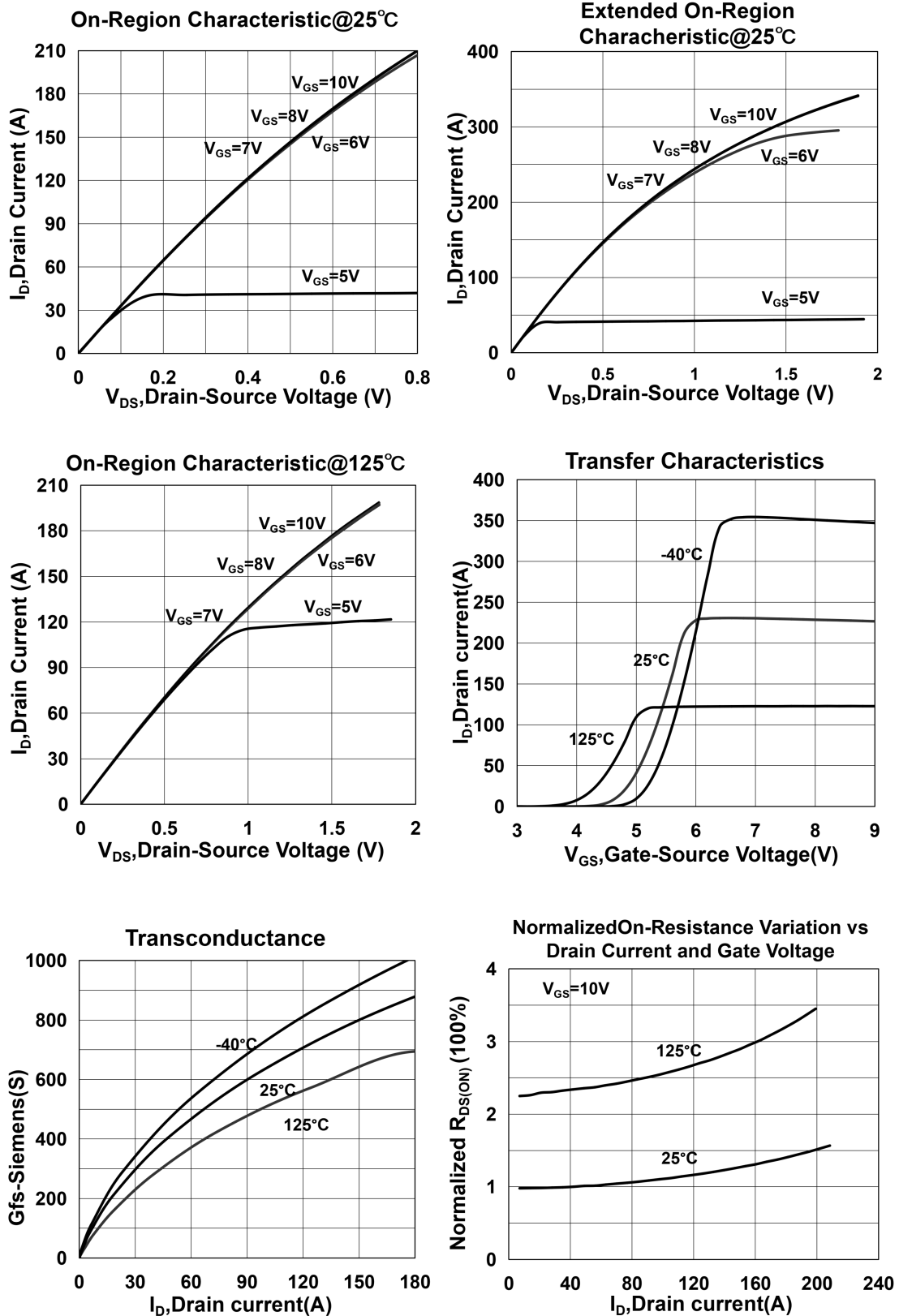
2) Gate Charge Test Circuit

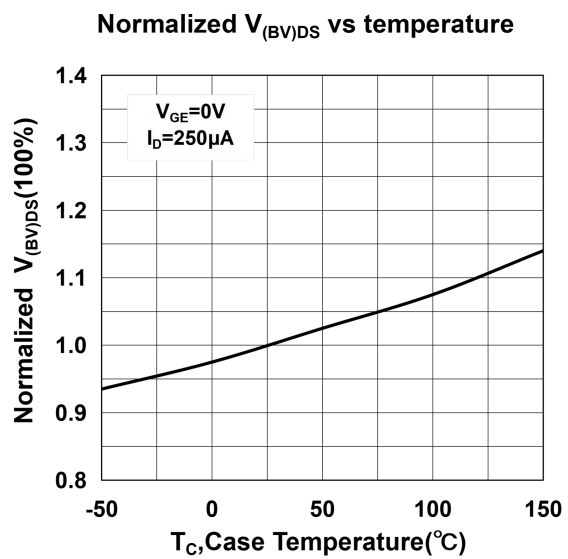
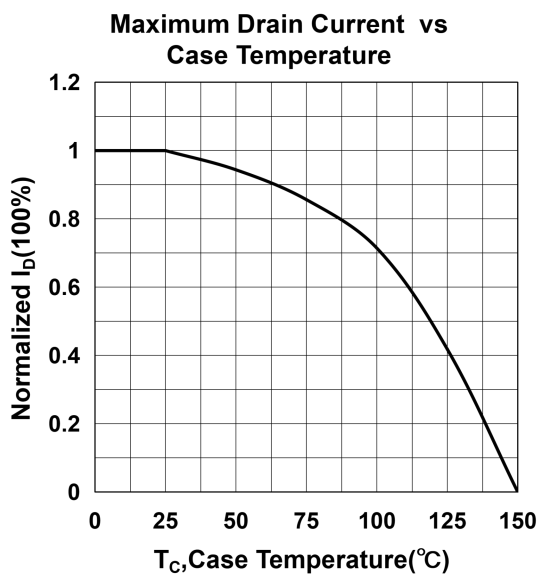
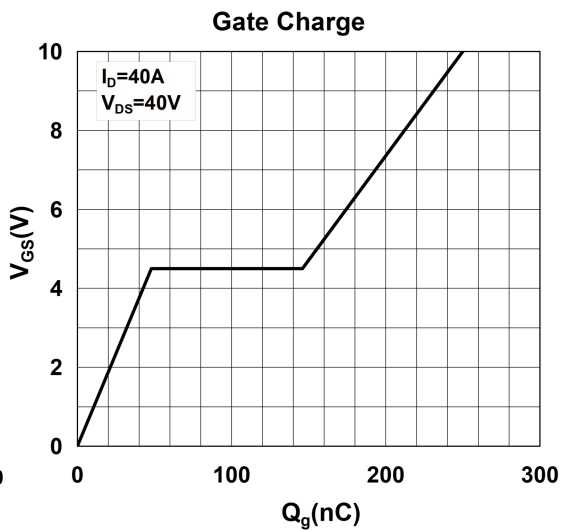
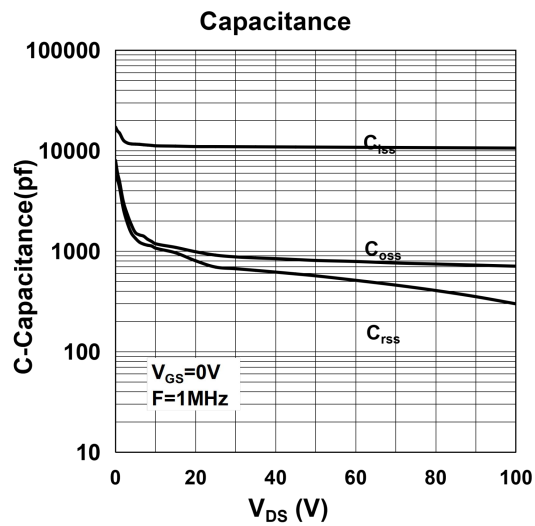
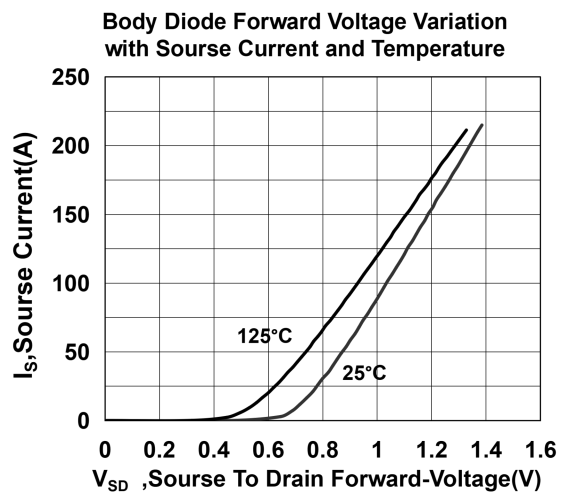
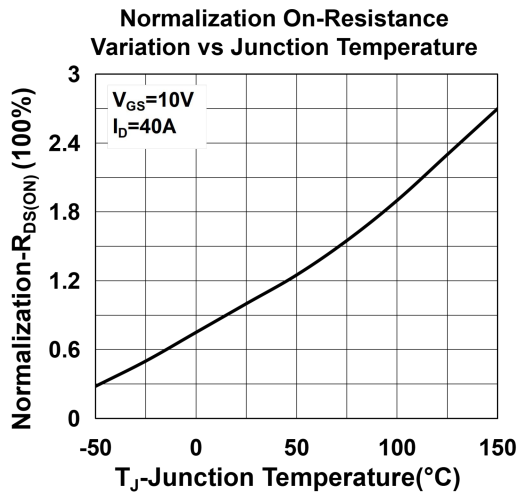


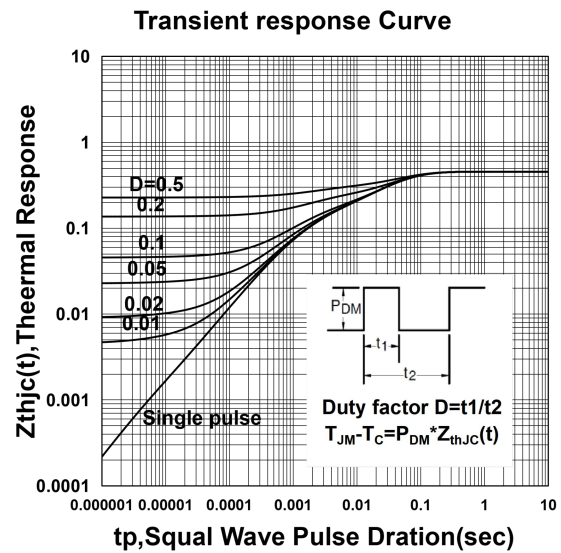
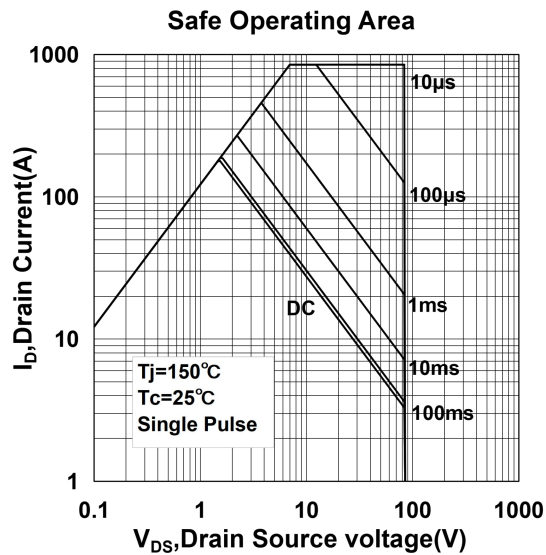
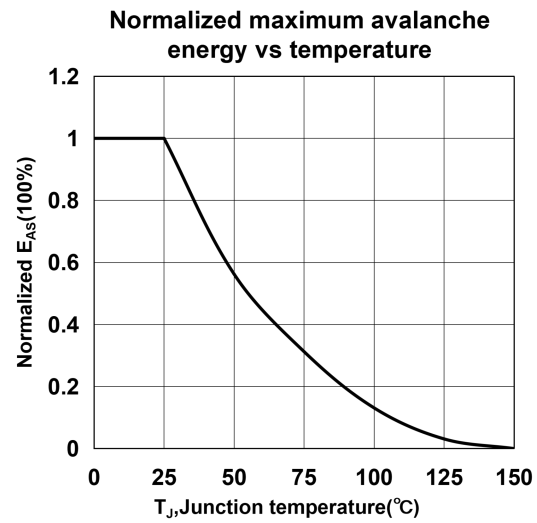
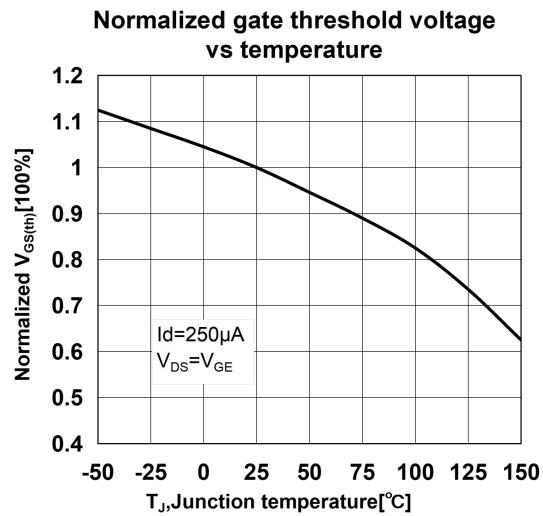
3) Switch Time Test Circuit



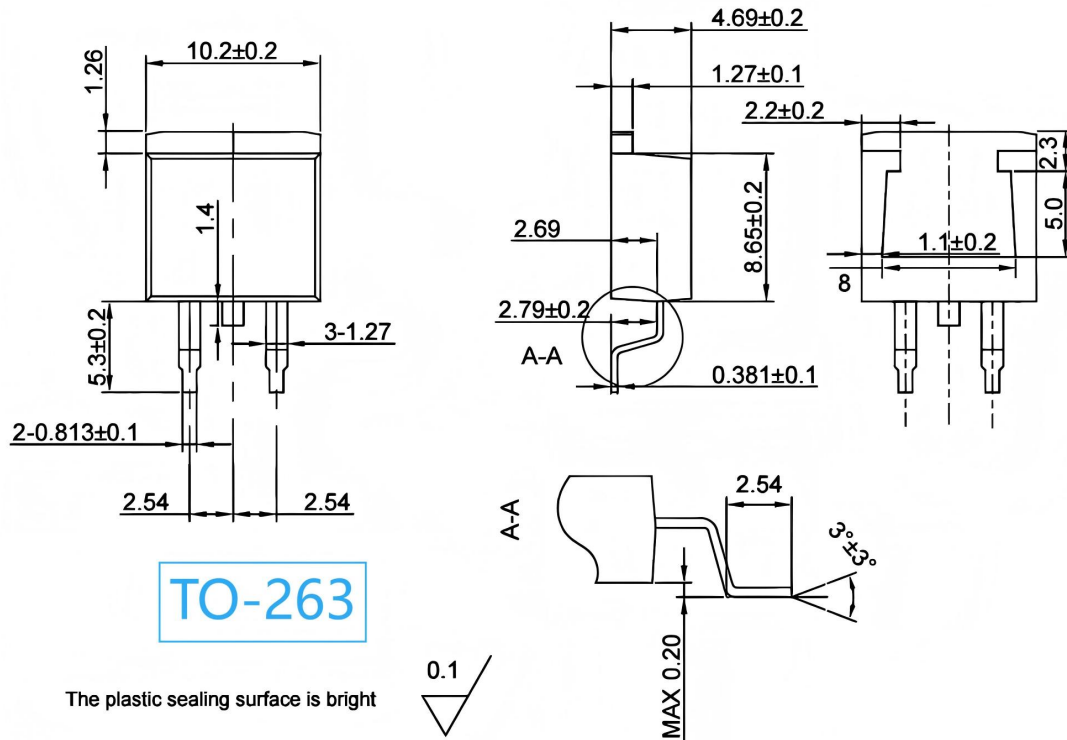
Typical Electrical and Thermal Characteristics (Curves)







Package Mechanical DATA



Notes:

1. Unmarked tolerance ± 0.15 mm; unmarked $R < 0.15$ mm
2. The resin body is not allowed to have defects, shrinkage holes, cracks, bubbles and other harmful defects
3. The drawing indicates that the leg has reinforcement
4. Unit : mm