

Product Specification

XBLW TPS3808

Low-Quiescent-Current, Programmable-Delay Supervisory Circuit

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Descriptions

The TPS3808 is a series of multifunctional microprocessor supervisory circuit that monitors system voltage rails from 0.4 V to 5 V. When the SENSE voltage drops below the factory-preset threshold or the manual reset pin ($\overline{\text{MR}}$) switches to logic low, the device asserts an open-drain $\overline{\text{RESET}}$ output signal. When the trigger conditions is removed, the $\overline{\text{RESET}}$ recovers after a user-defined delay time. The TPS3808 employs a high-precision internal bandgap voltage reference to provide 0.5% threshold accuracy for the entire input threshold voltage (V_{IT}) range. The reset delay time is adjustable by changing the connection of C_T pin. The delay time can be set to 20 ms by floating the C_T , 300 ms by connecting C_T to V_{DD} through a resistor, or vary from 1.25 ms to 10 s by alternating the capacitor value connected to C_T . The device features an ultra-low-power consumption. A quiescent current as low as 0.6 μA makes the device suitable for any power sensitive applications, for example battery-powered devices. It is available in SOT23-6L and DFN2 $\times$ 2-6L packages and is fully specified over a temperature range of -40°C to 125°C .

Applications

- Microprocessors or microcontroller applications
- Personal computers
- Battery-powered products
- Portable and hand-held products
- FPGA and ASIC applications

Features and Benefits

- Adjustable delay time: 1.25 ms to 10 s.
- Ultra-low quiescent current: 0.6 μA typical.
- High threshold accuracy: 0.5%
- Fixed threshold voltages for standard voltage rails from 0.9 V to 5 V or adjustable voltage down to 0.4V
- Manual reset input: $\overline{\text{MR}}$
- Open-drain output: $\overline{\text{RESET}}$
- Small packages: available in SOT23-6L and DFN2 $\times$ 2-6L
- Temperature range: -40°C to 125°C

Device Versions and Thresholds

Version	Nominal Supply Voltage	Threshold voltage
TPS3808G01	Adjustable by external resistor divider	0.405 V
TPS3808G09	0.9 V	0.84 V
TPS3808G12	1.2 V	1.12 V
TPS3808G125	1.25 V	1.16 V
TPS3808G15	1.5 V	1.40 V
TPS3808G18	1.8 V	1.67 V
TPS3808G19	1.9 V	1.77 V
TPS3808G25	2.5 V	2.33 V
TPS3808G30	3 V	2.79 V
TPS3808G33	3.3 V	3.07 V
TPS3808G50	5 V	4.65 V

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW TPS3808G01DBVR	SOT23-6L	AVW	Tape	3000Pcs/Reel
XBLW TPS3808G01DRVT	QFN2×2-6L	AVW	Tape	3000Pcs/Reel
XBLW TPS3808G09DBVR	SOT23-6L	AVV	Tape	3000Pcs/Reel
XBLW TPS3808G09DRVT	QFN2×2-6L	AVV	Tape	3000Pcs/Reel
XBLW TPS3808G12DBVR	SOT23-6L	CAC	Tape	3000Pcs/Reel
XBLW TPS3808G12DRVT	QFN2×2-6L	CAC	Tape	3000Pcs/Reel
XBLW TPS3808G125DBVR	SOT23-6L	AVY	Tape	3000Pcs/Reel
XBLW TPS3808G125DRVT	QFN2×2-6L	AVY	Tape	3000Pcs/Reel
XBLW TPS3808G15DBVR	SOT23-6L	AVS	Tape	3000Pcs/Reel
XBLW TPS3808G15DRVT	QFN2×2-6L	AVS	Tape	3000Pcs/Reel
XBLW TPS3808G18DBVR	SOT23-6L	AVR	Tape	3000Pcs/Reel
XBLW TPS3808G18DRVT	QFN2×2-6L	AVR	Tape	3000Pcs/Reel
XBLW TPS3808G19DBVR	SOT23-6L	CHP	Tape	3000Pcs/Reel
XBLW TPS3808G19DRVT	QFN2×2-6L	CHP	Tape	3000Pcs/Reel
XBLW TPS3808G25DBVR	SOT23-6L	AVQ	Tape	3000Pcs/Reel
XBLW TPS3808G25DRVT	QFN2×2-6L	AVQ	Tape	3000Pcs/Reel
XBLW TPS3808G30DBVR	SOT23-6L	AVP	Tape	3000Pcs/Reel
XBLW TPS3808G30DRVT	QFN2×2-6L	AVP	Tape	3000Pcs/Reel
XBLW TPS3808G33DBVR	SOT23-6L	AVO	Tape	3000Pcs/Reel
XBLW TPS3808G33DRVT	QFN2×2-6L	AVO	Tape	3000Pcs/Reel
XBLW TPS3808G50DBVR	SOT23-6L	AVN	Tape	3000Pcs/Reel
XBLW TPS3808G50DRVT	QFN2×2-6L	AVN	Tape	3000Pcs/Reel

Note: The stamp code batch will be updated with the production batch, please refer to the actual product.

Typical Applications Diagram

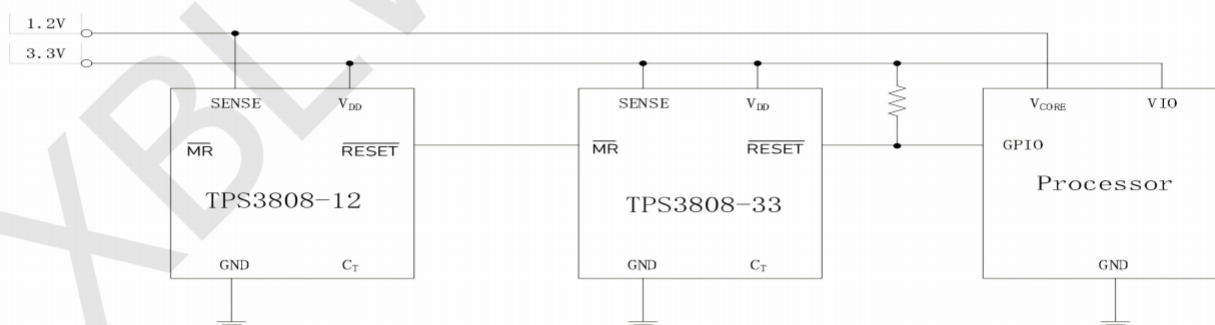
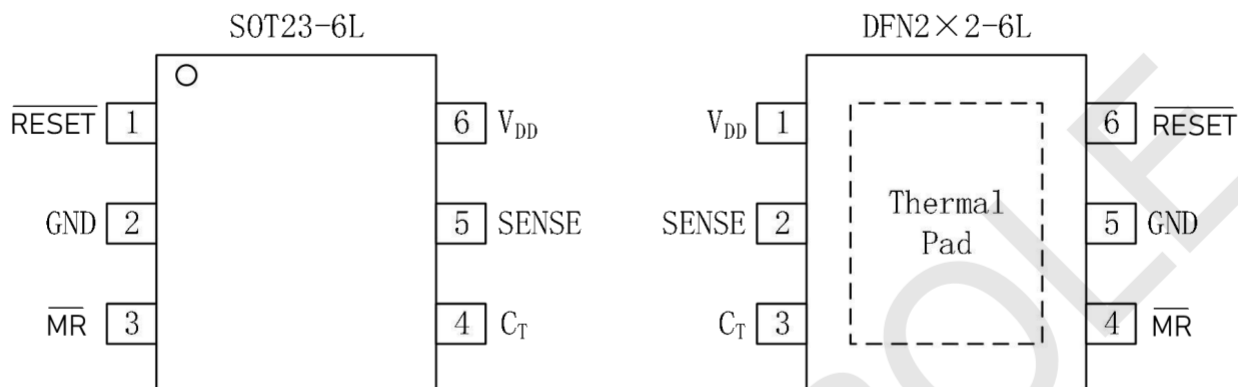


Figure 1. Dual supply rails monitoring

Absolute Maximum Ratings

Parameter	MIN	MAX	UNIT
$V_{DD}, V_{RESET}, V_{MR}, V_{SENSE}$	-0.3	7	V
V_{CT}	-0.3	$V_{DD}+0.3$	V
I_{RESET}	-5	5	mA
T_J	-40	150	°C
T_{STG}	-65	150	°C

Pin Configuration (Top View)



Pin Description

Symbol	Pin Number		Description
	SOT23-6L	DNF2x2-6L	
CT	4	3	Delay time programming pin. Detailed information is given in section 14.2.2.
GND	2	5	Ground pin.
MR	3	4	Manual reset pin. By driving MR low, RESET is asserted. MR is internally tied to VDD through a pull-up resistor.
RESET	1	6	Open-drain output pin. RESET remains to be logic low for user defined delay period after SENSE voltage recovers to be above VIT and MR is set to logic high. RESET pin requires an external 10 kΩ to 1 MΩ pull-up resistor to supply voltage which is allowed to be higher than VDD.
SENSE	5	2	Input pin connected to the voltage expected to be monitored. Once the voltage drops below the preset threshold voltage VIT, the RESET is asserted.
VDD	6	1	Supply voltage pin. It is recommended to place a 0.1 μF ceramic capacitor as close as possible to this pin.
Thermal Pad	NA	Thermal Pad	Thermal pad. Connect to ground plane for enhanced thermal performance.

ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V

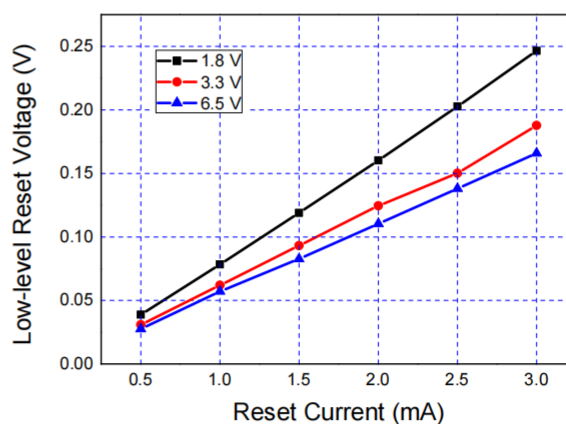
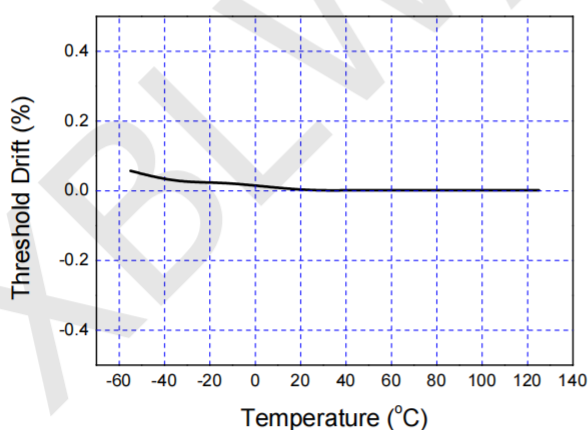
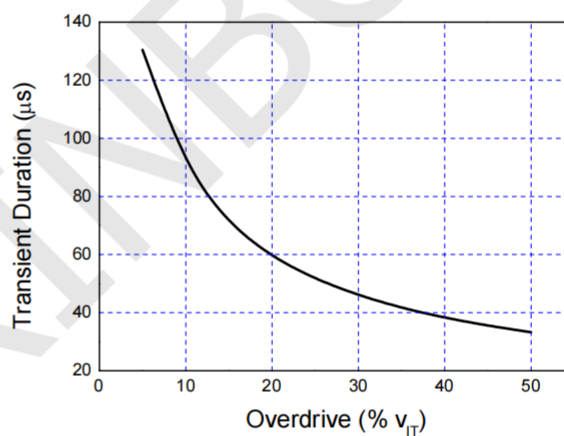
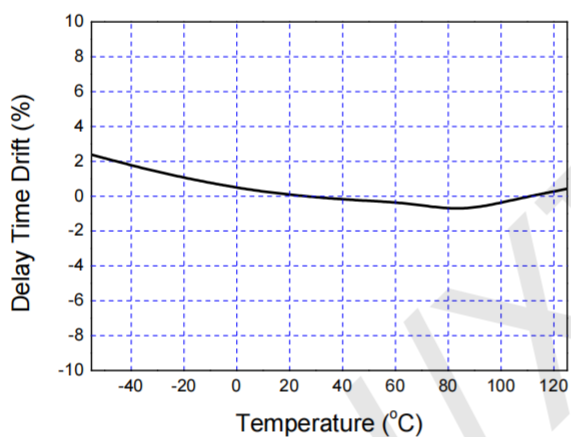
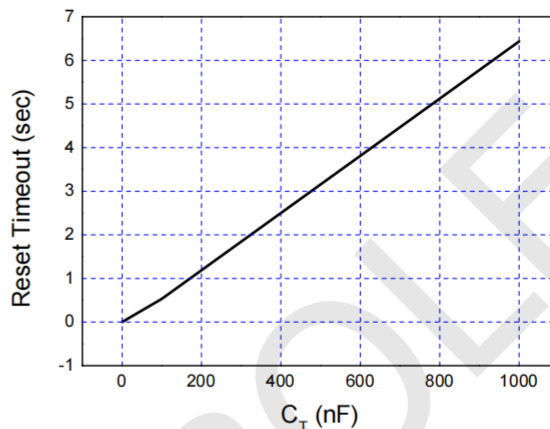
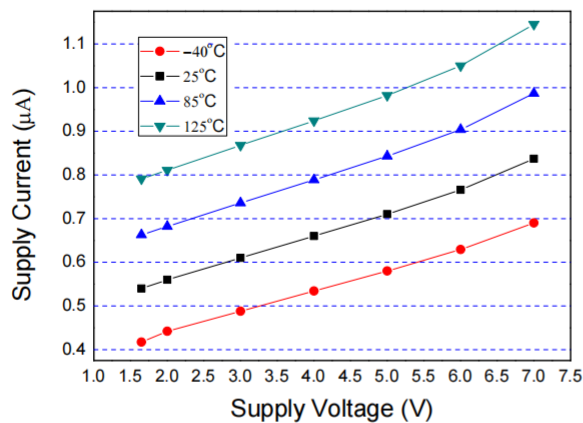
Electrical Characteristics

1.7 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = -40°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Conditions	Min	Typ	Max	Unit
V _{DD} , Input supply range	-40 °C ≤ T _J ≤ 125 °C	1.65		6.5	V
I _{DD} , Supply current	V _{DD} = 3.3 V, $\overline{\text{RE}}\overline{\text{ST}}$ not asserted, $\overline{\text{MR}}$, $\overline{\text{RE}}\overline{\text{ST}}$, and C _T open		0.6	1.18	μA
	V _{DD} = 6.5 V $\overline{\text{RE}}\overline{\text{ST}}$ not asserted, $\overline{\text{MR}}$, $\overline{\text{RE}}\overline{\text{ST}}$, and C _T open		0.75	1.44	
V _{OL} , Low-level output voltage	1.3 V ≤ V _{DD} ≤ 1.8 V, I _{OL} = 0.4 mA			0.05	V
	1.8 V ≤ V _{DD} ≤ 6.5 V, I _{OL} = 1 mA			0.07	
V _{POR} , Power-up reset voltage	V _{OL(max)} = 0.2 V, I _{RESET} = 15 μA			0.9	V
V _{IT} , Negative-going input threshold accuracy	All version, T _A = 25 °C	-0.16		0.2	%
	V _{IT} ≤ 3.3 V	-0.4		0.25	
	3.3 V ≤ V _{IT} ≤ 5 V	-0.4		0.4	
V _{HYS} , Hysteresis on V _{IT}	All versions			2.88	%
R _{MR} , $\overline{\text{MR}}$ internal pull-up resistance		77	100		kΩ
I _{SENSE} , Input current at SENSE pin	LTP3801, V _{SENSE} = V _{IT}	-16		16	nA
	The other versions, V _{SENSE} = 6.5 V		235		nA
I _{OH} , $\overline{\text{RESET}}$ leakage current	V _{RESET} = 6.5V, $\overline{\text{RE}}\overline{\text{ST}}$ not asserted			0.1	μA
C _{IN} , Input capacitance, any pin	C _T pin, V _{IN} = 0 V to 6.5 V		5		pF
	The other pins, V _{IN} = 0 V to 6.5 V		5		
V _{IL} , $\overline{\text{MR}}$ input logic low		0		0.3V _{DD}	V
V _{IH} , $\overline{\text{MR}}$ input logic high		0.7V _{DD}		V _{DD}	V
t _{SENSE} , Input pulse width to $\overline{\text{RESET}}$	V _{IH} = 1.05V _{IT} , V _{IL} = 0.95V _{IT}		25		μs
t _{MR} , Input pulse width to $\overline{\text{RESET}}$	V _{IH} = 0.7V _{IT} , V _{IL} = 0.3V _{IT}		100		ns
V _{TH-R AMP} , CT source threshold voltage			1.22		V
t _D , $\overline{\text{RESET}}$ delay time	C _T floating	13	20	28	ms
	C _T = V _{DD}	196	294	417	ms
	C _T = 100 pF	0.8	1.15	1.54	ms
t _{MR} , Propagation delay	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$		224		ns
t _{PRO} , High-to-low level $\overline{\text{RESET}}$ delay	SENSE to $\overline{\text{RESET}}$		24		μs

Typical Characteristics

$T_J = +25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$ and $R_{LRESET} = 100\text{ k}\Omega$, unless otherwise noted.



Functional Block Diagram

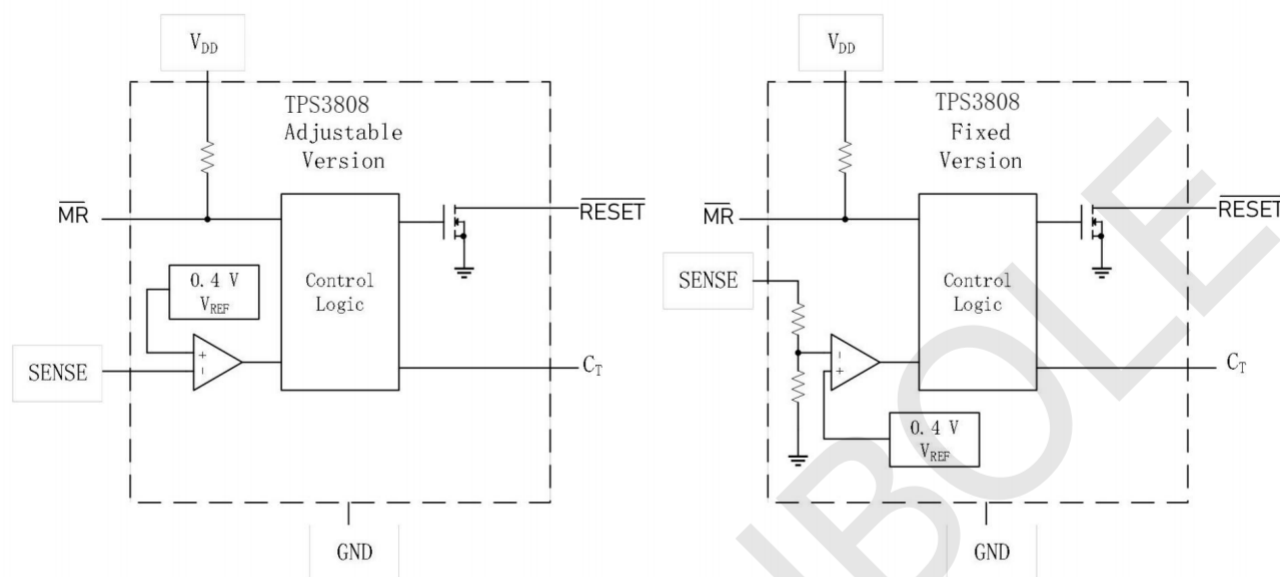


Figure 1. functional block diagram

Feature Description

The TPS3808 series provide options of a wide range of monitoring voltage threshold and reset delay time. Such property makes it suitable for various applications. Fixed threshold voltage versions could cover from 0.9 V up to 5 V as the supply voltage. The threshold voltage of adjustable version can be set to any voltage above 0.405V by external resistor divider. Users can select from two preset reset delay time: 20 ms by floating C_T pin and 300 ms by connecting C_T pin to V_{DD} through resistor, or users can choose any delay time from 1.25 ms to 10 s by varying the capacitance of external capacitor between C_T and ground

Sense Input

SENSE pin detects the input voltage to be monitored, and will assert the $\overline{\text{RESET}}$ if the detected voltage drops below the threshold. A built-in hysteresis of the comparator avoids uncertainty near the threshold value. It is recommended to place a 1 nF to 10 nF bypass capacitor on the SENSE pin to reduce transients and layout parasitics. The SENSE pin can endure short negative transients, and the endurable time is related to the hreshold overdrive shown in Figure X. The adjustable version LTP8301 can set the threshold voltage to any value above 0.405 V using circuit shown below.

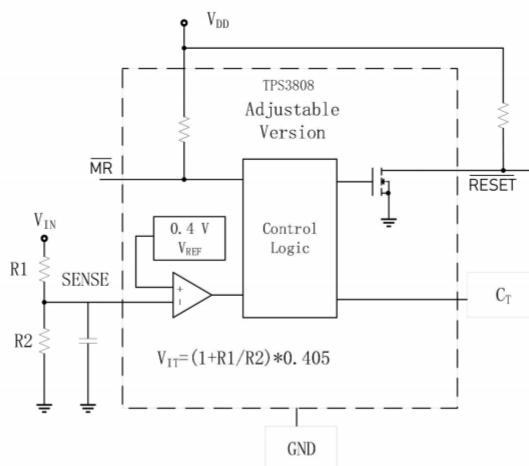


Figure 2. Adjustable threshold

Reset Delay Time

The reset delay time of the device can be selected from two fixed values or configured by varying the capacitance value connected to C_T pin. By floating C_T , a fixed 20 ms delay time is set. By connecting the C_T to VDD through a resistor, from 40 k Ω to 200 k Ω , a fixed 300 ms delay time is set. User defined delay time between 1.25 ms to 10 s can be programmed by an external ground-referenced capacitor.

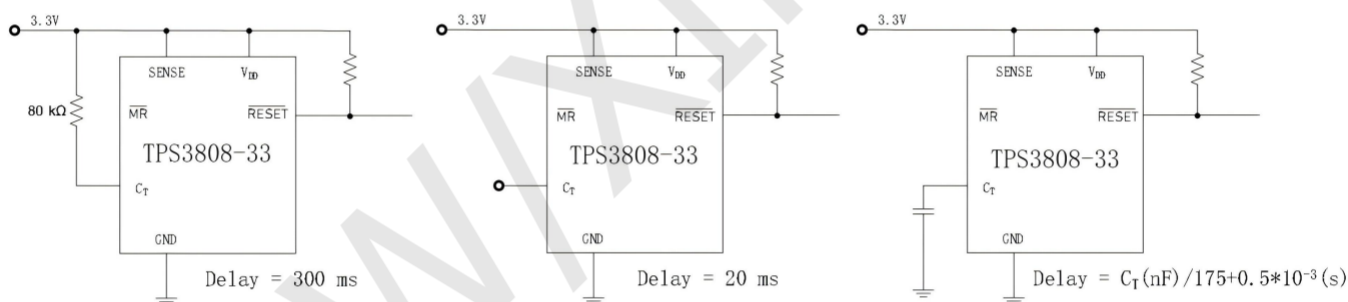


Figure 3. delay time configuration

The reset delay time is determined by the charging time of a precise internal 220 nA current source to charge the external capacitor to 1.23 V. It follows the relations shown as below:

$$T_D = C_T(\text{nF}) / 175 + 0.5 * 10^{-3}(\text{s})$$

When reset condition is triggered either by SENSE pin or manual reset pin, the capacitor discharges. When the conditions are removed, the current source starts to charge the capacitor until its voltage reaches 1.23 V, and therefore deassert $\overline{\text{RESET}}$. In order to have a smaller error in reset delay time, it is recommended to use low-leakage ceramic capacitor.

Manual Reset Input

The manual reset input provides an active way to trigger a reset, by switching $\overline{\text{MR}}$ to logic low. This pin is internally pulled up through a resistor to VDD, so this pin can be left floated. It is recommended to use a MOSFET to minimize drawing current in case the driving voltage on $\overline{\text{MR}}$ does not match with VDD.

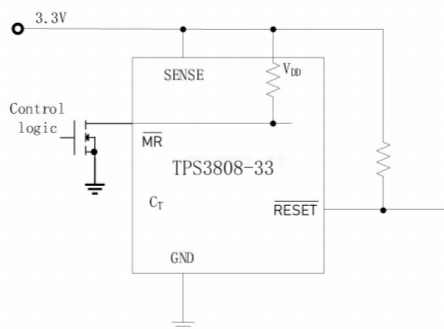


Figure 4. Use a MOSFET to deal with driving voltage mismatch

Reset Output

Either condition which is voltage to be monitored dropping below threshold or $\overline{\text{MR}}$ switching to logic low, will assert the reset output, driving the RESET pin to a low impedance. After both conditions are removed, the delay circuit starts up to provide a user-defined delay time. The external pull-up resistor help to get a voltage higher than V_{DD} .

Power-On Reset Function

Depending on power supply condition, the device works in three modes.

Normal Operation

When supply voltage V_{DD} meets the basic requirements to make the circuits work, i.e. greater than $V_{DD(\text{min})}$, the output RESET behaves according to voltage on the SENSE pin and the logic state of $\overline{\text{MR}}$ as introduced in previous sessions.

Above Power-On Reset Voltage but below $V_{DD(\text{min})}$

When the supply voltage is above power-on reset voltage V_{POR} but below $V_{DD(\text{min})}$, the $\overline{\text{RESET}}$ remains asserted and low impedance no matter what state of voltage is on SENSE pin and $\overline{\text{MR}}$.

Below Power-On Reset Voltage

When the supply voltage is below V_{POR} , $\overline{\text{RESET}}$ is not defined.

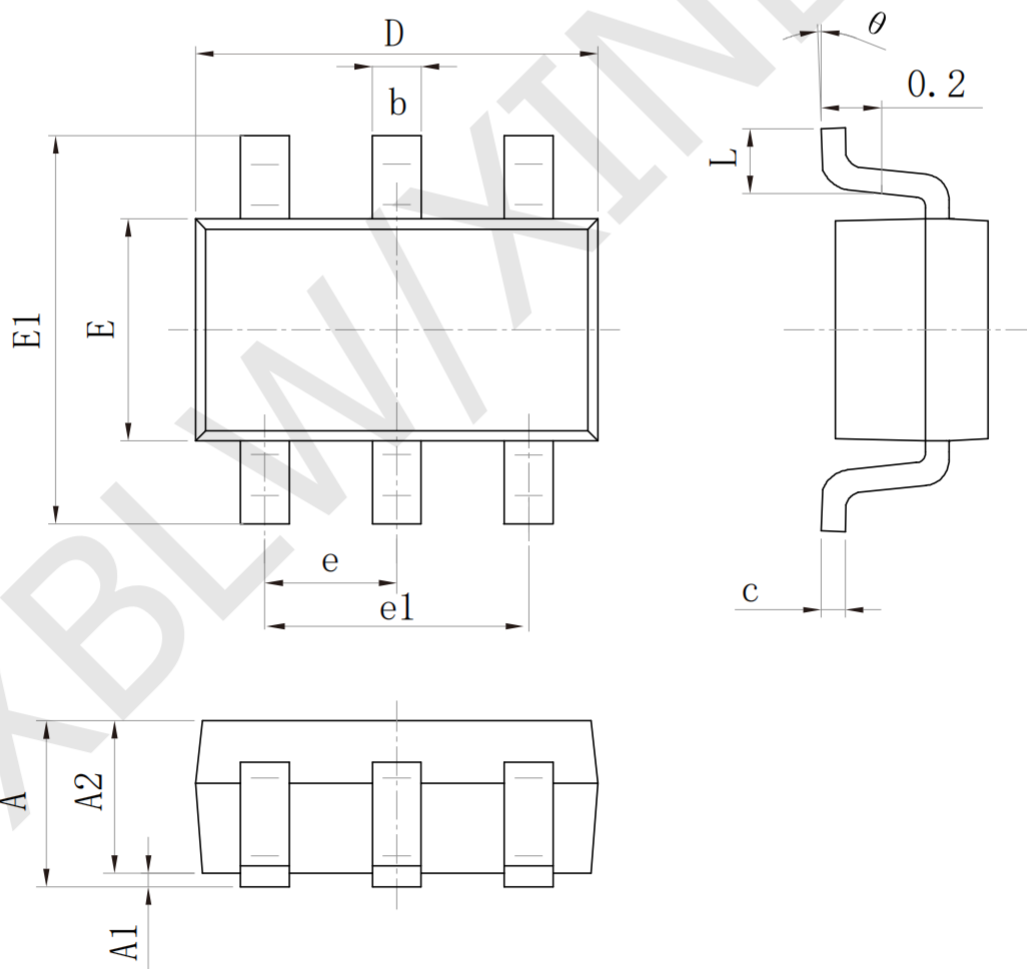
Specification information

Version	Release Date	New/Revised Content
V1.0	2023/10	Initial Writing
V2.0	2025/05	Update Template
V2.1	2026/09	Update packaging size diagram identification

Package Information

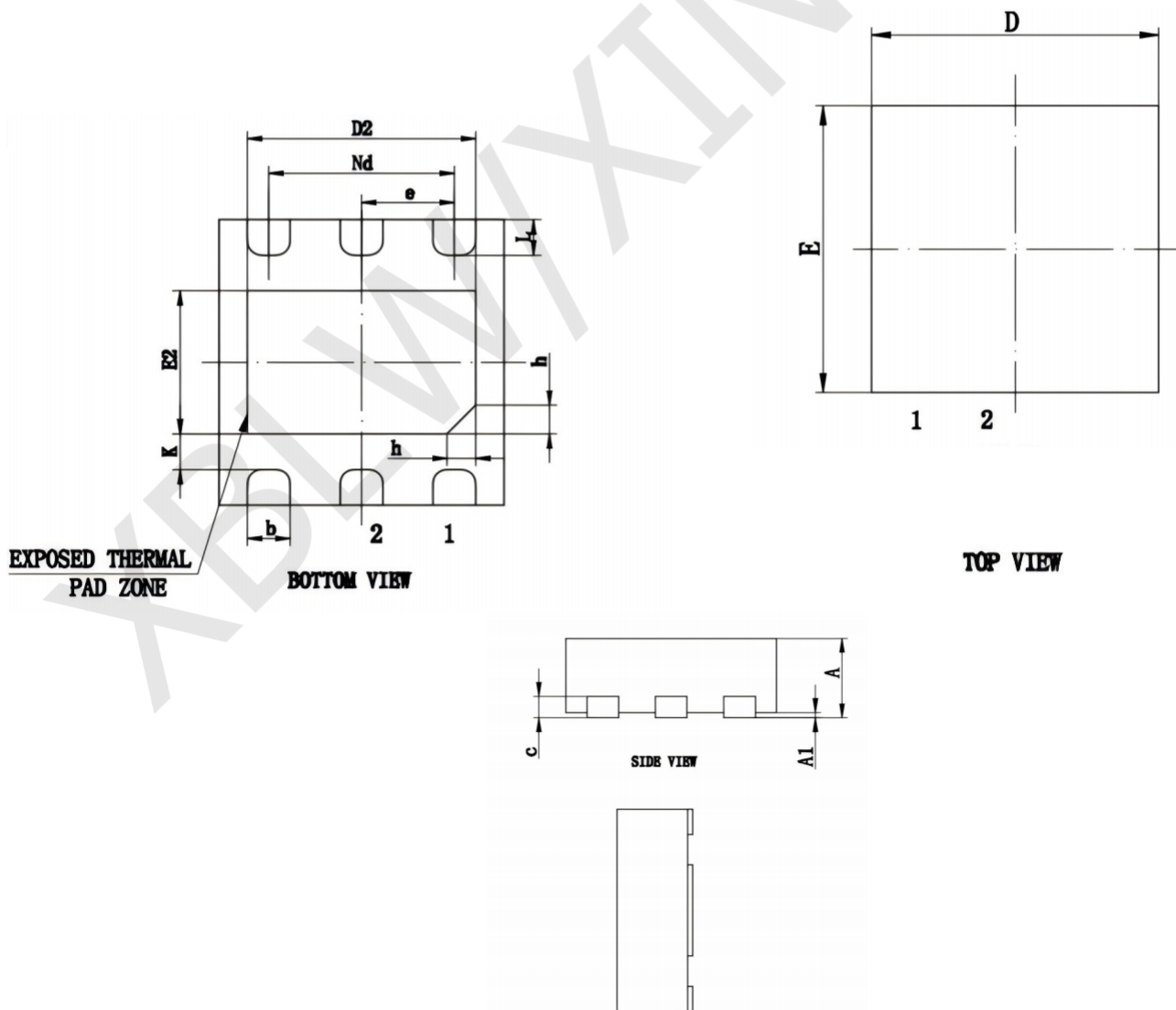
• SOT23-6

SIZE SYMBOL	Dimensions In Millimeters		SIZE SYMBOL	Dimensions In Inches	
	MIN (mm)	MAX (mm)		MIN (in)	MAX (in)
A	1.050	1.250	A	0.041	0.049
A1	0.000	0.100	A1	0.000	0.004
A2	1.050	1.150	A2	0.041	0.045
b	0.300	0.500	b	0.012	0.020
c	0.100	0.200	c	0.004	0.008
D	2.820	3.020	D	0.111	0.119
E	1.500	1.700	E	0.059	0.067
E1	2.650	2.950	E1	0.104	0.116
e	0.950 (BSC)		e	0.037 (BSC)	
e1	1.800	2.000	e1	0.071	0.079
L	0.300	0.600	L	0.012	0.024
θ	0°	8°	θ	0°	8°



DFN2*2-6L

Symbol	Size(mm)		
	Min.	Typ.	Max.
A	0.7	0.75	0.8
A1	---	0.02	0.05
b	0.25	0.3	0.35
c	0.18	0.2	0.25
D	1.9	2	2.1
D2	1.5	1.6	1.7
e	0.65BSC		
Nd	1.30BSC		
E	1.9	2	2.1
E2	0.9	1	1.1
K	0.2	---	---
L	0.2	0.25	0.3
L1	0.15	0.2	0.25



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