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MP4501

60V USB Type-C Port OVP and IEC ESD Protector

DESCRIPTION

The MP4501 is a highly integrated USB Type-C protector that provides 60V short-to-VBUS over-voltage protection (OVP) and IEC electrostatic discharge (ESD) protection.

USB Power Delivery (PD) Extended Power Range (EPR) mode allows the VBUS voltage (V_{BUS}) to reach up to 48V. In a USB Type-C connector, the CC1, CC2, SBU1, and SBU2 pins are the neighbor pins close to the USB Type-C port's VBUS pin that may be physically shorted to VBUS in abnormal connections. The MP4501 integrates four high-voltage MOSFETs that enhance the CCx and SBUx pins with 60V voltage tolerance. If a short-to-VBUS occurs, the MP4501 triggers OVP with a fast response and quickly disconnects the connector from the system controller side.

The MP4501 integrates IEC ESD protection for CCx and SBUx, which meets ±8kV contact discharge and ±15kV air discharge standards. The device offers a very compact solution with minimum external BOM cost.

It also features a fault indicator with OVP and over-temperature protection (OTP).

The MP4501 is available in a TQFN-20 (3mmx3mm) package.

FEATURES

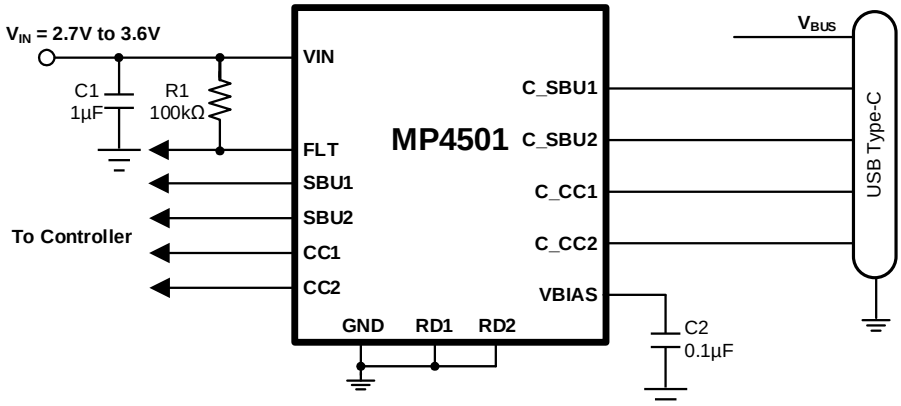
- 2.7V to 3.6V Operating Input Voltage (V_{IN}) Range
- 60V Voltage Rating for the C_CC1, C_CC2, C_SBU1, and C_SBU2 Pins
- Fast 40ns Over-Voltage Protection (OVP) Response Time
- 80µA Quiescent Current (I_Q) at V_{IN} = 3.3V
- Low 350mΩ On Resistance ($R_{DS(ON)}$) CCx MOSFET
- Low 2Ω $R_{DS(ON)}$ SBUx MOSFET
- CCx Pins Support 500mA Capable Current to Pass VCONN Power
- Supports R_D Resistor for Dead Battery Applications
- Over-Temperature Protection (OTP)
- Fault Indicator
- ±8kV Contact and ±15kV Air Discharge IEC ESD Rating for C_CC1, C_CC2, C_SBU1 and C_SBU2
- Available in a TQFN-20 (3mmx3mm) Package

APPLICATIONS

- USB PD Standard Power Range (SPR) and Extended Power Range (EPR)
- Monitors and Docking Stations
- Laptops
- TVs and Mobile Phones

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4501GQT	TQFN-20 (3mmx3mm)	*See Below*	1

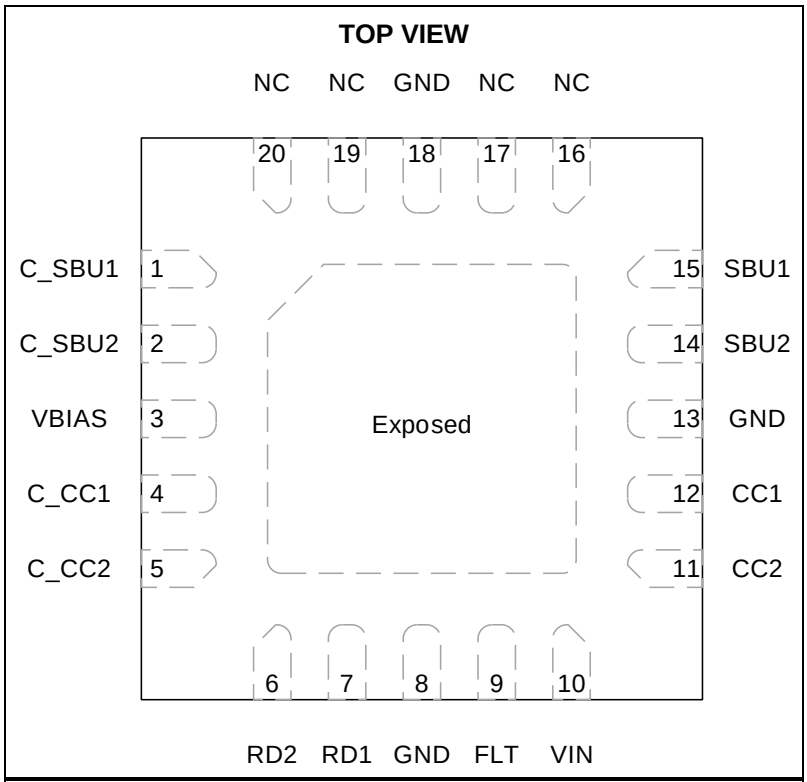
* For Tape & Reel, add suffix -Z (e.g. MP4501GQT-Z).

TOP MARKING

CEZY
LLLL

CEZ: Product code of MP4501GQT
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



TQFN-20 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	C_SBU1	**USB Type-C connector side SBU1.** Connect the C_SBU1 pin to either SBU pin of the USB Type-C connector.
2	C_SBU2	**USB Type-C connector side SBU2.** Connect the C_SBU2 pin to either SBU pin of the USB Type-C connector.
3	VBIAS	**ESD bias pin.** Place a capacitor between the VBIAS pin and GND.
4	C_CC1	**USB Type-C connector side CC1.** Connect the C_CC1 pin to either CC pin of the UBS Type-C connector.
5	C_CC2	**USB Type-C connector side CC2.** Connect the C_CC2 pin to either CC pin of the USB Type-C connector.
6	RD2	**R_D support for CC2.** Connect the RD2 pin to C_CC2 if dead battery resistors are required. Connect this pin to GND if not used.
7	RD1	**R_D support for CC1.** Connect the RD1 pin to C_CC1 if dead battery resistors are required. Connect this pin to GND if not used.
8, 13, 18	GND	**Ground.**
9	FLT	**Fault indicator.** Over-voltage protection (OVP) or over-temperature protection (OTP) can pull the FLT pin low. This pin is an open-drain output and requires external pull-up resistors. Float this pin or connect to it GND if it is not used.
10	VIN	**Supply voltage.** Connect a 1µF decoupling capacitor between the VIN pin and ground, placed as close as possible to the IC.
11	CC2	**System controller side CC2.** Connect the CC2 pin to either CC pin of the USB CC/PD controller.
12	CC1	**System controller side CC1.** Connect the CC1 pin to either CC pin of the USB CC/PD controller.
14	SBU2	**System controller side SBU2.** Connect the SBU2 pin to either SBU pin of the SBU multiplexer (mux).
15	SBU1	**System controller side SBU1.** Connect the SBU1 pin to either SBU pin of the SBU mux.
16, 17, 19, 20	NC	**Not connected.** The NC pin can be floated or connected to GND.
Exposed pad	-	**Exposed pad.** Connect to GND when designing the PCB layout.

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ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +4V
V_{C_CC1}, V_{C_CC2}, V_{C_SBU1}, V_{C_SBU2}, V_{BIAS}, R_{D1}, R_{D2}
…….....-0.3V to +61V
V_{CC1}, V_{CC2}, V_{SBU1}, V_{SBU2}, V_{FLT} .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) (7)
QFN-20 (3mmx3mm)..... 2.5W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (5)

Operating input voltage (V_{IN}).....2.7V to 3.6V
V_{C_CC1}, V_{C_CC2}, V_{CC1}, V_{CC2} .....0V to 5.25V
V_{C_SBU1}, V_{C_SBU2}, V_{SBU1}, V_{SBU2}.....0V to 4.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC_BOT}

TQFN-20 (3mmx3mm)
JESD51-7 (6).....61……..4.1°C/W
EV4501-Q-00A (7)……..…40.6.....…..°C/W

Ψ_{JT}

JESD51-7 (6)……..1.....°C/W
EV4501-Q-00A (7)……5.7.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) IEC 61000-4-2 330ohm and 150pF RC parameter for ESD generator discharge network.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) The device is not guaranteed to function outside of its operating conditions.
6) The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-2 and JESD51-14, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC_BOT} shows the thermal resistance from junction-to-case bottom, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
7) Measured on the EV4501-Q-00A, a 4cmx3cm, 4-layer PCB with 2oz. The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature in the real system, based on equation $T_J = \Psi_{JT} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of IC at real application, and T_{CASE_TOP} is the case top temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3V, T_J = -40°C to +125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
System						
Quiescent supply current	I_Q	V_{IN} = 3.3V, T_J = 25°C		80	120	µA
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		2.4	2.55	2.7	V
V_{IN} under UVLO threshold hysteresis	V_{UVLO_HYS}			220		mV
CCx pins leakage current	I_{CC_LKG}	V_{IN} = 3.3V, C_CCx connected to RDx, V_{C_CCx} = 3.6V, CCx floating, measure current into C_CCx		5		µA
SBUx pins leakage current	I_{SBU_LKG}	V_{IN} = 3.3V, V_{C_SBUx} = 3.6V, SBUx floating, measure current into C_SBUx		3		µA
Leakage current from C_CCx to CCx		V_{IN} = 0V, V_{C_CCx} = 60V, V_{CCx} = 0V			1	µA
Leakage current from C_SBUx to SBUx		V_{IN} = 0V, V_{C_SBUx} = 60V, V_{SBUx} = 0V			1	µA
Thermal shutdown [9]				160		°C
Thermal shutdown hysteresis [9]				20		°C
CCx MOSFETs						
CCx MOSFET on resistance	$R_{DS(ON)_CCx}$	V_{IN} = 3.3V, V_{CCx} = 5V		350		mΩ
On resistance flatness	$R_{DS(ON)_CCx_FLAT}$	Sweep CCx between 0V to 3.6V			10	mΩ
Over-voltage protection (OVP) rising threshold	V_{CCx_OVP}		5.3	5.5	5.7	V
OVP threshold hysteresis	$V_{CCx_OVP_HYS}$			120		mV
CCx clamp voltage [9]	V_{CCx_CLAMP}			8		V
Equivalent on capacitance [9]	C_{ON_CCx}	Capacitance from C_CCx, CCx to GND when power is on, V_{C_CCx}/V_{CCx} = 0V to 1.2V, measured AC signal frequency = 400kHz		50		pF
SBUx MOSFETs						
SBUx MOSFET on resistance	$R_{DS(ON)_SBUx}$	V_{IN} = 3.3V, V_{SBUx} = 3.6V		2		Ω
On resistance flatness	$R_{DS(ON)_SBUx_FLAT}$	Sweep SBUx between 0V to 3.6V			200	mΩ
OVP rising threshold	V_{SBUx_OVP}		4.6	4.8	5	V
OVP threshold hysteresis	$V_{SBUx_OVP_HYS}$			125		mV
SBUx clamp voltage [9]	V_{CC_SBUx}			8		V
3dB bandwidth [9]	BW_{CC}			210		MHz
Equivalent on capacitance [9]	C_{ON_SBUx}	Capacitance from C_SBUx, SBUx to GND when power is on, V_{C_SBUx}/V_{SBUx} = 0V to 3.6V, measured AC signal frequency = 100MHz		16		pF

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, T_J = -40°C to +125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Dead Battery (RD1, RD2)						
Dead battery pull-down resistance	R_D	V_{RDx} = 2.6V, T_J = -40°C to +125°C [8] 20% x 5.1kΩ range in USB Type-C specifications	4.1	5.1	6.1	kΩ
FLT						
Output low voltage	V_{OL}	I_{SINK} = 5mA			0.3	V
Leakage current [9]	I_{LKG_FLT}	V_{FLT} = 5.5V			1	µA
Timing Characteristics						
MOSFET on time	t_{ON_MOSFET}	Time from V_{IN} UVLO until CCx and SBUx MOSFETs are on		2.6		ms
R_D present time	t_{RD}	Time from V_{IN} UVLO and CCx MOSFETs are on until R_D is removed		6.7		ms
R_D present time after over-voltage (OV) condition	t_{RD_OVP}	Time from R_D is present after OVP occurs to R_D being removed		6.2		ms
OVP response time for CCx MOSFETs [9]	$t_{OVP_RES_CC}$	Time from OVP occurrence until MOSFETs turns off		40		ns
OVP response time for SBUx MOSFETs [9]	$t_{OVP_RES_SBU}$	Time from OVP occurrence until MOSFETs turns off		40		ns
Minimum OVP recovery time for CCx MOSFETs	$t_{MIN_OVP_RECOVER_CCx}$	Minimum time until CCx MOSFETs turn on again after OVP; OVP must be removed for MOSFETs to turn on		1.15		ms
Minimum OVP recovery time for SBUx MOSFETs	$t_{MIN_OVP_RECOVER_SBUx}$	Minimum time until SBUx MOSFETs turn on agian after OVP; OVP must be removed for MOSFETs to turn on		1.15		ms
FLT deglitch time	t_{FLT}	Time from OVP or OTP occurrence to FLT going low		20		µs
FLT OV recovery time	$t_{FLT_RECOVER_OV}$	Time from CC MOSFETs turning on after OVP to FLT going high		4.8		ms

Notes:

8) All min/max parameters are tested at T_J = 25°C. Limits over-temperature are derived by design, characterization, and correlation.
9) Guaranteed by design. Not tested in production.

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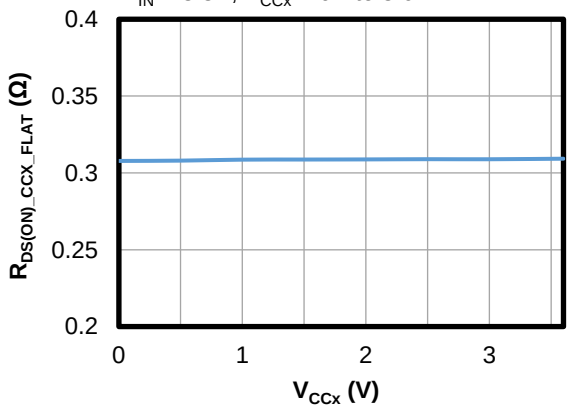
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TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

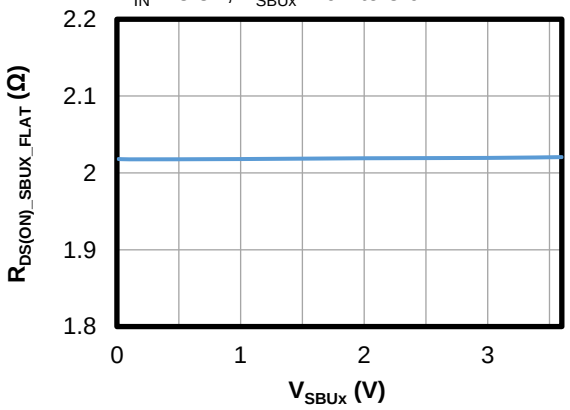
CCx On Resistance Flatness

V_{IN} = 3.3V, V_{CCx} = 0V to 3.6V



SBUx On Resistance Flatness

V_{IN} = 3.3V, V_{SBUx} = 0V to 3.6V



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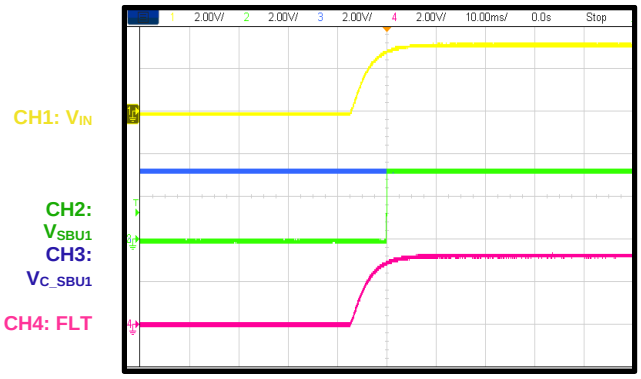
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TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

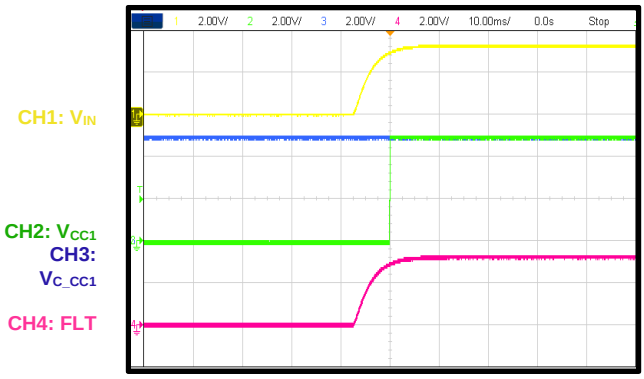
Start-Up through VIN

V_{C_SBU1} = 3.3V



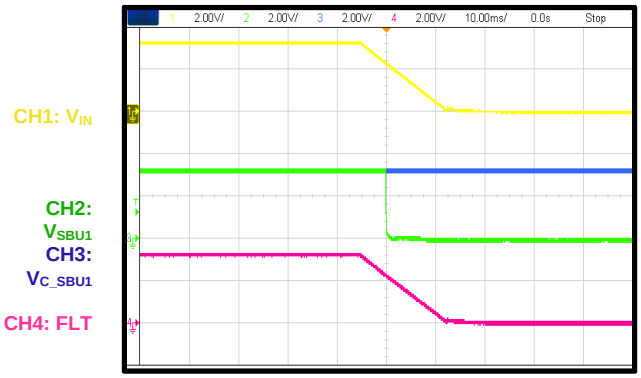
Start-Up through VIN

V_{C_CC1} = 5V



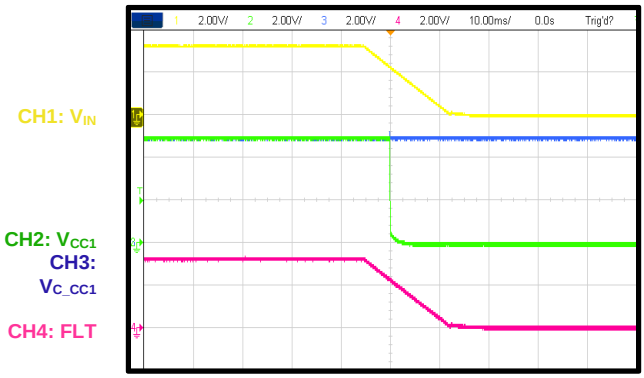
Shutdown through VIN

V_{C_SBU1} = 3.3V



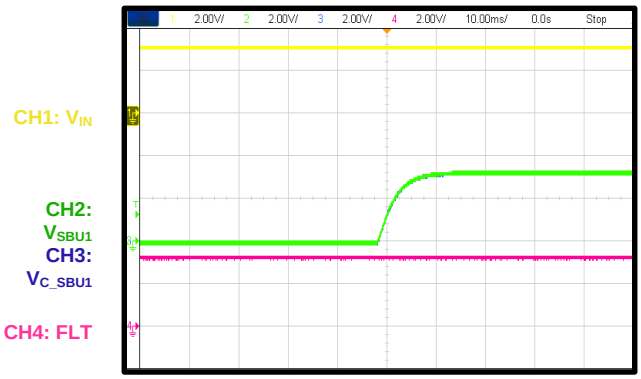
Shutdown through VIN

V_{C_CC1} = 5V



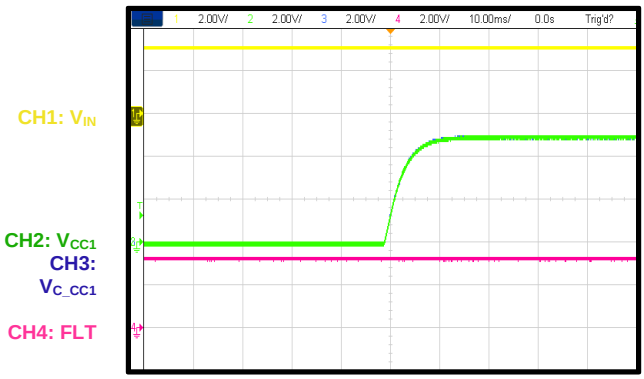
C_SBU1 On

V_{C_SBU1} = 3.3V



C_CC1 On

V_{C_CC1} = 5V



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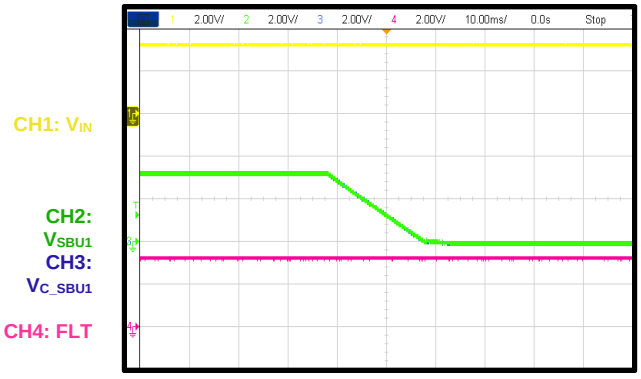
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

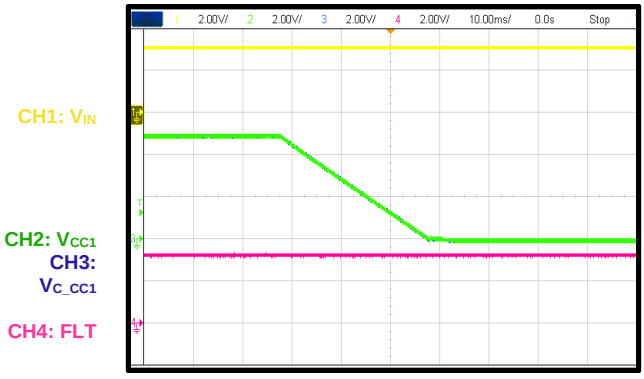
C_SBU1 Off

V_{C_SBU1} = 3.3V



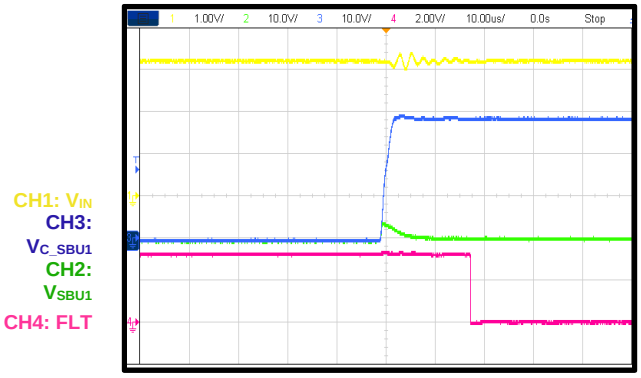
C_CC1 Off

V_{C_CC1} = 5V



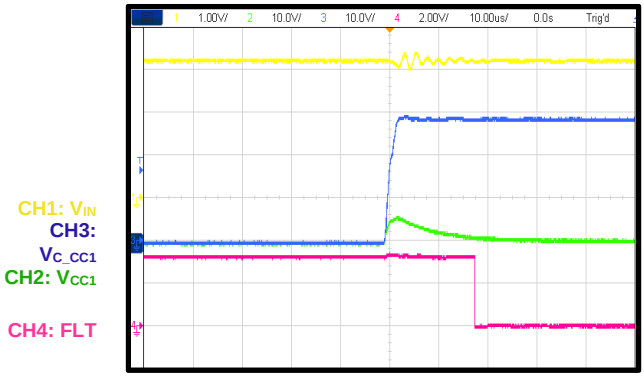
C_SBU1 28V OVP

V_{C_SBU1} short to 28V



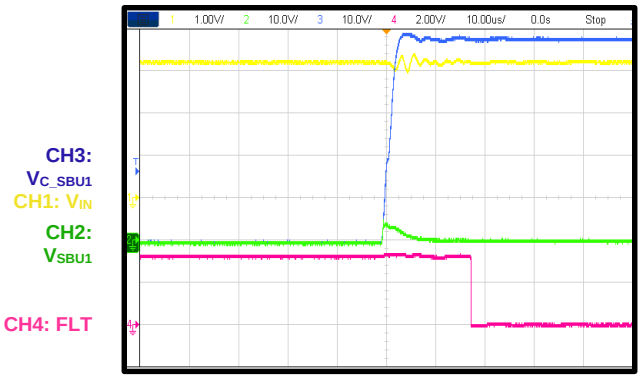
C_CC1 28V OVP

V_{C_CC1} short to 28V



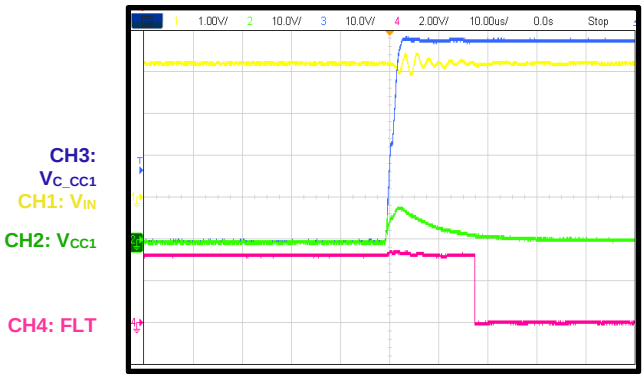
C_SBU1 48V OVP

V_{C_SBU1} short to 48V



C_CC1 48V OVP

V_{C_CC1} short to 48V



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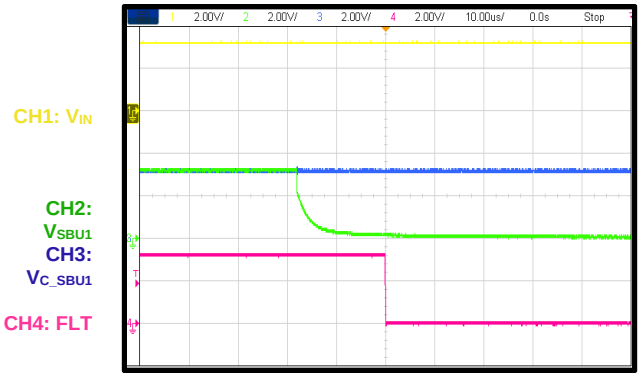
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

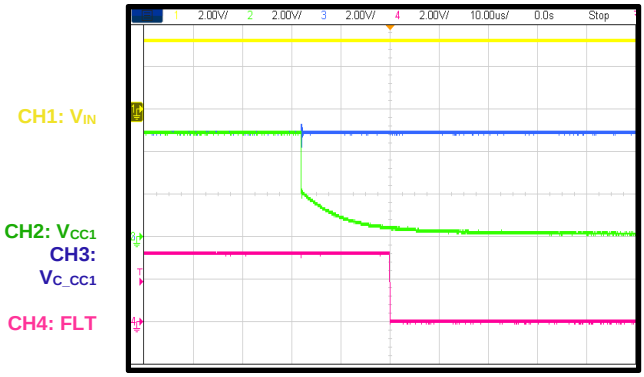
C_SBU1 OTP Entry

V_{C_SBU1} = 3.3V



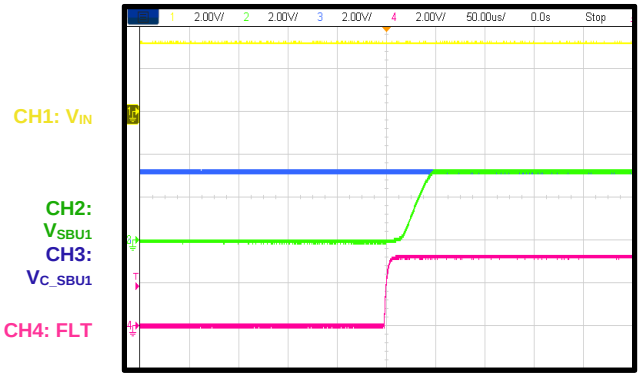
C_CC1 OTP Entry

V_{C_CC1} = 5V



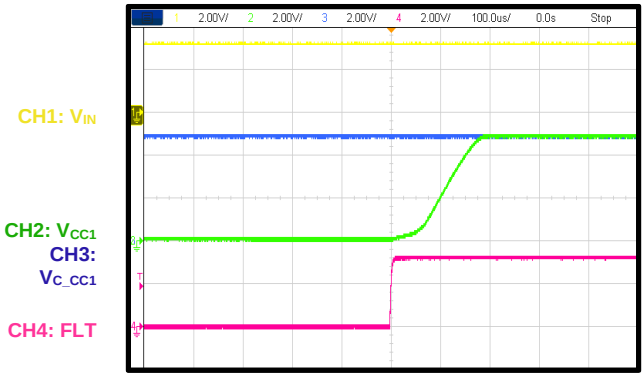
C_SBU1 OTP Recovery

V_{C_SBU1} = 3.3V



C_CC1 OTP Recovery

V_{C_CC1} = 5V



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FUNCTIONAL BLOCK DIAGRAM

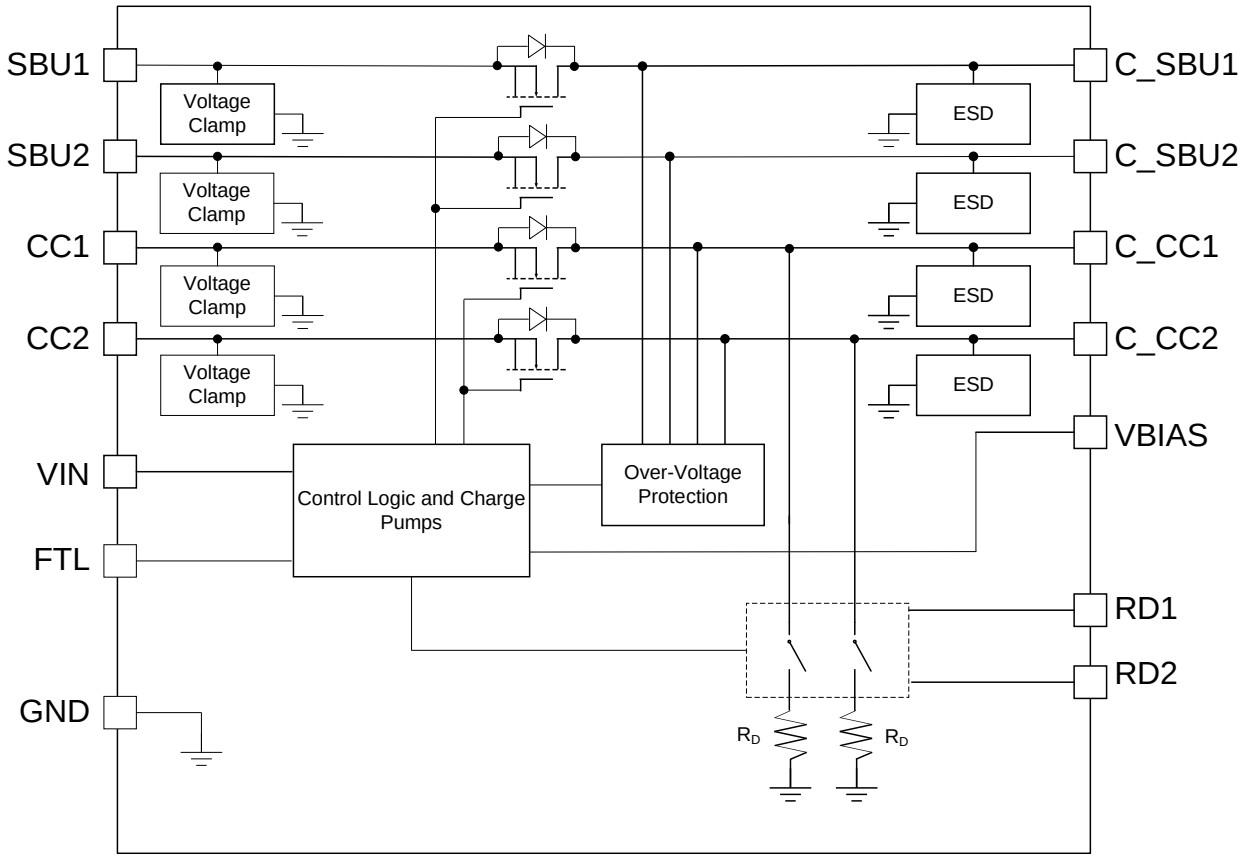


Figure 1: Functional Block Diagram

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OPERATION

The MP4501 is a highly integrated USB Type-C protector that provides four channels of 60V short-to-VBUS over-voltage protection (OVP). It is fully compatible with USB Power Deliver (PD) 3.1 Extended Power Range (EPR) mode and four channels of IEC electrostatic discharge (ESD) protection. Figure 1 on page 11 shows the internal block diagram.

Short-to-VBUS Over-Voltage Protection (OVP)

In USB Type-C connectors, the neighbor pins close to the VBUS pin (CC1, CC2, SBU1, and SBU2) may be shorted to VBUS in abnormal connections because of the small pin pitch. During a short-to-VBUS event, the CCx and SBUx pins must withstand 48V voltage stress to support the full USB PD3.1 power range. The MP4501 provides four channels of 60V OVP MOSFETs for the CCx and SBUx pins.

The MP4501 has a fast 40ns OVP response time to avoid high voltages on the CCx and SBUx pins. If the voltage on any C_CCx or C_SBUx pin exceeds the OVP threshold, the four MOSFETs turn off quickly. Once the voltage on all C_CCx and C_SBUx pins drops below the OVP threshold with hysteresis, the MOSFETs turn back on automatically. Figure 2 shows OVP and the OVP recovery process.

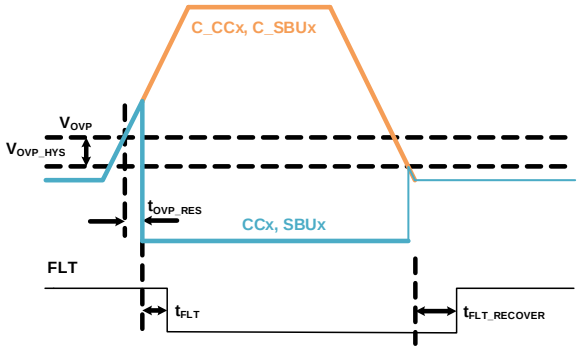


Figure 2: OVP and OVP Recovery

System-Side Voltage Clamp

The MP4501 has additional voltage clamps on the system controller side CCx and SBUx pins. If a short-to-VBUS occurs, the C_CCx voltage (V_{C_CCx}) and C_SBUx voltage (V_{C_SBUx}) increase rapidly. Even with a fast response time to turn off the MOSFETs during a short-to-VBUS event, voltage overshoot may still be seen on the system-side CCx and SBUx pins. The system-side voltage clamp circuit prevents the CCx voltage (V_{CCx}) and SBUx voltage (V_{SBUx}) from exceeding the clamp voltage threshold on the system side.

IEC Electrostatic Discharge (ESD) Protection

The MP4501 integrates four channels of IEC ESD protection on the C_CC1, C_CC2, C_SBU1, and C_SBU2 pins. The ESD protection meets ±8kV contact discharge and ±15kV air discharge standards as specified by IEC 61000-4-2. The MP4501 provides up to 60V short-to-VBUS and ESD protection in a single chip, which helps reduce the total cost of USB Type-C PD applications.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage (V_{IN}) and enables or disables the IC.

When V_{IN} is below its UVLO, the MP4501 is in shutdown mode; all circuitry is disabled and dead battery resistors (R_D) are present on the RD1 and RD2 pins. This allows the USB Type-C port to charge a dead battery with the default VBUS. Once V_{IN} rises above its UVLO, the MP4501 starts up and all the MOSFETs turn on. After the CCx MOSFETs are fully on, R_D is removed.

CCx MOSFETs Support 500mA Current Capability to VCONN Power Path

Once the connection between the source and sink is established, the unused CCx pin can be reassigned to function as a dedicated power supply pin (VCONN) to provide power to Electronically Marked (E-Marked) cables, VCONN-powered accessories or VCONN-powered USB devices. Typically, 1W is required to support VCONN. In addition, if USB Type-C PD Alternate Modes are used, higher power is allowed though VCONN.

The MP4501's CCx MOSFETs are designed with low conduction resistance (typically 350mΩ) to meet 500mA current capability and be compliant with USB PD specifications.

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CCx Dead Battery Resistor (RD1, RD2)

When the MP4501 is used as a sink or dual-role power (DRP), V_{IN} may be powered from the battery pack. If the battery pack is not used for a long time and stops to supply other circuits, the MP4501 will not start up, which is a called dead battery condition. In a dead battery condition, the V_{IN} is below its UVLO, the CCx MOSFETs are off, and the system USB Type-C controller's R_D is isolated from the source side. The MP4501 integrates a dead battery pull-down resistor (R_D) to enable VBUS and charge the battery. The R_D circuit has a 60V voltage tolerance.

Dead battery functionality is supported through the RD1 and RD2 pins. If dead battery functionality and R_D are required, connect RD1 to C_CC1 and connect RD2 to C_CC2. If dead battery functionality is not required, connect RD1 and RD2 to GND.

When V_{IN} is under its UVLO, R_D is always present. Once V_{IN} exceeds its UVLO, the CCx MOSFETs turn on and R_D is removed (see Figure 3). Then, R_D on the USB Type-C CC/PD controller is exposed on the CCx line. To ensure that R_D on the CC/PD controller takes over control correctly, the MP4501 removes its R_D after the CCx MOSFETs fully turn on.

If OVP occurs, R_D turns on for 5ms (typical) to keep the USB PD source connection alive, and then automatically removes R_D after 5ms. This helps avoid USB PD disconnection if a surge voltage triggers OVP.

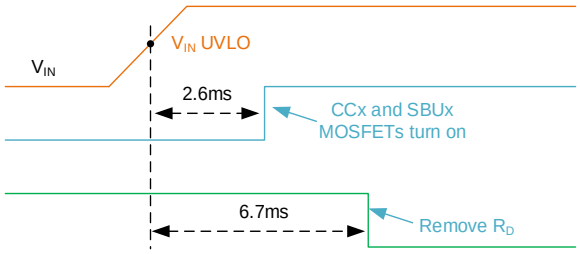


Figure 3: VIN Start-Up Sequence

Fault Indicator

FLT is the fault indicator pin. It is an open-drain output and should be pulled up to a voltage source. During normal operation, FLT is high. If OVP or thermal shutdown (TSD) occurs, FLT goes low to assert the fault. FLT does not latch, and returns to high after the fault is removed. Once the device recovers from OVP, FLT has a typical 4ms delay before going high again. Once the device recovers from TSD, FLT goes high again with no delay.

Thermal Shutdown (TSD)

The MP4501 offers thermal protection by monitoring the IC junction temperature (T_J) internally. This prevents the chip from operating at exceedingly high temperatures. If T_J exceeds the TSD threshold (typically 160°C), all MOSFETs turn off and FLT is pulled low. This is a non-latch protection; once T_J drops below the TSD threshold with hysteresis (typically 20°C), the MOSFETs turn back on and FLT goes high again.

Table 1 shows the MP4501's operation modes in normal conditions and fault conditions.

Table 1: Operation Mode

Conditions	OVP		TSD	Dead Battery R_D	FLT	CCx MOSFETs	SBUx MOSFETs
	C_CCx	C_SBUx					
V_{IN} < UVLO	X (10)	X	X	On	Open drain	Off	Off
V_{IN} > UVLO	0	0	0	Off	Open drain	On	On
	1	0	0	On for 6.7ms, then off	Low	Off	Off
	0	1	0	On for 6.7ms, then off	Low	Off	Off
	0	0	1	Off	Low	Off	Off

Notes:

10) "X" means any condition in the absolute limit range. "0" means the event has not occurred. "1" means the event has occurred.

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APPLICATION INFORMATION

Selecting the VBIAS capacitor

The MP4501 integrates four channels of IEC ESD protection on the C_CC1, C_CC2, C_SBU1, and C_SBU2 pins. The ESD protection meets ±8kV contact discharge and ±15kV air discharge standards specified by IEC 61000-4-2.

Adding a VBIAS capacitor (C_{VBIAS}) helps the device pass IEC 61000-4-2 ESD tests. The more capacitors there are, the better the IEC performance. Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR, small temperature coefficients, and excellent derating performance. A a 0.1µF 100V X7R capacitor is recommended.

Selecting the Input Capacitor

The VIN pin provides power to all of the MP4501's circuitry. It is recommended to use a 1µF ceramic decoupling capacitor for the input capacitor (C_{IN}).

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and improved ESD performance. A 4-layer layout is recommended. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the VIN decoupling capacitor (C_{IN}) as close to the VIN pin as possible.
2. Place the VBIAS ESD protection capacitor (C_{VBIAS}) as close to the VBIAS pin as possible.
3. Place nine vias on the exposed pad of the IC.
4. Connect the exposed pad to ground.
5. Use short, direct, and wide traces to connect CCx, SBUx, C_CCx, and C_SBUx to the USB Type-C connector.

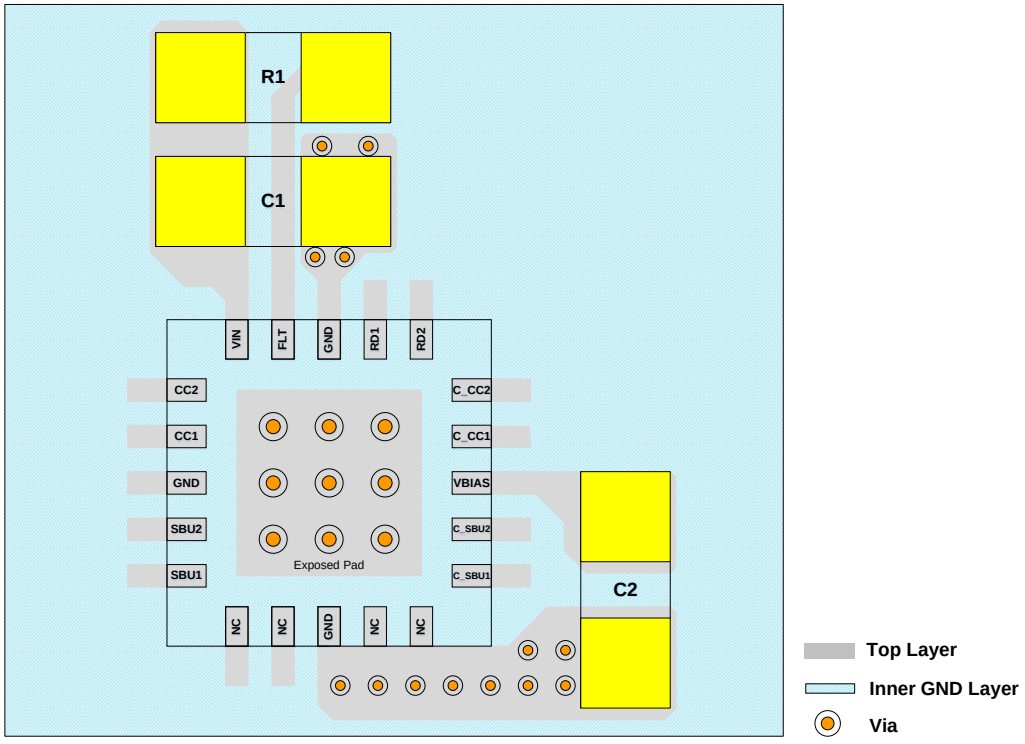


Figure 4: Recommended PCB Layout (12)

Note:

11) The recommended layout is based on Figure 6 on page 15.

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TYPICAL APPLICATION CIRCUITS

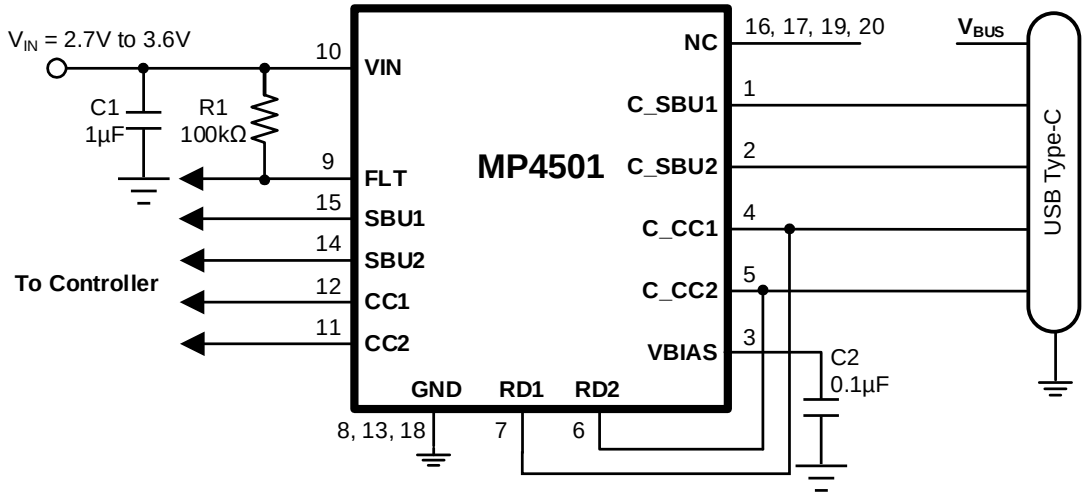


Figure 5: Typical Application Circuit with Dead Battery Support

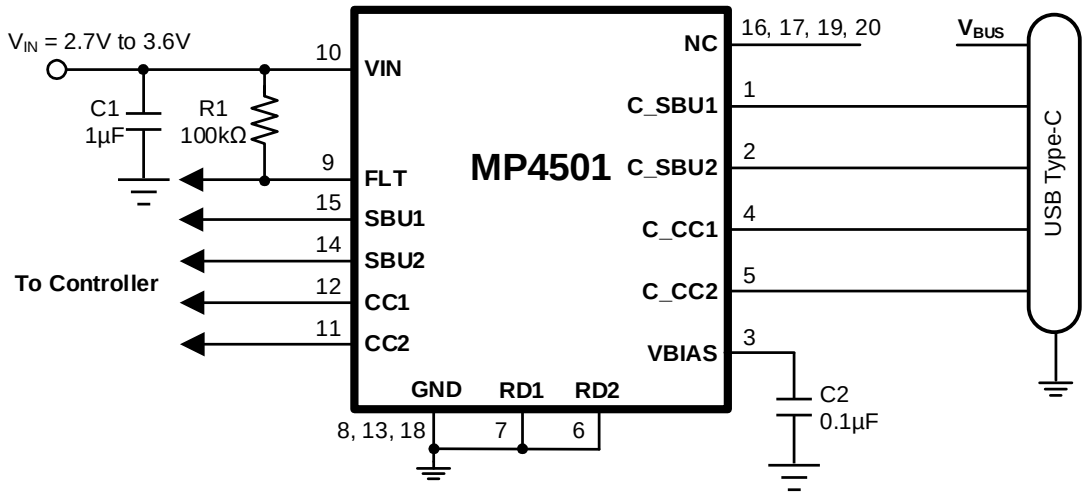


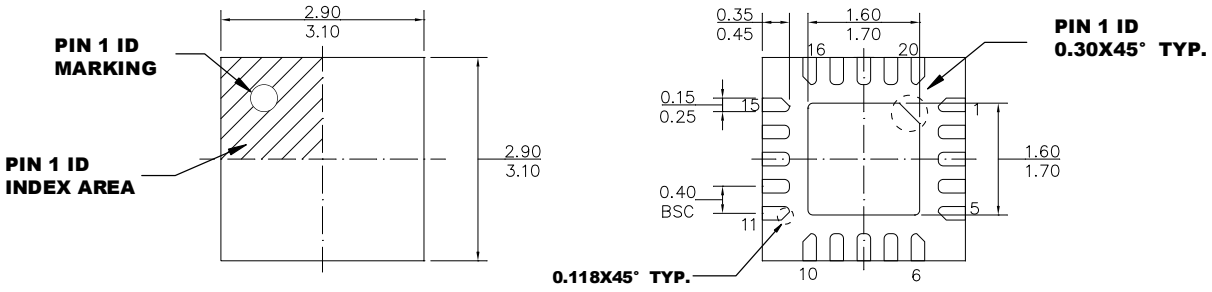
Figure 6: Typical Application Circuit without Dead Battery Support

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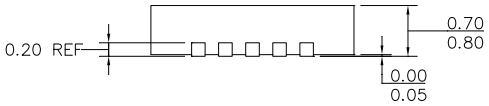
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PACKAGE INFORMATION

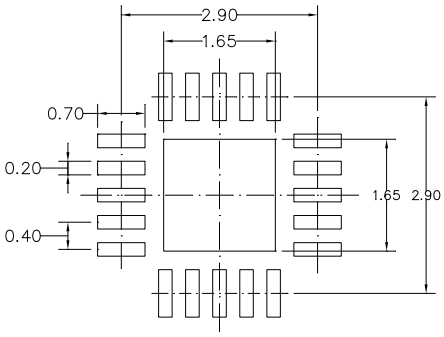
TQFN-20 (3mmx3mm)
Wettable Flank



TOP VIEW **BOTTOM VIEW**



SIDE VIEW



RECOMMENDED LAND PATTERN

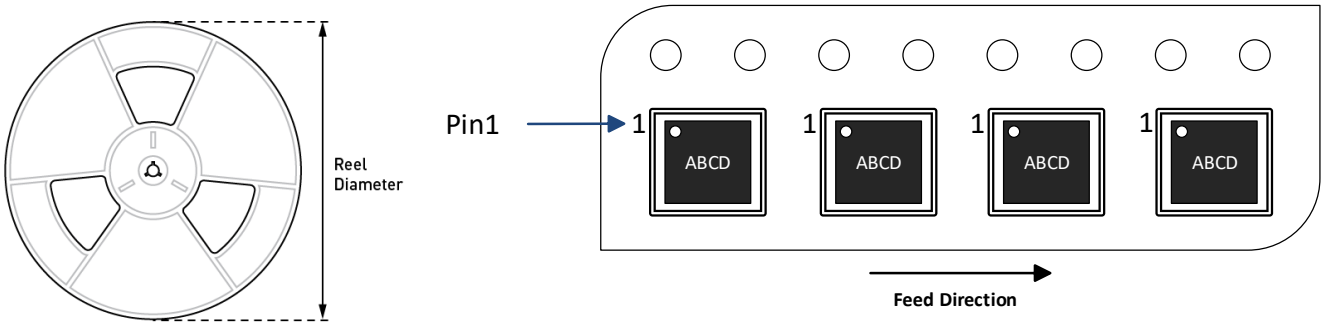
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1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4501GQT-Z	TQFN-20 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/15/2026	Initial Release	-

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