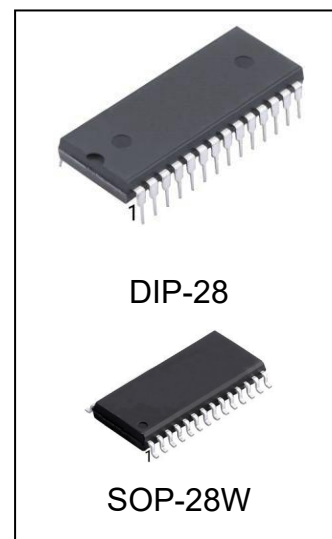


独立 CAN 控制器

功能特点

- 兼容默认的 BasicCAN 模式
- 扩展的 64byte 接收缓冲器 (FIFO)
- 与 CAN2.0B 协议兼容
- 同时支持 11 位和 29 位识别码
- 位速率高达 1Mbps/s
- PeliCAN 模式扩展功能
 - 可读/写访问的错误计数器
 - 可编程的错误报警限制
 - 最近一次错误代码寄存器
 - 对每一个 CAN 总线错误的中断
 - 具体控制位控制的仲裁丢失中断
 - 单次发送(无重发)
 - 只听模式(无确认出错)
 - 支持热插拔(软件位速率检测)
 - 验收滤波器扩展 (4 字节代码 4 字节屏蔽)
 - 自身信息接收(自接收请求)
- 24MHz 时钟频率
- 多类型微处理器的接口
- 可编程的 CAN 输出驱动器配置
- 工作温度范围-40~+125℃



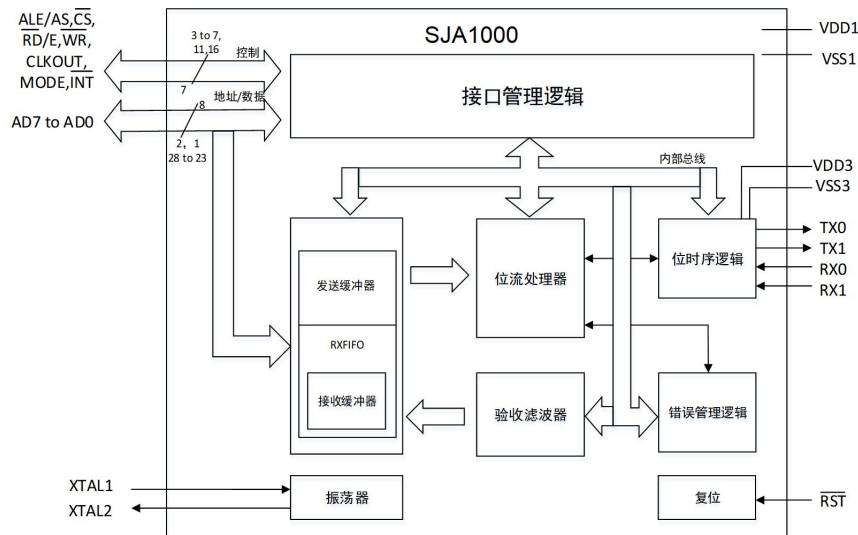
产品订购信息

产品名称	封装	打印名称	包装	包装数量
SJA1000N	DIP-28	SJA1000	管装	300 只/盒
SJA1000M/TR	SOP-28W	SJA1000	编带	1500 只/盘

概述

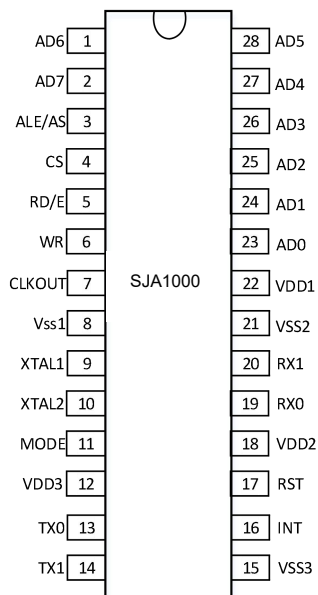
SJA1000 是一种独立 CAN 控制器，用于移动目标和一般工业环境中的区域网络控制。而且，它增加了一种新的工作模式 PeliCAN，这种模式支持具有很多新特性的 CAN 2.0B 协议。

功能框图



管脚排列图

SOP-28W/DIP-28



管脚排列

符号	引脚	说明
AD7-AD0	2, 1, 28-23	多路地址/数据总线
ALE/AS	3	ALE 输入信号(Intel 模式), AS 输入信号(Motorola 模式)
/CS	4	片选输入, 低电平允许访问 SJA1000
/RD /E	5	微控制器的/RD 信号(Intel 模式)或 E 使能信号(Motorola)模式
/WR	6	微控制器的/WR 信号(Intel 模式)或(R /WR) 信号(Motorola) (模式)
CLKOUT	7	SJA1000 产生的提供给微控制器的时钟输出信号, 时钟信号来源于内部振荡器且通过编程驱动, 时钟控制寄存器的时钟关闭位可禁止该引脚
VSS1	8	接地
XTAL1	9	输入到振荡器放大电路, 外部振荡信号由此输入 ^{注 1}
XTAL2	10	振荡放大电路输出, 使用外部振荡信号时左开路输出 ^{注 1}
MODE	11	模式选择输入 1=Intel 模式 0=Motorola 模式
VDD3	12	输出驱动的 5V 电压源
TX0	13	从 CAN 输出驱动器 0 输出到物理线路上
TX1	14	从 CAN 输出驱动器 1 输出到物理线路上
VSS3	15	输出驱动器接地
/INT	16	中断输出, 用于中断微控制器, /INT 在内部中断寄存器各位都被置位时低电平有效, /INT 是开漏输出, 且与系统中的其它/INT 是线或的, 此引脚上的低电平可以把 IC 从睡眠模式中激活
/RST	17	复位输入, 用于复位 CAN 接口 (低电平有效), 把/RST 引脚通过电容连到 VSS。通过电阻连到 VDD 可自动上电复位 (例如: C=1nF; R=50K)
VDD2	18	输入比较器的 5V 电压源
RX0 RX1	19, 20	从物理的 CAN 总线输入到 SJA1000 的输入比较器支配, 控制电平将会唤醒 SJA1000 的睡眠模式, 如果 RX1 比 RX0 的电平高就读支配(控制)电平, 反之读弱势电平, 如果时钟分频寄存器的 CBP 位被置位, 就旁路 CAN 输入比较器以减少内部延时(此时连有外部收发电路; 这种情况下只有 RX0 是激活的; 弱势电平被认为是高而支配电平被认为是低)
VSS2	21	输入比较器的接地端
VDD1	22	逻辑电路的 5V 电压源

注 1: XTAL1 和 XTAL2 引脚必须通过 15pF 的电容连到 VSS1。

极限值

符合 AMR (Absolute Maximum Rating) 系统 (IEC134) 规定 所有电压都是以 VSS 为参考的

符号	参数	条件	最小值	最大值	单位
VDD	电源		-0.5	+6.5	V
I _{I,IO}	除了 TX0 和 TX1 之外所有引脚的输入/输出电流		-	±4	mA
I _{OT(sink)}	TX0 和 TX1 共消耗的电流	注 2	-	30	mA
I _{OT(source)}	TX0 和 TX1 源电流的和	注 2	-	-20	mA
T _{amb}	工作环境温度*		-40	+125	°C
T _{stg}	储存温度		-65	+150	°C
P _{tot}	总功耗		-	1.0	W
V _{esd}	各引脚的放电	注 4	-1500	+1500	V
		注 5	-200	+200	V
T _{LEAD}	引脚温度 (焊接 10s)		-	260	°C

注：1、极限参数是指无论在任何条件下都不能超过的极限值。万一超过此极限值，将有可能造成产品劣化等物理性损伤；同时在接近极限参数下，不能保证芯片可以正常工作。

2、IOT 在总线失败情况下是允许的，因为此时 TX 输出在很短时间后（总线关闭状态）被自动关闭。正常操作时 IOT 是一峰值电流，宽度 t<100ms。每个 TX 输出平均输出电流不超过 10mA。

3、这个值是基于可允许的最大温度和封装热阻，而不是设备功耗。

4、人体模型：等效于通过 1.5kΩ 的电阻给 100pF 的电容放电。

5、机器模型：等效于通过 25Ω 和正 2.5μH 的 RL 电路给 200pF 的电容放电。

注*：-40~+125°C 范围为设计温度,该器件为工业级产品,非车规级产品,如需车规级产品需要自行按照 AEC-Q100 标准筛选,或者咨询本公司销售人员进行购买。

直流特性

VDD=5V (±10%) VSS=0V; Tamb=-40~+125Ω; 所有电压均参考于 VSS; 除非有特殊说明。

符号	参数	条件	最小值	最大值	单位
电源					
VDD	电压源		4.5	5.5	V
IDD	工作电流	fOSC=24MHz;注 1	-	15	mA
Ism	睡眠模式电流	振荡器非激活状态; 注 2	-	40	uA
输入					
VIL1	在引脚 ALE/AS /CS (/RD)/E /WR和 MODE 上的低电平输入		-0.5	+0.8	V
VIL2	在引脚 XTAL1 和/INT 上的低电平输入电压		-	0.3 VDD	V
VIL3	在引脚 /RST,AD0-AD7和 RX0 上的低电平输入电压		-0.5	+0.6	V
VIH1	在引脚 ALE/AS,/CS (/RD)/E/WR 和 MODE 上的高电平输入电压		2.0	VDD+0.5	V
VIH2	在引脚 XTAL1 和/INT 上的高电平输入电压		0.7VDD	-	V
VIH3	在引脚 /RST,AD0-AD7和 RX0 上的高电平输入电压		2.4	VDD+0.5	V
hysRST	在引脚 /RST,AD0-AD7和 RX0 ⁽⁵⁾ 上的输入滞后		500	-	mA
ILI	除XTAL1,RX0 和RX1 外各引脚的漏电流	0.45V<VI(D)<VDD;注 3	-	±2	uA
输出					
VOL	在引脚 AD0-AD7,CLKOUT 和/INT 上的低电平输出电压	IOL=4Ma	-	0.4	V
VOH	在引脚 AD0-AD7,CLKOUT 和/INT 上的高电平输出电压	IOH=-4mA	VDD-0.4	-	V
CAN 输入比较器					
Vth(I)(diff)	差动输入阈值电压	VDD=5V±10%; 1.4V<VI(RX)<VDD-1.4V 注 4 和 6	-	32	mV
Vhys	迟滞电压		8	30	mV
Ii	输入电流		-	±400	nA
CAN 输出驱动器					
VOL(TX)	在引脚 TX0 和 TX1 上的低电平输入电压	VDD=5V±10% IO=1.2mA; 注 6 IO=10mA	- -	0.05 0.4	V
VOH(TX)	在引脚 TX0 和 TX1 上的高电平输入电压	VDD=5V±10% IO=1.2mA; 注 6 IO=10mA	VDD-0.05 VDD-0.4	- -	V

注：

AD0-AD7=ALE=/RD=/WR=/CS=VDD;/RST=MODE=VSS;RX0=2.7V;RX1=2.3V;XTAL1=0.5V 或 VDD-0.5V;所有输出都是空载

AD0-AD7=ALE=/RD=/WR=/INT=/RST=/CS=MODE=RX0=VDD;RX1=XTAL1=VSS;所有输出空载

VI D=数据输入引脚的输入电压

VI RX=RX0 和 RX1 引脚上的输入电压

只在比较器忽略模式时

生产时不检测

交流特性

符号	参数	条件	最小值	最大值	单位
fOSC	振荡器频率		-	24	MHz
tSU(A-AL)	对 ALE/AS 低电平的地址建立时间		8	-	ns
tH(AL-A)	ALE 为低的保持时间		2	-	ns
tW(AL)	ALE/AS 的脉冲宽度		8	-	ns
tRLQV	/RD 为低 输出有效数据	Intel 模式	-	50	ns
tEHQV	E 为高 输出有效数据	Motorola 模式	-	50	ns
tRHDZ	/RD 为高 数据悬空	Intel 模式	-	30	ns
tELDZ	E 为低 数据悬空	Motorola 模式	-	30	ns
tDVWH	/WR 为高 输入数据有效	Intel 模式	8	-	ns
tWHDX	/WR 为高后的数据保持时间	Intel 模式	8	-	ns
tWHLH	/WR 为高到下一个 ALE 高		15	-	ns
tELAH	E 为低到下一个 AS 高	Motorola 模式	15	-	ns
tSU(I)(D-EL)	E 为低的输入数据建立时间	Motorola 模式	8	-	ns
tH(I)(EL-D)	E 为低的输入数据保持时间	Motorola 模式	8	-	ns
tLLWL	ALE 低到 /WR 低	Intel 模式	10	-	ns
tLLRL	ALE 低到 /RD 低	Intel 模式	10	-	ns
tLLEH	AS 低到 E 高	Motorola 模式	10	-	ns
tSU(R-EH)	RD/ (WR) 到 E 高的建立时间	Motorola 模式	5	-	ns
tW(W)	/WR 脉冲宽度	Intel 模式	20	-	ns
tW(R)	/RD 脉冲宽度	Intel 模式	40	-	ns
tW(E)	E 脉冲宽度	Motorola 模式	40	-	ns
tCLWL	/CS 低到 /WR 低	Intel 模式	0	-	ns
tCLRL	/CS 低到 /RD 低	Intel 模式	0	-	ns
tCLEH	/CS 低到 E 高	Motorola 模式	0	-	ns
tWHCH	/WR 高到 /CS 高	Intel 模式	0	-	ns
tRHCH	/RD 高到 /CS 高	Intel 模式	0	-	ns
tELCH	E 低到 /CS 高	Motorola 模式	0	-	ns
tW(RST)	/RST 脉冲宽度		100	-	ns
输入比较器/输出驱动器					
tSD	输入和输出延迟之和	VDD=5±10% VDIF=±32mV 1.4V<VI(RX)<VDD -1.4V;注 2	-	40	ns

VDD=5V±10%;VSS=0V;CL=50pF(输出引脚);Tamb=-40~+125; 除非另有说明; 注 1

注:

1. 生产过程中是不检测交流特性的。
2. 如果使用了外部发送接收电路 模拟输入比较器可以通过时钟分频寄存器的 CBP 位的设置来内部 忽略掉 这样会减少延时 (<26ns) VI (RX) =RX0 和 RX1 引脚上的输入电压。

Table 1 BasicCAN address allocation; note 1

CAN ADDRESS	SEGMENT	OPERATING MODE		RESET MODE	
		READ	WRITE	READ	WRITE
0	control	control	control	control	control
1		(FFH)	command	(FFH)	command
2		status	-	status	-
3		interrupt	-	interrupt	-
4		(FFH)	-	acceptance code	acceptance code
5		(FFH)	-	acceptance mask	acceptance mask
6		(FFH)	-	bus timing 0	bus timing 0
7		(FFH)	-	bus timing 1	bus timing 1
8		(FFH)	-	output control	output control
9		test	test; note 2	test	test; note 2
10	transmit buffer	identifier (10 to 3)	identifier (10 to 3)	(FFH)	-
11		identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC	(FFH)	-
12		data byte 1	data byte 1	(FFH)	-
13		data byte 2	data byte 2	(FFH)	-
14		data byte 3	data byte 3	(FFH)	-
15		data byte 4	data byte 4	(FFH)	-
16		data byte 5	data byte 5	(FFH)	-
17		data byte 6	data byte 6	(FFH)	-
18		data byte 7	data byte 7	(FFH)	-
19		data byte 8	data byte 8	(FFH)	-
20	receive buffer	identifier (10 to 3)	identifier (10 to 3)	identifier (10 to 3)	identifier (10 to 3)
21		identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC
22		data byte 1	data byte 1	data byte 1	data byte 1
23		data byte 2	data byte 2	data byte 2	data byte 2
24		data byte 3	data byte 3	data byte 3	data byte 3
25		data byte 4	data byte 4	data byte 4	data byte 4
26		data byte 5	data byte 5	data byte 5	data byte 5
27		data byte 6	data byte 6	data byte 6	data byte 6
28		data byte 7	data byte 7	data byte 7	data byte 7
29		data byte 8	data byte 8	data byte 8	data byte 8
30		(FFH)		(FFH)	
31		clock divider	clock divider; note 3	clock divider	clock divider

Notes

1. It should be noted that the registers are repeated within higher CAN address areas (the most significant bits of the 8-bit CPU address are not decoded: CAN address 32 continues with CAN address 0 and so on).
2. Test register is used for production testing only. Using this register during normal operation may result in undesired behaviour of the device.
3. Some bits are writeable in reset mode only (CAN mode and CBP).

RESET VALUES

Detection of a 'reset request' results in aborting the current transmission/reception of a message and entering the reset mode. On the '1-to-0' transition of the reset request bit, the CAN controller returns to the operating mode.

Table 2 Reset mode configuration; notes 1 and 2

REGISTER	BIT	SYMBOL	NAME	VALUE	
				RESET BY HARDWARE	SETTING BIT CR.0 BY SOFTWARE OR DUE TO BUS-OFF
Control	CR.7	-	reserved	0	0
	CR.6	-	reserved	X	X
	CR.5	-	reserved	1	1
	CR.4	OIE	Overrun Interrupt Enable	X	X
	CR.3	EIE	Error Interrupt Enable	X	X
	CR.2	TIE	Transmit Interrupt Enable	X	X
	CR.1	RIE	Receive Interrupt Enable	X	X
	CR.0	RR	Reset Request	1 (reset mode)	1 (reset mode)
Command	CMR.7	-	reserved	note 3	note 3
	CMR.6	-	reserved		
	CMR.5	-	reserved		
	CMR.4	GTS	Go To Sleep		
	CMR.3	CDO	Clear Data Overrun		
	CMR.2	RRB	Release Receive Buffer		
	CMR.1	AT	Abort Transmission		
	CMR.0	TR	Transmission Request		
Status	SR.7	BS	Bus Status	0 (bus-on)	X
	SR.6	ES	Error Status	0 (ok)	X
	SR.5	TS	Transmit Status	0 (idle)	0 (idle)
	SR.4	RS	Receive Status	0 (idle)	0 (idle)
	SR.3	TCS	Transmission Complete Status	1 (complete)	X
	SR.2	TBS	Transmit Buffer Status	1 (released)	1 (released)
	SR.1	DOS	Data Overrun Status	0 (absent)	0 (absent)
	SR.0	RBS	Receive Buffer Status	0 (empty)	0 (empty)
Interrupt	IR.7	-	reserved	1	1
	IR.6	-	reserved	1	1
	IR.5	-	reserved	1	1
	IR.4	WUI	Wake-Up Interrupt	0 (reset)	0 (reset)
	IR.3	DOI	Data Overrun Interrupt	0 (reset)	0 (reset)
	IR.2	EI	Error Interrupt	0 (reset)	X; note 4
	IR.1	TI	Transmit Interrupt	0 (reset)	0 (reset)
	IR.0	RI	Receive Interrupt	0 (reset)	0 (reset)

Acceptance code	AC.7 to 0	AC	Acceptance Code	X	X
Acceptance mask	AM.7 to 0	AM	Acceptance Mask	X	X
Bus timing 0	BTR0.7	SJW.1	Synchronization Jump Width 1	X	X
	BTR0.6	SJW.0	Synchronization Jump Width 0	X	X
	BTR0.5	BRP.5	Baud Rate Prescaler 5	X	X
	BTR0.4	BRP.4	Baud Rate Prescaler 4	X	X
	BTR0.3	BRP.3	Baud Rate Prescaler 3	X	X
	BTR0.2	BRP.2	Baud Rate Prescaler 2	X	X
	BTR0.1	BRP.1	Baud Rate Prescaler 1	X	X
	BTR0.0	BRP.0	Baud Rate Prescaler 0	X	X
Bus timing 1	BTR1.7	SAM	Sampling	X	X
	BTR1.6	TSEG2.2	Time Segment 2.2	X	X
	BTR1.5	TSEG2.1	Time Segment 2.1	X	X
	BTR1.4	TSEG2.0	Time Segment 2.0	X	X
	BTR1.3	TSEG1.3	Time Segment 1.3	X	X
	BTR1.2	TSEG1.2	Time Segment 1.2	X	X
	BTR1.1	TSEG1.1	Time Segment 1.1	X	X
	BTR1.0	TSEG1.0	Time Segment 1.0	X	X
Output control	OC.7	OCTP1	Output Control Transistor P1	X	X
	OC.6	OCTN1	Output Control Transistor N1	X	X
	OC.5	OCPOL1	Output Control Polarity 1	X	X
	OC.4	OCTP0	Output Control Transistor P0	X	X
	OC.3	OCTN0	Output Control Transistor N0	X	X
	OC.2	OCPOL0	Output Control Polarity 0	X	X
	OC.1	OCMODE1	Output Control Mode 1	X	X
	OC.0	OCMODE0	Output Control Mode 0	X	X
Transmit buffer	-	TXB	Transmit Buffer	X	X
Receive buffer	-	RXB	Receive Buffer	X; note 5	X; note 5
Clock divider	-	CDR	Clock Divider Register	00000000 (Intel); 00000101 (Motorola)	X

Notes

1. X means that the value of these registers or bits is not influenced.
2. Remarks in brackets explain functional meaning.
3. Reading the command register will always reflect a binary '11111111'.
4. On bus-off the error interrupt is set, if enabled.
5. Internal read/write pointers of the RXFIFO are reset to their initial values. A subsequent read access to the RXB would show undefined data values (parts of old messages). If a message is transmitted, this message is written in parallel to the receive buffer but no receive interrupt is generated and the receive buffer area is not locked. So, even if the receive buffer is empty, the last transmitted message may be read from the receive buffer until it is overridden by the next received or transmitted message. Upon a hardware reset, the RXFIFO pointers are reset to the physical RAM address '0'. Setting CR.0 by software or due to the bus-off event will reset the RXFIFO pointers to the currently valid FIFO start address which is different from the RAM address '0' after the first release receive buffer command.

CONTROL REGISTER (CR)

The contents of the control register are used to change the behaviour of the CAN controller. Bits may be set or reset by the attached microcontroller which uses the control register as a read/write memory.

Table 3 Bit interpretation of the control register (CR); CAN address 0

BIT	SYMBOL	NAME	VALUE	FUNCTION
CR.7	-	-	-	reserved; note 1
CR.6	-	-	-	reserved; note 2
CR.5	-	-	-	reserved; note 3
CR.4	OIE	Overrun Interrupt Enable	1	enabled; if the data overrun bit is set, the microcontroller receives an overrun interrupt signal (see also status register; Table 5)
			0	disabled; the microcontroller receives no overrun interrupt signal from the SJA1000
CR.3	EIE	Error Interrupt Enable	1	enabled; if the error or bus status change, the microcontroller receives an error interrupt signal (see also status register; Table 5)
			0	disabled; the microcontroller receives no error interrupt signal from the SJA1000
CR.2	TIE	Transmit Interrupt Enable	1	enabled; when a message has been successfully transmitted or the transmit buffer is accessible again, (e.g. after an abort transmission command) the SJA1000 transmits a transmit interrupt signal to the microcontroller
			0	disabled; the microcontroller receives no transmit interrupt signal from the SJA1000
CR.1	RIE	Receive Interrupt Enable	1	enabled; when a message has been received without errors, the SJA1000 transmits a receive interrupt signal to the microcontroller
			0	disabled; the microcontroller receives no transmit interrupt signal from the SJA1000
CR.0	RR	Reset Request; note 4	1	present; detection of a reset request results in aborting the current transmission/reception of a message and entering the reset mode
			0	absent; on the '1-to-0' transition of the reset request bit, the SJA1000 returns to the operating mode

Notes

- Any write access to the control register has to set this bit to logic 0 (reset value is logic 0).
- In the PCA82C200 this bit was used to select the synchronization mode. Because this mode is not longer implemented, setting this bit has no influence on the microcontroller. Due to software compatibility setting this bit is allowed. This bit will not change after hardware or software reset. In addition the value written by users software is reflected.
- Reading this bit will always reflect a logic 1.
- During a hardware reset or when the bus status bit is set to logic 1 (bus-off), the reset request bit is set to logic 1 (present). If this bit is accessed by software, a value change will become visible and takes effect first with the next positive edge of the internal clock which operates with 1/2 of the external oscillator frequency. During an external reset the microcontroller cannot set the reset request bit to logic 0 (absent). Therefore, after having set the reset request bit to logic 0, the microcontroller must check this bit to ensure that the external reset pin is not being held LOW. Changes of the reset request bit are synchronized with the internal divided clock. Reading the reset request bit reflects the synchronized status. After the reset request bit is set to logic 0 the SJA1000 will wait for: a) One occurrence of bus-free signal (11 recessive bits), if the preceding reset request has been caused by a hardware reset or a CPU-initiated reset b) 128 occurrences of bus-free, if the preceding reset request has been caused by a CAN controller initiated bus-off, before re-entering the bus-on mode; it should be noted that several registers are modified if the reset request bit was set (see also Table 2).

COMMAND REGISTER (CMR)

A command bit initiates an action within the transfer layer of the SJA1000. The command register appears to the microcontroller as a write only memory. If a read access is performed to this address the byte '11111111' is returned. Between two commands at least one internal clock cycle is needed to process. The internal clock is divided by two from the external oscillator frequency.

Table 4 Bit interpretation of the command register (CMR); CAN address 1

BIT	SYMBOL	NAME	VALUE	FUNCTION
CMR.7	-	-	-	reserved
CMR.6	-	-	-	reserved
CMR.5	-	-	-	reserved
CMR.4	GTS	Go To Sleep; note 1	1	sleep; the SJA1000 enters sleep mode if no CAN interrupt is pending and there is no bus activity
			0	wake up; SJA1000 operates normal
CMR.3	CDO	Clear Data Overrun; note 2	1	clear; data overrun status bit is cleared
			0	no action
CMR.2	RRB	Release Receive Buffer; note 3	1	released; the receive buffer, representing the message memory space in the RXFIFO is released
			0	no action
CMR.1	AT	Abort Transmission; note 4	1	present; if not already in progress, a pending transmission request is cancelled
			0	absent; no action
CMR.0	TR	Transmission Request; note 5	1	present; a message will be transmitted
			0	absent; no action

Notes

1. The SJA1000 will enter sleep mode if the sleep bit is set to logic 1 (sleep); there is no bus activity and no interrupt is pending. Setting of GTS with at least one of the previously mentioned exceptions valid will result in a wake-up interrupt. After sleep mode is set, the CLKOUT signal continues until at least 15 bit times have passed, to allow a host microcontroller clocked via this signal to enter its own standby mode before the CLKOUT goes LOW. The SJA1000 will wake up when one of the three previously mentioned conditions is negated: after 'Go To Sleep' is set LOW (wake-up), there is bus activity or **INT** is driven LOW (active). On wake-up, the oscillator is started and a wake-up interrupt is generated. A sleeping SJA1000 which wakes up due to bus activity will not be able to receive this message until it detects 11 consecutive recessive bits (bus-free sequence). It should be noted that setting of GTS is not possible in reset mode. After clearing of reset request, setting of GTS is possible first, when bus-free is detected again.
2. This command bit is used to clear the data overrun condition indicated by the data overrun status bit. As long as the data overrun status bit is set no further data overrun interrupt is generated. It is allowed to give the clear data overrun command at the same time as a release receive buffer command.
3. After reading the contents of the receive buffer, the microcontroller can release this memory space of the RXFIFO by setting the release receive buffer bit to logic 1. This may result in another message becoming immediately available within the receive buffer. This event will force another receive interrupt, if enabled. If there is no other message available no further receive interrupt is generated and the receive buffer status bit is cleared.
4. The abort transmission bit is used when the CPU requires the suspension of the previously requested transmission, e.g. to transmit a more urgent message before. A transmission already in progress is not stopped. In order to see if the original message had been either transmitted successfully or aborted, the transmission complete status bit should be checked. This should be done after the transmit buffer status bit has been set to logic 1 (released) or a transmit interrupt has been generated.
5. If the transmission request was set to logic 1 in a previous command, it cannot be cancelled by setting the transmission request bit to logic 0. The requested transmission may be cancelled by setting the abort transmission bit to logic 1

STATUS REGISTER (SR)

The content of the status register reflects the status of the SJA1000. The status register appears to the microcontroller as a read only memory.

Table 5 Bit interpretation of the status register (SR); CAN address 2

BIT	SYMBOL	NAME	VALUE	FUNCTION
SR.7	BS	Bus Status; note 1	1	bus-off; the SJA1000 is not involved in bus activities
			0	bus-on; the SJA1000 is involved in bus activities
SR.6	ES	Error Status; note 2	1	error; at least one of the error counters has reached or exceeded the CPU warning limit
			0	ok; both error counters are below the warning limit
SR.5	TS	Transmit Status; note 3	1	transmit; the SJA1000 is transmitting a message
			0	idle; no transmit message is in progress
SR.4	RS	Receive Status; note 3	1	receive; the SJA1000 is receiving a message
			0	idle; no receive message is in progress
SR.3	TCS	Transmission Complete Status; note 4	1	complete; the last requested transmission has been successfully completed
			0	incomplete; the previously requested transmission is not yet completed
SR.2	TBS	Transmit Buffer Status; note 5	1	released; the CPU may write a message into the transmit buffer
			0	locked; the CPU cannot access the transmit buffer; a message is waiting for transmission or is already in process
SR.1	DOS	Data Overrun Status; note 6	1	overrun; a message was lost because there was not enough space for that message in the RXFIFO
			0	absent; no data overrun has occurred since the last clear data overrun command was given
SR.0	RBS	Receive Buffer Status; note 7	1	full; one or more messages are available in the RXFIFO
			0	empty; no message is available

Notes

1. When the transmit error counter exceeds the limit of 255 [the bus status bit is set to logic 1 (bus-off)] the CAN controller will set the reset request bit to logic 1 (present) and an error interrupt is generated, if enabled. It will stay in this mode until the CPU clears the reset request bit. Once this is completed the CAN controller will wait the minimum protocol-defined time (128 occurrences of the bus-free signal). After that the bus status bit is cleared (bus-on), the error status bit is set to logic 0 (ok), the error counters are reset and an error interrupt is generated, if enabled.
2. Errors detected during reception or transmission will affect the error counters according to the CAN 2.0B protocol specification. The error status bit is set when at least one of the error counters has reached or exceeded the CPU warning limit of 96. An error interrupt is generated, if enabled.
3. If both the receive status and the transmit status bits are logic 0 (idle) the CAN-bus is idle.
4. The transmission complete status bit is set to logic 0 (incomplete) whenever the transmission request bit is set to logic 1. The transmission complete status bit will remain at logic 0 (incomplete) until a message is transmitted successfully.
5. If the CPU tries to write to the transmit buffer when the transmit buffer status bit is at logic 0 (locked), the written byte will not be accepted and will be lost without being indicated.
6. When a message that shall be received has passed the acceptance filter successfully (i.e. earliest after arbitration field), the CAN controller needs space in the RXFIFO to store the message descriptor. Accordingly there must be enough space for each data byte which has been received. If there is not enough space to store the message, that message will be dropped and the data overrun condition will be indicated to the CPU only, if this received message has no errors until the last but one bit of end of frame (message becomes valid).
7. After reading a message stored in the RXFIFO and releasing this memory space with the command release receive buffer, this bit is cleared. If there is another message available within the FIFO this bit is set again with the next bit quantum (t_{sc1}).

INTERRUPT REGISTER (IR)

The interrupt register allows the identification of an interrupt source. When one or more bits of this register are set, the $\overline{\text{INT}}$ pin is activated (LOW). After this register is read by the microcontroller, all bits are reset what results in a floating level at $\overline{\text{INT}}$. The interrupt register appears to the microcontroller as a read only memory.

Table 6 Bit interpretation of the interrupt register (IR); CAN address 3

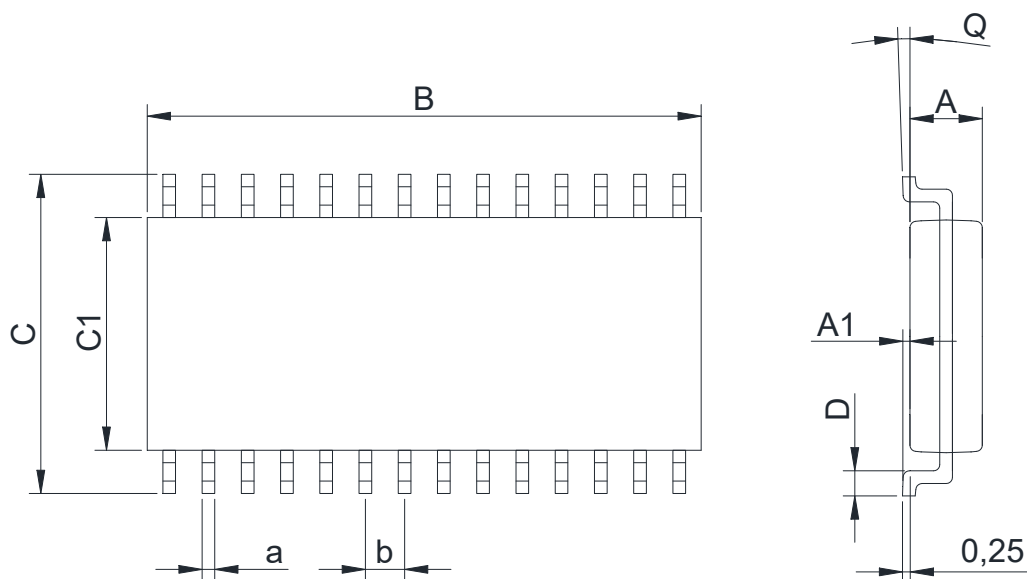
BIT	SYMBOL	NAME	VALUE	FUNCTION
IR.7	-	-	-	reserved; note 1
IR.6	-	-	-	reserved; note 1
IR.5	-	-	-	reserved; note 1
IR.4	WUI	Wake-Up Interrupt; note 2	1	set; this bit is set when the sleep mode is left
			0	reset; this bit is cleared by any read access of the microcontroller
IR.3	DOI	Data Overrun Interrupt; note 3	1	set; this bit is set on a '0-to-1' transition of the data overrun status bit, when the data overrun interrupt enable is set to logic 1 (enabled)
			0	reset; this bit is cleared by any read access of the microcontroller
IR.2	EI	Error Interrupt	1	set; this bit is set on a change of either the error status or bus status bits if the error interrupt enable is set to logic 1 (enabled)
			0	reset; this bit is cleared by any read access of the microcontroller
IR.1	TI	Transmit Interrupt	1	set; this bit is set whenever the transmit buffer status changes from logic 0 to logic 1 (released) and transmit interrupt enable is set to logic 1 (enabled)
			0	reset; this bit is cleared by any read access of the microcontroller
IR.0	RI	Receive Interrupt; note 4	1	set; this bit is set while the receive FIFO is not empty and the receive interrupt enable bit is set to logic 1 (enabled)
			0	reset; this bit is cleared by any read access of the microcontroller

Notes

1. Reading this bit will always reflect a logic 1.
2. A wake-up interrupt is also generated if the CPU tries to set go to sleep while the CAN controller is involved in bus activities or a CAN interrupt is pending.
3. The overrun interrupt bit (if enabled) and the data overrun status bit are set at the same time.
4. The receive interrupt bit (if enabled) and the receive buffer status bit are set at the same time. It should be noted that the receive interrupt bit is cleared upon a read access, even if there is another message available within the FIFO. The moment the release receive buffer command is given and there is another message valid within the receive buffer, the receive interrupt is set again (if enabled) with the next t_{scf}

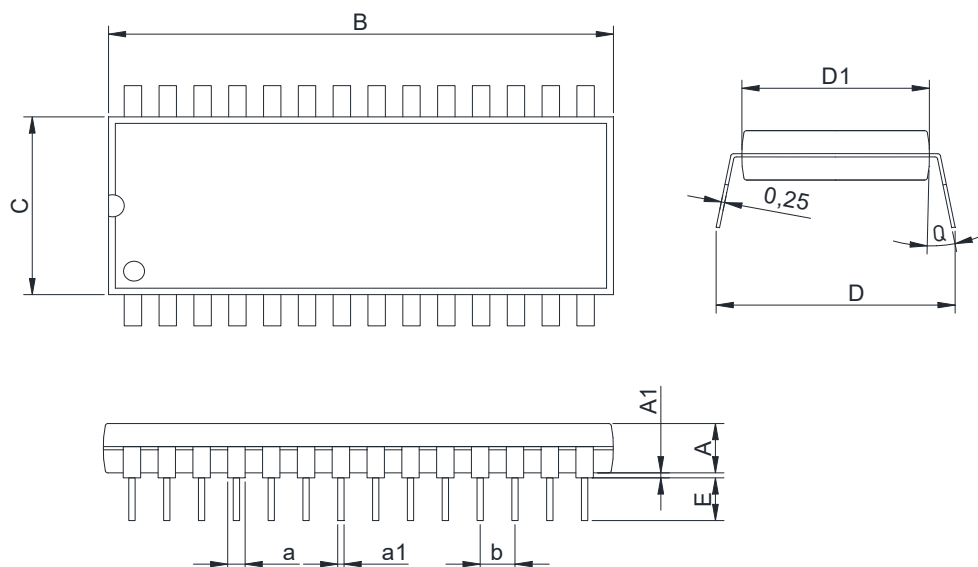
封装外型尺寸

SOP-28W



Dimensions In Millimeters(SOP-28W)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.25	0.1	17.8	10.1	7.42	0.60	0°	0.35	1.27BSC
Max:	2.35	0.3	18.0	10.4	7.59	1.0	8°	0.48	

DIP-28



Dimensions In Millimeters(DIP-28)											
Symbol:	A	B	C	D	D1	E	Q	a	a1	A1	b
Min:	3.56	36.7	13.4	15.7	13.4	3.20	0°	1.4	0.46	0.38	2.54BSC
Max:	4.0	36.9	14.2	17.2	13.9	3.40	15°	1.6	0.56	0.70	

修订历史

版本编号	日期	修改内容	页码
V1.0	2014-6	新修订	1-9
V1.1	2021-9	更新封装、增加极限参数注释	1、4
V1.2	2024-10	添加表寄存器地址、更新引脚焊接温度	4、7-13
V1.3	2025-12	更新重要声明	16

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