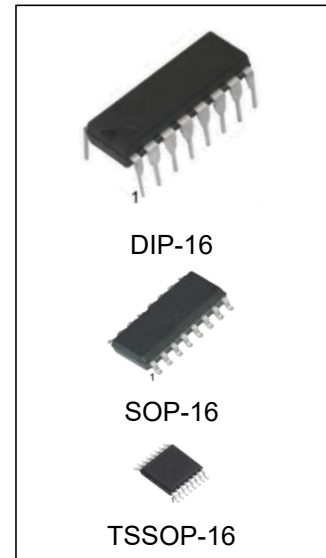


Presetable Synchronous BCD Decade up/down Counter; Asynchronous Reset

Features:

- Input levels: CMOS level
- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Specified from -40°C to +125°C
- Packaging information: DIP-16/SOP-16/TSSOP-16



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC192N	DIP-16	74HC192	TUBE	1000pcs/box
74HC192M/TR	SOP-16	74HC192	REEL	2500pcs/reel
74HC192MT/TR	TSSOP-16	74HC192	REEL	2500pcs/reel

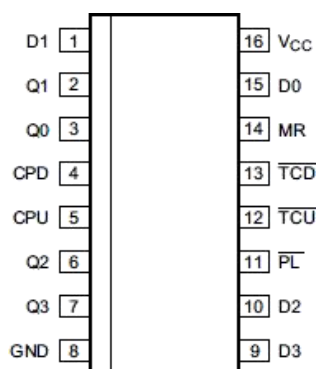
General Description

The 74HC192 is a synchronous BCD up/down counter. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time to guarantee predictable behavior. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The terminal count up ($\overline{TCU}$) and terminal count down ($\overline{TCD}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause $\overline{TCU}$ to go LOW. $\overline{TCU}$ will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the $\overline{TCD}$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Pin Configurations



DIP-16/SOP-16/TSSOP-16

Pin Description

Pin No.	Pin Name	Description
1	D1	data input 1
2	Q1	flip-flop output 1
3	Q0	flip-flop output 0
4	CPD	count down clock input
5	CPU	count up clock input
6	Q2	flip-flop output 2
7	Q3	flip-flop output 3
8	GND	ground (0V)
9	D3	data input 3
10	D2	data input 2
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TCU}$	terminal count up (carry) output (active LOW)
13	$\overline{TCD}$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15	D0	data input 0
16	VCC	supply voltage

Note: CPD, CPU is LOW-to-HIGH, edge triggered

Block Diagram

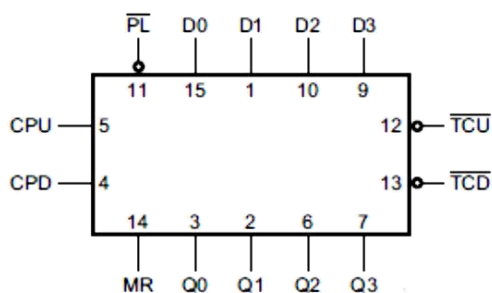


Figure 1. Logic symbol

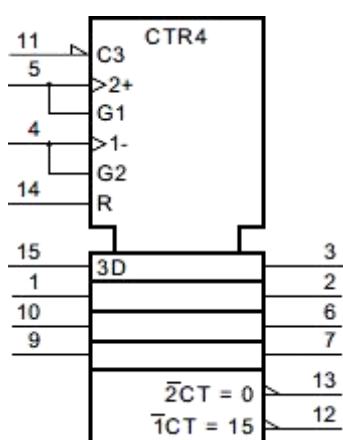


Figure 2. IEC logic symbol

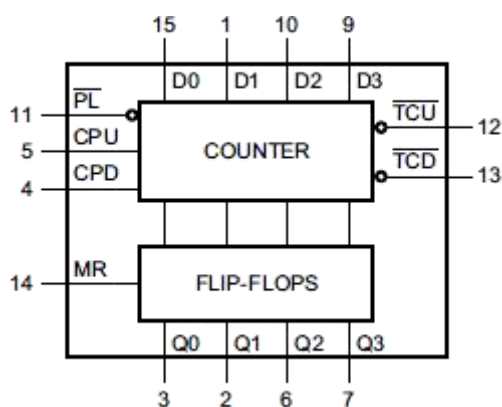


Figure 3. Functional diagram

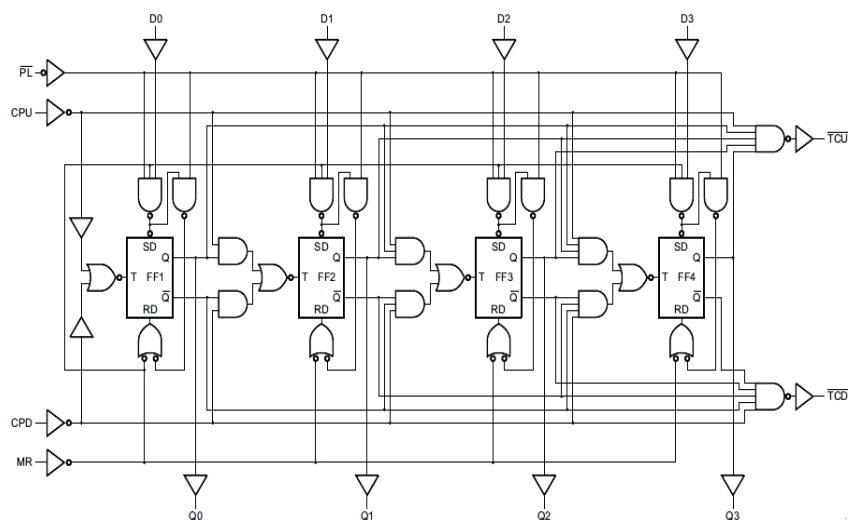


Figure 4. Logic diagram

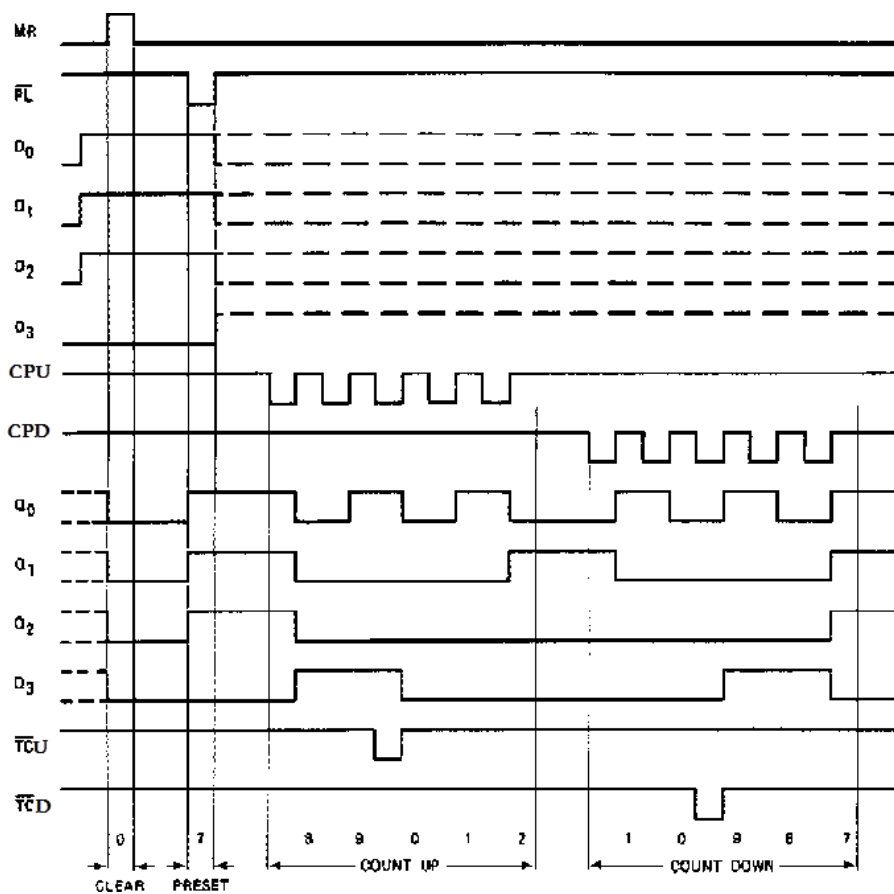


Figure 5. Typical clear, load and count sequence

Function Table

Operating mode	Input								Output					
	MR	PL	CPU	CPD	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{\text{TCU}}$	$\overline{\text{TCD}}$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	Qn=Dn				L	H
	L	L	H	X	H	X	X	H	Qn=Dn				H	H
count up	L	H	↑	H	X	X	X	X	count up				H	H
count down	L	H	H	↑	X	X	X	X	count down				H	H

Note:

- 1) H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH transition.
- 2) $\overline{\text{TCU}}$ =CPU at terminal count up (HLLH).
- 3) $\overline{\text{TCD}}$ =CPD at terminal count down (LLLL).

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	±20	mA
output current	I_O	$V_O = -0.5V$ to $(V_{CC}+0.5V)$	-	±25	mA
supply current	I_{CC}	-	-	50	mA
ground current	I_{GND}	-	-	-50	mA
Storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		°C

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	-	$V_{CC}=2.0V$	-	-	625 ns/V
			$V_{CC}=4.5V$	-	1.67	139 ns/V
			$V_{CC}=6.0V$	-	-	83 ns/V
Ambient temperature	T_{amb}	-	-40	-	+85	°C

Electrical Characteristics

DC Characteristics 1

($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	1.2	-	V
		V _{CC} =4.5V		3.15	2.4	-	V
		V _{CC} =6.0V		4.2	3.2	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	0.8	0.5	V
		V _{CC} =4.5V		-	2.1	1.35	V
		V _{CC} =6.0V		-	2.8	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-4mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.48	5.81	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =4mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =5.2mA; V _{CC} =6.0V	-	0.16	0.26	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8.0	uA
Input capacitance	C _I	-		-	3.5	-	pF

DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-4mA; V _{CC} =4.5V	3.84	-	-	V
			I _O =-5.2mA; V _{CC} =6.0V	5.34	-	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =4mA; V _{CC} =4.5V	-	-	0.33	V
			I _O =5.2mA; V _{CC} =6.0V	-	-	0.33	V
input leakage current	I _I	V _I =V _{CC} or GND;V _{CC} =6.0V		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA

AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, $GND=0V$, $t_r=t_f=6\text{ns}$, $C_L=50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit		
propagation delay	t _{pd}	CPU, CPD to Qn; see Figure 7	V _{CC} =2.0V	-	66	215	ns		
			V _{CC} =4.5V	-	23	43	ns		
			V _{CC} =5.0V; C _L =15pF	-	24	-	ns		
			V _{CC} =6.0V	-	19	37	ns		
		CPU to $\overline{\text{TCU}}$; see Figure 8	V _{CC} =2.0V	-	33	125	ns		
			V _{CC} =4.5V	-	12	25	ns		
			V _{CC} =6.0V	-	10	21	ns		
		CPD to $\overline{\text{TCD}}$; see Figure 8	V _{CC} =2.0V	-	39	125	ns		
			V _{CC} =4.5V	-	14	25	ns		
			V _{CC} =6.0V	-	11	21	ns		
		$\overline{\text{PL}}$ to Qn; see Figure 9	V _{CC} =2.0V	-	69	215	ns		
			V _{CC} =4.5V	-	25	43	ns		
			V _{CC} =6.0V	-	20	37	ns		
		MR to Qn; see Figure 10	V _{CC} =2.0V	-	63	200	ns		
			V _{CC} =4.5V	-	23	40	ns		
			V _{CC} =6.0V	-	18	34	ns		
		Dn to Qn; see Figure 9	V _{CC} =2.0V	-	91	275	ns		
			V _{CC} =4.5V	-	33	55	ns		
			V _{CC} =6.0V	-	26	47	ns		
		$\overline{\text{PL}}$ to $\overline{\text{TCU}}$, $\overline{\text{PL}}$ to $\overline{\text{TCD}}$; see Figure 12	V _{CC} =2.0V	-	102	315	ns		
			V _{CC} =4.5V	-	37	63	ns		
			V _{CC} =6.0V	-	30	54	ns		
		MR to $\overline{\text{TCU}}$, MR to $\overline{\text{TCD}}$; see Figure 12	V _{CC} =2.0V	-	96	285	ns		
			V _{CC} =4.5V	-	35	57	ns		
			V _{CC} =6.0V	-	28	48	ns		
		Dn to $\overline{\text{TCU}}$, Dn to $\overline{\text{TCD}}$; see Figure 12	V _{CC} =2.0V	-	83	290	ns		
			V _{CC} =4.5V	-	30	58	ns		
			V _{CC} =6.0V	-	24	49	ns		
		transition time	t _t	see Figure 10	V _{CC} =2.0V	-	19	75	ns
					V _{CC} =4.5V	-	7	15	ns
					V _{CC} =6.0V	-	6	13	ns
		pulse width	t _w	up clock pulse width HIGH or LOW; see Figure 7	V _{CC} =2.0V	120	39	-	ns
V _{CC} =4.5V	24				14	-	ns		
down clock pulse width HIGH or LOW; see Figure 7	V _{CC} =6.0V			20	11	-	ns		
	V _{CC} =2.0V			140	50	-	ns		
	V _{CC} =4.5V			28	18	-	ns		
master reset pulse width HIGH; see Figure 10	V _{CC} =6.0V			24	14	-	ns		
	V _{CC} =2.0V			80	22	-	ns		
	V _{CC} =4.5V			16	8	-	ns		
parallel load pulse width LOW; see Figure 9	V _{CC} =6.0V			14	6	-	ns		
	V _{CC} =2.0V			80	22	-	ns		
	V _{CC} =4.5V			16	8	-	ns		
V _{CC} =6.0V	14			6	-	ns			

recovery time	t_{rec}	$\overline{PL}$ to CPU, CPD; see Figure 9	$V_{CC}=2.0V$	50	3	-	ns
			$V_{CC}=4.5V$	10	1	-	ns
			$V_{CC}=6.0V$	9	1	-	ns
		MR to CPU, CPD; see Figure 10	$V_{CC}=2.0V$	50	0	-	ns
			$V_{CC}=4.5V$	10	0	-	ns
			$V_{CC}=6.0V$	9	0	-	ns
set-up time	t_{su}	Dn to $\overline{PL}$; see Figure 11; note: CPU=CPD=HIGH	$V_{CC}=2.0V$	80	22	-	ns
			$V_{CC}=4.5V$	16	8	-	ns
			$V_{CC}=6.0V$	14	6	-	ns
hold time	t_h	Dn to $\overline{PL}$; see Figure 11	$V_{CC}=2.0V$	0	-14	-	ns
			$V_{CC}=4.5V$	0	-5	-	ns
			$V_{CC}=6.0V$	0	-4	-	ns
		CPU to CPD, CPD to CPU; see Figure 13	$V_{CC}=2.0V$	80	19	-	ns
			$V_{CC}=4.5V$	16	7	-	ns
			$V_{CC}=6.0V$	14	6	-	ns
maximum frequency	f_{max}	CPU, CPD; see Figure 7	$V_{CC}=2.0V$	4.0	12	-	MHz
			$V_{CC}=4.5V$	20	36	-	MHz
			$V_{CC}=5.0V$; $C_L=15pF$	-	40	-	MHz
			$V_{CC}=6.0V$	24	43	-	MHz
Power dissipation capacitance	C_{PD}	$V_I=GND$ to V_{CC}		-	24	-	pF

Note:

- 1) t_{pd} is the same as t_{PLH} and t_{PHL} .
- 2) t_t is the same as t_{THL} and t_{TLH} .
- 3) C_{PD} is used to determine the dynamic power dissipation (PD in uW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i =input frequency in MHz;
 f_o =output frequency in MHz;
 C_L =output load capacitance in pF;
 V_{CC} =supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $GND = 0V$, $t_r = t_f = 6\text{ns}$, $C_L = 50\text{pF}$, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t _{pd}	CPU, CPD to Qn; see Figure 7	V _{CC} =2.0V	-	-	270	ns
			V _{CC} =4.5V	-	-	54	ns
			V _{CC} =6.0V	-	-	46	ns
		CPU to $\overline{TCU}$; see Figure 8	V _{CC} =2.0V	-	-	155	ns
			V _{CC} =4.5V	-	-	31	ns
			V _{CC} =6.0V	-	-	26	ns
		CPD to $\overline{TCD}$; see Figure 8	V _{CC} =2.0V	-	-	155	ns
			V _{CC} =4.5V	-	-	31	ns
			V _{CC} =6.0V	-	-	26	ns
		$\overline{PL}$ to Qn; see Figure 9	V _{CC} =2.0V	-	-	270	ns
			V _{CC} =4.5V	-	-	54	ns
			V _{CC} =6.0V	-	-	46	ns
		MR to Qn; see Figure 10	V _{CC} =2.0V	-	-	250	ns
			V _{CC} =4.5V	-	-	50	ns
			V _{CC} =6.0V	-	-	43	ns
		Dn to Qn; see Figure 9	V _{CC} =2.0V	-	-	345	ns
			V _{CC} =4.5V	-	-	69	ns
			V _{CC} =6.0V	-	-	59	ns
		$\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Figure 12	V _{CC} =2.0V	-	-	395	ns
			V _{CC} =4.5V	-	-	79	ns
			V _{CC} =6.0V	-	-	67	ns
		MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Figure 12	V _{CC} =2.0V	-	-	355	ns
			V _{CC} =4.5V	-	-	71	ns
			V _{CC} =6.0V	-	-	60	ns
		Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Figure 12	V _{CC} =2.0V	-	-	365	ns
			V _{CC} =4.5V	-	-	73	ns
			V _{CC} =6.0V	-	-	62	ns
transition time	t _t	see Figure 10	V _{CC} =2.0V	-	-	95	ns
			V _{CC} =4.5V	-	-	19	ns
			V _{CC} =6.0V	-	-	16	ns
pulse width	t _w	up clock pulse width HIGH or LOW; see Figure 7	V _{CC} =2.0V	150	-	-	ns
			V _{CC} =4.5V	30	-	-	ns
			V _{CC} =6.0V	26	-	-	ns
		down clock pulse width HIGH or LOW; see Figure 7	V _{CC} =2.0V	175	-	-	ns
			V _{CC} =4.5V	35	-	-	ns
			V _{CC} =6.0V	30	-	-	ns
		master reset pulse width HIGH; see Figure 10	V _{CC} =2.0V	100	-	-	ns
			V _{CC} =4.5V	20	-	-	ns
			V _{CC} =6.0V	17	-	-	ns
		parallel load pulse width LOW; see Figure 9	V _{CC} =2.0V	100	-	-	ns
			V _{CC} =4.5V	20	-	-	ns
			V _{CC} =6.0V	17	-	-	ns

recovery time	t_{rec}	$\overline{PL}$ to CPU, CPD; see Figure 9	$V_{CC}=2.0V$	65	-	-	ns
			$V_{CC}=4.5V$	13	-	-	ns
			$V_{CC}=6.0V$	11	-	-	ns
		MR to CPU, CPD; see Figure 10	$V_{CC}=2.0V$	65	-	-	ns
			$V_{CC}=4.5V$	13	-	-	ns
			$V_{CC}=6.0V$	11	-	-	ns
set-up time	t_{su}	Dn to $\overline{PL}$; see Figure 11; note: CPU=CPD=HIGH	$V_{CC}=2.0V$	100	-	-	ns
			$V_{CC}=4.5V$	20	-	-	ns
			$V_{CC}=6.0V$	17	-	-	ns
hold time	t_h	Dn to $\overline{PL}$; see Figure 11	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
		CPU to CPD, CPD to CPU; see Figure 13	$V_{CC}=2.0V$	100	-	-	ns
			$V_{CC}=4.5V$	20	-	-	ns
			$V_{CC}=6.0V$	17	-	-	ns
maximum frequency	f_{max}	CPU, CPD; see Figure 7	$V_{CC}=2.0V$	3.2	-	-	MHz
			$V_{CC}=4.5V$	16	-	-	MHz
			$V_{CC}=6.0V$	19	-	-	MHz

Note:

- 1) t_{pd} is the same as t_{PLH} and t_{PHL} .
- 2) t_t is the same as t_{THL} and t_{TLH} .

Testing Circuit

AC Testing Circuit

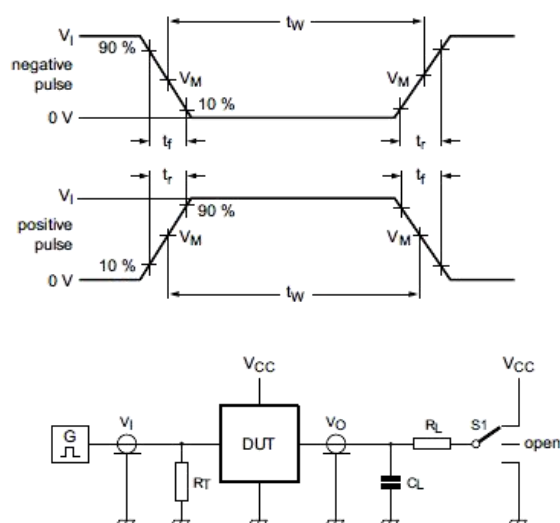


Figure 6. Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

AC Testing Waveforms

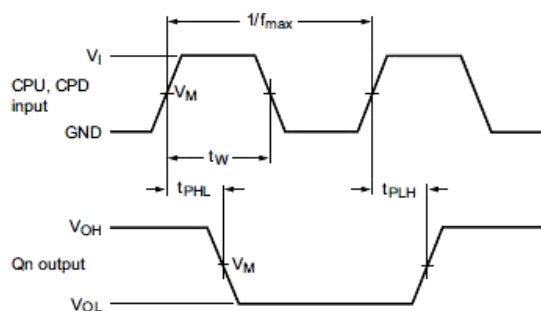


Figure 7. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency

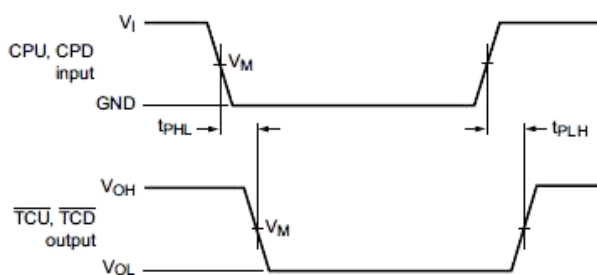


Figure 8. The clock (CPU, CPD) to terminal count output ($\overline{TCU}$, $\overline{TCD}$) propagation delays

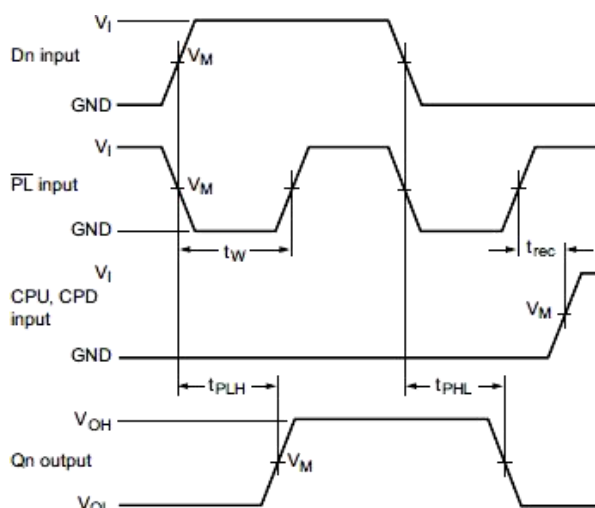


Figure 9. The parallel load input (PL) and data (Dn) to Qn output propagation delays and PL removal time to clock input (CPU, CPD)

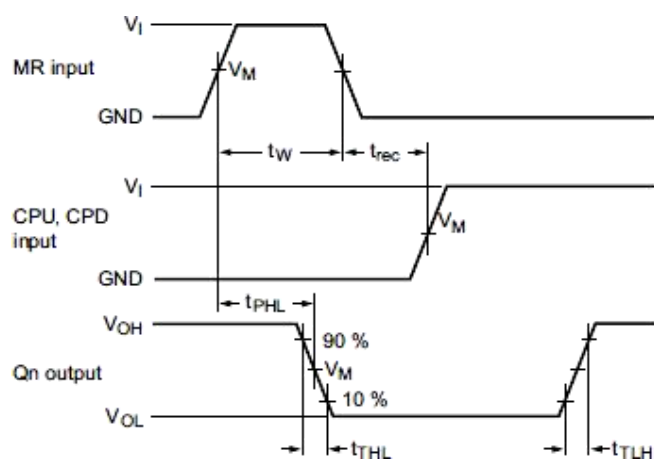


Figure 10. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times

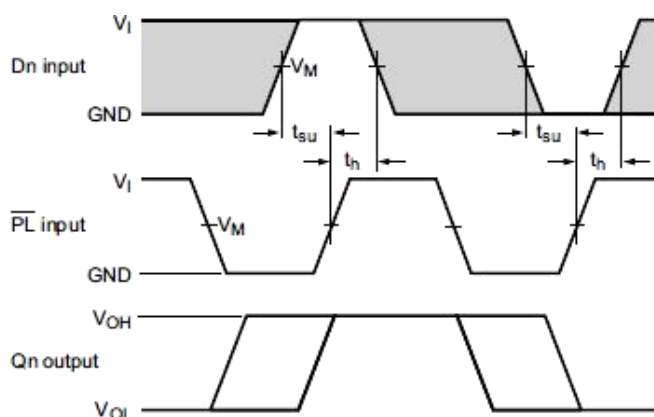


Figure 11. The data input (Dn) to parallel load input (PL) set-up and hold times

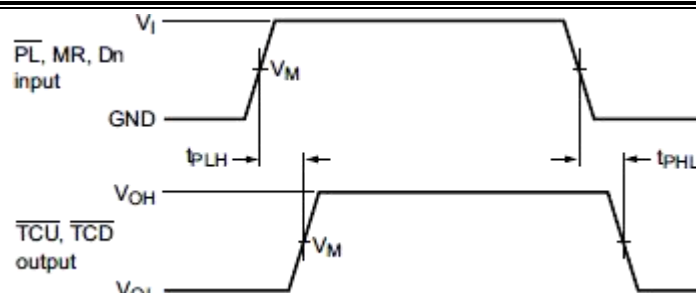


Figure 12. The data input (Dn), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TCU}$, $\overline{TCD}$) propagation delays

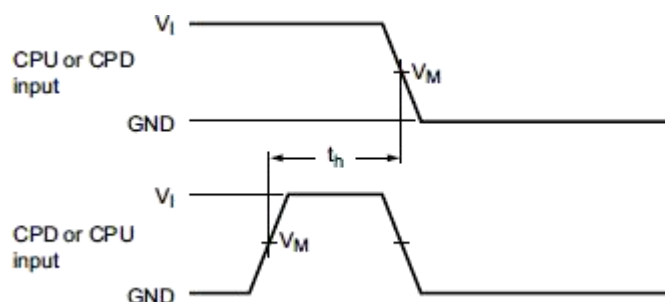


Figure 13. The CPU to CPD or CPD to CPU hold times

Measurement Points

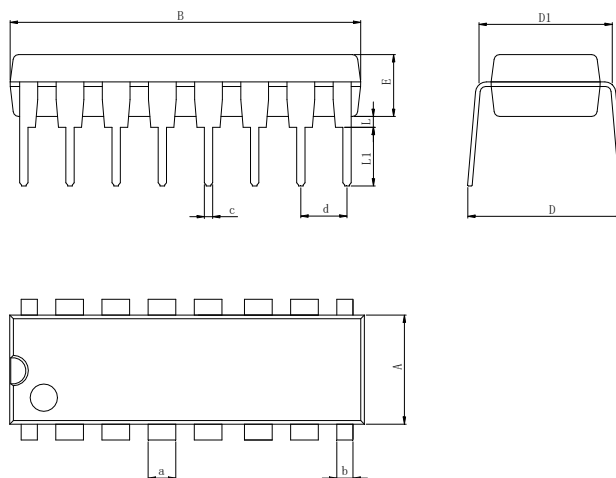
Type	Input		Output
	V_I	V_M	V_M
74HC192	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Test Data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC192	V_{CC}	6ns	15pF, 50pF	1k Ω	open

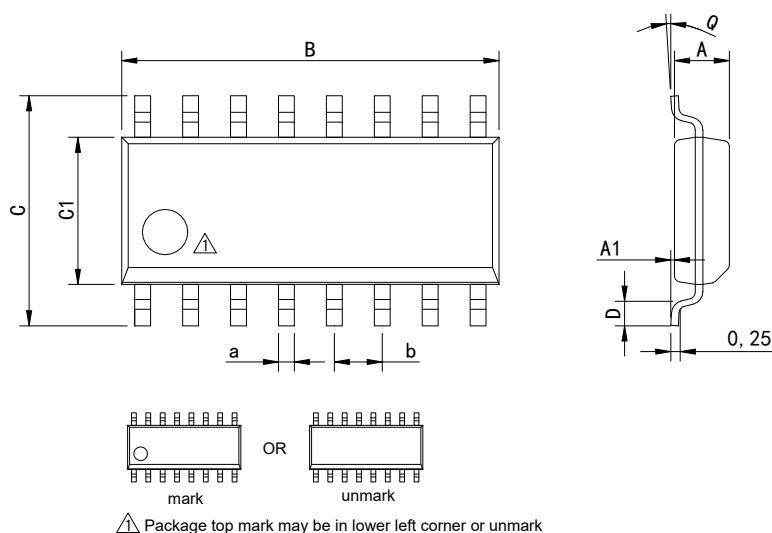
Physical Dimensions

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

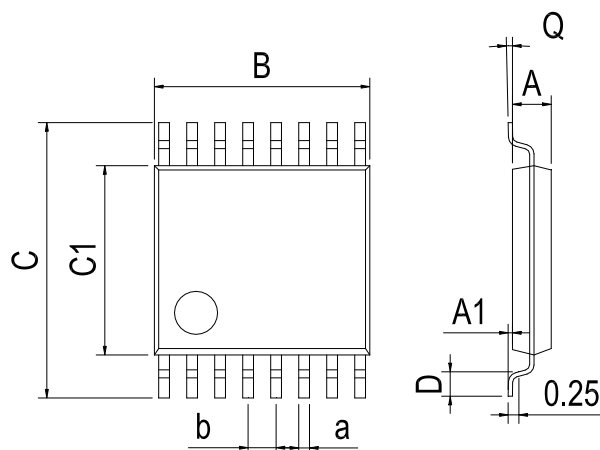
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2018-6	New	1-20
V1.1	2025-11	Document Reformatting	1-19

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