Octal D-type flip-flop; positive edge-trigger; 3-state

Features:

- Input levels: CMOS level
- Octal bus interface
- Non-inverting 3-state outputs
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Specified from -40℃ to +85℃
- Packaging information: DIP-20/SOP-20W/TSSOP-20

DIP-20

SOP-20W

TSSOP-20

Ordering information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC374N	DIP-20	74HC374	TUBE	720pcs/box
74HC374M/TR	SOP-20W	74HC374	REEL	2000pcs/reel
74HC374MT/TR	TSSOP-20	HC374	REEL	2500pcs/reel

General Description

The 74HC374 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. Thedevice features a clock (CP) and output enable ($\overline{OE}$) inputs. The flip-flops will store the state of theirindividual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP)transition. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Block Diagram

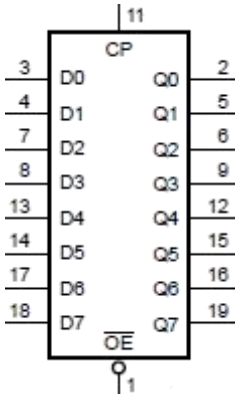


Figure 1. Logic symbol

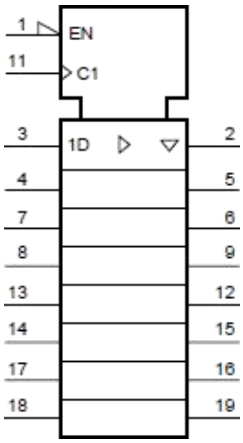


Figure 2. IEC logic symbol

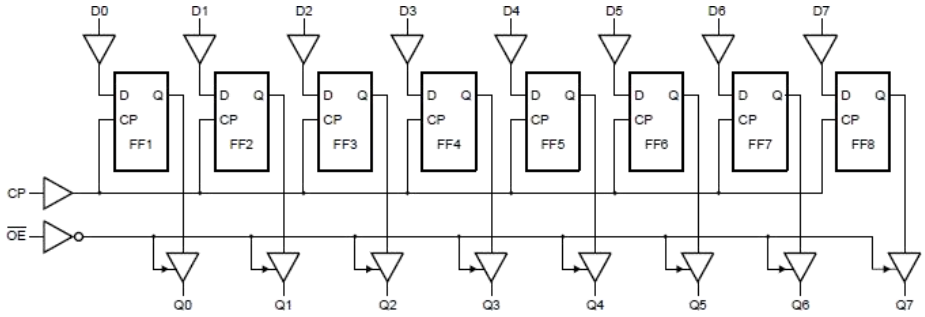


Figure 3. Logic diagram

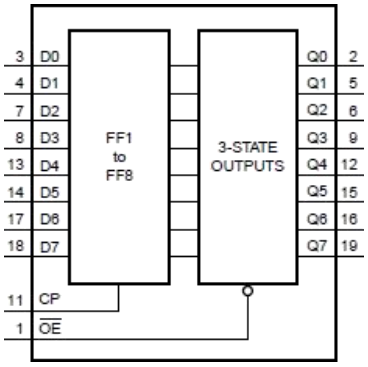
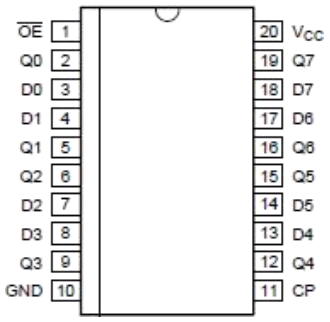


Figure 4. Functional diagram

Pin Configurations



DIP-20/SOP-20/TSSOP-20

Pin Description

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	$\overline{OE}$	output enable input (active LOW)	11	CP	clock input (LOW-to-HIGH, edge-triggered)
2	Q0	data output	12	Q4	data output
3	D0	data input	13	D4	data input
4	D1	data input	14	D5	data input
5	Q1	data output	15	Q5	data output
6	Q2	data output	16	Q6	data output
7	D2	data input	17	D6	data input
8	D3	data input	18	D7	data input
9	Q3	data output	19	Q7	data output
10	GND	ground (0V)	20	V_{CC}	supply voltage

Function Table

Operating modes	Input			Internal flip-flops	Output
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑=LOW-to-HIGH clock transition.

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clampingcurrent	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	±20	mA
output clampingcurrent	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	±20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$	-	±35	mA
supply current	I_{CC}	-	-	70	mA
ground current	I_{GND}	-	-70	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total powerdissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:1、Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

2、For DIP20 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

3、For SOP20 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

4、For TSSOP20 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

Recommended Operationg Conditions

74HC374

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
Input transitionrise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient emperature	T_{amb}	-	-40	-	+85	℃

Electrical Characteristics

DC Characteristics 1

(Tamb=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±0.5	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V;V_O=V_{CC} or GND		-	-	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
input capacitance	C_I	-		-	-	-	pF

AC Characteristics 1

(Tamb=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CP to Qn propagationdelay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	50	165	ns
			V_{CC}=4.5V	-	18	33	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	18	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 7	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=6.0V	-	12	26	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 7	V_{CC}=2.0V	-	50	150	ns
			V_{CC}=4.5V	-	18	30	ns
			V_{CC}=6.0V	-	14	26	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	14	60	ns
			V_{CC}=4.5V	-	5	12	ns
			V_{CC}=6.0V	-	4	10	ns
pulse width	t_W	CP; HIGH orLOW; see Figure 6	V_{CC}=2.0V	80	19	-	ns
			V_{CC}=4.5V	16	7	-	ns
			V_{CC}=6.0V	14	6	-	ns
Dn to CP set-up time	t_{su}	see Figure 6	V_{CC}=2.0V	60	14	-	ns
			V_{CC}=4.5V	12	5	-	ns
			V_{CC}=6.0V	10	4	-	ns
Dn to CPhold time	t_h	see Figure 6	V_{CC}=2.0V	5	-6	-	ns
			V_{CC}=4.5V	5	-2	-	ns
			V_{CC}=6.0V	5	-2	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	6.0	23	-	MHz
			V_{CC}=4.5V	30	70	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	77	-	MHz
			V_{CC}=6.0V	35	83	-	MHz
power dissipation capacitance	C_{PD}	per flip-flop; V_I=GND to V_{CC}		-	17	-	pF

Note:

1. t_{pd} is the same as t_{PLH} and t_{PHL}.
2. t_{en} is the same as t_{PZL} and t_{PZH}.
3. t_{dis} is the same as t_{PLZ} and t_{PHZ}.
4. t_t is the same as t_{THL} and t_{TLH}.
5. C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
   $P_D=C_{PD}\times V\ 2\times fi\times N+\sum(C_L\times V_{CC}^2\times fo)$ where:
   fi=input frequency in MHz;
   fo=output frequency in MHz;
   C_L=output load capacitance in pF;
   V_{CC}=supply voltage in V;
   N=number of inputs switching;
   $\sum(C_L\times V_{CC}^2\times f_O)$=sum of outputs.

AC Characteristics 2

(Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

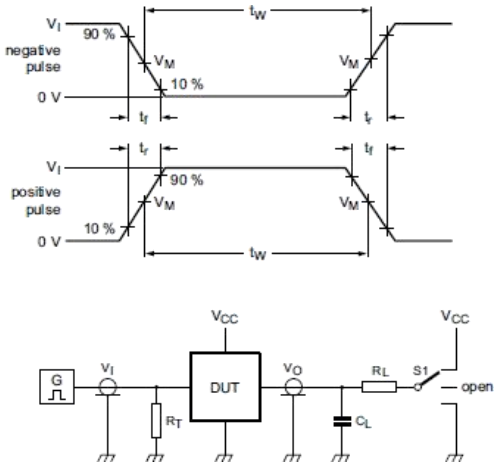
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CP to Qn propagation delay	t_{pd}	see Figure 6	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=5.0V; C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	35	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 7	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 7	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
transition time	t_t	Qn output; see Figure 6	V_{CC}=2.0V	-	-	75	ns
			V_{CC}=4.5V	-	-	15	ns
			V_{CC}=6.0V	-	-	13	ns
pulse width	t_W	CP; HIGH orLOW; see Figure 6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
Dn to CP set-up time	t_{su}	see Figure 6	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
Dn to CPhold time	t_h	see Figure 6	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
maximumfrequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
power dissipation capacitance	C_{PD}	per flip-flop; V_I=GND to V_{CC}		-	-	-	pF

Note:

6. t_{pd} is the same as t_{PLH} and t_{PHL}.
7. t_{en} is the same as t_{PZL} and t_{PZH}.
8. t_{dis} is the same as t_{PLZ} and t_{PHZ}.
9. t_t is the same as t_{THL} and t_{TLH}.
10. C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
    $P_D=C_{PD}\times V\ 2\times fi\times N+\sum(C_L\times V_{CC}^2\times fo)$ where:
    fi=input frequency in MHz; fo=output frequency in MHz;
    C_L=output load capacitance in pF;
    V_{CC}=supply voltage in V;
    N=number of inputs switching;
    $\sum(C_L\times V_{CC}^2\times f_O)$=sum of outputs.

Testing Circuit

AC Testing Circuit



Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.S1=Test selection switch.

Figure 5. Test circuit for measuring switching times

AC Testing Waveforms

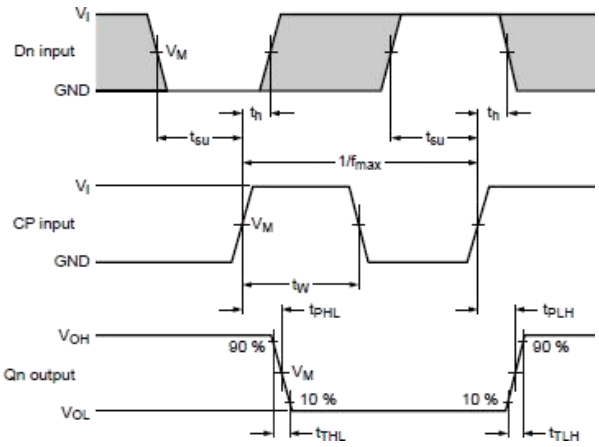


Figure 6. Clock input (CP) to output (Qn) propagation delay, clock pulse width, data (Dn) to clock (CP)set-up and hold times, output transition times (Qn) and maximum clock frequency

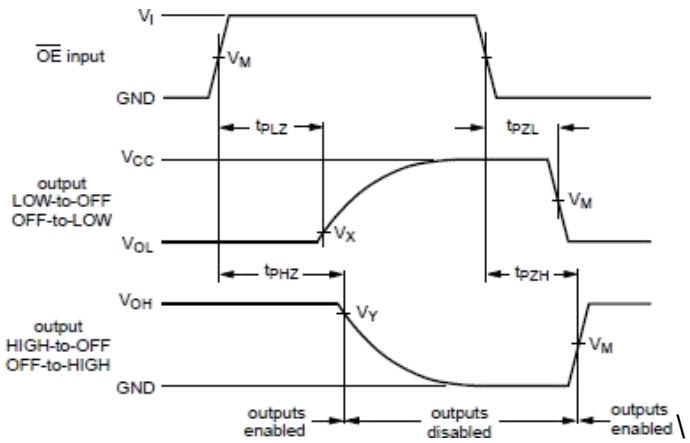


Figure 7.3-state enable and disable times

Measurement Points

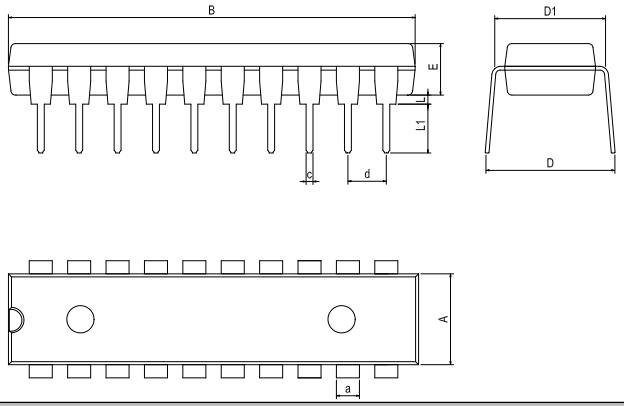
Type	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
74HC374	GND to V_{CC}	0.5×V_{CC}	0.5×V_{CC}	0.1×V_{CC}	0.9×V_{CC}

Test Data

Type	Input		Load		S1 position		
	V_I	t_r , t_f	C_L	R_L	t_{PHL},t_{PLH}	t_{PZH},t_{PHZ}	t_{PZL},t_{PLZ}
74HC374	GND to V_{CC}	6ns	15pF, 50pF	1kΩ	open	GND	V_{CC}

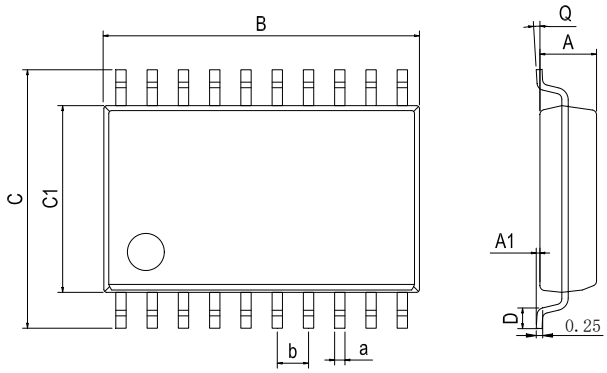
Physical Dimensions

DIP-20



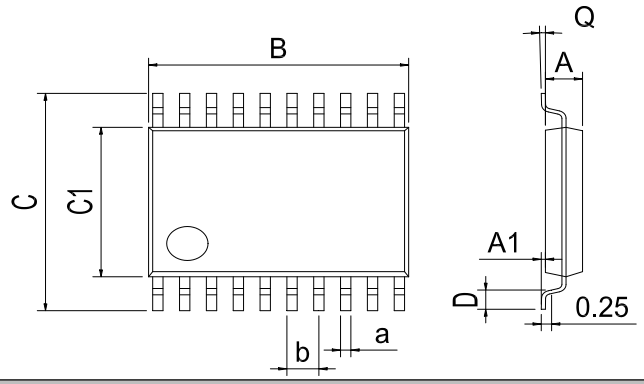
Dimensions In Millimeters(DIP-20)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	24.95	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	26.55	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

SOP-20W



Dimensions In Millimeters(SOP-20W)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.10	0.05	12.50	10.21	7.40	0.45	0°	0.35	1.27 BSC
Max:	2.50	0.25	13.00	10.61	7.60	1.25	8°	0.45	

TSSOP-20



Dimensions In Millimeters(TSSOP-20)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	6.40	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	1.05	0.20	6.60	6.60	4.50	0.80	8°	0.25	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2019-8	New	1-14
V1.1	2023-9	Updated DIP-20 dimension、Add annotation for Maximum Ratings.	4、11
V1.2	2024-11	Update packages model SOP-20W、Update Lead Temperature	1、4
V1.3	2025-9	Update important statements	14

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