



CW1051B

2~5 Channel Secondary Protection IC

Features

- 2~5 Cells Application
- Overcharge Protection
 - Threshold from 3.650V to 4.650V, 25mV Steps, $\pm 20\text{mV}$ Accuracy
- Internal Overcharge Protection Delay Time
- Overcharge Delay Counter Reset Time
- Open Wire Protection
- Low Power Dissipation
 - Normal Working $2\mu\text{A}$ (25°C)
- Package Type: MSOP8L, DFN3*4-8L

Applications

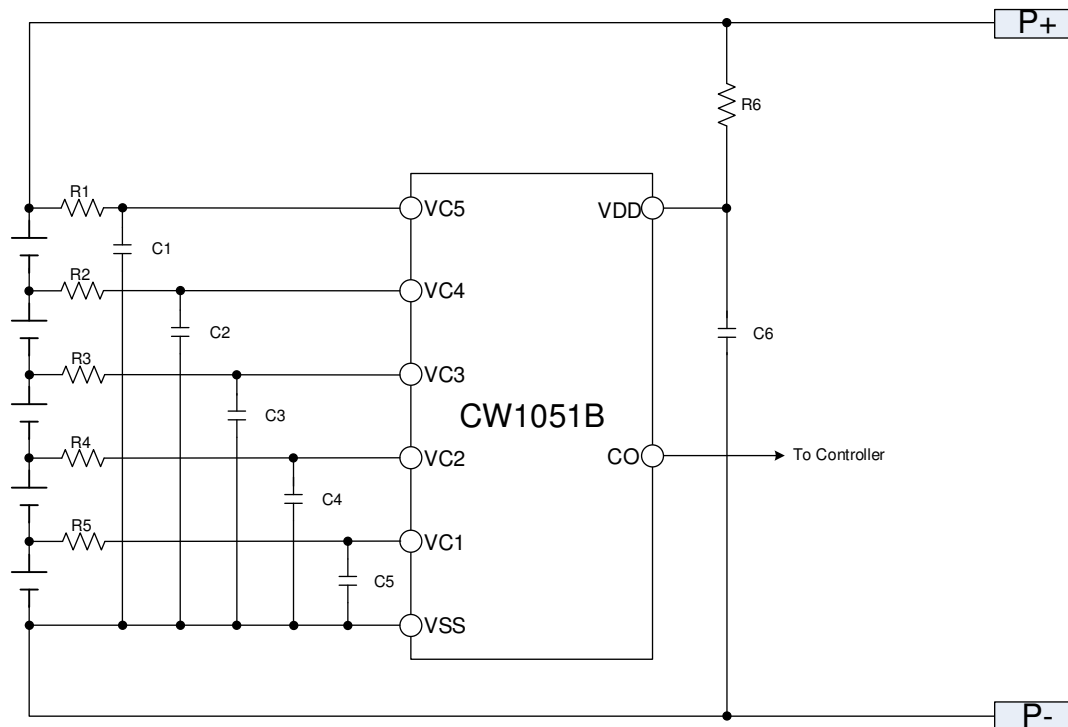
- NoteBook
- Tablet PC
- E-Tools
- Backup Power Supply
- Other Lithium-ion or Lithium Polymer Battery Packs

General Description

The CW1051B series products are highly integrated secondary protection ICs for 2 to 5 lithium-ion and lithium polymer battery cells connected in series. CW1051B provides overcharge protection for battery pack by measuring each cell's voltage.

Application Circuits

For 5 cell connect in series (CMOS, Active H)

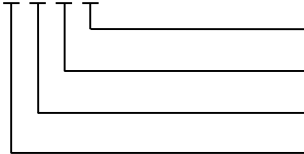


Recommended parameter

SYMBOL	TYPICAL	RANGE	UNIT
R1,R2,R3,R4,R5	1000	200~2000	Ω
R6	200	200~1000	Ω
C1,C2,C3,C4,C5	0.1	0.1~0.22	μF
C6	0.1	0.1~0.47	μF

Product Name

CW1051 X X X X



Package type, D: DFN3*4-8L M: MSOP8L

Parameter option, from A to Z

Battery type, L: Lithium F: Lithium iron phosphate

Function and revision option, from A to Z

Ordering Information

Part Number	Temperature Range	Package And Pin	Top Mark* ¹	Shipping
CW1051BLAM	-40°C to 85°C	MSOP8	1051BL AMXXXX	Tape&Reel 3000
CW1051BLBM	-40°C to 85°C	MSOP8	1051BL BMXXXX	Tape&Reel 3000
CW1051BLCM	-40°C to 85°C	MSOP8	1051BL CMXXXX	Tape&Reel 3000
CW1051BLFM	-40°C to 85°C	MSOP8	1051BL FMXXXX	Tape&Reel 3000
CW1051BLGM	-40°C to 85°C	MSOP8	1051BL GMXXXX	Tape&Reel 3000
CW1051BLHM	-40°C to 85°C	MSOP8	1051BL HMXXXX	Tape&Reel 3000
CW1051BLIM	-40°C to 85°C	MSOP8	1051BL IMXXXX	Tape&Reel 3000
CW1051BLJM	-40°C to 85°C	MSOP8	1051BL JMXXXX	Tape&Reel 3000
CW1051BLMD	-40°C to 85°C	DNF3*4-8L	1051BL MDXXXX	Tape&Reel 3000
CW1051BLQD	-40°C to 85°C	DNF3*4-8L	1051BL QDXXXX	Tape&Reel 3000
CW1051BLRM	-40°C to 85°C	MSOP8	1051BL RMXXXX	Tape&Reel 3000
CW1051BLSM	-40°C to 85°C	MSOP8	1051BL SMXXXX	Tape&Reel 3000
CW1051BLXM	-40°C to 85°C	MSOP8	1051BL XMXXXX	Tape&Reel 3000
CW1051BLXD	-40°C to 85°C	DNF3*4-8L	1051BL XDXXXX	Tape&Reel 3000
CW1051BLUM	-40°C to 85°C	MSOP8	1051BL UMXXXX	Tape&Reel 3000

*1:The mark “XXXX” is the manufacture information

Ordering Information

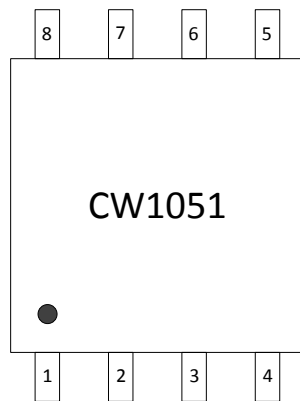
Type	Over Charge Threshold [V _{oc}] (V)	Hysteresis Voltage* ¹ [V _{hys}] (V)	Delay Time* ² [T _{oc}] (s)	Output Type* ³
CW1051BLAM	4.220	0.300	1	CMOS Active H
CW1051BLBM	4.220	0.050	1	CMOS Active L
CW1051BLCM	4.350	0.050	6	CMOS Active H
CW1051BLFM	4.300	0.300	4	CMOS Active H
CW1051BLGM	4.300	0.300	1	CMOS Active H
CW1051BLHM	4.275	0.050	2	NMOS open drain Active L
CW1051BLIM	4.175	0.100	4	CMOS, Active H
CW1051BLJM	4.250	0.100	1	CMOS Active H
CW1051BLMD	4.200	0.050	1	NMOS open drain Active L
CW1051BLQD	4.350	0.300	4	CMOS, Active H
CW1051BLRM	4.200	0.100	1	CMOS, Active L
CW1051BLSM	4.200	0.100	1	CMOS, Active H
CW1051BLXM	4.275	0.050	1	CMOS, Active H
CW1051BLXD	4.275	0.050	1	CMOS, Active H
CW1051BLUM	3.800	0.100	1	CMOS, Active H

*1 Optional hysteresis voltage: 0V, 0.050V, 0.100V, 0.150V, 0.200V, 0.250V, 0.300V, 0.350V

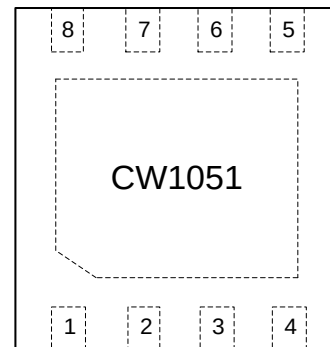
*2 Optional delay time: 1s, 2s, 4s, 6s

*3 Optional output type: CMOS active H, CMOS Active L, open drain Active L

Pin Configuration



MSOP8L Package



DFN3*4-8L Package

Pin Descriptions

PIN	NAME	DESCRIPTION
1	VDD	Power supply
2	VC5	Positive input of cell5
3	VC4	Positive input of cell4
4	VC3	Positive input of cell3
5	VC2	Positive input of cell2
6	VC1	Positive input of cell1
7	VSS	Ground
8	CO	Overcharge output driver

Absolute Maximum Ratings

		VALUE		UNITS
		MIN	MAX	
PIN voltage range respect to VSS	VDD, VCx	-0.3	36	V
PIN voltage range respect	CO	-0.3	VDD+0.3	V
Operation Temperature	T _A	-40	85	°C
Storage Temperature	T _{STG}	-40	125	°C

Caution:

Stresses beyond "Absolute Maximum Ratings" condition may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

			MAX	UNITS
V _(ESD) Rating	Electrostatic discharge	Human body model (HBM) ESD stress voltage	±3000	V
		Charged device model (CDM) ESD stress voltage	±1000	V

Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input Voltage Range	V _{DD}		4.0		25	V
VDD Input Voltage Range	V _{DD}	From -40°C to 85°C	4.5		25	V
VCx Input Voltage Range	V _{Cx}		0		4.5	V

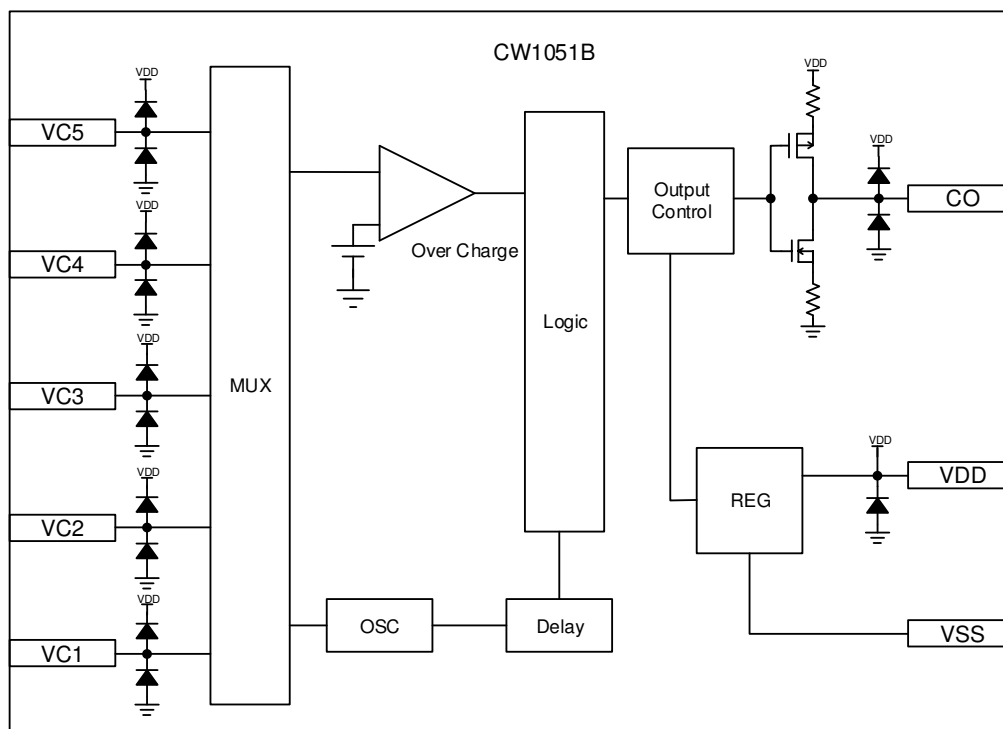
Electrical Characteristics

Operation under 25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CURRENT						
Operation Current	I _{OPR}	VC1=VC2=VC3=VC4=VC5=3.7V		2	4	μA
		VC1=VC2=VC3=VC4=VC5=3.7V		1.5	3	μA
		Output type: CMOS active H				
Channel Current	I _{CX}	VC1=VC2=VC3=VC4=VC5=3.7V	-0.8		0.8	μA
VOLTAGE/TEMPERATURE DETECT AND PROTECTION THRESHOLD						
Overcharge Threshold	V _{OC}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 3.7V to 4.5V	V _{OC} - 0.020	V _{OC}	V _{OC} + 0.020	V
Overcharge Threshold in whole Temperature Range		From 0°C to 60°C	V _{OC} - 0.025	V _{OC}	V _{OC} + 0.025	V
		From -40°C to 110°C	V _{OC} - 0.050	V _{OC}	V _{OC} + 0.050	V
OC Release Threshold V _{OCR} =V _{OC} -V _{HYS}	V _{OCR}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 4.5V to 3.7V	V _{OCR} - 0.030	V _{OCR}	V _{OCR} + 0.030	V
Open-wire Threshold	V _{OW}	VC1=VC2=VC3=VC4=2V sweep VC5 from 0V to -0.3V	-0.100	-0.150	-0.200	V
ACTION DELAY						
Overcharge Delay	t _{OC}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 3.7V to 4.5V	0.80* t _{OC}	t _{OC}	1.30* t _{OC}	s
Overcharge Release Delay	t _{OCR}	VC1=VC2=VC3=VC4=3.7V Sweep VC5 from 4.5V to 3.7V	3	4	6	ms
Overcharge Reset Delay	t _{RESET}		9	12	15	ms
Open-wire Detection Delay	t _{OW}			1		s
Open-wire Release Delay	t _{OWR}		3	4	100	ms
PIN OUTPUT VOLTAGE						
CO Logic High Output	V _{OC}	VC1=VC2=VC3=VC4=VC5=3.7V	VDD- 0.3			V
CO Logic Low Output* ¹		VC1=VC2=VC3=VC4=VC5=4.5V			0.3	V
PIN DRIVE ABILITY						
CO High Output Drive Ability	CO	V _{OC} =VDD-0.5V		210		μA
		Source resistance (VDD side)	1.7	2.5	3.3	kΩ
CO Low Output Drive Ability		V _{OC} =VSS+0.5V		0.8		mA
		Sink resistance (VSS side)	0.3	0.5	0.7	kΩ

*1 There is several output types, detail please refer to the product selection table. Take CMOS Active H for example here.

Functional Block Diagram



Notes: Some buffer blocks omitted

Detailed Description

Normal State

CW1051B works under a normal state when each cell voltage is less than V_{oc} .

Overcharge State

When any cell voltage becomes higher than overcharge threshold voltage (V_{oc}) and stays longer than overcharge protection delay time (t_{oc}), CO will output a high-level signal, and CW1051B enters over charge state. CO signal can be used to inform the external device or control the MOSFET. If within t_{oc} , cell voltage drops lower than V_{oc} but stays shorter than overcharge reset delay time (t_{RESET}) before rising up over V_{oc} again, this spike will be ignored. Otherwise, accumulated delay time of overcharge will be reset. Overcharge protection state will release when all the cell voltages are less than the overcharge release threshold (V_{OCR}) and stay longer than the release delay time (t_{OCR}).

Open-wire Detection

Any wire connected between the battery cell and IC will be monitored.

When the wire disconnects and maintains (t_{ow}) time, IC will enter to the open-wire protection state.

CO outputs a high-level voltage to cut off the charge loop.

Open-wire protection will release when all wires reconnect and stay longer than the release delay time (t_{owr}).

Test Mode

Test mode is used to reduce the protection delay time for test of mass production.

CW1051B will enter the test mode when add a $V_{DD}+7V$ voltage on VDD pin and maintains 50ms. Test mode lasts 5s then recovers to the normal status.

Detailed test mode timing is illustrated as bellow:

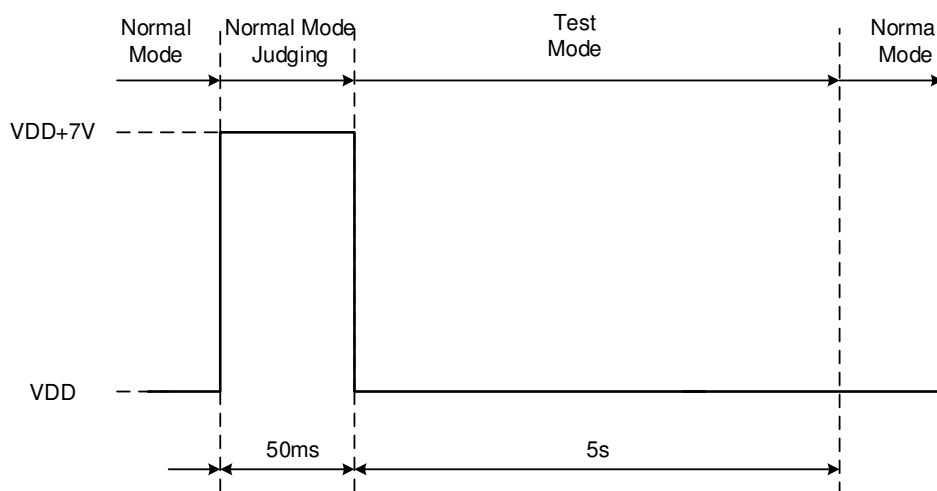
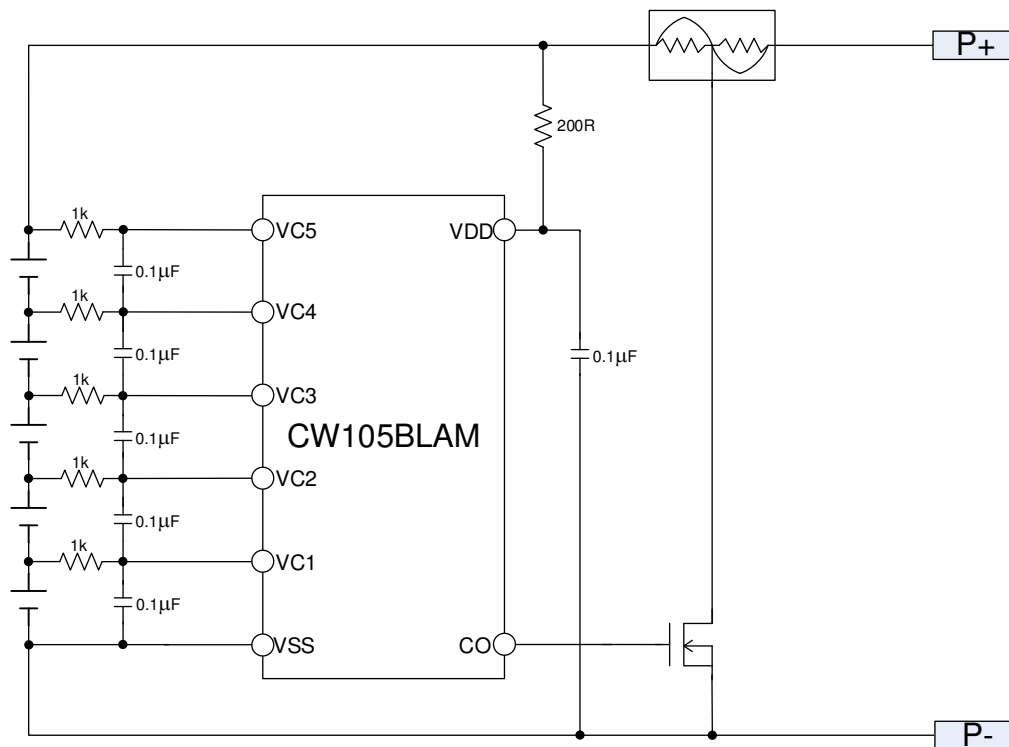
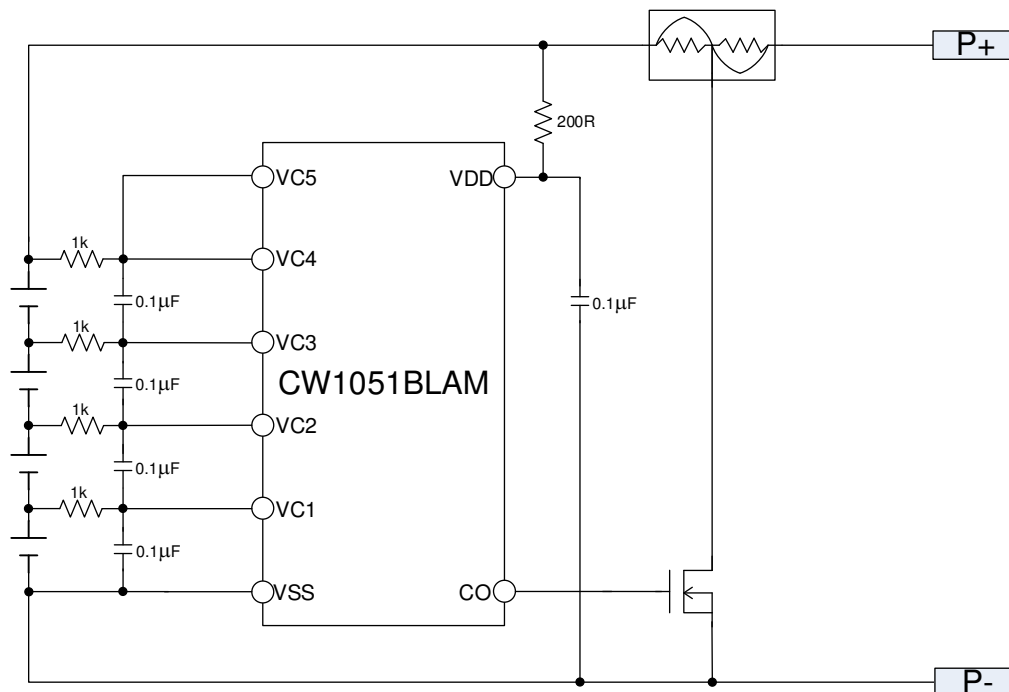


Figure 1. Test Mode Timing

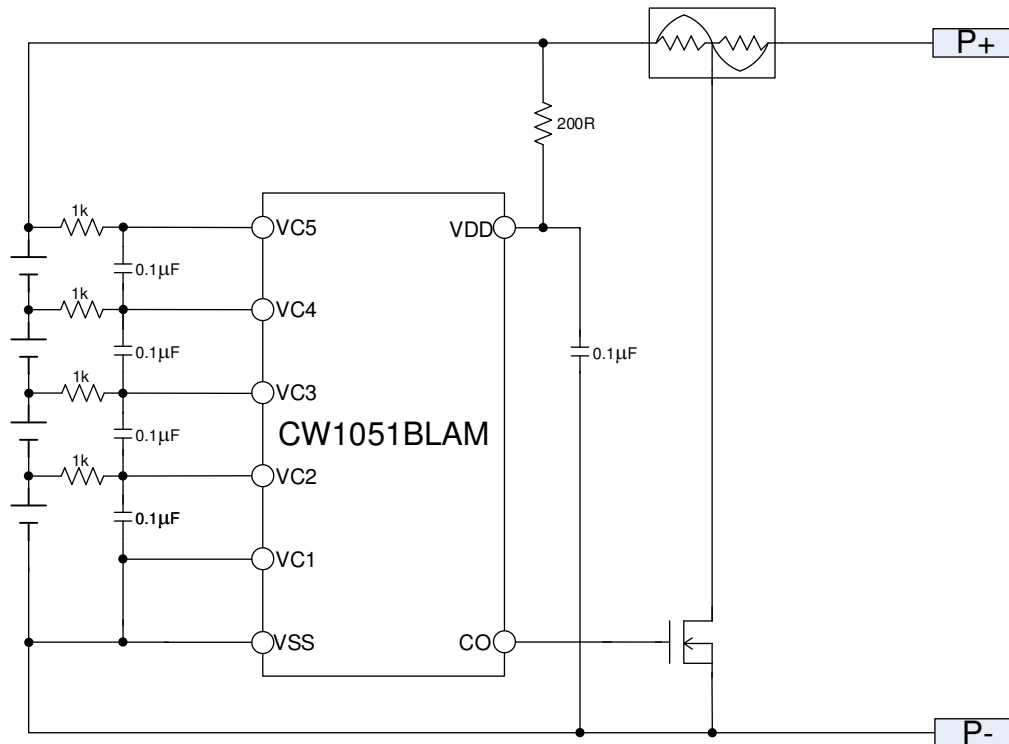
Reference Schematic



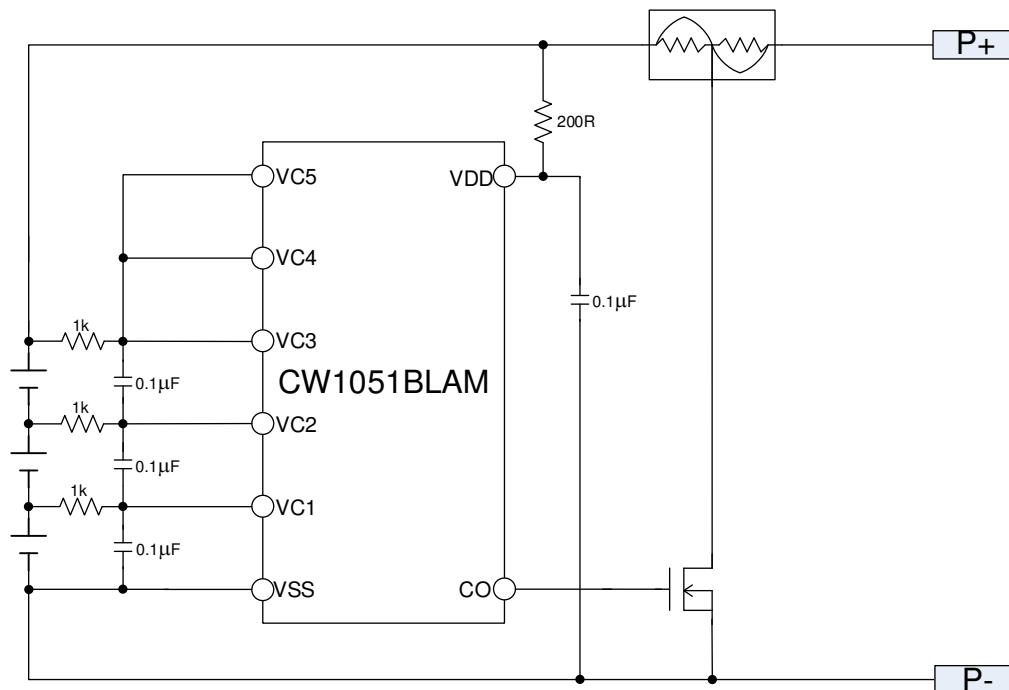
Reference Schematic for 5 cells



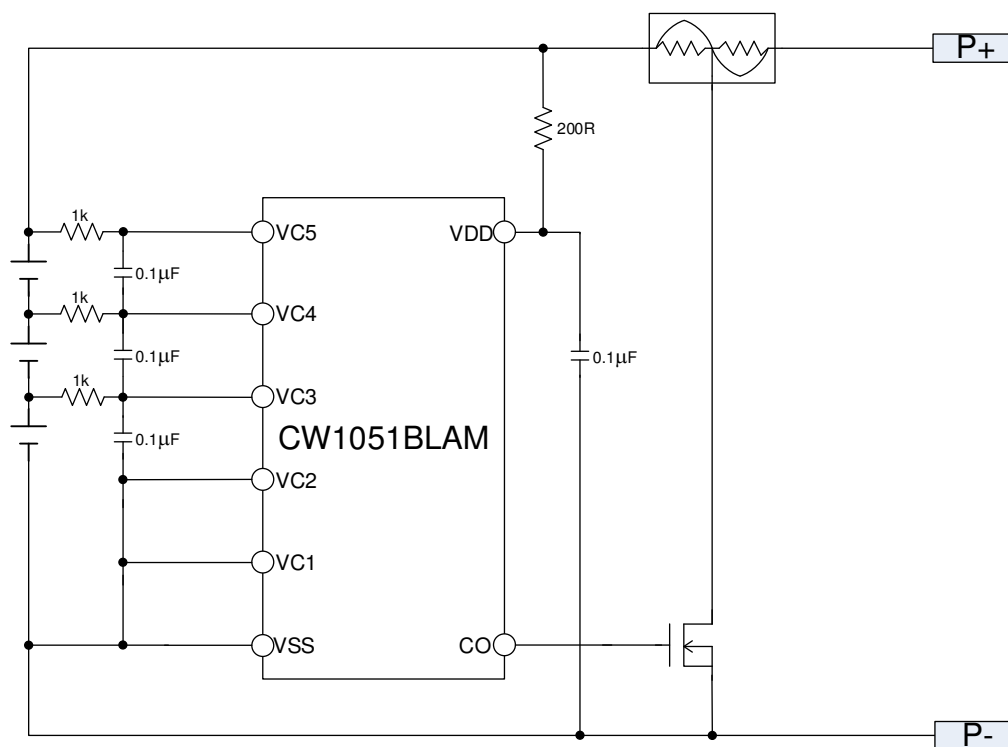
Reference Schematic for 4 cells(connect high side cell)



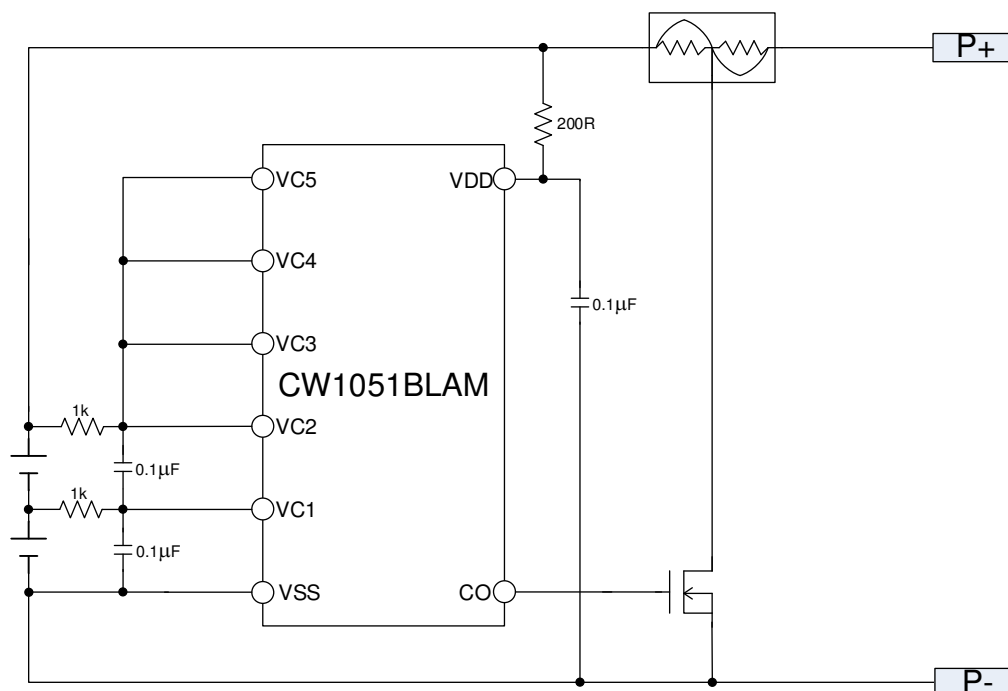
Reference Schematic for 4 cells (connect low side cell)



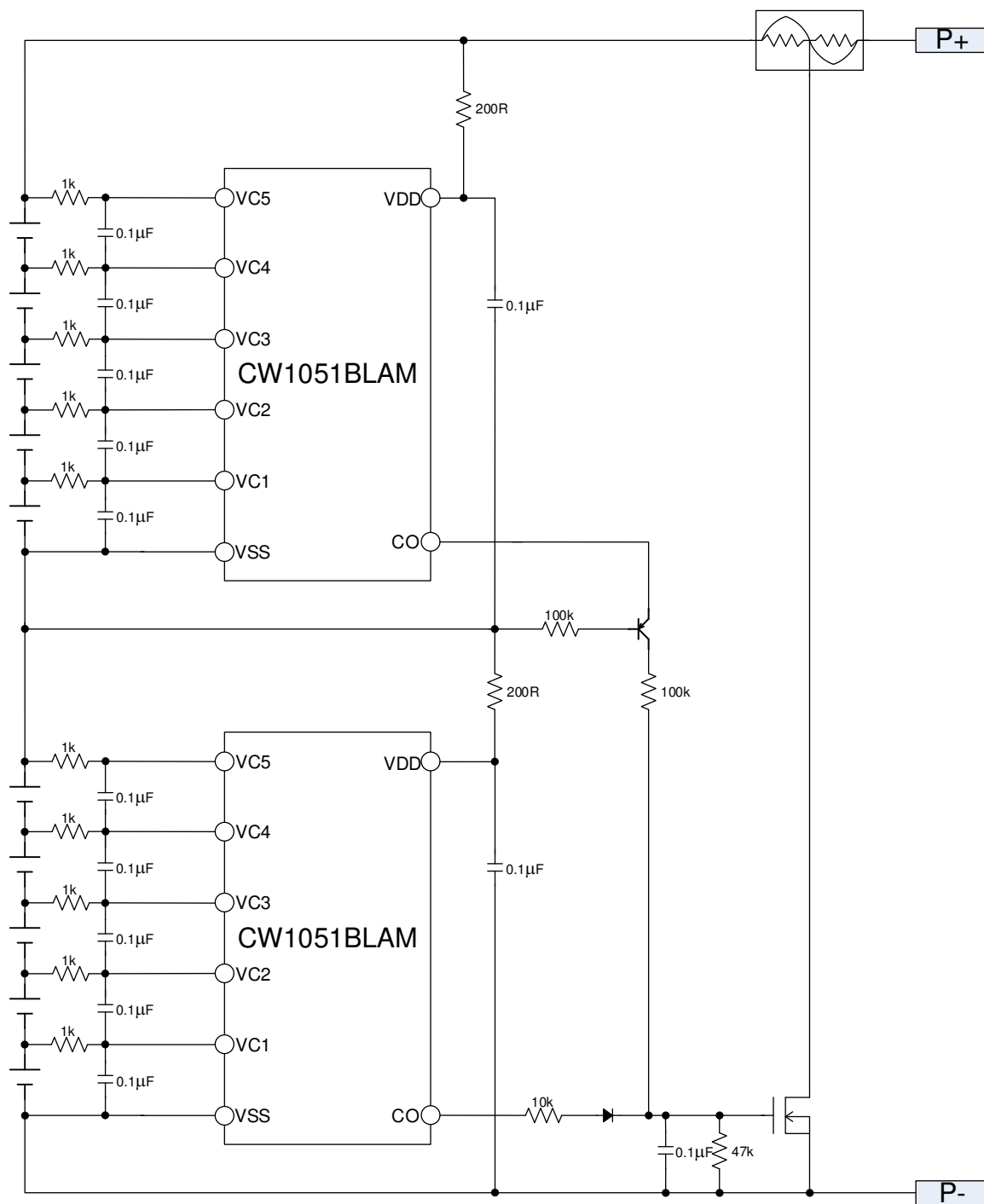
Reference Schematic for 3 cells (connect high side cell)



Reference Schematic for 3 cells (connect low side cell)



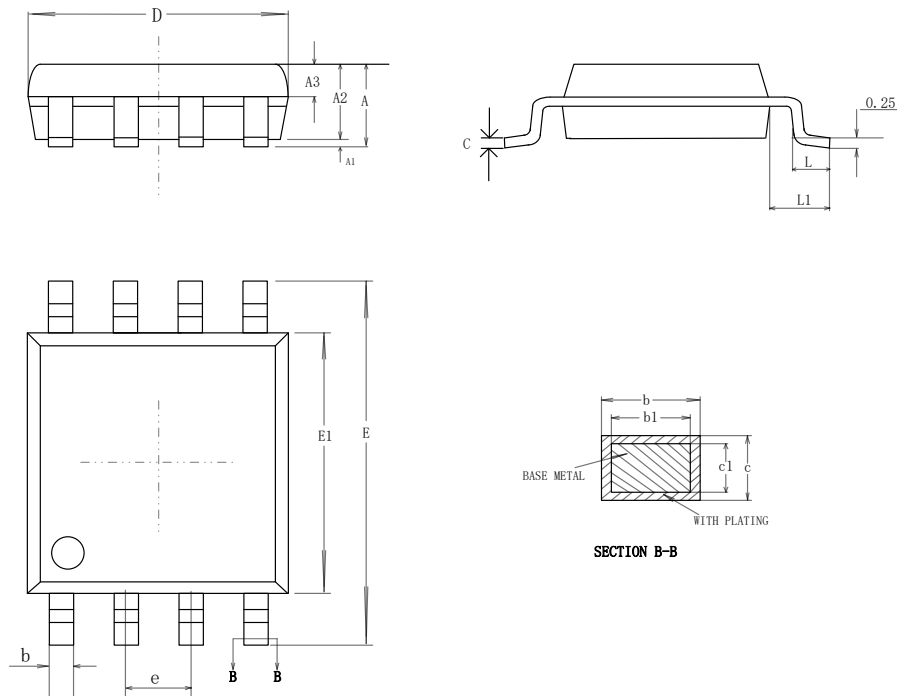
Reference Schematic for 2 cells(connect high side cell)



Reference Schematic for 10 cells

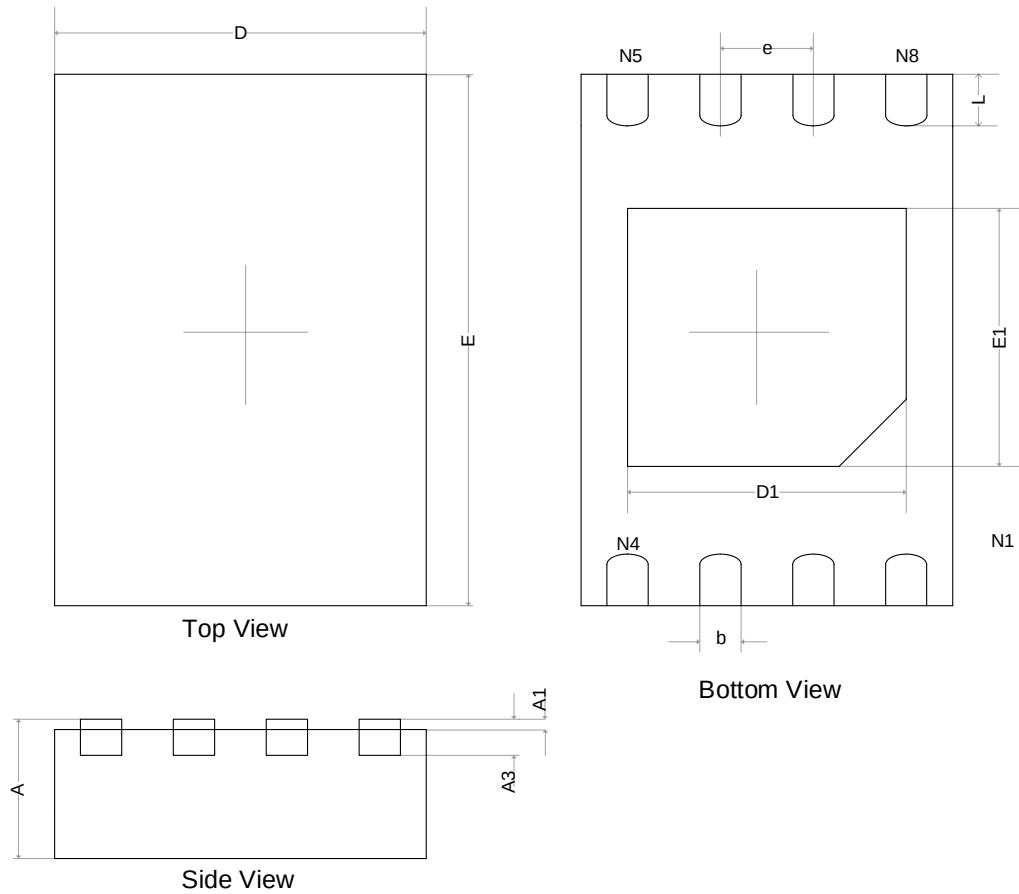
Package Information

MSOP8L PACKAGE OUTLINE DIMENSIONS



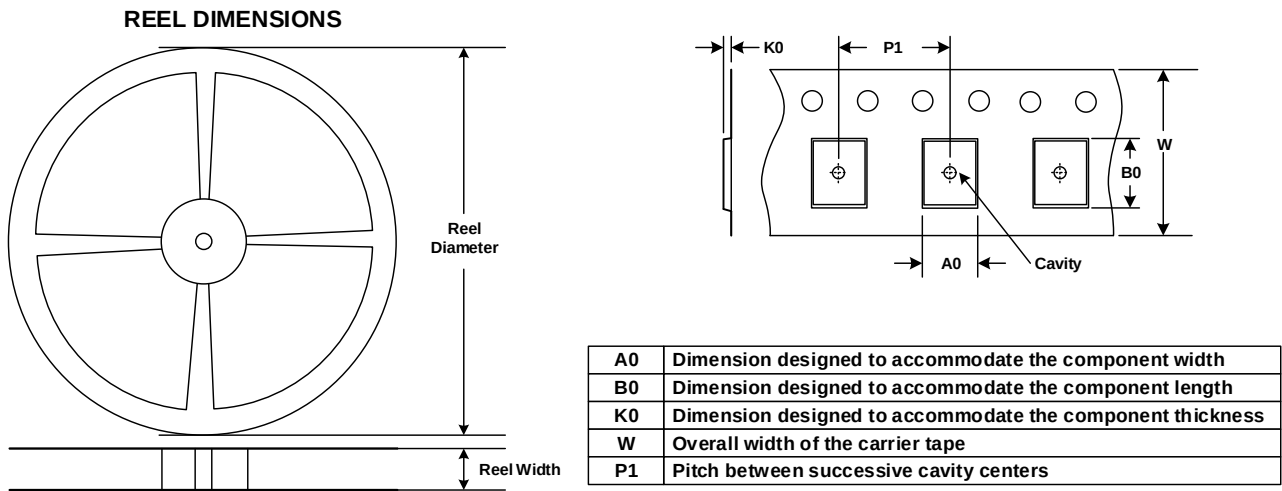
SYMBOL	MILLIMETER	
	MIN.	MAX.
A		1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.9	3.1
E	4.7	5.1
E1	2.9	3.1
e	0.65BSC	
L	0.40	0.70
L1	0.95BSC	

DFN3X4-8L PACKAGE OUTLINE DIMENSIONS

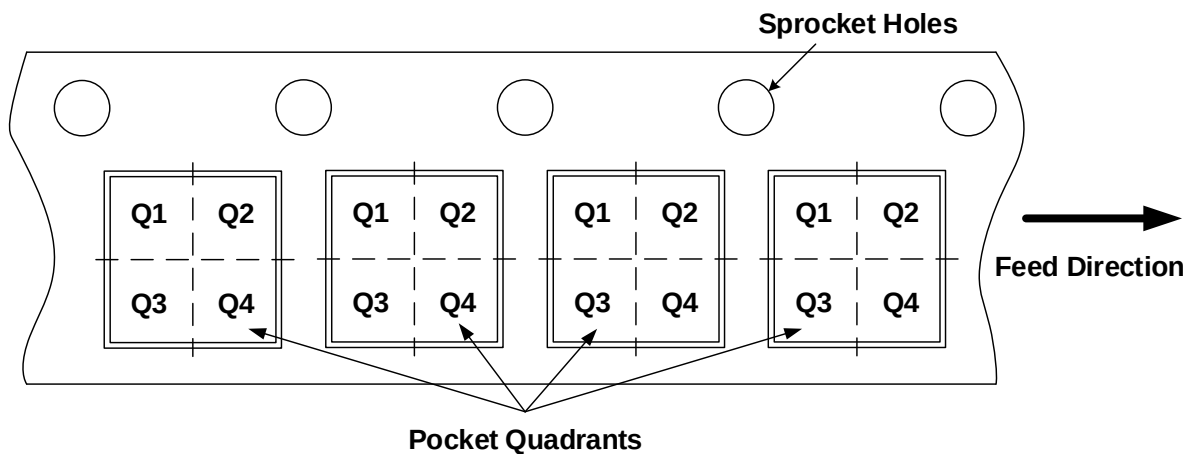


SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	-	0.02	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	3.90	4.00	4.10
D1	2.20	2.30	2.40
E1	1.70	1.80	1.90
b	0.15	0.20	0.25
e	0.650BSC		
L	0.35	0.40	0.45

Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	P1 (mm)	Pin 1 Quadrant
CW1051B	DNF-8L	180	8.60	3.26	3.30	1.40	8.00	4.00	Q2
CW1051B	MSOP-8L	330	12.40	5.40	3.40	1.40	12.00	8.00	Q1

Note: All dimensions are nominal.

Revision History

Release No.	Date	Revision Description
1.0	2024-07	Initial Release

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