

Automotive LPDDR4X Datasheet

Ver.4.0

2024.05

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Revision History

Version	Date	Description
1.0	2023.3.1	First Release
2.0	2024.4.10	Update Operating temperature range
3.0	2024.5.14	Integration of industrial and automotive grades
4.0	2024.5.21	Update power consumption

Table of Contents

Revision History	2
1. Features	4
2. Product Information	5
2.1 MR0, MR[6:5], MR8, MR13, MR24 Definition	6
2.2 Part Numbering	7
2.3 Package Block Diagrams	7
2.4 Package Dimension	8
2.5 Ball Assignments	9
2.6 IDD Parameters(b)Single Die	11
3. AC Timing	13
3.1 AC Timing Parameters	13
3.2 CA Rx Voltage and Timing	22
4. CA Rx Voltage and Timing	23
5. DQ Tx Voltage and Timing	26
5.1 DRAM Data Timing	26
6. Clock Specification	31
6.1 tCK(abs), tCH(abs), and tCL(abs)	32
7. Clock Period Jitter	33
7.1 Clock Period Jitter Effects on Core Timing Parameters	33
7.2 Cycle Time Derating for Core Timing Parameters	33
7.3 Clock Cycle Derating for Core Timing Parameters	33
7.4 Clock Jitter Effects on Command/Address Timing Parameters	33
7.5 Clock Jitter Effects on READ Timing Parameters	34
7.6 Clock Jitter Effects on WRITE Timing Parameters	34

1.Features

- Ultra-low-voltage core and I/O power supplies
 - VDD1 = 1.70–1.95V; 1.80V nominal
 - VDD2 = 1.06–1.17V; 1.10V nominal
 - VDDQ = 0.57–0.65V; 0.60V nominal
 - or VDDQ = 1.06–1.17V; 1.10V nominal
- Frequency range – 2133 – 10 MHz (data rate range: 4266–20 Mb/s/ pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies(RL/WL)
- Programmable and on-the-fly burst lengths(BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.5 GB/s per die
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS&REACH-compliant, “green” packaging
- Programmable VSS (ODT) termination

Options

- VDD1/VDD2/VDDQ: 1.80V/1.10V/0.60V or 1.1V
- Array configuration
 - 512 Meg x 32 (2 channels x 16 I/O)
- Device configuration
 - 512M32 x1 die in package
- FBGA “green” package
 - 200-ball FBGA (10mm x 14.5mm)
- Speed grade, cycle time
 - 468ps@RL=36/40
 - 535ps@RL=32/36
 - 625ps@RL=28/32
- Operating temperature range
 - Industrial Grade: -40°C ~ +95°C
 - Automotive Grade2: -40°C ~ +105°C

[Table 1] Key Timing Parameters

Clock Rate (MHz)	Data Rate (Mb/s/pin)	Write Latency		Read Latency	
		Set A	Set B	DBI Disabled	DBI Enabled
2133	4266	18	34	36	40
1866	3733	16	30	32	36
1600	3200	14	26	28	32

2. Product Information

Part ID	Capacity	Size	Package	Temperature	Grade
BWMZAX32H2A-16GI-X	16Gb	10mm*14.5mm*0.9mm	FBGA200	-40~95°C	Industrial
BWLGYA002GN6ZA	16Gb	10mm*14.5mm*0.9mm	FBGA200	-40~105°C	Automotive

		512M32 (16Gb/package)
Die organization in the package	Channel A, rank 0	x16 mode × 1 die
	Channel B, rank 0	
	Channel A, rank 1	-
	Channel B, rank 1	
Density per die		16Gb
Density per channel		8Gb
Configuration		64Mb × 16 DQ × 8 banks × 2 channels
Number of channels (per die)		2
Number of banks (per channel)		8
Array prefetch (bits, per channel)		256
Number of rows (per channel)		65,536
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		8,589,934,592
Total density (bits per die)		17,179,869,184
Bank address		BA[2:0]
×16	Row address	R[15:0]
	Column address	C[9:0]
Burst starting address boundary		64bit

Note:

1.Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

2.1 MR0, MR[6:5], MR3,MR8, MR13, MR24,MR25 Definition

[Table 2] Mode Register Definition

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			Single-ended mode			RFM support	Latency mode	REF
	OP[0] = 1b: Only modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[2] = 0b: Device supports TRR OP[5] = 1b: Device supports single-ended mode							
MR3						PPRP ₃		
	OP[2] = 0b: PPR protection disabled (default) 1b: PPR protection enabled							
MR5	Manufacturer ID							
	1111 1111b							
MR6	Revision ID1							
	0000 0111b							
MR8	I/O width		Density					
	OP[7:6] = 00b: x16/channel		OP[5:2] = 0100b: 16Gb dual-channel die					
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the V _{REF(CA)} value on DQ7 and V _{REF(DQ)} value on DQ6							
MR24	TRR mode				Unlimited MAC	MAC value		
	OP[3:0] = 1000b: Unlimited MAC OP[7] = 0b: Disable (default) 1b: Reserved							
MR25	PPR resources ⁴							
	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0
	0b: PPR resource is not available 1b: PPR resource is available							

Notes:

- 1.The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.
- 2.Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.
- 3.When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry.(MR3 OP[2]=1b).
- 4.Before using PPR function, confirm the availability of PPR resource by reading MR25.

2.2 Part Numbering

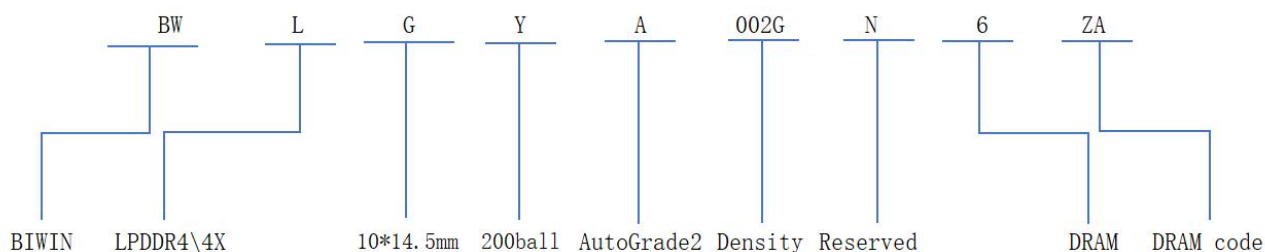


Figure 1-1: Automotive Part Numbering

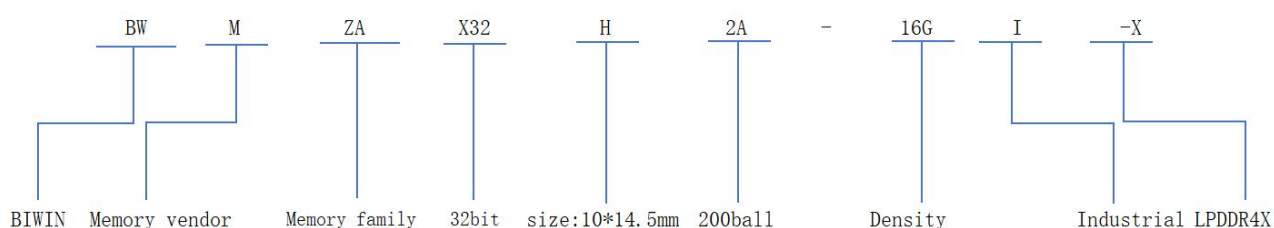


Figure 1-2: Industrial Part Numbering

2.3 Package Block Diagrams

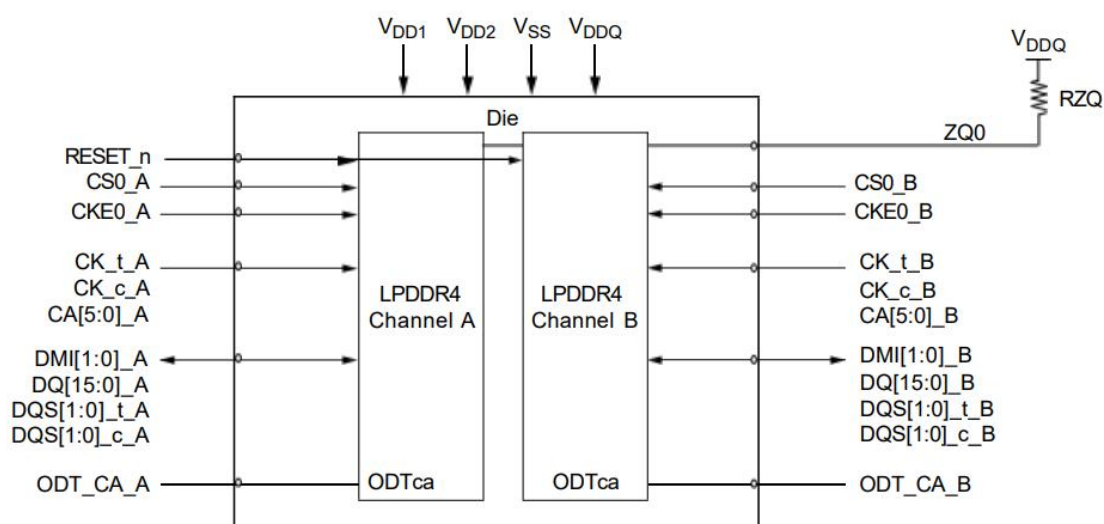
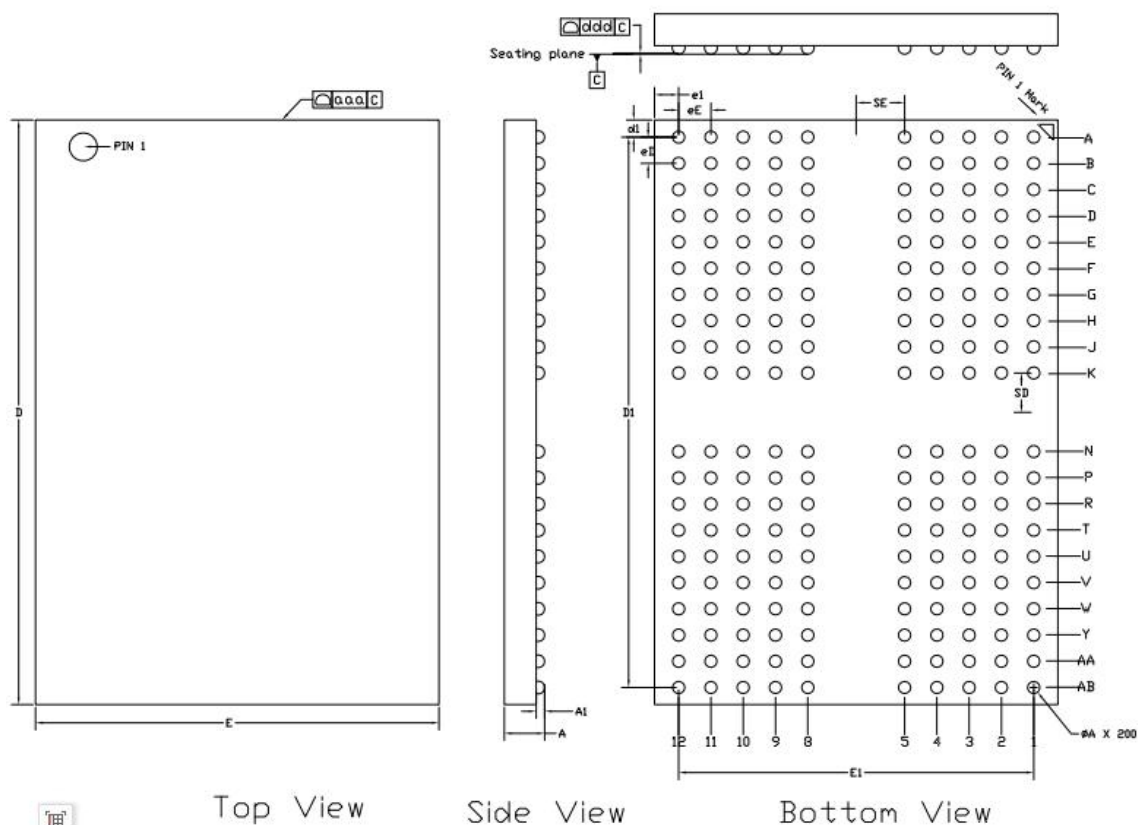
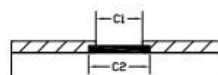


Figure 2 Single-Die, Dual-Channel Package Block Diagram

2.4 Package Dimension



ITEM	Symbol	Unit:mm		
		MIN	NORM	MAX
BODY SIZE	D	14.40	14.50	14.60
	E	9.90	10.00	10.10
TOTAL THICKNESS	A	0.80	0.90	1.00
STAND OFF	A1	0.18	0.21	0.24
EDGE BALL (CENTER TO CENTER)	D1	13.65		
	E1	8.80		
BALL PITCH	eD	0.65		
	eE	0.80		
even number of balls ($eE/2, eD/2$)	SE	1.20		
odd number of balls (O)	SD	0.98		
BALL COUNT	n	200		
BALL WIDTH (after reflow)	ΦA	0.29	0.32	0.35
Solder mask opening	C1	0.27	0.30	0.33
Ball pad diameter	C2	0.33	0.36	0.39
BALL TO OUTLINE	d1	0.32	0.42	0.52
	e1	0.50	0.60	0.70
Mold package warpage	ccc	0.08		
COPLANARITY	ddd	0.08		



200ball $\Phi 0.3\text{mm}$ Dimensions apply
to solder balls postreflow
on $\Phi 0.3\text{mm}$ SMD ball pads.

Notice:

1. Ball diameter: 0.3mm
2. "●" --- bumping ball location
3. In the diagram, there are 200 ball locations in all.

Figure 3 Package Dimension (10mm*14.5mm*0.9mm)

2.5 Ball Assignments

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ0			RFU	VDD2	VSS	NC	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1_A	DM0_A	DQ6_A	VSS			VSS	DQ14_A	DM1_A	DQ9_A	VSS
D	VDDQ	VSS	DQSO_T_A	VSS	VDDQ			VDDQ	VSS	DQS1_T_A	VSS	VDDQ
E	VSS	DQ2_A	DQSO_C_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	RFU	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	RFU			CK_T_A	CK_C_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	RFU			CK_T_B	CK_C_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	RFU	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQSO_C_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_C_B	DQ10_B	VSS
W	VDDQ	VSS	DQSO_T_B	VSS	VDDQ			VDDQ	VSS	DQS1_T_B	VSS	VDDQ
Y	VSS	DQ1_B	DM0_B	DQ6_B	VSS			VSS	DQ14_B	DM1_B	DQ9_B	VSS
AA	NC	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	NC
AB	NC	NC	VSS	VDD2	VSS			VSS	VDD2	VSS	NC	NC

Figure 4 Dual-Channel, Single-Rank Discrete FBGA

[Table 3] Ball/Pad Description

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel has its own clock pair.
CKE0_A, CKE1_A, CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B, CS1_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating

		ranks are bonded to VSS (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]__t__A, DQS[1:0]__c__A, DQS[1:0]__t__B, DQS[1:0]__c__B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	-	Do not use: Must be grounded or left floating.
NC	-	No connect: Not internally connected.
RFU		Reserved for future use on larger capacity configurations

Notes: ZQ1, CKE1_A, CKE1_B, CS1_A and CS1_B balls are reserved for 2-rank package. For 1-rank package those balls are NC.

2.6 IDD Parameters Single Die

VDD2 = 1.06–1.17V, VDDQ = 0.57–0.65V or VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V

[Table 4] IDD Parameters – Single-Die

Symbol	Supply	Speed Grade:4266 Mb/s		Unit	Note
		95°C	105°C		
I _{DD01}	V _{DD1}	8.40	8.80	mA	
I _{DD02}	V _{DD2}	59.00	60.00		
I _{DD0Q}	V _{DDQ}	1.50	1.50		
I _{DD2P1}	V _{DD1}	2.40	2.40	mA	
I _{DD2P2}	V _{DD2}	5.40	7.20		
I _{DD2PQ}	V _{DDQ}	1.50	1.50		
I _{DD2PS1}	V _{DD1}	2.40	2.40	mA	
I _{DD2PS2}	V _{DD2}	5.40	7.20		
I _{DD2PSQ}	V _{DDQ}	1.50	1.50		
I _{DD2N1}	V _{DD1}	2.40	2.40	mA	
I _{DD2N2}	V _{DD2}	33.00	35.00		
I _{DD2NQ}	V _{DDQ}	1.50	1.50		
I _{DD2NS1}	V _{DD1}	2.40	2.40	mA	
I _{DD2NS2}	V _{DD2}	25.00	29.00		
I _{DD2NSQ}	V _{DDQ}	1.50	1.50		
I _{DD3P1}	V _{DD1}	2.40	2.40	mA	
I _{DD3P2}	V _{DD2}	9.80	10.00		
I _{DD3PQ}	V _{DDQ}	1.50	1.50		
I _{DD3PS1}	V _{DD1}	2.40	2.40	mA	
I _{DD3PS2}	V _{DD2}	9.80	10.00		
I _{DD3PSQ}	V _{DDQ}	1.50	1.50		
I _{DD3N1}	V _{DD1}	3.40	3.40	mA	
I _{DD3N2}	V _{DD2}	44.00	46.00		
I _{DD3NQ}	V _{DDQ}	1.50	1.50		
I _{DD3NS1}	V _{DD1}	3.40	3.40	mA	
I _{DD3NS2}	V _{DD2}	36.00	41.00		
I _{DD3NSQ}	V _{DDQ}	1.50	1.50		
I _{DD4R1}	V _{DD1}	15.00	15.00	mA	2, 3
I _{DD4R2}	V _{DD2}	400.00	400.00		
I _{DD4RQ}	V _{DDQ}	126.10	126.10		
I _{DD4W1}	V _{DD1}	15.00	15.00	mA	2
I _{DD4W2}	V _{DD2}	300.00	300.00		
I _{DD4WQ}	V _{DDQ}	1.50	1.50		
I _{DD51}	V _{DD1}	35.00	35.00	mA	
I _{DD52}	V _{DD2}	195.00	200.00		
I _{DD5Q}	V _{DDQ}	1.50	1.50		

Symbol	Supply	Speed Grade:4266 Mb/s		Unit	Note
		95°C	105°C		
I _{DD5AB1}	V _{DD1}	7.80	8.00	mA	
I _{DD5AB2}	V _{DD2}	41.00	45.00		
I _{DD5ABQ}	V _{DDQ}	1.50	1.50		
I _{DD5PB1}	V _{DD1}	6.70	7.00	mA	
I _{DD5PB2}	V _{DD2}	41.00	45.00		
I _{DD5PBQ}	V _{DDQ}	1.50	1.50		

Notes:

1. Published IDD values except IDD4RQ are the maximum IDD values considering the worst- case conditions of process, temperature, and voltage.

2. BL = 16, DBI disabled.

3. IDD4RQ value is reference only. Typical value. V_{OH} = 0.5 × V_{DDQ}; TC = 25°C

4. IDD values reflect dual-channel operation with the same pattern for each channel.

V_{DD2} = 1.06–1.17V, V_{DDQ} = 0.57–0.65V or V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

[Table 5] Full-Array Self Refresh Current

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	V _{DD1}	0.65	mA
	V _{DD2}	1.33	
	V _{DDQ}	0.02	
85°C	V _{DD1}	5.00	
	V _{DD2}	12.00	
	V _{DDQ}	1.50	

Notes:

1. IDD625°C is the typical value in the distribution with nominal VDD and a referenceonly value. IDD6 85°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.

2. IDD values reflect dual-channel operation with the same pattern for each channel.

3. AC Timing

3.1 AC Timing Parameters

[Table 6] Clock Timing

Parameter	Symbol	Min/Max	Data Rate				Unit
			1600	3200	3733	4267	
Average clock period	tCK(AVG)	Min	1250	625	535	468	ps
		Max	100	100	100	100	ns
Average HIGH pulse width	tCH(AVG)	Min	0.46				tCK(AVG)
		Max	0.54				
Average LOW pulse width	tCL(AVG)	Min	0.46				tCK(AVG)
		Max	0.54				
Absolute clock period	tCK(ABS)	Min	tCK(AVG)min + tJIT(per)min				ps
Absolute clock HIGH pulse width	tCH(ABS)	Min	0.43				tCK(AVG)
		Max	0.57				
Absolute clock LOW pulse width	tCL(ABS)	Min	0.43				tCK(AVG)
		Max	0.57				
Clock period jitter	tJIT(per)allowed	Min	−70	−40	−34	−30	ps
		Max	70	40	34	30	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	tJIT(cc)allowed	Max	140	80	68	60	ps

[Table 7] Read Output Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
DQS output access time from CK_t/CK_c	tDQSCK	Min	1500								ps	1
		Max	3500									
DQS output access time from CK_t/CK_c - voltage variation	tDQSCK VOLT	Max	7								ps/mV	2
DQS output access time from CK_t/CK_c - temperature variation	tDQSCK TEMP	Max	4								ps/°C	3
CK to DQS rank to rank variation	tDQSCK_rank2rank	Max	1.0								ns	4, 5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	MIN(tQSH,tQSL)								ps	6

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Data output valid window time total, per pin (DBI-Disabled)	tQW_to- tal	Min	0.75			0.73		0.70			UI	6, 11
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	Min	MIN(tQSH_DBI,tQSL_DBI)								ps	6
Data output valid window time total, per pin (DBI-Enabled)	tQW_to- tal_DBI	Min	0.75		0.73		0.70			UI	6, 11	
DQS_t, DQS_c differential output LOW time (DBI-Disabled)	tQSL	Min	tCL(ABS) - 0.05								tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI-Disabled)	tQSH	Min	tCH(ABS) - 0.05								tCK(AVG)	10, 11
DQS_t, DQS_c differential output LOW time (DBI-Enabled)	tQSL-DBI	Min	tCL(ABS) - 0.045								tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI-Enabled)	tQSH-DBI	Min	tCH(ABS) - 0.045								tCK(AVG)	10, 11
Read preamble	tRPRE	Min	1.8								tCK(AVG)	
Read postamble	tRPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(AVG)	
DQS Low-Z from clock	tLZ(DQS)	Min	(RL × tCK) + tDQSCK(MIN) - (tRPRE(MAX) × tCK) - 200ps								ps	
DQ Low-Z from clock	tLZ(DQ)	Min	(RL × tCK) + tDQSCK(MIN) - 200ps								ps	
DQS High-Z from clock	tHZ(DQS)	Max	(RL × tCK) + tDQSCK(MAX)+(BL/2 × tCK) + (tRPST(MAX) × tCK) - 100ps								ps	
DQ High-Z from clock	tHZ(DQ)	Max	(RL × tCK) + tDQSCK(MAX) + tDQSQ(MAX) + (BL/2 × tCK) - 100ps								ps	

Notes:

1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.

2. t_{DQSCK_volt} max delay variation as a function of DC voltage variation for VDDQ and VDD2. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the MAX [ABS($t_{DQSCK}(MIN)$ @V1 - $t_{DQSCK}(MAX)$ @V2), ABS($t_{DQSCK}(MAX)$ @V1 - $t_{DQSCK}(MIN)$ @V2)] / ABS(V1 - V2).

3. t_{DQSCK_temp} MAX delay variation as a function of temperature.

4. The same voltage and temperature are applied to $t_{DQSCK_rank2rank}$.

5. $t_{DQSCK_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.

6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.

7. The deterministic component of the total timing.

8. This parameter will be characterized and guaranteed by design.

9. t_{QSL} describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.

10. t_{QSH} describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.

11. This parameter is a function of input clock jitter. These values assume MIN $t_{CH}(ABS)$ and $t_{CL}(ABS)$. When the input clock jitter MIN $t_{CH}(ABS)$ and $t_{CL}(ABS)$ is 0.44 or greater than $t_{CK}(AVG)$, the minimum value of t_{QSL} will be $t_{CL}(ABS)$.

[Table 8] Write Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Rx timing window total at V dIVW voltage levels	TdIVW_-total	Max	0.22					0.25			UI	1, 2, 3
DQ and DMI input pulse width (at V CENT_DQ)	TdIPW	Min	0.45								UI	7
DQ-to-DQS offset	tDQS2DQ	Min	200								ps	6
		Max	800									
DQ-to-DQ offset	tDQDQ	Max	30								ps	7
DQ-to-DQS offset temperature variation	tDQS2DQ_temp	Max	0.6								ps/° C	8
DQ-to-DQS offset voltage variation	tDQS2DQ_volt	Max	33								ps/50mV	9
DQ-to-DQS offset rank to rank variation	tDQS2DQ_rank2rank	Max	200								ps	10, 11
WRITE command to first DQS transition	tDQSS	Min	0.75								tCK(AVG)	
		Max	1.25									
DQS input HIGH-level width	tDQSH	Min	0.4								tCK(AVG)	
DQS input LOW-level width	tDQSL	Min	0.4								tCK(AVG)	
DQS falling edge to CK setup time	tDSS	Min	0.2								tCK(AVG)	
DQS falling edge from CK hold time	tDSH	Min	0.2								tCK(AVG)	
Write postamble	tWPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(AVG)	
Write preamble	tWPRE	Min	1.8								tCK(AVG)	

- 0.04 and t_{QSH} will be $t_{CH}(ABS) - 0.04$

Notes:

- 1.Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
- 2.Rx differential DQ-to-DQS jitter total timing window at the VdIVW voltage levels.
3. Defined over the DQ internal V REF range. The Rx mask at the pin must be within the internal VREF(DQ) range irrespective of the input signal common mode.
- 4.R Rx mask defined for one pin toggling with other DQ signals in a steady state.
- 5.DQ-only minimum input pulse width defined at the VCENT_DQ(pin_mid) .
- 6.DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.
- 7.DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. $t_{DQS2DQ}^{(MAX)}$ delay variation as a function of temperature.
9. $t_{DQS2DQ}^{(MAX)}$ delay variation as a function of the DC voltage variation for V DDQ and VDD2. It includes the V DDQ and V DD2AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.
- 10.The same voltage and temperature are applied to $t_{DQS2DQ_rank2rank}$.
11. $t_{DQS2DQ_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
12. $UI = t_{CK}^{(AVG)}(MIN)/2$.

[Table 9] CKE Input Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
CKE minimum pulse width (HIGH and LOW pulse width)	t_{CKE}	Min	MAX(7.5ns, 4nCK)				ns	1
Delay from valid command to CKE input LOW	t_{CMDCKE}	Min	MAX(1.75ns, 3nCK)				ns	1
Valid clock requirement after CKE input LOW	t_{CKELCK}	Min	MAX(5ns, 5nCK)				ns	1
Valid CS requirement before CKE input LOW	t_{CSCKE}	Min	1.75				ns	
Valid CS requirement after CKE input LOW	t_{CKELCS}	Min	MAX(5ns, 5nCK)				ns	1
Valid Clock requirement before CKE Input HIGH	t_{CKCKEH}	Min	MAX(1.75ns, 3nCK)				ns	1
Exit power-down to next valid command delay	t_{XP}	Min	MAX(7.5ns, 5nCK)				ns	1
Valid CS requirement before CKE input HIGH	t_{CSCKEH}	Min	1.75				ns	
Valid CS requirement after CKE input HIGH	t_{CKEHCS}	Min	MAX(7.5ns, 5nCK)				ns	1
Valid clock and CS requirement after CKE input LOW after MRW command	$t_{MRWCKEL}$	Min	MAX(14ns, 10nCK)				ns	1
Valid clock and CS requirement after CKE input LOW after ZQCAL START command	t_{ZQCKE}	Min	MAX(1.75ns, 3nCK)				ns	1

Note:

1. Delay time has to satisfy both analog time(ns) and clock count (nCK). For example, t_{CMDCKE} will not expire until CK has toggled through at least 3 full cycles (3tCK) and 3.75ns has transpired. The case that 3nCK is applied to is shown below.

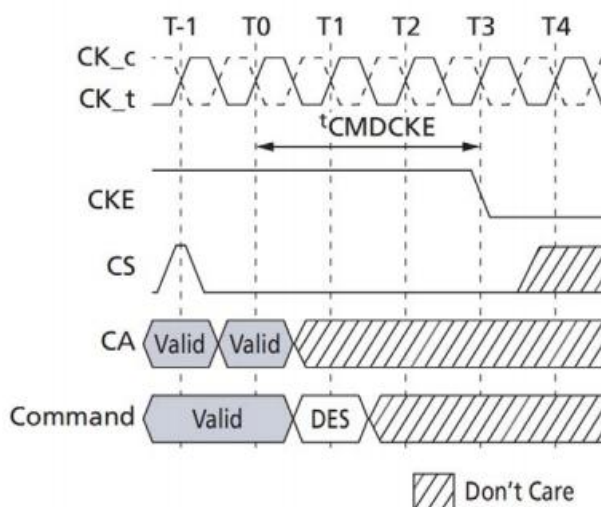


Figure 5 t_{CMDCKE} Timing

[Table 10] Command Address Input Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Command/address valid window (referenced from CA VIL/VIH to CK VIX)	t_{ClVW}	Min	0.3								$t_{CK(AVG)}$	1, 2, 3
Address and control input pulse width (referenced to V REF)	t_{ClPW}	Min	0.55	0.55	0.55	0.6	0.6	0.6	0.6	0.6	$t_{CK(AVG)}$	4

Notes:

- 1.CA Rx mask timing parameters at the pin including voltage and temperature drift.
- 2.Rx differential CA to CK jitter total timing window at the V_{ClVW} voltage levels.
- 3.Defined over the CA internal V REF range. The Rx mask at the pin must be within the internal V REF(CA)range irre-spective of the input signal common mode.
- 4.CA only minimum input pulse width defined at the V CENT_CA(pin mid).

[Table 11] Boot Timing Parameters (10–55 MHz)

Parameter	Symbol	Min/ Max	Value	Unit
Clock cycle time	t_{CKb}	Min	18	ns
		Max	100	
DQS output data access time from CK	t_{DQSCKb}	Min	1.0	ns
		Max	10.0	
DQS edge to output data edge	t_{DQSQb}	Max	1.2	ns

[Table 12] Mode Register Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
MODE REGISTER WRITE (MRW) command period	t_{MRW}	Min	MAX(10ns, 10nCK)				ns
MODE REGISTER SET command delay	t_{MRD}	Min	MAX(14ns, 10nCK)				ns
MODE REGISTER READ (MRR) command period	t_{MRR}	Min	8				$t_{CK(AVG)}$
Additional time after t_{XP} has expired until the MRR command may be issued	t_{MRRI}	Min	$t_{RCD(MIN)} + 3nCK$				ns
Delay from MRW command to DQS driven out	t_{SDO}	Max	MAX(12nCK, 20ns)				ns

[Table 13] Core Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
READ latency (DBI disabled)	RL-A	Min	6	10	14	20	24	28	32	36	tCK(AVG)	
READ latency (DBI enabled)	RL-B	Min	6	12	16	22	28	32	36	40	tCK(AVG)	
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	16	18	tCK(AVG)	
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	30	34	tCK(AVG)	
ACTIVATE-to-ACTIVATE command period (same bank)	t _{RC}	Min	$t_{RAS} + t_{RPab}$ (with all-bank precharge) $t_{RAS} + t_{RPpb}$ (with per-bank precharge)								ns	
Minimum self refresh time (entry to exit)	t _{SR}	Min	MAX(15ns, 3nCK)								ns	
Self refresh exit to next valid command delay	t _{XSR}	Min	MAX(t _{RFCab} + 7.5ns, 2nCK)								ns	
CAS-to-CAS delay	t _{CCD}	Min	8								tCK(AVG)	
CAS-to-CAS delay masked write	t _{CCDMW}	Min	32								tCK(AVG)	
Internal READ-to-PRE-CHARGE command delay	t _{RTP}	Min	MAX(7.5ns, 8nCK)								ns	
RAS-to-CAS delay	t _{RCD}	Min	MAX(18ns, 4nCK)								ns	
Row precharge time (single bank)	t _{RPpb}	Min	MAX(18ns, 3nCK)								ns	
Row precharge time (all banks)	t _{RPab}	Min	MAX(21ns, 3nCK)								ns	
Row active time	t _{RAS}	Min	MAX(42ns, 3nCK)								ns	
		Max	MIN(9 * t _{REFI} * Refresh Rate, 70.2)								μs	
Write recovery time	t _{WR}	Min	MAX(18ns, 4nCK)								ns	
Write-to-read delay	t _{WTR}	Min	MAX(10ns, 8nCK)								ns	
Active bank A to active bank B	t _{RRD}	Min	MAX(10ns, 4nCK)							MAX(7.5ns, 4nCK)	ns	1
Precharge-to-precharge delay	t _{PPD}	Min	4								tCK(AVG)	2
Four-bank activate window	t _{FAW}	Min	40							30	ns	1
Delay from SRE command to CKE input LOW	t _{ESCKE}	Min	MAX(1.75ns, 3nCK)								—	3

Notes:

1.4267 Mb/s timing value is supported at lower data rates if the device is supporting 4266 Mb/s speed grade.

2.Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.

3.Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

4.The refresh rate is determined by the value in MR4 OP[2:0].

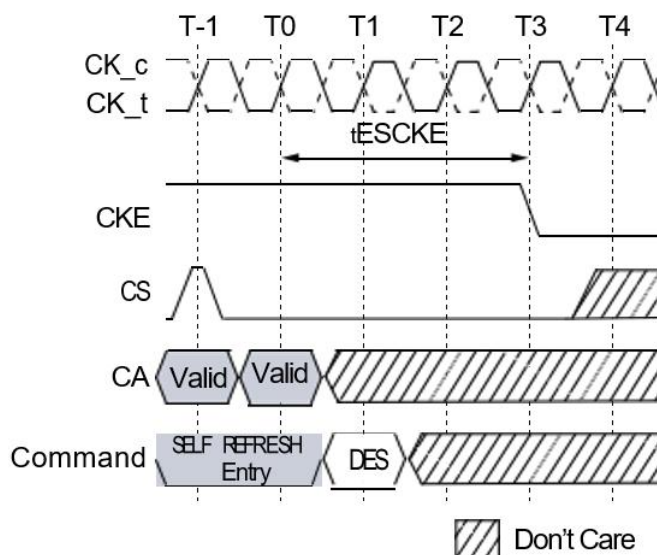


Figure 6:tESCKE Timing

[Table 14] CA Bus ODT Timing

Parameter	Symbol	Min/ Max	Data Rate
			533-4267
CA ODT value update time	tODTUP	Min	RU(20ns/tCK(AVG))

[Table 15] CA Bus Training Parameters

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5nCK)				tCK	
Data setup for V REF training mode	tDStrain	Min	2				ns	
Data hold for V REF training mode	tDHtrain	Min	2				ns	
Asynchronous data read	tADR	Max	20				ns	
CA BUS TRAINING command-to-command delay	tCACD	Min	RU(tADR/tCK)				tCK	1
Valid strobe requirement before CKE LOW	tDQSCKE	Min	10				ns	
First CA BUS TRAINING command following CKE LOW	tCAENT	Min	250				ns	
V REF step time – multiple steps	tVREFca_LONG	Max	250				ns	
V REF step time – one step	tVREF-ca_SHORT	Max	80				ns	

Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
Valid clock requirement before CS HIGH	$t_{CKPRECS}$	Min	$2t_{CK} + t_{XP}$				–	
Valid clock requirement after CS HIGH	$t_{CKPSTCS}$	Min	$MAX(7.5ns, 5nCK)$				–	
Minimum delay from CS to DQS toggle in command bus training	t_{CS_VREF}	Min	2				t_{CK}	
Minimum delay from CKE HIGH to strobe High-Z	$t_{CKEHDQS}$	Min	10				ns	
CA bus training CKE HIGH to DQ tri-state	t_{MRZ}	Min	1.5				ns	
ODT turn-on latency from CKE	$t_{CKELODTon}$	Min	20				ns	
ODT turn-off latency from CKE	$t_{CKEHODToff}$	Min	20				ns	
Exit command bus training mode to next valid command delay	t_{XCBT_Short}	Min	$MAX(200ns, 5nCK)$				–	2
	t_{XCBT_Middle}	Min	$MAX(200ns, 5nCK)$				–	2
	t_{XCBT_Long}	Min	$MAX(250ns, 5nCK)$					2

Notes:

1.If t_{CACD} is violated, the data for samples which violate t_{CACD} will not be available, except for the last sample (where t_{CACD} after this sample is met). Valid data for the last sample will be available after t_{ADR} .

2.Exit command bus training mode to next valid command delay time depends on value of $V_{REF(CA)}$ setting:

MR12 OP[5:0] and $V_{REF(CA)range}$: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in t_{FC} value mapping table. Additionally exit command bus training mode to next valid command delay time may affect $V_{REF(DQ)}$ setting. Settling time of $V_{REF(DQ)}$ level is same as $V_{REF(CA)}$ level.

[Table 16] Asynchronous ODT Turn On and Turn Off Timing

Symbol	800–2133 MHz	Unit
$t_{ODTon(MIN)}$	1.5	ns
$t_{ODTon(MAX)}$	3.5	ns
$t_{ODToff(MIN)}$	1.5	ns
$t_{ODToff(MAX)}$	3.5	ns

[Table 17] Temperature Derating Parameters

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
DQS output access time from CK_t/CK_c (derated)	t_{DQSCKd}	Max	3600				ps
RAS-to-CAS delay (derated)	t_{RCDd}	Min	$t_{RCD} + 1.875$				ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	t_{RCd}	Min	$t_{RC} + 3.75$				ns
Row active time (derated)	t_{RASd}	Min	$t_{RAS} + 1.875$				ns
Row precharge time (derated)	t_{RPd}	Min	$t_{RP} + 1.875$				ns
Active bank A to active bank B (der-ated)	t_{RRDd}	Min	$t_{RRD} + 1.875$				ns

Note:

- At higher temperatures ($>85^{\circ}\text{C}$), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b.

[Table 18] Refresh Requirement Parameters

Parameter	Symbol	8Gb per Channel	Unit
REFRESH cycle time (all banks)	tRFCab	280	ns
REFRESH cycle time (per bank)	tRFCpb	140	ns
per bank refresh to per bank refresh time (different bank)	tPBR2PBR	90	ns

Note:

- This table only describes refresh parameters which are density dependent, Refer to Refresh Requirement section.

3.2 CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

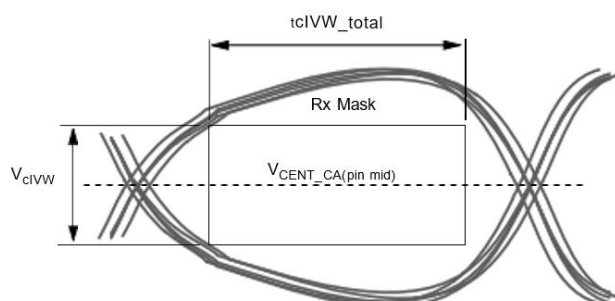


Figure 7: CA Receiver (Rx) Mask

4. CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

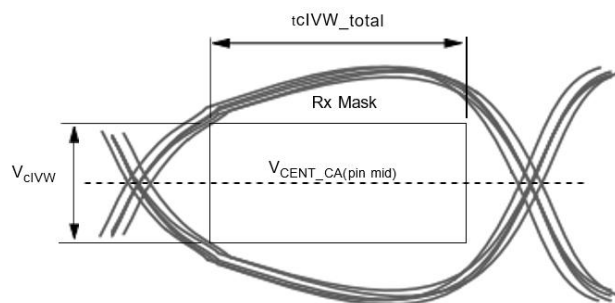


Figure 7: CA Receiver (Rx) Mask

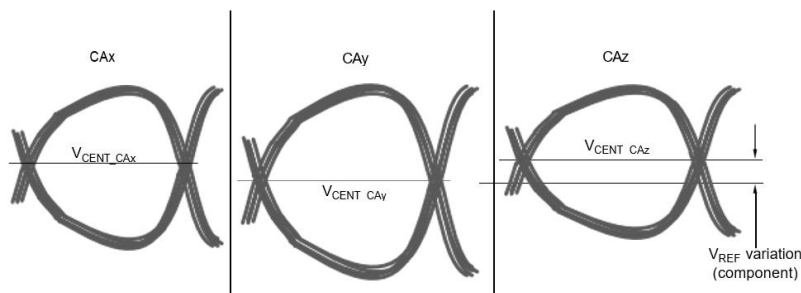


Figure 8: Across Pin $V_{REF (CA)}$ Voltage Variation

$V_{CENT_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{CENT_CA} voltage level and the smallest V_{CENT_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{CENT} level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level V_{REF} will be set by the system to account for RON and ODT settings.

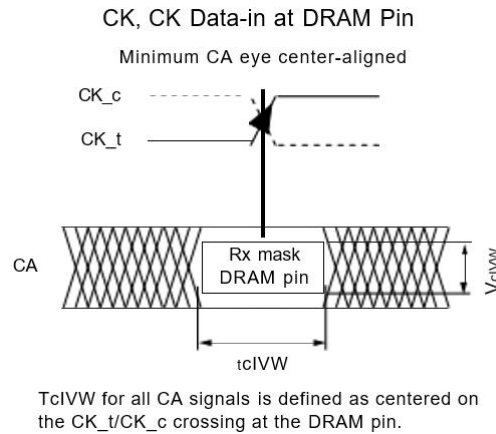


Figure 9: CA Timings at the DRAM Pins

Note:

1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around VCENT_CA(pin mid).

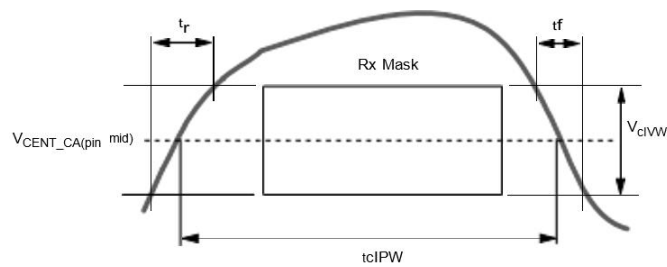


Figure 10: CA 'clPW and SRIN_cIVW Definition (for Each Input Pulse)

Note:

1. $SRIN_cIVW = V_{clVW_total} / (t_r \text{ or } t_f)$; signal must be monotonic within t_r and t_f range.

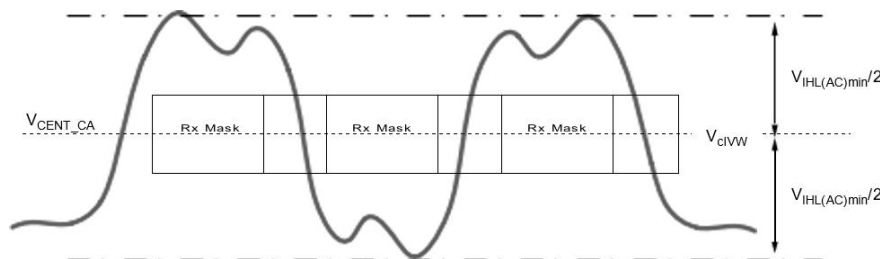


Figure 11: CA V IHL_AC Definition (for Each Input Pulse)

[Table 19] DRAM CMD/ADR, CS

Symbol	Parameter	DQ – 13337		DQ – 1600/1867		DQ – 3200/3733		DQ – 4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V _{clVW}	Rx mask voltage peak-to-peak	–	175	–	175	–	155	–	145	mV	1, 2, 3
V _{IHL(AC)}	CA AC input pulse amplitude peak-to-peak	210	–	210	–	190	–	180	–	mV	4, 6
SRIN _{-clVW}	Input slew rate over V _{clVW}	1	7	1	7	1	7	1	7	V/ns	5

Notes:

- 1.CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
- 2.Rx mask voltage V_{clVW} total(MAX) must be centered around V_{CENT_CA(pin mid)}.
- 3.Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF(CA)} range irrespective of the input signal common mode.
- 4.CA-only input pulse signal amplitude into the receiver must meet or exceed V_{IHL(AC)} at any point over the total UI. No timing requirement above level. V_{IHL(AC)} is the peak-to-peak voltage centered around V_{CENT_CA(pin mid)}, such that V_{IHL(AC)/2 (MIN)} must be met both above and below V_{CENT_CA}.
- 5.Input slew rate over V_{clVW} mask is centered at V_{CENT_CA(pin mid)}.
- 6.V_{IHL(AC)} does not have to be met when no transitions are occurring.
- 7.The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the t_{clVW} (ps) = 450ps at or below 1333 operating frequencies.
- 8.UI = t_{CK(AVG)}MIN.

5. DQ Tx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask (V_{DIVW_total} , T_{DIVW_total}) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

5.1 DRAM Data Timing

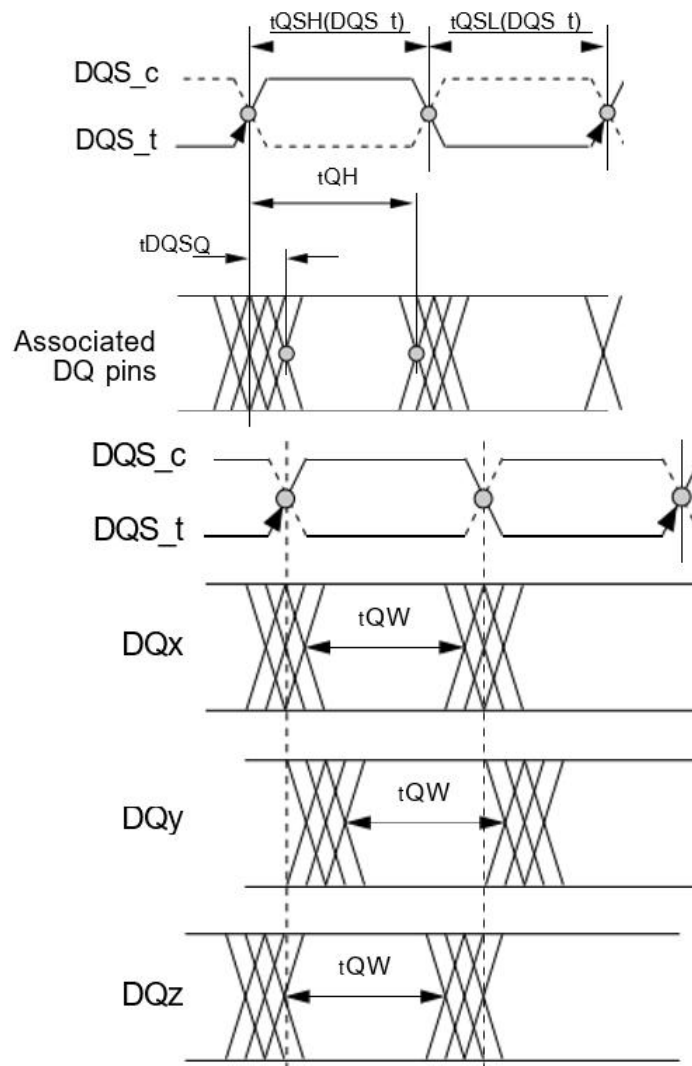


Figure 12: Read Data Timing Definitions – tQH and $tDQSQ$ Across DQ Signals per DQS Group

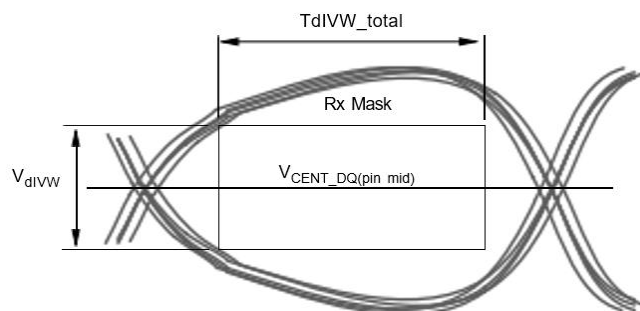


Figure 13: DQ Receiver (Rx) Mask

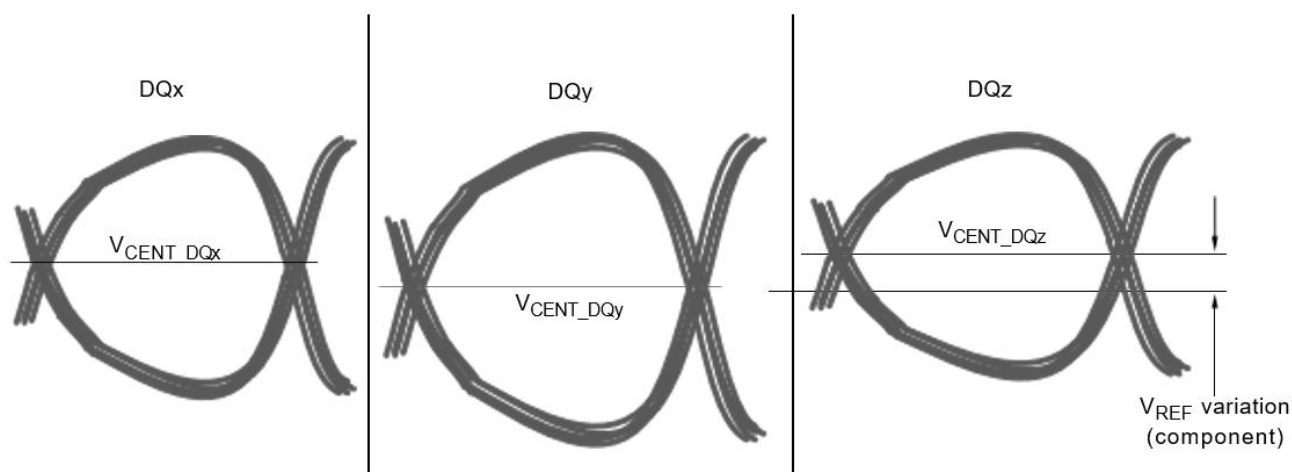


Figure 14: Across Pin VREFDQ Voltage Variation

$V_{CENT_DQ(pin_mid)}$ is defined as the midpoint between the largest V_{CENT_DQ} voltage level and the smallest V_{CENT_DQ} voltage level across all DQ pins for a given DRAM component. Each V_{CENT_DQ} is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component-level V_{REF} will be set by the system to account for RON and ODT settings.

DQS, DQs Data-in Skews at DRAM

Nonminimum data-eye/maximum Rx mask

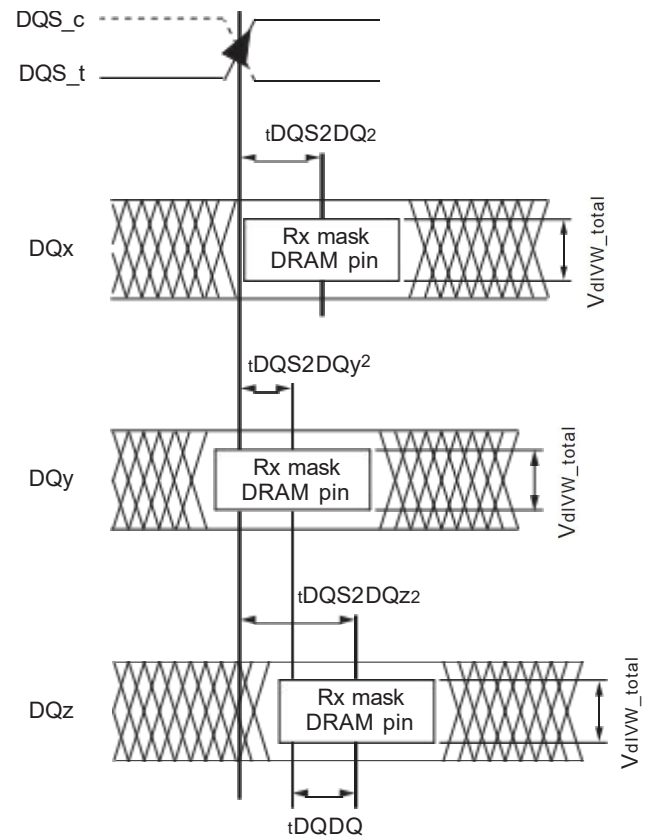


Figure 15: DQ-to-DQS tDQS2DQ and tDQDQ

Notes:

1. These timings at the DRAM pins are referenced from the internal latch.
2. tDQS2DQ is measured at the center (midpoint) of the TdIVW window.
3. DQz represents the MAX tDQS2DQ in this example.
4. DQy represents the MIN tDQS2DQ in this example.

All of the timing terms in DQ to DQS_t are measured from the DQS_t/DQS_c to the center (midpoint) of the TdIVW window taken at the V dIVW_{totalvoltage} levels centered around V CENT_{DQ}(pin_{mid}). In figure above, the timings at the pins are referenced with respect to all DQ signals center-aligned to the DRAM internal latch. The data-to-data offset is defined as the difference between the MIN and MAX ^tDQS2DQ for a given component.

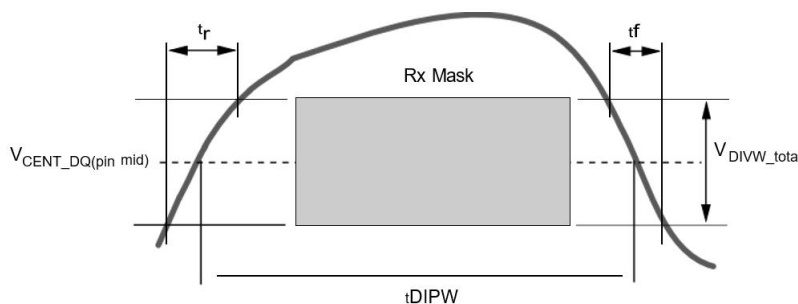
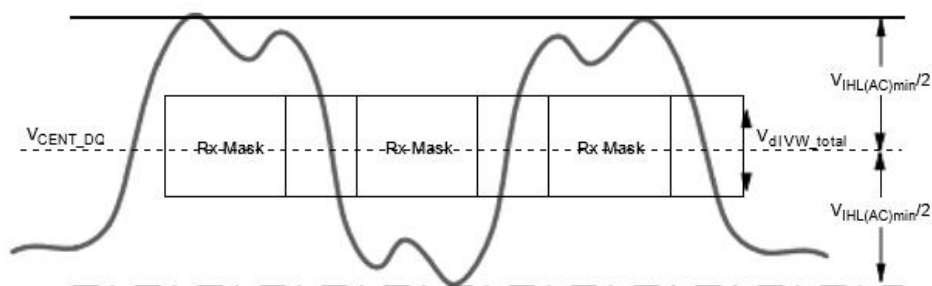


Figure 16: DQ tDIPW and SRIN_dIVW Definition for Each Input Pulse

$$UI = t_{CK}(AVG) \text{ MIN}/2$$

Note:

1. $SRIN_dIVW = V_{dIVW_total} / (t_r \text{ or } t_f)$ signal must be monotonic within t_r and t_f range.



[Table 20] DQs In Receive Mode

Symbol	Parameter	1600/1867		2133/2400		3200/3733		4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{dIVW_total}	Rx mask voltage peak-to-peak	–	140	–	140	–	140	–	120	mV	1, 2, 3
$V_{IHL(AC)}$	DQ AC input pulse amplitude peak-to-peak	180	–	180	–	180	–	170	–	mV	1, 7
$SRIN_dIVW$	Input slew rate over V_{dIVW_total}	1	7	1	7	1	7	1	7	V/ns	6

Notes:

1.Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.

2.Rx mask voltage $V_{dIVW_total}(MAX)$ must be centered around $V_{CENT_DQ}(pin_mid)$.

3. Defined over the DQ internal VREF range. The Rx mask at the pin must be within the internal VREF DQ range irrespective of the input signal common mode.

4.Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design.

5.DQ-only input pulse amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around

$V_{CENT_DQ(pin_mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_DQ} .

6.Input slew rate over V_{dIVW} mask centered at $V_{CENT_DQ(pin_mid)}$.

7. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.

8. $UI = t_{CK(AVG)}(MIN)/2$.

6. Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

[Table 21] Definitions and Calculations

Symbol	Description	Calculation	Notes
$t_{CK}(avg)$ and n_{CK}	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit $t_{CK}(avg)$ represents the actual clock average $t_{CK}(avg)$ of the input clock under operation. Unit n_{CK} represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. $t_{CK}(avg)$ can change no more than $\pm 1\%$ within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$t_{CK}(avg) = [\sum_{j=1}^N t_{CKj}] / N$ Where $N=200$	
$t_{CK}(abs)$	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
$t_{CH}(avg)$	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH}(avg) = [\sum_{j=1}^N t_{CHj}] / (N \times t_{CK}(avg))$ Where $N=200$	
$t_{CL}(avg)$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL}(avg) = [\sum_{j=1}^N t_{CLj}] / (N \times t_{CK}(avg))$ Where $N=200$	
$t_{JIT}(per)$	The single-period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK}(avg)$.	$t_{JIT}(per) = \min / \max \text{ of } [t_{CKi} - t_{CK}(avg)]$ Where $i = 1 \text{ to } 200$	
$t_{JIT}(per), act$	The actual clock jitter for a given system.		
$t_{JIT}(per), allowed$	The specified clock period jitter allowance.		
$t_{JIT}(cc)$	The absolute difference in clock periods between two consecutive clock cycles. $t_{JIT}(cc)$ defines the cycle-to-cycle jitter.	$t_{JIT}(cc) = \max \text{ of } [t_{CKi+1} - t_{CKi}]$	1
$t_{ERR}(nper)$	The cumulative error across n multiple consecutive cycles from $t_{CK}(avg)$.	$t_{ERR}(nper) = [\sum_{j=1}^{i+n-1} t_{CKj}] - (n \times t_{CK}(avg))$	1
$t_{ERR}(nper), act$	The actual clock jitter over n cycles for a given system.		
$t_{ERR}(nper), allowed$	The specified clock jitter allowance over n cycles.		
$t_{ERR}(nper), min$	The minimum $t_{ERR}(nper)$.	$t_{ERR}(nper), min = (1 + 0.68LN(n)) \times t_{JIT}(per), min$	2
$t_{ERR}(nper), max$	The maximum $t_{ERR}(nper)$.	$t_{ERR}(nper), max = (1 + 0.68LN(n)) \times t_{JIT}(per), max$	2
$t_{JIT}(duty)$	Defined with absolute and average specifications for t_{CH} and t_{CL} respectively.	$t_{JIT}(duty), min = \min((t_{CH}(abs), min - t_{CH}(avg), min), (t_{CL}(abs), min - t_{CL}(avg), min)) \times t_{CK}(avg)$ $t_{JIT}(duty), max = \max((t_{CH}(abs), max - t_{CH}(avg), max), (t_{CL}(abs), max - t_{CL}(avg), max)) \times t_{CK}(avg)$	

Notes:

1. Not subject to production testing.
2. Using these equations, $t_{ERR}(nper)$ tables can be generated for each $t_{JIT}(per), act$ value.

6.1 tCK(abs), tCH(abs), and tCL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

[Table 22] tCK(abs), tCH(abs), and tCL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps ¹
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min + tJIT(duty),min ² /tCK(avg),min	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min + tJIT(duty),min ² /tCK(avg),min	tCK(avg)

Notes:

1. tCK(avg),min is expressed in ps for this table.

2. tJIT(duty),min is a negative value.

7. Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter ($t_{JIT(per)}$) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

7.1 Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (t_{RCD} , t_{RP} , t_{RTP} , t_{WR} , t_{WRA} , t_{WTR} , t_{RC} , t_{RAS} , t_{RRD} , t_{FAW}) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support $t_{nPARAM} = RU[t_{PARAM}/t_{CK(avg)}]$. During device operation where clock jitter is outside specification limits, the number of clocks, or $t_{CK(avg)}$, may need to be increased based on the values for each core timing parameter.

7.2 Cycle Time Derating for Core Timing Parameters

For a given number of clocks (t_{nPARAM}), when $t_{CK(avg)}$ and $t_{ERR}(t_{nPARAM})_{act}$ exceed $t_{ERR}(t_{nPARAM})_{allowed}$, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left\lceil \frac{t_{PARAM} + t_{ERR}(t_{nPARAM})_{act} - t_{ERR}(t_{nPARAM})_{allowed} - t_{CK(avg)}}{t_{nPARAM}} \right\rceil, 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

7.3 Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (t_{nPARAM}), clock cycle derating should be specified with $t_{JIT(per)}$.

For a given number of clocks (t_{nPARAM}), when $t_{CK(avg)}$ plus $t_{ERR}(t_{nPARAM})_{act}$ exceed the supported cumulative $t_{ERR}(t_{nPARAM})_{allowed}$, derating is required. If the equation below results in a positive value for a core timing parameter (t_{CORE}), the required clock cycle derating will be that positive value (in calocks)

$$\text{ClockCycleDerating} = RU\left\lceil \frac{t_{PARAM} + t_{ERR}(t_{nPARAM})_{act} - t_{ERR}(t_{nPARAM})_{allowed}}{t_{CK(avg)}} \right\rceil - t_{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

7.4 Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (t_{IS} , t_{IH} , t_{ISb} , t_{IHb}) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the $t_{JIT(per)}$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

7.5 Clock Jitter Effects on READ Timing Parameters

^tRPRE

When the device is operated with input clock jitter, ^tRPRE must be derated by the ^tJIT(per),act,max of the input clock that exceeds ^tJIT(per),allowed,max. Output deratings are relative to the input clock:

$${}^t\text{RPRE}(\text{min,derated}) = 0.9 - \left[\frac{{}^t\text{JIT}(\text{per}),\text{act,max} - {}^t\text{JIT}(\text{per}),\text{allowed,max}}{{}^t\text{CK}(\text{avg})} \right]$$

For example, if the measured jitter into a LPDDR4 device has ^tCK(avg) = 625ps, ^tJIT(per),act,min = -xx, and ^tJIT(per),act,max = +xx ps, then ^tRPRE,min,derated = 0.9 - (^tJIT(per),act,max - ^tJIT(per),allowed,max)/^tCK(avg) = 0.9 - (xx - xx)/xx = yy ^tCK(avg).

^tLZ(DQ),^tHZ(DQ),^tDQSCK,^tLZ(DQS),^tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DMn or DQm, where: n= 0,1; and m= 0–15, and specified timings must be met with respect to that clock edge. Therefore, they are not affected by ^tJIT(per).

^tQSH,^tQSL

These parameters are affected by duty cycle jitter, represented by ^tCH(abs)min and ^tCL(abs)min. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = MIN {^tQSH (abs)min - ^tDQSQmax), (^tQs L(abs)min - ^tDOSQmax)}

This minimum data valid window must be met at the target frequency regardless of clock jitter.

^tRPST

^tRPST is affected by duty cycle jitter, represented by ^tCL(abs). Therefore, ^tRPST(abs)min can be specified by ^tCL(abs)min. ^tRPST(abs)min = ^tCL(abs)min - 0.05 = ^tQSL(abs)min.

7.6 Clock Jitter Effects on WRITE Timing Parameters

^tDS,^tDH

These parameters are measured from a data signal (DMIn or DQm, where n= 0, 1 and m= 0–15) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: n = 0,1) crossing. The specification values are not affected by the amount of ^tJIT(per) applied, because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^tDSS,^tDSH

These parameters are measured from a data signal (DQS_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^tJIT(per)act of the input clock in excess of the allowed period jitter ^tJIT(per)allowed.

^tDQSS

^tDQSS is measured from a data strobe signal (DQSn_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual ^tJIT(per),act of the input clock in excess of ^tJIT(per)allowed.

$$tDQSS(\text{min}, \text{derated}) = 0.75 - \left[\frac{tJIT(\text{per}), \text{act}, \text{mti}(\text{per}) - tJIT(\text{per}), \text{allowed}, \text{min}}{CK(\text{avg})} \right]$$

$$tDQSS(\text{max}, \text{derated}) = 1.25 - \left[\frac{tJIT(\text{per}), \text{act}, \text{max} - tJIT(\text{per}), \text{allowed}, \text{max}}{tckl(\text{oavg})} \right]$$

For example, if the measured jitter into an LPDDR4 device has $tCK(\text{avg}) = 625\text{ps}$, $tJIT(\text{per}), \text{act}, \text{min} = -xx\text{ps}$, and $tJIT(\text{per}), \text{act}, \text{max} = +xx\text{ps}$, then:

$$tDQSS(\text{min}, \text{derated}) = 0.75 - (-xx + yy)/625 = \text{xxxx } tCK(\text{avg})$$

$$tDQSS(\text{max}, \text{derated}) = 1.25 - (xx - yy)/625 = \text{xxxx } tCK(\text{avg})$$

8. Marking

1 Row: BIWIN Logo

2 Row: Sales Item P/N

3 Row: LOT No. + Serial Number



Renderings, for reference only(Industrial)



Renderings, for reference only(Automotive)