XTM4220

H-Bridge Motor Driver

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18V1.5A Single Channel H-Bridge Motor Driver

GENERAL DESCRIPTION

The XTM4220 is an integrated motor driver with four N-channel power FETs, charge pump regulator, and protection circuitry. The charge pump integrates all capacitors to reduce the overall solution size of the motor driver on a PCB and allows for 100% duty cycle operation.

The XTM4220 supports multiple control interface modes including: PWM (IN1/IN2), phase/enable (PH/EN), independent half-bridge, and parallel half-bridge. Each interface supports a low-power sleep mode to achieve ultra-low quiescent current draw by shutting down most of the internal circuitry.

The device can supply up to 1.5 A of continuous output current. It operates with a supply voltage from 3.7 to 18 V. The driver offers internal protection features include supply undervoltage lockout (UVLO), output overcurrent (OCP), and device overtemperature (TSD).

FEATURES

- 3.7V to 18V operating supply voltage range
- High output current capability:
  - Full-bridge: 1.5-A continuous
  - Half-bridge: 1.5-A continuous per output
  - Parallel half-bridge: 3-A continuous
- N-channel H-bridge motor driver
  - MOSFET on-resistance (HS + LS): 0.53 Ω
  - Drives one bidirectional brushed DC motor
  - Two unidirectional brushed DC motors
  - One single- or dual-coil latching relay
  - Push-pull and bistable solenoids
  - Other resistive, inductive, or LED loads
- Multiple interfaces for flexibility and reduced GPIO
- Standard PWM Interface (IN1/IN2)
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Ultra low-power sleep mode
  - 600 nA @ V_M = 12 V, T_J = 25°C
  - Timed autosleep mode to reduce GPIO
- Protection features
  - Undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
- RoHS Compliant and 100% Lead (Pb)-Free
- DFN 2x2-8L Package

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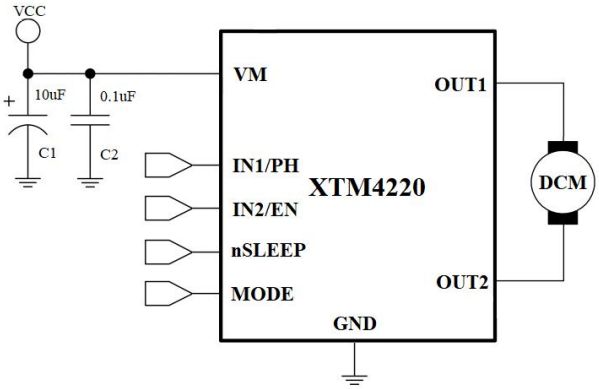
APPLICATIONS

- Video Security Cameras
- Brushed DC motor, solenoid, & relay driving
- Water, gas, & electricity meters
- IP network camera IR cut filter
- Video doorbell
- Machine vision camera
- Circuit breakers
- Electronic smart lock
- Electronic and robotic toys
- Blood pressure monitors
- Infusion pumps
- Electric toothbrush
- Beauty & grooming

APPLICATION SCHEMATIC



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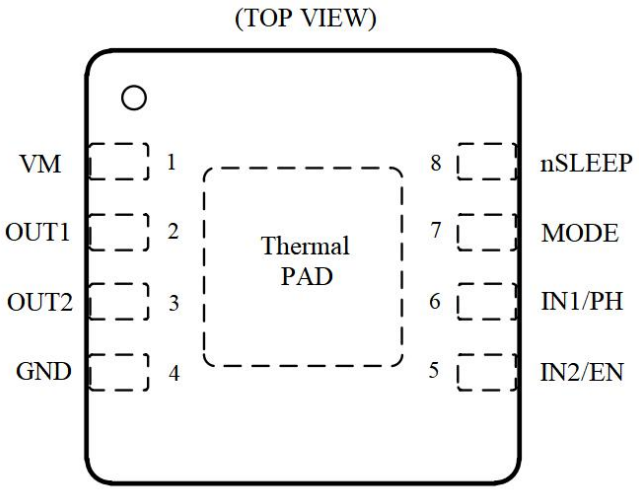
PIN CONFIGURATIONS



NAME	NO.	TYPE	DESCRIPTION
VM	1	P	Power Supply
OUT1	2	O	H-Bridge Output 1
OUT2	3	O	H-Bridge Output 2
GND	4	G	GND
IN2/EN	5	I	Control Logic Input
IN1/PH	6	I	Control Logic Input
MODE	7	I	H-bridge control input mode
nSLEEP	8	I	Sleep mode input.
Thermal PAD	-	G	Thermal pad Connect to GND

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PACKAGE/ORDERING INFORMATION

Part Number	Package	Qty/TR	Operating Temperature Range
XTM4220AD3CT	DFN2*2-8L	3000	-40°C~85°C

ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
Power Supply	V_M	-0.5	20.0	V
Output Current (Peak)	I_{PEAK}	0	2.2	A
Input Logic Voltage	$V_{IN1/PH}$,$V_{IN2/EN}$,V_{nSLEEP},V_{MODE}	-0.5	5.5	V
ESD (HBM)	ESD	2000	-	V
Operating Temperature	T_{OPR}	-40	125	°C
Storage Temperature	T_{stg}	-65	150	°C
Junction Temperature	T_j	-40	150	°C

RECOMMENDED OPERATING CONDITIONS（Unless otherwise noted, Ta=25°C）

Parameter		Min	Max	Unit
Power Supply	V_M	3.7	18	V
Input Logic Voltage	$V_{IN1/PH}$,$V_{IN2/EN}$,V_{nSLEEP},V_{MODE}	0	5	V
Output Current (continuously)	I_{OUT}	0	1.5	A
Input PWM Frequency	f_{PWM}	0	100	KHz

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ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_M=12V, Ta=25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
I_{MQ}	Standby Current	MODE=nSLEEP=L, noload	-	-	1	uA
I_M	Operating Current	INx=50KHz PWM, nSLEEP=H, no load	-	0.5	0.8	mA
t_{WAKE}	Turn-on time	Sleep mode to active mode delay	-	-	80	μs
$t_{AUTOSLEEP}$	Autosleep turn-off time	Active mode to autosleep mode delay,nSLEEP=3.3V	0.5	-	2.5	ms
t_{SLEEP}	Turn-off time	Active mode to sleep mode delay,nSLEEP =0V	-	1	-	μs
INPUT LOGIC						
V_{INH}	Input High Voltage		1.5	-	5.5	V
V_{INL}	Input Low Voltage		-	-	0.6	V
I_{INH}	Input High Current	V_{INx}=3.3V	20	-	50	uA
I_{INL}	Input Low Current	V_{INx}=0V	-	0	-	μA
R_{IN}	Pulldown resistance		-	100	-	KΩ
TRI-LEVEL INPUTS (MODE)						
V_{TIL}	Tri-level input logic low voltage		0	-	0.23 ×V_{nSLEEP}	V
V_{TIZ}	Tri-level input Hi-Z voltage	R_I = Hi-Z	0.6 ×V_{nSLEEP}	-	0.675×V_{nSLEEP}	V
V_{TIH}	Tri-level input logic high voltage		0.74 ×V_{nSLEEP}	-	5	V
R_{TPD}	Tri-level pull down resistance	to GND, sleep mode	-	1	-	MΩ
		to GND, active mode	-	130	-	KΩ
R_{TPU}	Tri-level pull up resistance	to nSLEEP buffered reference	-	75	-	kΩ

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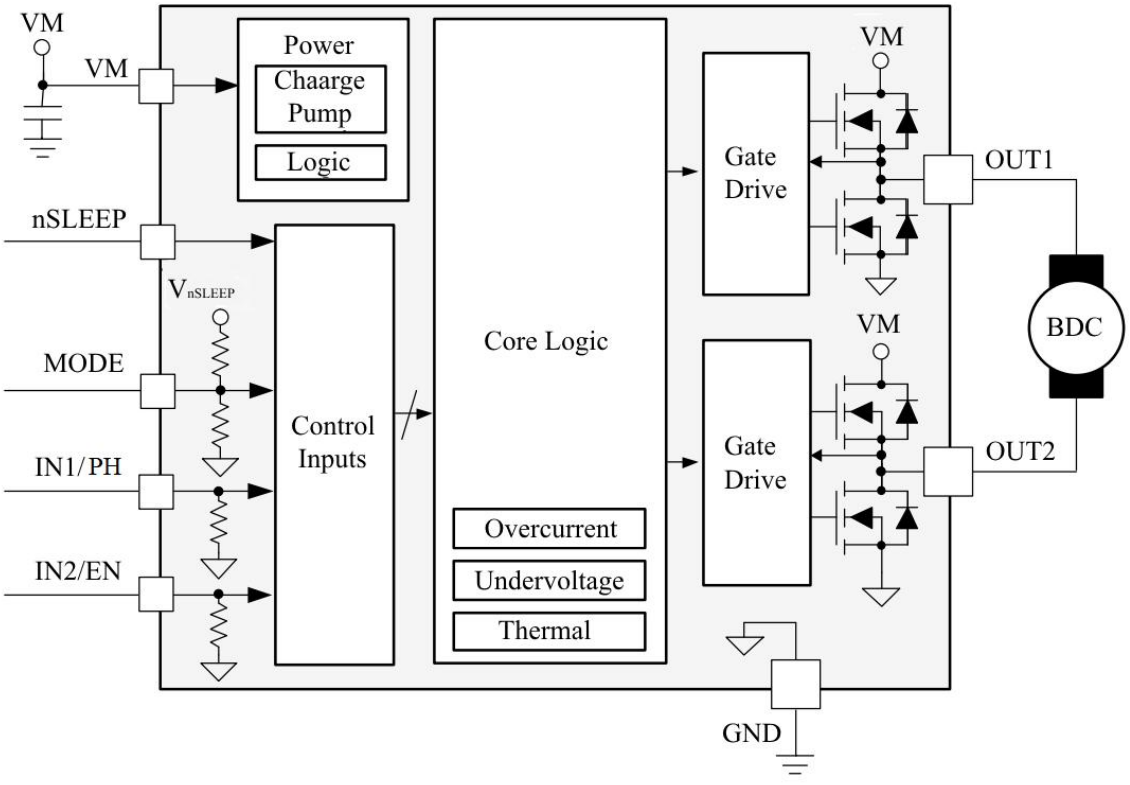
H-Bridge FETs						
$R_{DS(ON)}$	HS+LS FETs on-resistance	I_{LOAD}=0.5A, HS+LS	-	0.53	0.75	Ω
t_{RISE}	Output rise time	V_{OUTx} rising from 10% to 90% of V_{VM}	-	150	-	ns
t_{FALL}	Output fall time	V_{OUTx} falling from 90% to 10% of V_{VM}	-	150	-	ns
t_{PD}	Input to output propagation delay	Input crosses 0.8 V to V OUTx = 0.1×V_{VM}, I_O = 1 A		150		ns
t_{DEAD}	Output dead time	Internal dead time	-	300	-	ns
PROTECTION CIRCUITS						
T_{TSD}	Thermal shutdown temperature		-	160	-	℃
T_{HYS}	Thermal shutdown hysteresis		-	20	-	℃
V_{UVLO}	VM supply under-voltage lockout		-	3	-	V
$V_{UVLOHYS}$	Supply UVLO hysteresis		-	100	-	mV
I_{OCP}	Overcurrent protection trip point		2.2	-	-	A

BLOCK DIAGRAM



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1 DETAILED DESCRIPTION

XTM4220 is an integrated H-bridge driver with multiple control interface options: PWM (IN1/IN2) interface, PH/EN, or half-bridge interface. To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and its capacitors. XTM4220 support a timed auto-sleep mode which reduces microcontroller GPIO connections by eliminating a disable/sleep pin and automatically putting the device into a low-power sleep mode when the inputs remain inactive for 1-2 ms. When using autosleep for PWM or PH/EN mode, the nSLEEP pin may be tied high. The nSLEEP pin allows the device to be put to sleep in half-bridge mode where autosleep is not available.

The PWM interface is a standard 2-pin (IN1/IN2) motor drive interface. The PH/EN interface allows bi-directional PWM control using only one PWM resource from the controller. PWM and PH/EN interfaces can drive loads like brushed DC motors and bistable relays bidirectionally. Independent half-bridge mode allows for full control over each half-bridge. The half-bridges can independently control two loads with each channel acting as a high-side or low-side driver with half of the $R_{DS(ON)}$ of full-bridge driving. Alternatively, half-bridge mode also allows the inputs and outputs to be connected together, or "paralleled," to drive a single load as a high-side or low-side driver with one-forth the $R_{DS(ON)}$ of full-bridge driving.

The integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

2 Control Modes Description

The XTM4220 provides three modes to support different control schemes with the PH/IN1 and EN/IN2 pins. The MODE pin selects the control interface mode by setting it either logic low, logic high, or Hi-Z as shown in the table below. The MODE pin does not latch its state, so it may be changed during operation.

MODE PIN Functions

MODE STATE	CONTROL MODE
MODE = Logic Low	PWM
MODE = Logic High	PH/EN
MODE = Hi-Z	Half-Bridge

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The inputs can accept DC or pulse-width modulated (PWM) voltage signals with duty cycles from 0% to 100%. By default, the INx, PH/IN1, and EN/IN2 pins have internal pull-down resistors to ensure the outputs are Hi-Z if no inputs are present (the only exception is half-bridge mode, where OUTx = L if INx is floating).

The following sections show the truth tables for each control mode. Additionally, the XTM4220 automatically handles the dead-time generation when switching between the high-side and low-side MOSFET of a half-bridge. Figure 1 describes the naming and configuration for the various H-bridge states described in the following sections.

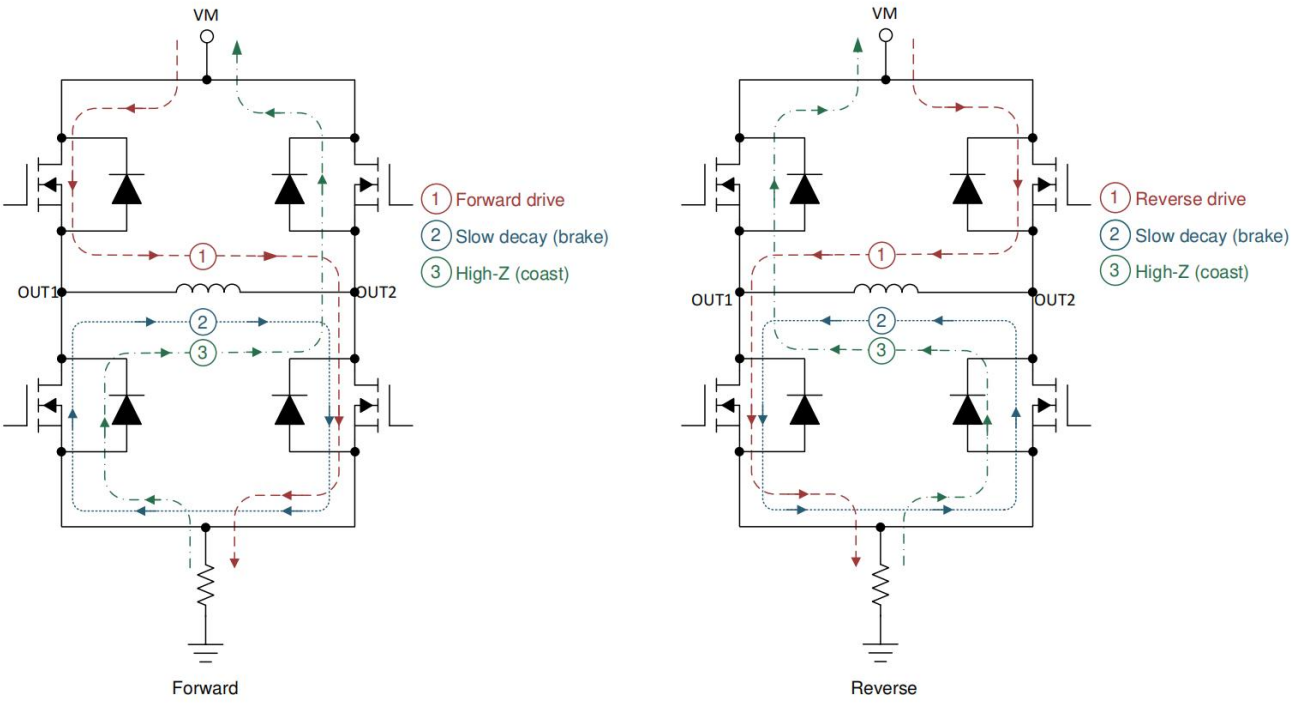

Figure 1. H-bridge states

2.1 PWM Control Mode(MODE=0)

The PWM interface (IN1/IN2) controls the OUTx pins according to the logic table in Table 1-1. Setting the MODE pin logic low selects PWM mode. The coast/Hi-Z state doubles as an automatic sleep mode. After staying in the coast/Hi-Z state for t_{SLEEP}, the device will automatically go into low-power sleep mode (autosleep).

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nSLEEP	IN1	IN2	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Low-power sleep mode
1	0	0	Hi-Z	Hi-Z	Coast (H-bridge Hi-Z)/ low-power automatic sleep mode
1	0	1	L	H	Reverse (OUT2 → OUT1)
1	1	0	H	L	Forward (OUT1 → OUT2)
1	1	1	L	L	Brake (low-side slow decay)

Table 1-1. PWM control mode with automatic sleep and sleep pin

2.2 PH/EN Control Mode(MODE=1)

When the MODE pin is logic high on power up, the device selects "phase-enable" mode (PH/EN). PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. Table 1-2 shows the truth table for PH/EN mode. When the EN pin is low, the device enters brake mode. This allows the controller to use a single PWM generator peripheral on the EN pin while a standard GPIO pin controls directions using the PH pin. However, if the EN pin remains low for longer than t_{SLEEP}, the device goes into low-power sleep mode and the outputs are disabled.

nSLEEP	EN	PH	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Low-power sleep mode (H-Bridge Hi- Z)
1	0	X	L → Hi-Z	L → Hi-Z	Brake (low-side slow decay) for tSLEEP, then auto-sleep mode (H- bridge Hi-Z)
1	1	0	L	H	Reverse (OUT2 → OUT1)
1	1	1	H	L	Forward (OUT1 → OUT2)

Table 1-2. PH/EN control mode

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2.3 Half-Bridge Control Mode(MODE=Hi-Z)

When the MODE pin is floating (Hi-Z), selects the half-bridge control mode. This mode allows for each half- bridge to be directly controlled in order to support high-side slow decay (or brake), driving two independent loads, or paralleling the outputs for higher current capability for a single load. Table 1-3 shows the truth table for independent half-bridge mode. Because this mode does not have an autosleep state, the nSLEEP pin must be used to bring the device in and out of sleep mode.

nSLEEP	EN	PH	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Low-power sleep mode
1	0	X	L	X	OUT1 low-side On
1	1	X	H	X	OUT1 high-side On
1	X	0	X	L	OUT2 low-side On
1	X	1	X	H	OUT2 high-side On

Table 1-3. Half-bridge control mode

2.4 Low-Power Sleep Mode

The XTM4220 supports a low-power sleep mode to reduce current consumption from VM when the driver is not active. In low-power sleep mode, the device draws minimal current denoted by I_{VMQ}. There are two ways to enter low-power sleep mode : autosleep and using the nSLEEP pin. Table1-4 describes how to enter low-power sleep mode.

Input pin state	OUT1	OUT2	Description
MODE = 0, IN1 = IN2 = 0	Hi-Z	Hi-Z	Autosleep for PWM interface: Upon entering this state, the outputs are disabled. The device remains in Active Mode for t_{SLEEP}, then goes into low-power mode.
MODE = 1, EN = 0	L → Hi-Z	L → Hi-Z	Autosleep for PH/EN interface: Upon entering this state, both outputs go into brake mode by turning the low-side FETs on. The device remains in this state for t_{SLEEP}, then goes into low-power mode. Once in low-power mode, the outputs are disabled.
nSLEEP = 0	Hi-Z	Hi-Z	Sleep pin: When the nSLEEP pin goes low, the outputs are disabled, and the device goes into low-power sleep mode immediately.

Table 1-4. XTM4220 sleep mode summary

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The device returns to active mode when the input pins move to a state other than the ones in table 1-4. To wake up the device from autosleep mode, the INx pins or EN pin (depending on MODE state and package variant) must be asserted high for longer than t_{WAKE} before receiving PWM input signals. When using the nSLEEP pin, nSLEEP must be asserted high longer than t_{WAKE} and the INx or EN pins must not be in an autosleep state.

XTX recommends tying the nSLEEP pin to the logic supply rail when using autosleep in PWM or PH/EN interface modes. For applications where a microcontroller controls nSLEEP, designers must ensure that nSLEEP is not floating while VM > V_{UVLO}. This may cause unintended outputs, depending on the state of the MODE, IN1/PH, and IN2/EN pins. If this condition may occur in the system, then XTX recommends using a 100 kΩ pulldown resistor on nSLEEP.

2.5 Mode Pin Tri-Level Input

Figure 2 shows the input structure for the tri-level input pin, MODE. The MODE pin references its input state to the voltage of the nSLEEP pin to determine logic high, logic low, or high-impedance (Hi-Z) input states. However, these internal resistors do not draw current from the sleep pin when the device is in autosleep mode. This helps to reduce overall current draw from the device when in sleep mode.

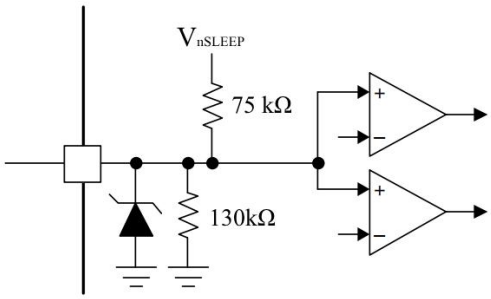

Figure 2. MODE tri-level input

3 APPLICATION INSTRUCTIONS

3.1 Application Information

The XTM4220 can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, bistable latching relays, and actuators. These devices can also drive many common passive loads such as LEDs, resistive elements, relays, etc. This section highligts some application examples for the XTM4220.

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3.2 Typical Application

3.2.1 Full-Bridge Driving

A typical application for the XTM4220 is to drive a brushed DC motor or single-coil latching relay bidriectionally (in forward and reverse) using the outputs as a full-bridge, or H-bridge, configuration. Figure 3 show examples for driving a motor with the PWM interface. Figure 4 shows an example of driving a single-coil latching relay with the PWM interface. Figure 5 shows an example of driving a motor with the PH/EN interface.

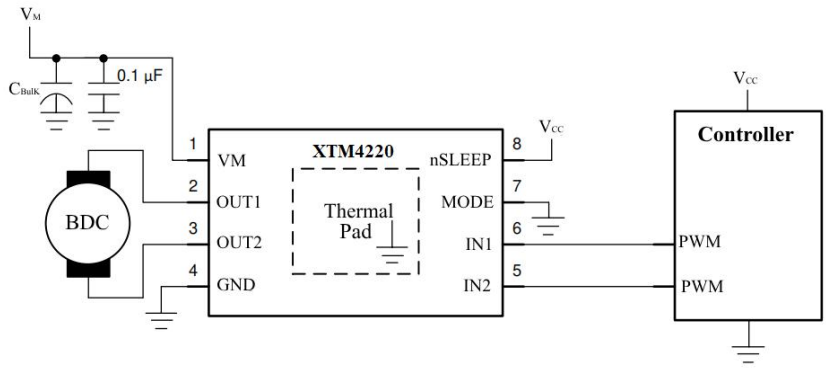

Figure 3. PWM interface motor-driving application

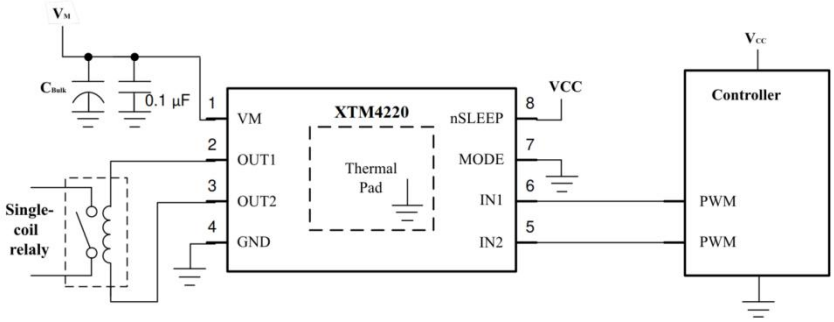

Figure 4. PWM interface single-coil latching relay application

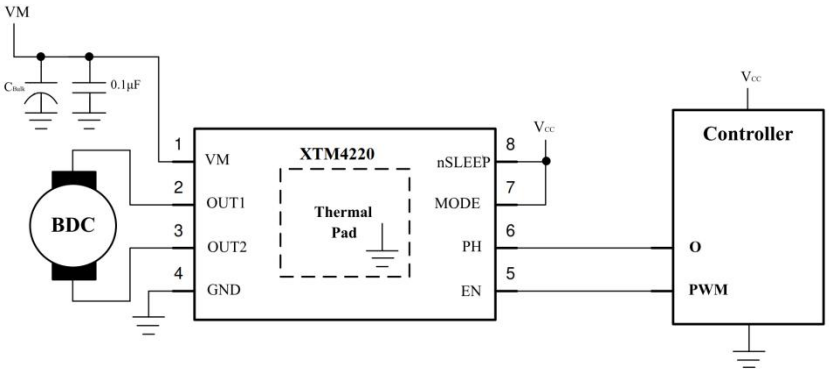

Figure 5. PH/EN interface motor-driving application

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3.2.2 Half-Bridge Driving

The XTM4220 can be configured to half-bridge mode by leaving the MODE pin floating. In this mode, the device outputs can be used as low-side or high-side drivers. This allows the device to drive various loads such as one or two motors unidirectionally (only in one direction), solenoids, valves, and relays. Figure 6 shows the device used as a low-side driver on OUT1 and high-side driver on OUT2. Both loads may also be driven from the high-side or from the low-side. By tying the INx pins together and OUTx pins together, as shown in Figure 7 and Figure 8, the device can drive a single load with half of the $R_{DS(ON)}$. This can accommodate larger current requirements. This configuration is called "parallel half-bridge mode."

In half-bridge mode, the other FETs and body diodes in the half-bridge will recirculate freewheeling current during the off-time of the PWM duty cycle, so extra external diodes are not needed.

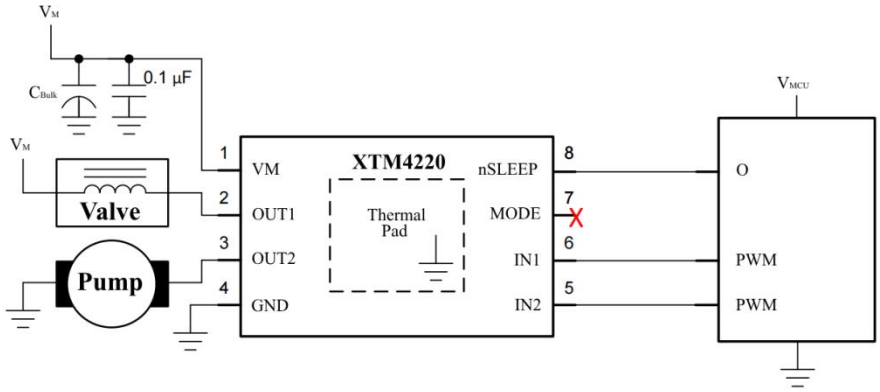

Figure 6. Half-bridge mode used as a high-side and low-side driver for two load

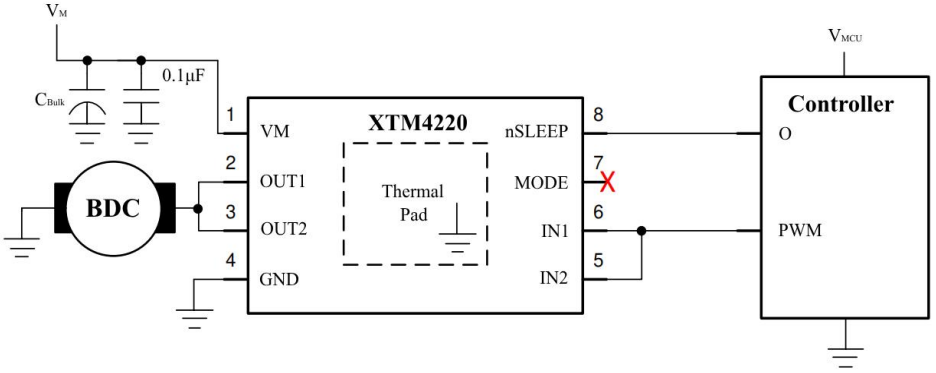

Figure 7. Half-bridge mode used as a high-side driver with outputs paralleled

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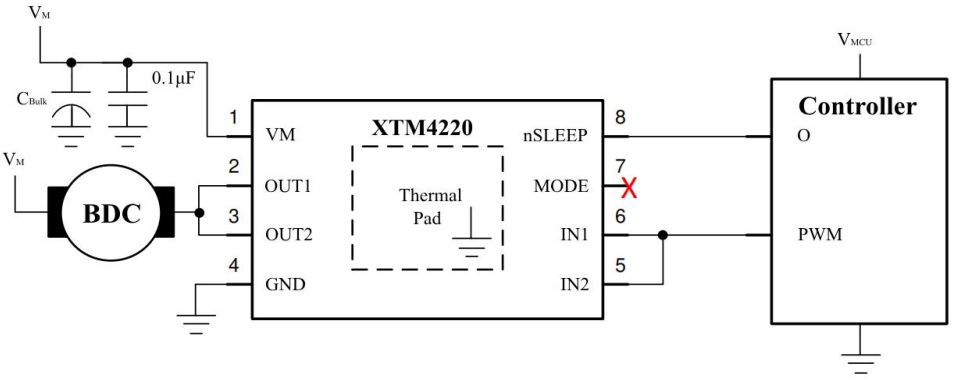

Figure 8. Half-bridge mode used as a low-side driver with outputs paralleled

3.2.3 Dual-Coil Relay Driving

The PWM interface may also be used to drive a dual-coil latching relay. The figures 9 in this section show example schematics.

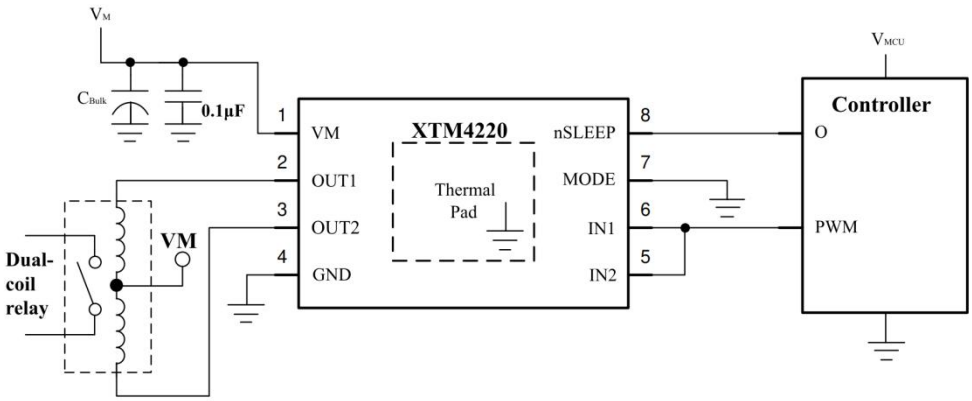

Figure 9. Dual-coil relay driving

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4 Detailed Design Procedure

4.1 Supply Voltage

The appropriate supply voltage depends on the ratings of the load (motor, solenoid, relay, etc.). In the case of a brushed DC motor, the supply voltage will impact the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive windings of a motor, solenoid, or relay.

4.2 Control Interface

XTX recommends connecting the the MODE pin directly to the GND net as shown in Figure 3. However, if other interface states are required in the application, the MODE pin may be connected to a GPIO pin to select the other interface options during operation.

The autosleep feature allows for bidirectional control of the motor and low-power mode using only two pins. This eliminates the need for another GPIO to control a sleep pin.

4.2.1 Full-Bridge Driving Control

The following table lists the signals used as reference in PWM control mode.

IN1	IN2	Function
PWM	0	Forward,Fast decay
1	PWM	Forward,Slow decay
0	PWM	Reverse,Fast decay
PWM	1	Reverse,Slow decay

Positive correlation between motor speed and D(duty cycle).

Connecting the MODE pin to the microcontroller supply selects the PH/EN interface. PH/EN mode helps to reduce the number of microcontroller PWM generators needed for motor driving by toggling only the EN pin. The PH pin controls the direction of motor driving with this interface. The device will enter sleep mode if EN is held low for longer than t SLEEP.

The following table lists the signals used as reference in PH/EN control mode.

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EN	PH	Function
PWM	0	Forward,low-side slow decay,then auto-sleep mode
PWM	1	Reverse,low-side slow decay,then auto-sleep mode

4.2.2 Half-Bridge Driving Control

The XTM4220 can be configured to half-bridge mode by leaving the MODE pin floating. In this mode, the device outputs can be used as low-side or high-side drivers. This allows the device to drive various loads such as one or two motors unidirectionally (only in one direction), solenoids, valves, and relays. Independent half-bridge mode,as Figure 8,shows the device used as a low-side driver on OUT1 and high-side driver on OUT2. By changing INx=H/L to control the H/L side NMOS of OUTx ON.

By tying the INx pins together and OUTx pins together, as shown in Figure 9 and Figure 10, the device can drive a single load with half of the $R_{DS(ON)}$. This can accommodate larger current requirements. This configuration is called "parallel half-bridge mode."

In half-bridge mode, the other FETs and body diodes in the half-bridge will recirculate freewheeling current during the off-time of the PWM duty cycle, so extra external diodes are not needed.

4.2.2.1 Half-Bridge Low-Power Operation

Bringing nSLEEP to 0 V puts the XTM4220 to sleep in half-bridge mode. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power. To wake up the XTM4220 in half-bridge mode, bring nSLEEP high, then set IN1 or IN2 high for longer than t WAKE before returning low or sending a PWM signal.

To minimize leakage current into the OUTx pins (especially in battery-powered applications), connect the load from OUTx to GND. As mentioned earlier, connecting the load from OUTx to VM is also possible, but there may be some small leakage current into OUTx when it is disabled. No leakage current is expected if loads are connected in H-bridge configuration.

4.2.3 Dual-Coil Relay Driving

The PWM interface may also be used to drive a dual-coil latching relay as Figure 9.

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4.2.3.1 Control Interface

The PWM interface can be used to drive dual-coil relays.Figure 10 and Figure 11 show a schematic and timing diagram for driving a dual-coil relay with the PWM interface.

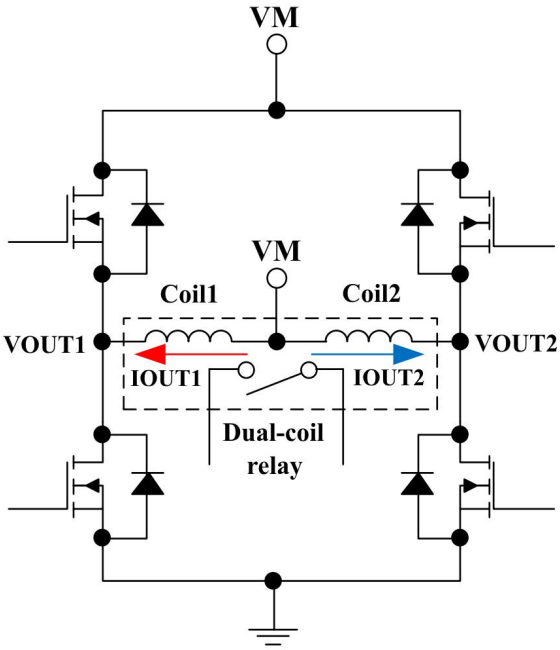

Figure 10. Schematic of dual-coil relay driven by the OUTx H-bridge

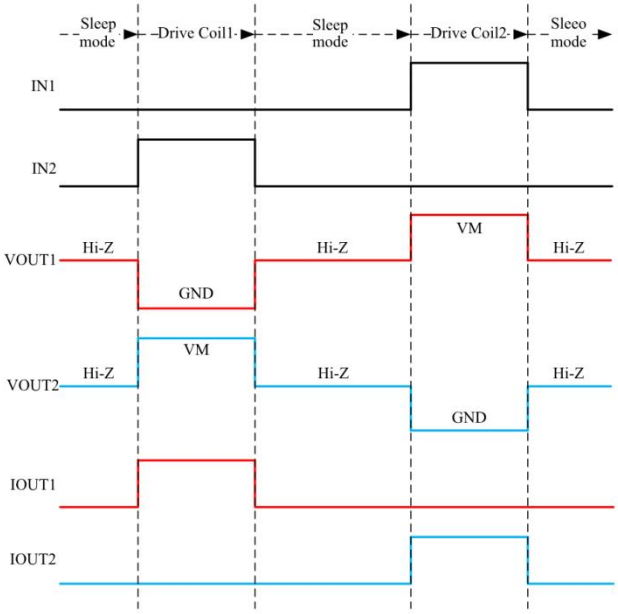

Figure 11.Timing diagram for driving a dual-coil relay with PWM interface

The following table shows the logic table for the PWM interface. The descriptions in this table reflect how the input and output states drive the dual coil relay. When Coil1 is driven (OUT1 voltage is at GND), The voltage at OUT2 will go to VM. Because the center tap of the relay is also at VM, no current flows through Coil2. The same is true when Coil2 is driven; Coil1 shorts to VM. The body diodes of the high-side FETs act as freewheeling diodes, so extra external diodes are not needed.

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Outputs disabled (H-Bridge Hi-Z)
0	1	L	H	Drive Coil1
1	0	H	L	Drive Coil2
1	1	L	L	Drive Coil1 and Coil2 (invalid state for a dual-coil latching relay)

18V1.5A Single Channel H-Bridge Motor Driver

APPLICATION CIRCUIT NOTE

1.The operating condition over the absolute parameters of the chip is not allowed

2.Don’t short the two outputs or the power supply and ground. If the peak current is too high, the IC will be burned

3.If the motor exceeds the peak current designed by the IC when locked, the IC will also be damaged

4.The bypass capacitor of VM should be as close to the VM pin of the chip as possible

5.The ground wire connecting the motor needs to be isolated in the layout

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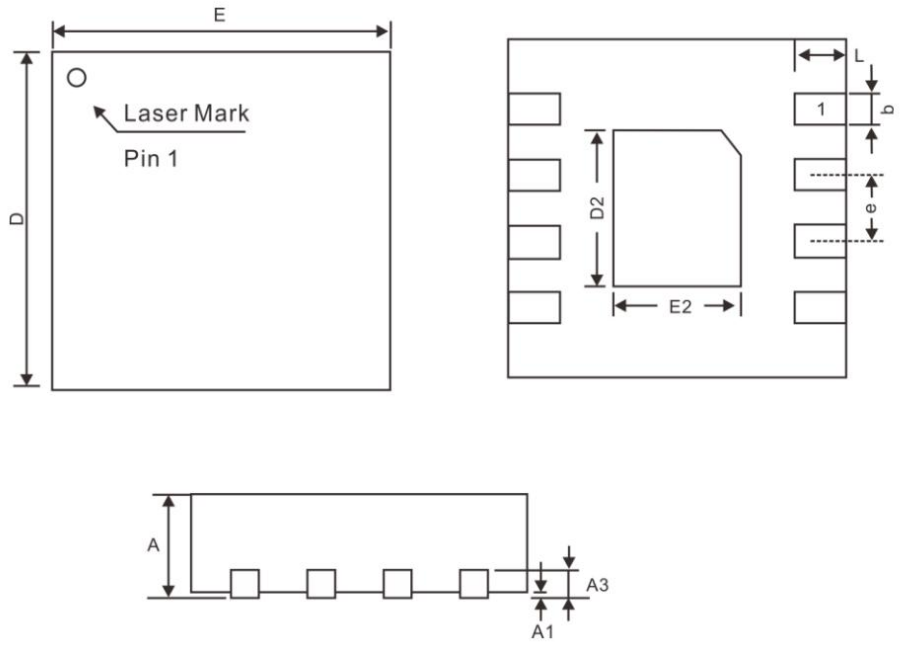
PACKAGE INFORMATION

DFN2*2-8L



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D		2.00BSC	
E		2.00BSC	
e		0.50BSC	
D2	1.50	1.60	1.65
E2	0.80	0.90	0.95
L	0.25	0.30	0.35

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REVISION HISTORY

Number	Date	Description
Rev 0.0	2024/01	XTM4220 datasheet release