钍地半导体
Tudi Semiconductor

Product Specification

TUDI-ADM4850-ADM4857

5 V, Slew Rate Limited, Half-Duplex and Full Duplex RS-485/RS-422 Transceivers

网址 www.sztdbdt.com

用芯智造·卓越品质

semiconductor device manufacturer

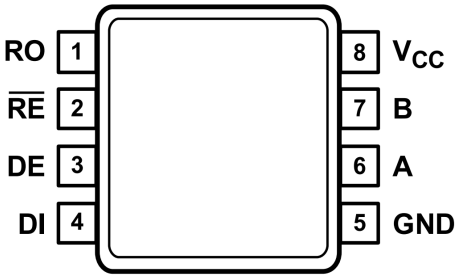
- Design
- research and development
- production
- and sales

FEATURES

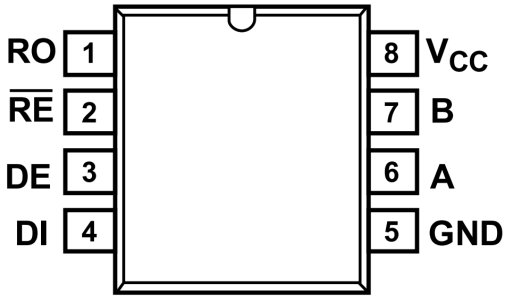
- Electronics industries alliance (EIA) RS-485/RS-422 compliant
- Data rate options

ADM4850/ADM4854: 115 kbps
ADM4851/ADM4855: 500 kbps
ADM4852/ADM4856: 2.5 Mbps
ADM4853/ADM4857: 10 Mbps

- Half-duplex and full duplex options
- Reduced slew rates for low electromagnetic interference (EMI)
- True fail-safe receiver inputs
- 5 μA (maximum) supply current in shutdown mode
- Up to 256 transceivers on one bus
- Outputs high-Z when disabled or powered off
- -7 V to +12 V bus common-mode range
- Thermal shutdown and short-circuit protection
- Pin-compatible with the MAX308x
- Specified over the -40°C to +85°C temperature range
- Available in 8-lead SOIC, 8-lead LFCSP, and 8-lead MSOP
- Qualified for automotive applications



ADM4850 MSOP8



ADM4850/ ADM4851/
ADM4852/ ADM4853
SOP8

APPLICATIONS

- Low power RS-485 applications
- EMI sensitive systems
- DTE to DCE interfaces
- Industrial control
- Packet switching
- Local area networks
- Level translators

DESCRIPTION

The ADM4850/ADM4851/ADM4852/ADM4853/ADM4854/ ADM4855/ADM4856/ADM4857 are differential line transceivers suitable for high speed, half-duplex and full duplex data communication on multipoint bus transmission lines. They are designed for balanced data transmission and comply with EIA Standards RS-485 and RS-422. The ADM4850/ADM4851/ ADM4852/ADM4853 are half-duplex transceivers that share differential lines and have separate enable inputs for the driver and receiver. The full duplex ADM4854/ADM4855/ADM4856/ ADM4857 transceivers have dedicated differential line driver outputs and receiver inputs.

The devices have a 1/8-unit load receiver input impedance, which allows up to 256 transceivers on one bus. Because only one driver must be enabled at any time, the output of a disabled or powered down driver is three-stated to avoid overloading the bus. The receiver inputs have a true fail-safe feature, which ensures a logic high output level when the inputs are open or shorted. This guarantees that the receiver outputs are in a known state before communication begins and when communication ends. The driver outputs are slew rate limited to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit. The devices are fully specified over the commercial and industrial temperature ranges and are available in 8-lead SOIC (ADM4850 through ADM4857), 8-lead LFCSP (ADM4850/ADM4852/ ADM4853), and 8-lead MSOP (ADM4850 only) packages.

ADM4850/ADM4851/ADM4852/ADM4853, MSOP8 and SOP8, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output.When RO is enabled and(A-B)≥-30 mV,RO is high. When RO is enabled and(A-B)≤-200mV,RO is low.
2	RE	Receiver Output Enable.A low level on RE enables the receiver output(RO).A high level on RE places RO into a highimpedance state.
3	DE	Driver Output Enable.A high level on DE enables the driver differential outputs(A and B).A low level on DE placesthe driver differential outputs into a high impedance state.
4	DI	Driver Input.When the driver is enabled,a logic low on DI forces A low and B high,whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	V_{CC}	5V Power Supply.

ADM4850/ADM4852/ADM4853, LFCSP8, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output.When RO is enabled and(A-B)≥-30 mV,RO is high. When RO is enabled and(A-B)≤-200 mV,RO is low.
2	RE	Receiver Output Enable.A low level on RE enables the receiver output (RO).A high level on RE places RO into a high impedance state.
3	DE	Driver Output Enable.A high level on DE enables the driver differential outputs(A and B).A low level places the driver differential outputs into ahigh impedance state.
4	DI	Driver Input.When the driver is enabled,a logic low on DI forces A low and B high,whereas a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Noninverting Driver Output A.
7	B	Inverting Receiver Input B/Inverting Driver Output B.
8	Vcc	5V Power Supply.
	EPAD	Exposed Pad.The exposed paddle on the underside of the package must be soldered to the ground plane to increase the reliability of the solder joints and to maximize the thermal capability of the package.

ADM4854/ADM4855/ADM4856/ADM4857, SOP8, Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Vcc	5VPower Supply.
2	RO	Receiver Output.When RO is enabled and(A-B)≥-30mV,RO is high. When RO is enabled and(A-B)≤-200mV,RO is low.
3	DI	Driver Input.When the driver is enabled,a logic low on DIforces Y low and Z high,whereas a logic high on DI forces Y high and Zlow.
4	GND	Ground.
5	Y	Noninverting Driver Output.
6	Z	Inverting Driver Output.
7	B	Inverting Receiver Input.
8	A	Noninverting Receiver Input.

SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter		Min	Typ	Max	Unit	Test Conditions/ Comments
DRIVER Differential Output Voltage	V_{OD}			V_{cc}	V	R=∞,see Figure 1[1]
		2.0		5	V	R=50Ω(RS-422), see Figure 1
		1.5		5	V	R=27Ω(RS-485), see Figure 1
Differential Output Voltage over Common- Mode Range	$\|V_{OD3}\|$	1.5		5	V	V_{TST}=-7V to+12V, see Figure 2
△$\|V_{OD}\|$for Complementary Output States				0.2	V	R=27Ω or 50Ω, see Figure 1
Common-Mode Output Voltage	V_{OC}			3	V	R=27Ω or 50 Ω, see Figure 1
△$\|V_{OC}\|$ for Complementary Output States				0.2	V	R=27 Ω or 50Ω, see Figure 1
Output Short-Circuit Current						-7V<V_{OUT}<+12V
V_{OUT}=High		-200		+200	mA	
V_{OUT}=Low		-200		+200	mA	
DRIVER INPUT LOGICCMOS Input Logic Threshold						
Low				0.8	V	
High		2.0			V	
CMOS LogicInput Current(DI)				± 1	μA	
DEInput Resistance to GND			220		kΩ	
RECEIVE RDifferential Input Threshold Voltage	V_{TH}	-200	-125	-30	mV	-7V<V_{OC}<+12V
Input Hysteresis			20		mV	-7V<V_{OC}<+12V
Input Resistance(A,B)		96	150		kΩ	-7V<V_{OC}<+12V
Input Current(A,B)				0.125	mA	V_{IN}=12V
				-0.1	mA	V_{IN}=-7V
CMOS Logic Input Current(RE)				± 1	μA	

SPECIFICATIONS(continued)

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter		Min	Typ	Max	Unit	Test Conditions/ Comments
CMOS Output Voltage						
Low				0.4	V	I_{OUT}=4mA
High		4.0			V	I_{OUT}=-4mA
Output Short-Circuit Current		7		85	mA	V_{OUT}=GND or V_{CC}
Three-State Output Leakage Current				±2	μA	0.4V≤V_{OUT}≤2.4V
POWER SUPPLY CURRENT 115kbps Options (ADM4850/ADM4854)				5	μA	DE=0V,RE=V_{CC}(shutdown)
			36	60	μA	DE=0V,RE=0V
			100	160	μA	DE=V_{CC}
500 kbps Options(ADM4855)				5	μA	DE=0V,RE=V_{CC}(shutdown)
			80	120	μA	DE=0V,RE=0V
			120	200	μA	DE=V_{CC}
2.5 Mbps Options(ADM4852/ ADM4856)				5	μA	DE=0V,RE=V_{CC}(shutdown)
			250	400	μA	DE=0V,RE=0V
			320	500	μA	DE=V_{CC}
10 Mbps Options(ADM4853/ ADM4857)				5	μA	DE=0V,RE=Vcc(shutdown)
			250	400	μA	DE=0V,RE=0V
			320	500	μA	DE=V_{CC}

ADM4850/ADM4854 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER Maximum Data Rate		115			kbps	
Propagation Delay	t_{PLH},t_{PHL}	600		2500	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF, see Figure 3 and Figure 7
Skew	t_{SKEW}			70	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF, see Figure 3 and Figure 7
Rise/Fall Times	t_R,t_F	600		2400	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF, see Figure 3 and Figure 7
Enable Time	t_{ZH},t_{ZL}			2000	ns	R_L=500Ω,C_L=100pF,see Figure 4 and Figure 9(ADM4850 only)
Disable Time	t_{LZ},t_{HZ}			2000	ns	R_L=500Ω,C_L=15pF,see Figure 4 and Figure 9(ADM4850 only)
Enable Time from Shutdown			4000		ns	R_L=500Ω,C_L=100 pF, see Figure 4(ADM4850 only)
RECEIVER Propagation Delay	t_{PLH},t_{PHL}	400		1000	ns	C_L=15 pF, see Figure 5 and Figure 8
Differential Skew	t_{SKEW}			255	ns	C_L=15 pF,see Figure 5 and Figure 8
Enable Time	t_{ZH},t_{ZL}		5	50	ns	R_L=1kΩ,C_L=15 pF,see Figure 6 and Figure 10(ADM4850 only)
Disable Time	t_{LZ},t_{HZ}		20	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4850 only)
Enable Time from Shutdown			4000		ns	R_L=1kΩ,C_L=15 pF, see Figure 6(ADM4850 only)
Time to Shutdown		50	330	3000	ns	ADM4850 only[1]

1 The half-duplex device is put into shutdown mode by driving RE high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4851/ADM4855 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER Maximum Data Rate		500			kbps	
Propagation Delay	t_{PLH},t_{PHL}	250		600	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Skew	t_{SKEW}			40	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Rise/Fall Times	t_R,t_F	200		600	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Enable Time	t_{ZH},t_{ZL}			1000	ns	R_L=500Ω,C_L=100 pF,see Figure 4 and Figure 9(ADM4851 only)
Disable Time	t_{LZ},t_{HZ}			1000	ns	R_L=500Ω,C_L=100pF,see Figure 4 and Figure 9(ADM4851 only)
Enable Time from Shutdown			4000		ns	R_L=500Ω,C_L=100 pF,see Figure 4 (ADM4851 only)
RECEIVER Propagation Delay	t_{PLH},t_{PHL}	400		1000	ns	C_L=15 pF,see Figure 5 and Figure 8
Differential Skew	t_{SKEW}			250	ns	C_L=15pF,see Figure 5 and Figure 8
Enable Time	t_{ZH},t_{ZL}		5	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4851 only)
Disable Time	t_{LZ},t_{HZ}		20	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4851 only)
Enable Time from Shutdown			4000		ns	R_L=1kΩ,C_L=15 pF,see Figure 6 (ADM4851 only)
Time to Shutdown		50	330	3000	ns	ADM4851 only[1]

1 The half-duplex device is put into shutdown mode by driving RE high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4852/ADM4856 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER Maximum Data Rate		2.5			Mbps	
Propagation Delay	t_{PLH},t_{PHL}	50		180	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Skew	t_{SKEW}			50	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Rise/Fall Times	t_R,t_F			140	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Enable Time	t_{ZH},t_{ZL}			180	ns	R_L=500Ω,C_L=100 pF,see Figure 4 and Figure 9(ADM4852 only)
Disable Time	t_{LZ},t_{HZ}			180	ns	R_L=500Ω,C_L=100 pF,see Figure 4 and Figure 9(ADM4852 only)
Enable Time from Shutdown			4000		ns	R_L=500Ω,C_L=100 pF,see Figure 4 (ADM4852 only)
RECEIVER Propagation Delay	t_{PLH},t_{PHL}	55		190	ns	C_L=15pF,see Figure 5 and Figure 8
Differential Skew	t_{SKEW}			50	ns	C_L=15pF,see Figure 5 and Figure 8
Enable Time	t_{ZH},t_{ZL}		5	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4852 only)
Disable Time	t_{LZ},t_{HZ}		20	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4852 only)
Enable Time from Shutdown			4000		ns	R_L=1kΩ,C_L=15 pF,see Figure 6 (ADM4852 only)
Time to Shutdown		50	330	3000	ns	ADM4852 only[1]

1 The half-duplex device is put into shutdown mode by driving RE high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ADM4853/ADM4857 TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER Maximum Data Rate		10			Mbps	
Propagation Delay	t_{PLH},t_{PHL}	0		30	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Skew	t_{SKEW}			10	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Rise/Fall Times	t_R,t_F			30	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100 pF,see Figure 3 and Figure 7
Enable Time	t_{ZH},t_{ZL}			35	ns	R_L=500Ω,C_L=100pF,see Figure 4 and Figure 9(ADM4853 only)
Disable Time	t_{LZ},t_{HZ}			35	ns	R_L=500Ω,C_L=100pF,see Figure 4 and Figure 9(ADM4853 only)
Enable Time from Shutdown			4000		ns	R_L=500Ω,C_L=100 pF,see Figure 4 (ADM4853 only)
RECEIVER Propagation Delay	t_{PLH},t_{PHL}	55		190	ns	C_L=15 pF,see Figure 5 and Figure 8
Differential Skew	t_{SKEW}			30	ns	C_L=15 pF,see Figure 5 and Figure 8
Enable Time	t_{ZH},t_{ZL}		5	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4853 only)
Disable Time	t_{LZ},t_{HZ}		20	50	ns	R_L=1kΩ,C_L=15pF,see Figure 6 and Figure 10(ADM4853 only)
Enable Time from Shutdown			4000		ns	R_L=1kΩ,C_L=15 pF,see Figure 6 (ADM4853 only)
Time to Shutdown		50	330	3000	ns	ADM4853 only[1]

1 The half-duplex device is put into shutdown mode by driving RE high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to enter shutdown mode.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{CC} to GND	6V
Digital Input/Output Voltage(DE,RE,DI,RO)	-0.3V to V_{CC} +0.3V
Driver Output/Receiver Input Voltage	-9V to+14V
Operating Temperature Range	-40℃to +85℃
Storage Temperature Range	-65℃ to +125℃
θ_{JA}Thermal Impedance 8-Lead SOIC	110℃/W
8-Lead LFCSP	62℃/W
8-Lead MSOP	133.1℃/W
Lead Temperature Soldering(10 sec)	300℃
Vapor Phase(60 sec)	215℃
Infrared(15 sec)	220℃

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

ESD CAUTION

ESD(electrostatic discharge)sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD.Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TEST CIRCUITS

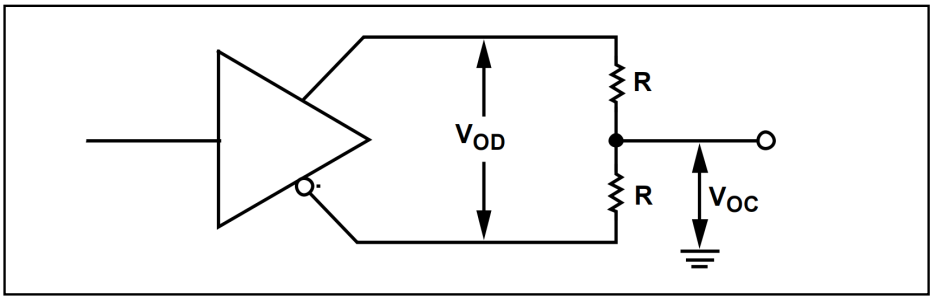


Figure 1. Driver Voltage Measurement

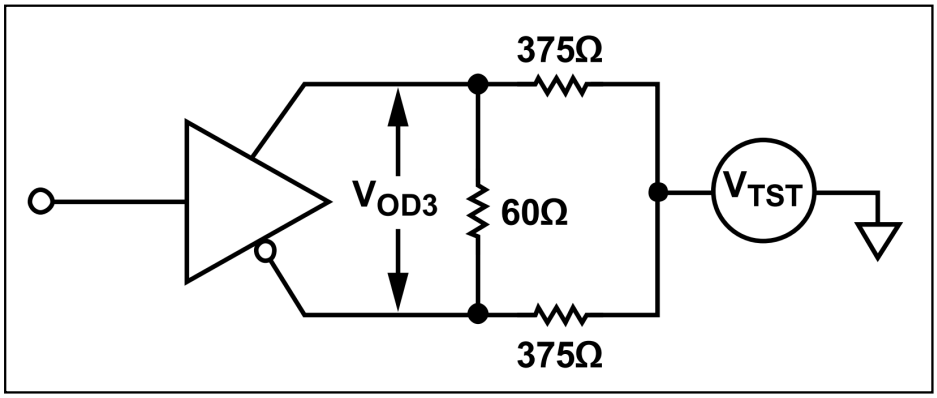


Figure 2. Driver Voltage Measurement over Common-Mode Voltage Range

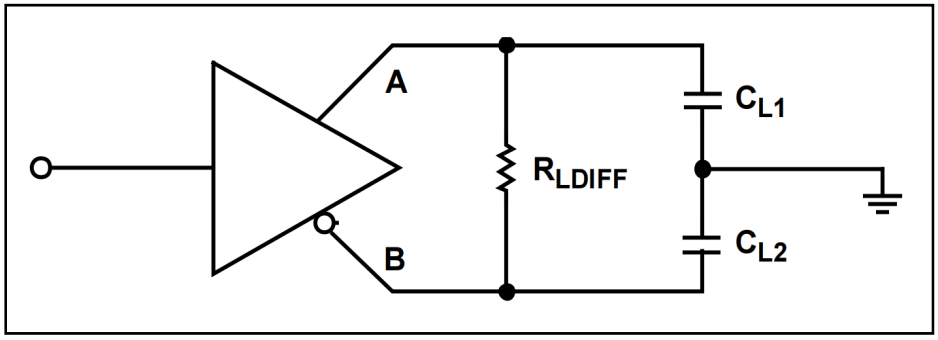


Figure 3. Driver Propagation Delay

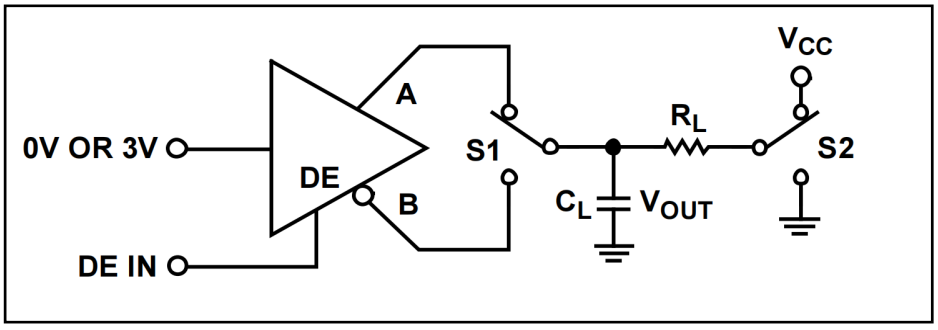


Figure 4. Driver Enable/Disable (ADM4850/ADM4852/ADM4853)

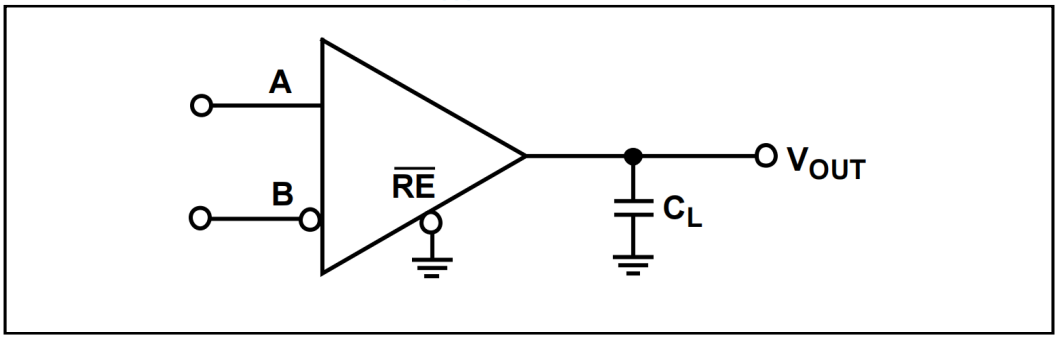


Figure 5. Receiver Propagation Delay

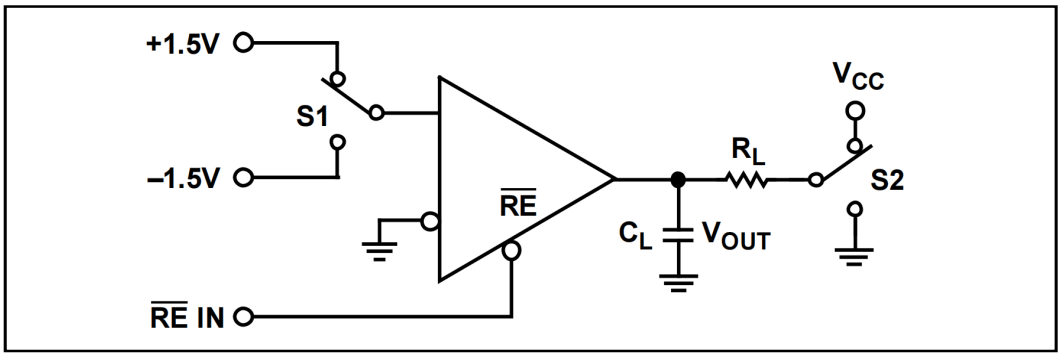


Figure 6. Receiver Enable/Disable (ADM4850/ADM4852/ADM4853)

SWITCHING CHARACTERISTICS

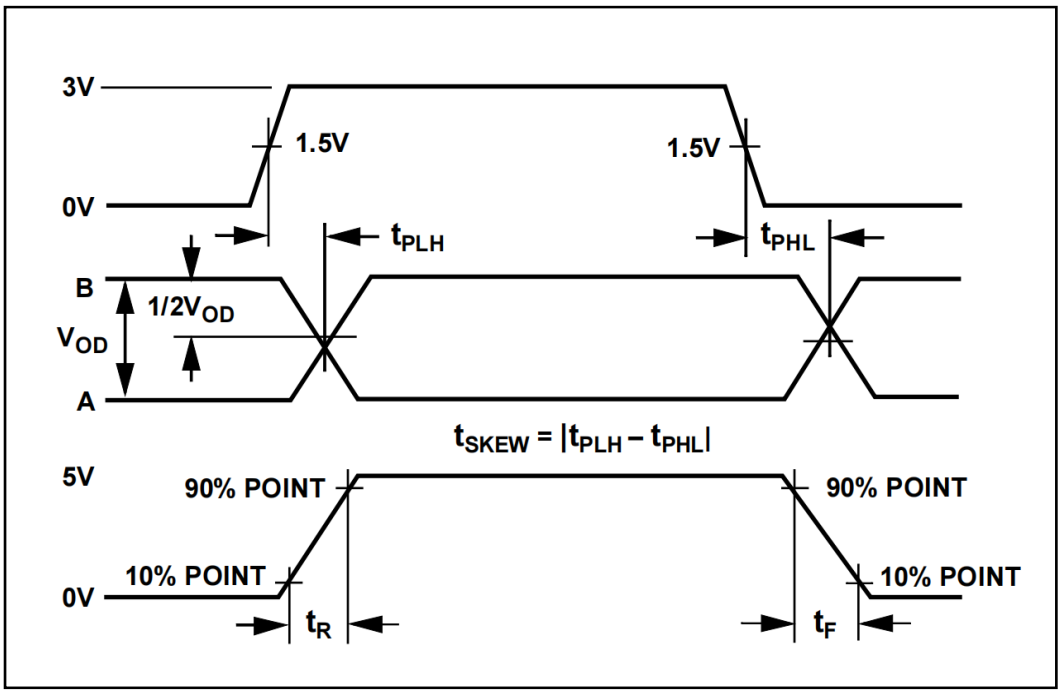


Figure 7. Driver Propagation Delay, Rise/Fall Timing

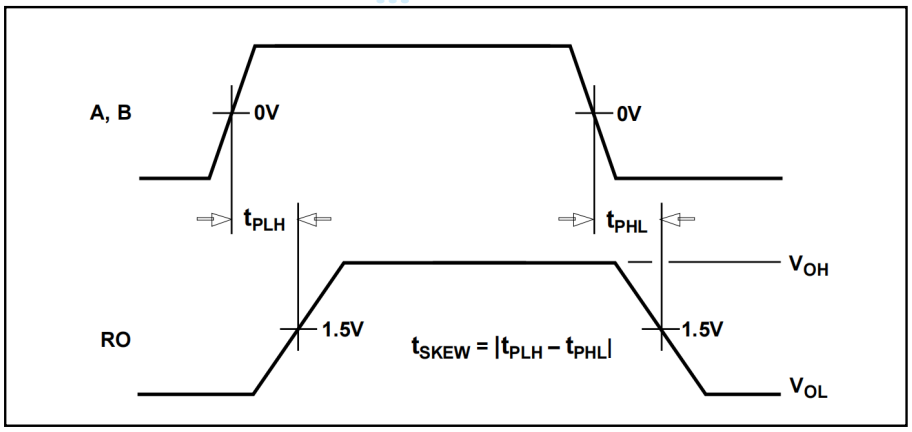


Figure 8. Receiver Propagation Delay

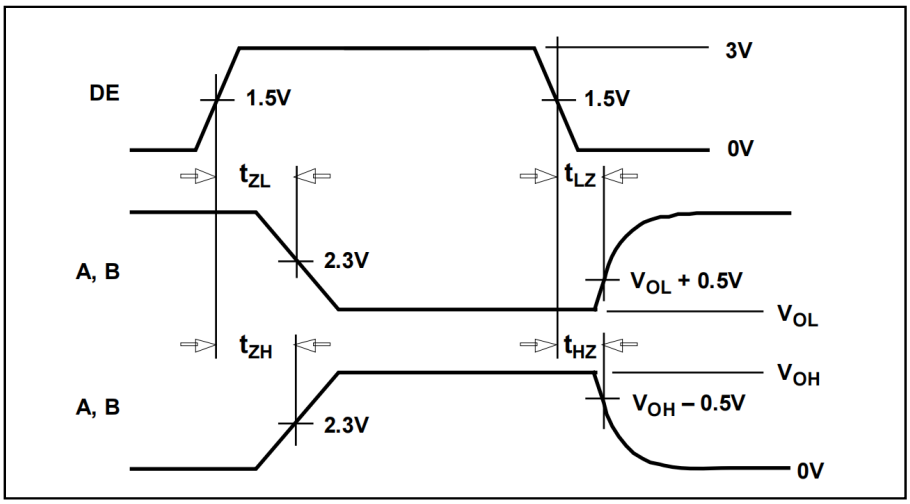


Figure 9. Driver Enable/Disable Timing

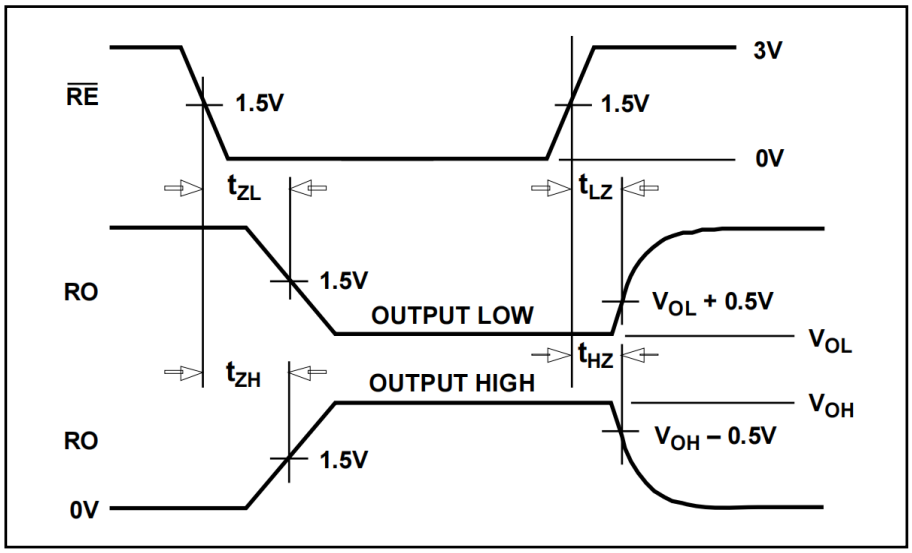


Figure 10. Receiver Enable/Disable Timing

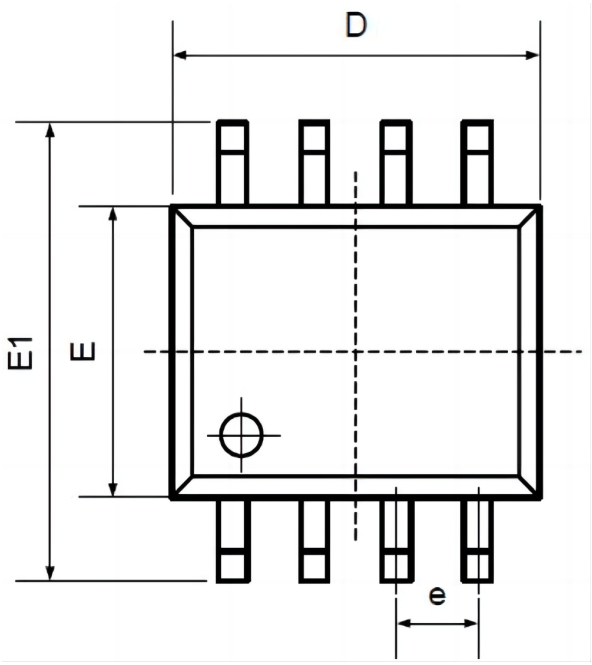
Order information

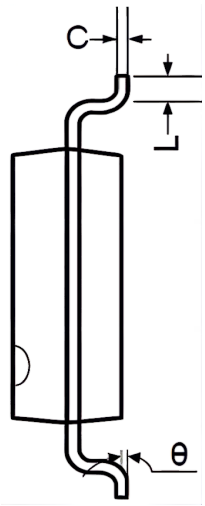
Order Number	Package	Package Quantity	Marking On The park	Temperature
ADM4850ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4850A	-40℃ to+85℃
ADM4850ARMZ-REEL-TUDI	MSOP8	Tape,Reel,4000	M8Q	
ADM4851ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4851A	
ADM4853ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4853A	
ADM4853WARZ-RL-TUDI	SOP8	Tape,Reel,4000	ADM4853W	
ADM4854ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4854A	
ADM4855ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4855A	
ADM4856ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4856A	
ADM4857ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM4857A	
ADM4850ACPZ-TUDI	DIP8	Tube,50,A box of 2000	ADM4850ACPZ	
ADM4852ACPZ-TUDI	DIP8	Tube,50,A box of 2000	ADM4852ACPZ	
ADM4853ACPZ-TUDI	DIP8	Tube,50,A box of 2000	ADM4853ACPZ	

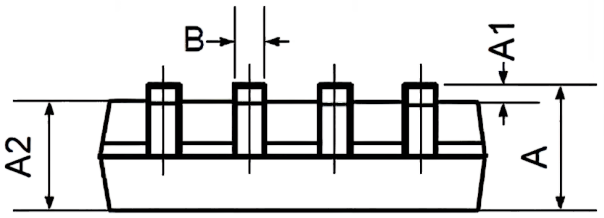
Revision history

	Date	Revision	Page
V1.0	2022/4/16	New	1-18

Package SOP8

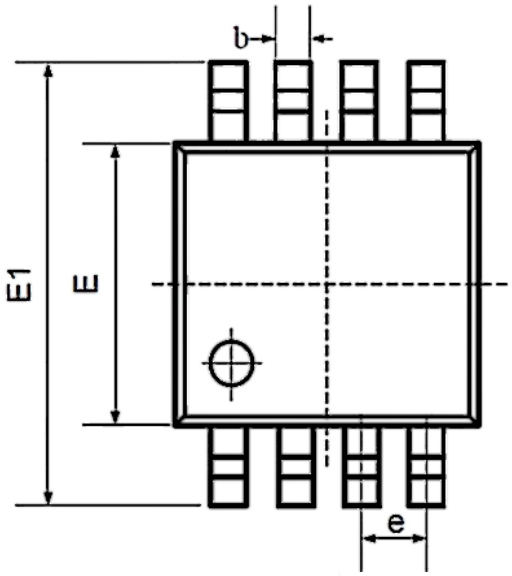


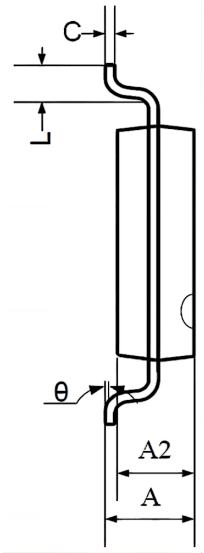


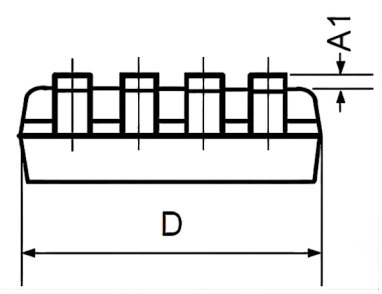


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package MSOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

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