钍地半导体
Tudi Semiconductor

Product Specification

TUDI-24AA128/24LC128

128-Kbit I^2C Serial EEPROM

网址 www.sztdbdt.com

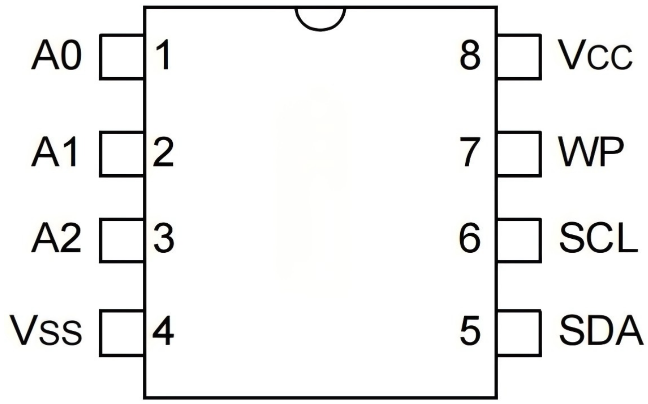
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- ●Single Supply with Operation down to 1.7V for 24AA128/24FC128 devices, 2.5V for 24LC128 Devices
- ●Low-Power CMOS Technology:
  - Write current 3 mA, maximum
  - Standby current 1 µA, maximum (I-temp.)
- ●Two-Wire Serial Interface, I^2C Compatible
- ●Cascadable up to Eight Devices
- ●Schmitt Trigger Inputs for Noise Suppression
- ●Output Slope Control to Eliminate Ground Bounce
- ●100 kHz, 400 kHz and 1 MHz Compatibility
- ●Page Write Time: 5 ms, Maximum
- ●Self-Timed Erase/Write Cycle
- ●64-Byte Page Write Buffer
- ● Hardware Write-Protect
- ●ESD Protection > 4,000V
- ● More than 1 Million Erase/Write Cycles
- ● Data Retention > 200 years
- ● Factory Programming Available
- ●RoHS Compliant
- ●Temperature Ranges:
  - Industrial (I): -40C to +85C
  - Extended (E) -40C to +125C
- ●Automotive AEC-Q100 Qualified

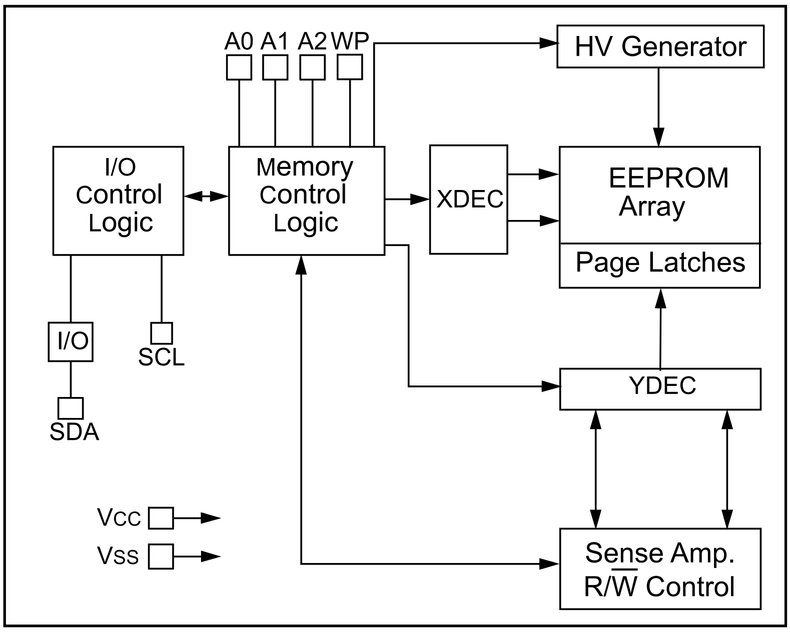


SOP8/DIP8/MSOP8/DIP8

Description

The 24XX128 is a 16K x 8 (128 Kbit) Serial Electrically Erasable PROM (EEPROM), capable of operation across a broad voltage range (1.7V to 5.5V). It has been developed for advanced, low-power applications such as personal communications or data acquisition. This device also has a page write capability of up to 64 bytes of data. This device is capable of both random and sequential reads up to the 128K boundary. Functional address lines allow up to eight devices on the same bus, for up to 1 Mbit address space.

Block Diagram



Absolute Maximum Ratings

V_{CC}...6.5V
All inputs and outputs w.r.t. V_{SS} ....-0.6V to V_{CC} +1.0V
Storage temperature .... -65°C to +150°C
Ambient temperature with power applied.. -40°C to +125°C
ESD protection on all pins .... ≧ 4 kV

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (1):Vcc=+1.7V to 5.5V TA=-40℃ to +85℃ Extended (E): Vcc=+2.5V to 5.5V TA=-40℃ to +125℃			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
D1	V_{IH}	High-Level Input Voltage	0.7 Vcc	—	V	
D2	V_{IL}	Low-Level Input Voltage	—	0.3 Vcc	V	Vcc≥2.5V
			—	0.2 Vcc	V	Vcc<2.5V
D3	V_{HYS}	Hysteresis of Schmitt Trigger Inputs(SDA,SCL pins)	0.05 Vcc	—	V	Vcc≥2.5V(Note 1)
D4	V_{OL}	Low-Level Output Voltage	—	0.40	V	I_{OL}=3.0 mA@Vcc=4.5V I_{OL}=2.1 mA @Vcc=2.5V
D5	I_{LI}	Input Leakage Current	—	±1	μA	V_{IN}=Vss or Vcc,WP=Vss V_{IN} =Vss or Vcc,WP=Vcc
D6	I_{LO}	Output Leakage Current	—	±1	μA	V_{OUT} =Vss or Vcc
D7	C_{IN},C_{OUT}	Pin Capacitance(all inputs/ outputs)	—	10	pF	Vcc=5.0V(Note 1)TA=+25 ℃,FCLK=1MHz
D8	Icc Read	Operating Current	—	400	μA	Vcc=5.5V,SCL=400 kHz
D9	Icc Write		—	3	mA	Vcc=5.5V
D10	Iccs	Standby Current	—	1	μA	SDA=SCL=Vcc=5.5V A0,A1,A2,WP=Vss,I-Temp
			—	5	μA	SDA=SCL=Vcc=5.5V A0,A1,A2,WP=Vss,E-Temp

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial(1):Vcc=+1.7V to 5.5V TA=-40℃ to +85℃ Extended(E):Vcc=+2.5V to 5.5V TA=-40℃ to +125℃			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
1	F_{CLK}	Clock Frequency	—	100	kHz	1.7V≤Vcc<2.5V
			—	400	kHz	2.5V≤Vcc≤5.5V
2	T_{HIGH}	Clock High Time	4000	—	ns	1.7V≤Vcc<2.5V
			600	—	ns	2.5V≤Vcc≤5.5V
3	T_{LOW}	Clock Low Time	4700	—	ns	1.7V≤Vcc<2.5V
			1300	—	ns	2.5V≤Vcc≤5.5V
4	T_R	SDA and SCL Rise Time	—	1000	ns	1.7V≤Vcc<2.5V(Note 1)
			—	300	ns	2.5V≤Vcc≤5.5V(Note 1)
5	T_F	SDA and SCLFall Time	—	300	ns	All except,24FC128(Note 1)
6	$T_{HD:STA}$	Start Condition HoldTime	4000	—	ns	1.7V≤Vcc<2.5V
			600	—	ns	2.5V≤Vcc≤5.5V
7	$T_{SU:STA}$	Start Condition SetupTime	4700	—	ns	1.7V≤Vce<2.5V
			600	—	ns	2.5V≤Vcc≤5.5V
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	ns	Note 2
9	$T_{SU:DAT}$	Data Input Setup Time	250	—	ns	1.7V≤Vcc<2.5V
			100	—	ns	2.5V≤Vcc≤5.5V
10	$T_{SU:STO}$	Stop ConditionSetup Time	—	4000	kHz	1.7V≤Vcc<2.5V
			—	600	kHz	2.5V≤Vcc≤5.5V
11	$T_{SU:WP}$	WP Setup Time	4000	—	ns	1.7V≤Vcc<2.5V
			600	—	ns	2.5V≤Vcc≤5.5V
12	$T_{HD:WP}$	WP Hold Time	4700	—	ns	1.7V≤Vcc<2.5V
			1300	—	ns	2.5V≤Vcc≤5.5V
13	T_{AA}	Output Valid FromClock	—	3500	ns	1.7V≤Vcc<2.5V(Note 2)
			—	900	ns	2.5V≤Vcc≤5.5V(Note 2)
14	T_{BUF}	Bus Free Time:TheTime The Bus Must Be Free Before a New Transmission CanStart	4700	—	ns	1.7V≤Vcc<2.5V
			1300	—	ns	2.5V≤Vcc≤5.5V

TABLE 2: AC CHARACTERISTICS（Continue）

AC CHARACTERISTICS			Industrial(1):Vcc=+1.7V to 5.5V TA=-40℃ to +85℃ Extended(E):Vcc=+2.5V to 5.5V TA=-40℃ to +125℃			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
15	T_{OF}	Output Fall Time from V_{IH} Minimum to V_{IL} Maximum $C_B \leq 100pF$	$10+0.1C_B$	250	ns	All except,24FC128(Note 1)
			—	250	ns	24FC128(Note 1)
16	T_{SP}	Input Filter Spike Suppression(SDAand SCL pins)	—	50	ns	All except,24FC128(Note 1and Note 3)
17	T_{WC}	Write Cycle Time(byte orpage)	—	5	ms	
18		Endurance	1,000,000	—	cycles	+25℃,5.5V,Page Mode(Note 4)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.
4: This parameter is not tested but ensured by characterization.

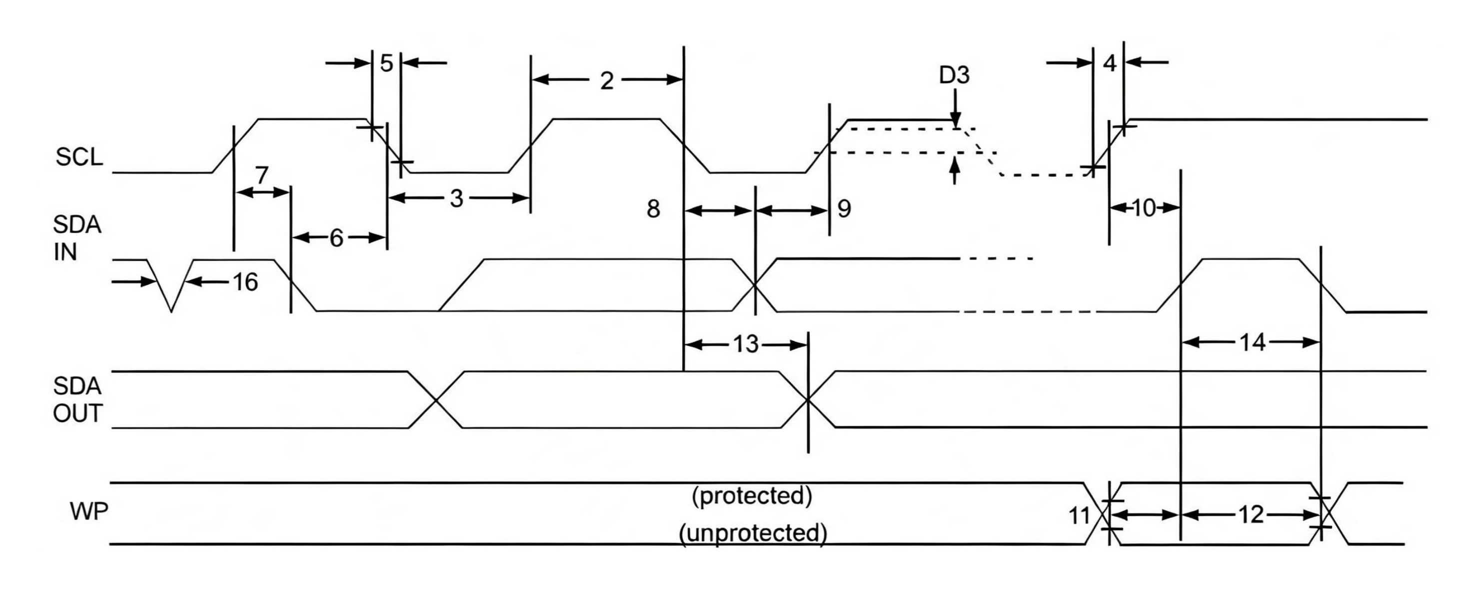


FIGURE 1: BUS TIMING DATA

PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3.

TABLE 3: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	Function
A0	1	1	1	User Configurable Chip Select
A1	2	2	2	User Configurable Chip Select
A2	3	3	3	User Configurable Chip Select
Vss	4	4	4	Ground
SDA	5	5	5	Serial Address/Data I/O
SCL	6	6	6	Serial Clock
WP	7	7	7	Write-Protect Input
Vcc	8	8	8	Power Supply

Serial Data (SDA)：This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an opendra interminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10kΩ for 100 kHz, 2kΩ for 400 kHz and 1 MHz). For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

Serial Clock (SCL)：This input is used to synchronize the data transfer to and from the device.

Write-Protect (WP)：This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited but read operations are not affected.

FUNCTIONAL DESCRIPTION

The 24XX128 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions while the 24XX128 works as a client . Both host and client can operate as a transmitter or receiver, but the host device determines which mode is activated.

BUS CHARACTERISTICS

The following bus protocol has been defined:
●Data transfer may be initiated only when the bus is not busy.
●During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.
Accordingly, the following bus conditions have been defined (Figure 2).

Bus Not Busy (A)：Both data and clock lines remain high.

Start Data Transfer (B)：A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

Stop Data Transfer (C)：A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

Data Valid (D)：The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is, theoretically, unlimited (although only the last 64 will be stored when doing a write operation). When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

Acknowledge：Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The host device must generate an extra clock pulse, which is associated with this Acknowledge bit.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX128) will leave the data line high to enable the host to generate the Stop condition.

Note: The 24XX128 does not generate any Acknowledge bits if an internal programming cycle is in progress.

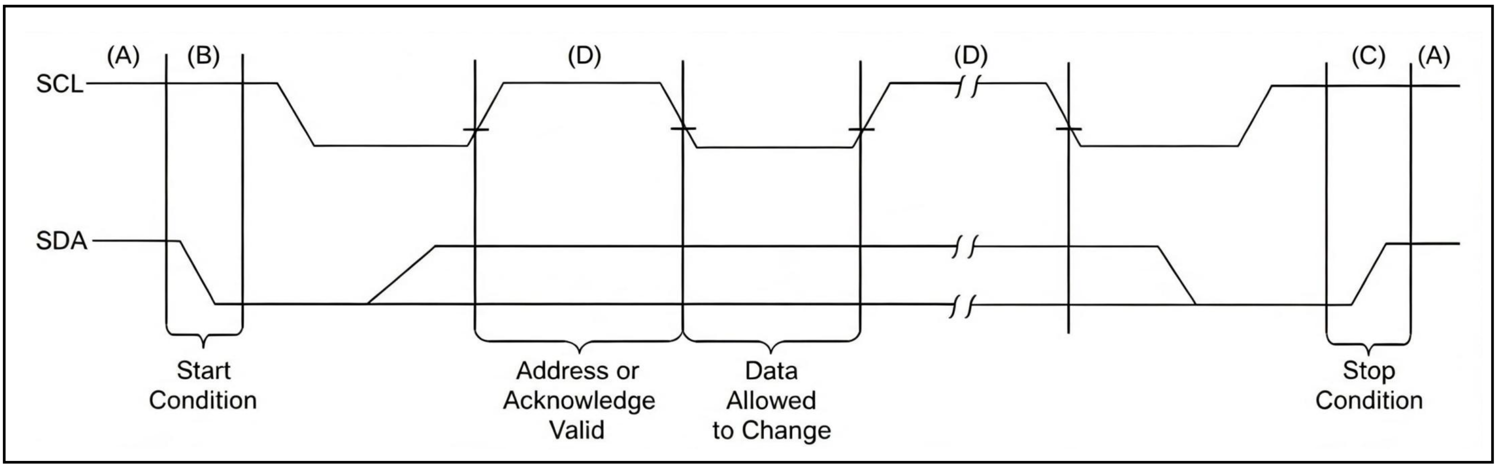


FIGURE 2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

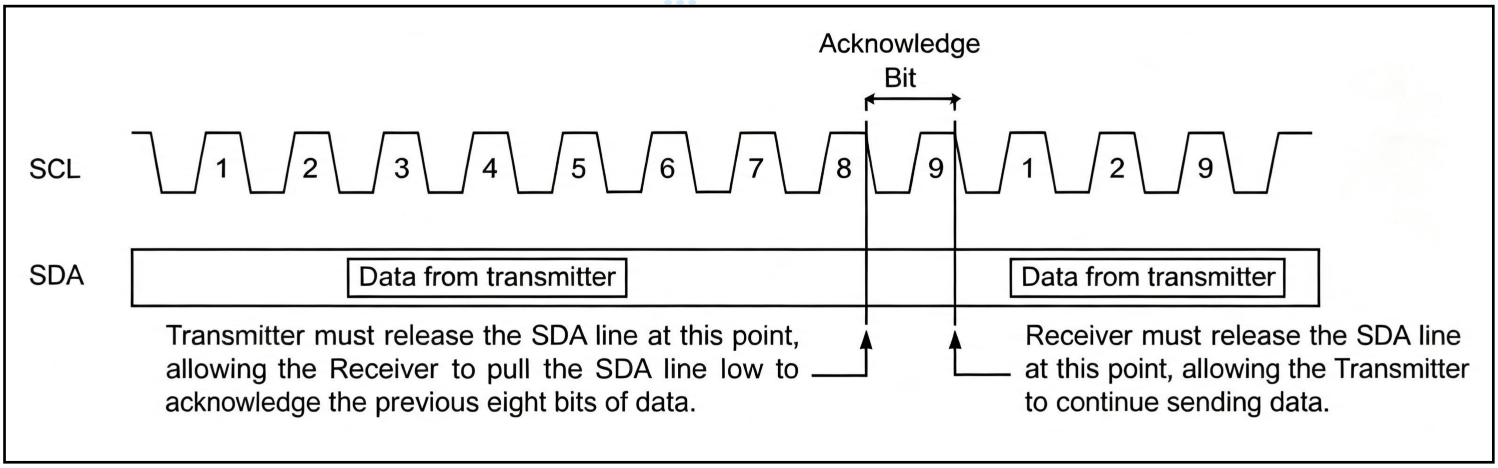


FIGURE 3: ACKNOWLEDGE TIMING

DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a 4-bit control code. For the 24XX128, this is set as ‘1010’ binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX128 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits, in effect, are the three Most Significant bits of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

The last bit of the control byte is the Read/Write (R/W) bit and it defines the operation to be performed. When set to a ‘1’, a read operation is selected. When set to a ‘0’, a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5). Because only A13…A0 are used, the upper two address bits are “don’t care” bits. The upper address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24XX128 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a ‘1010’ code and appropriate device select bits, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24XX128 will select a read or write operation.

Contiguous Addressing Across Multiple Devices： The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 1 Mbit by adding up to eight 24XX128 devices on the same bus. In this case, software can use A0 of the control byte as address bit A14; A1 as address bit A15; and A2 as address bit A16. It is not possible to sequentially read across device boundaries.

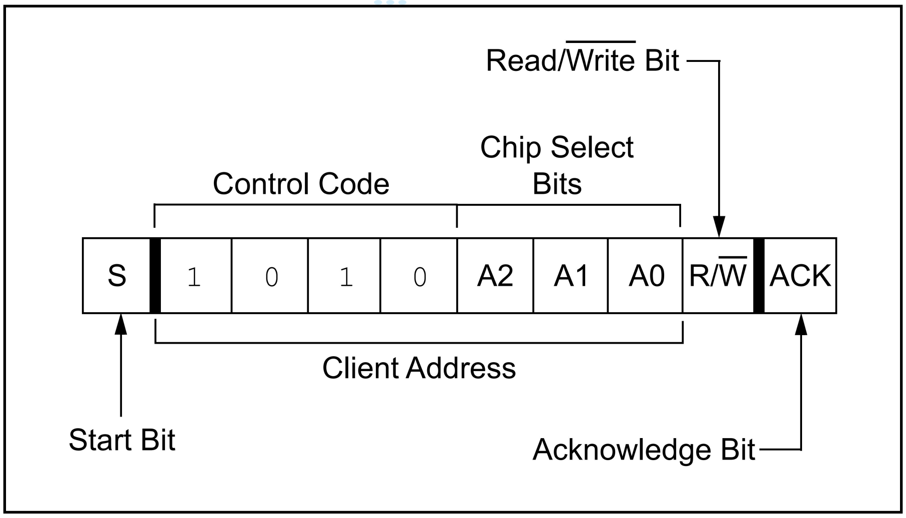


FIGURE 4: CONTROL BYTE FORMAT

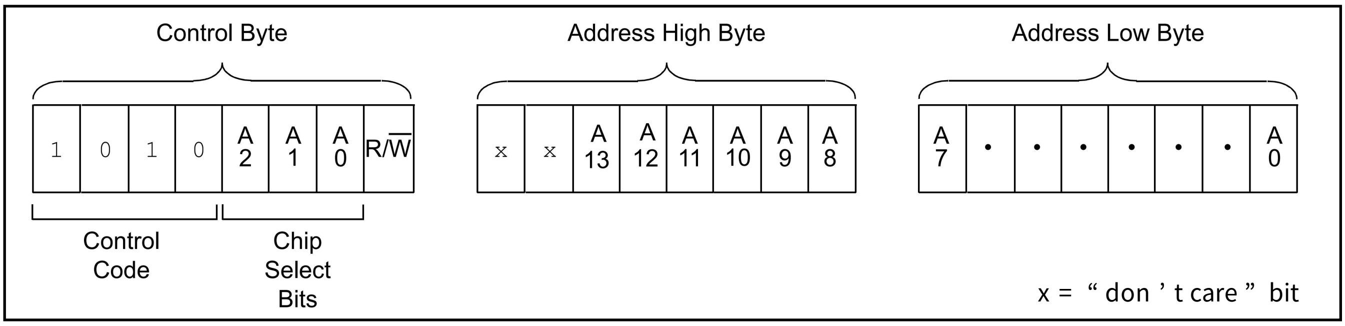


FIGURE 5: ADDRESS SEQUENCE BIT ASSIGNMENTS

WRITE OPERATIONS

Byte Write： Following the Start condition from the host, the control code (4 bits), the Chip Select (3 bits) and the R/W bit (which is a logic low)are clocked onto the bus by the host transmitter. This indicates to the addressed client receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the high-order byte of the word address and will be written into the Address Pointer of the 24XX128. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX128, the host device will transmit the data word to be written into the addressed memory location. The 24XX128 acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and during this time, the 24XX128 will not generate Acknowledge signals (Figure 6). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

Note: When doing a write of less than 64 bytes, the data in the rest of the page are refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, for this reason endurance is specified per page.

Page Write：The write control byte, word address and the first data byte are transmitted to the 24XX128 in much the same way as in a byte write. The exception is that instead of generating a Stop condition, the host transmits up to 63 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory once the host has transmitted a Stop condition. Upon receipt of each word, the six lower Address Pointer bits, which form the byte counter, are internally incremented by one. If the host should transmit more than 64 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will imme-diately accept a new command.

Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘ page size ’) and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the begin-ning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

Write Protection：The WP pin allows the user to write-protect the entire array (0000-3FFF) when the pin is tied to VCC. If tied to VSS the write protection is disabled. The WP pin is sampled at the Stop bit for every write command (Figure 1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

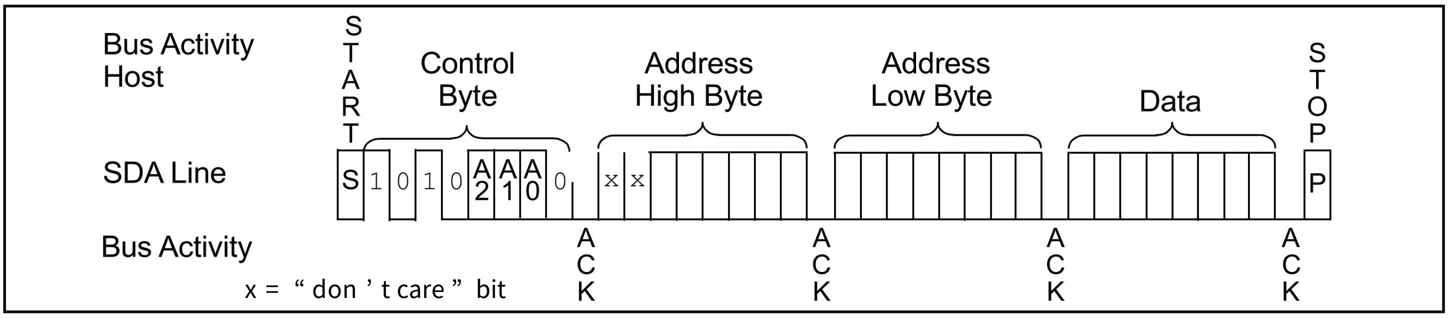


FIGURE 6: BYTE WRITE

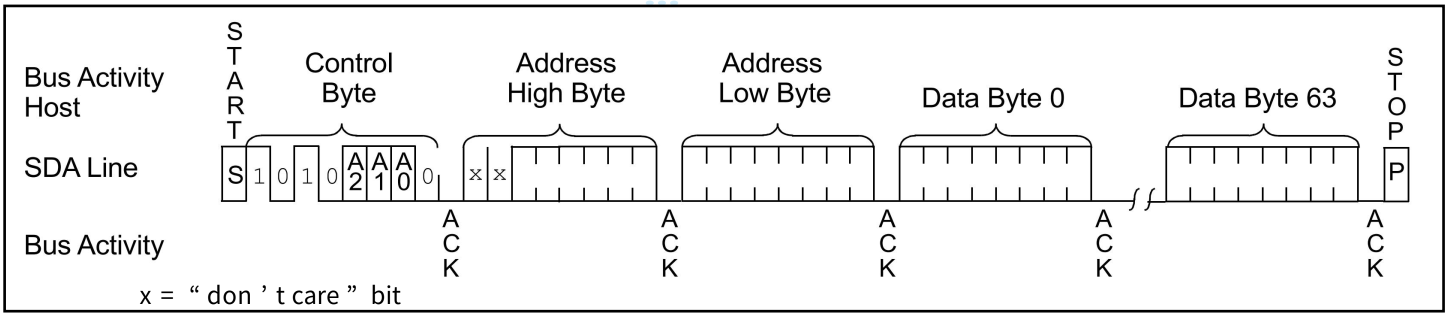


FIGURE 7: PAGE WRITE

ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write com-mand has been issued from the host, the device initi-ates the internally timed write cycle. ACK polling can be initiated immediately. This involves the host sending a Start condition, followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK and the host can then proceed with the next read or write command. See Figure 8 for flow diagram.

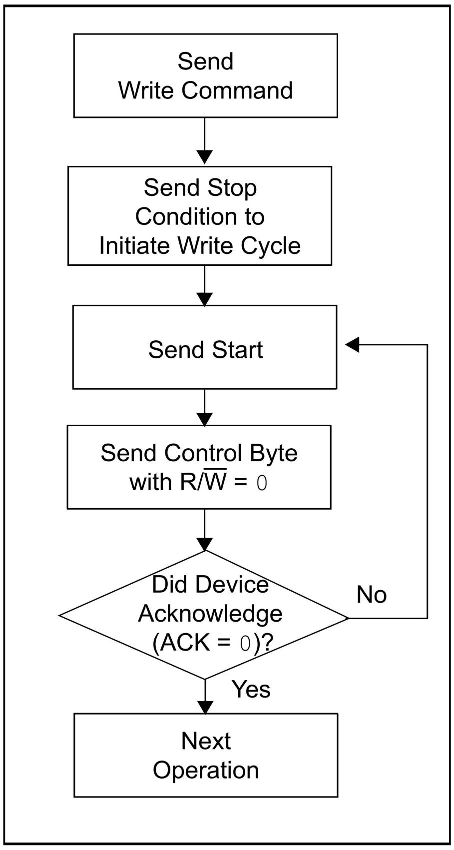


FIGURE 8: ACKNOWLEDGE POLLING FLOW

READ OPERATION：Read operations are initiated in much the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are three basic types of read operations: current address read,random read and sequential read.

Current Address Read：The 24XX128 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n+1. Upon receipt of the control byte with R/W bit set to ‘1’, the 24XX128 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX128 discontinues transmission (Figure 9).

Random Read：Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24XX128 as part of a write operation (R/W bit set to ‘0’). Once the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/W bit set to a ‘1’.
The 24XX128 will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer but does generate a Stop condition, which causes the 24XX128 to discontinue transmission (Figure 10). After a random read command, the internal address counter will point to the address location following the one that was just read.

Sequential Read：Sequential reads are initiated in the same way as a random read except that after the 24XX128 transmits the first data byte, the host issues an Acknowledge (as opposed to the Stop condition used in a random read). This Acknowledge directs the 24XX128 to transmit the next sequentially addressed 8-bit word (Figure 11). Following the final byte transmitted to the host, the host will not generate an Acknowledge but will generate a Stop condition.
To provide sequential reads, the 24XX128 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address 3FFF to address 0000 if the host acknowledges the byte received from the array address 3FFF.

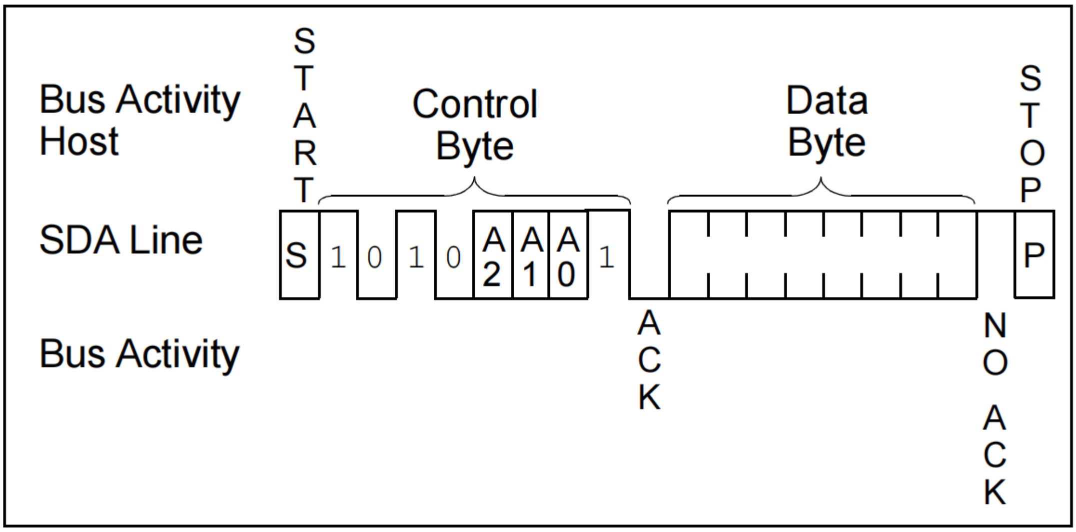


FIGURE 9: CURRENT ADDRESS READ

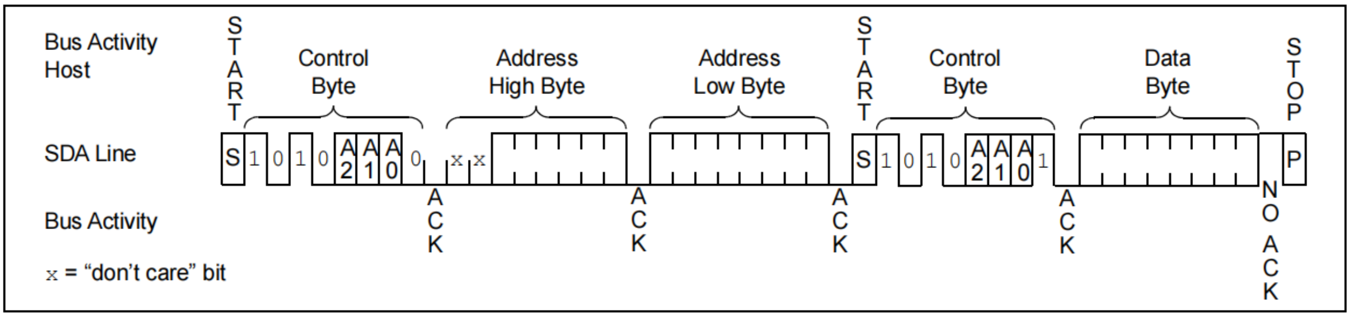


FIGURE 10: RANDOM READ

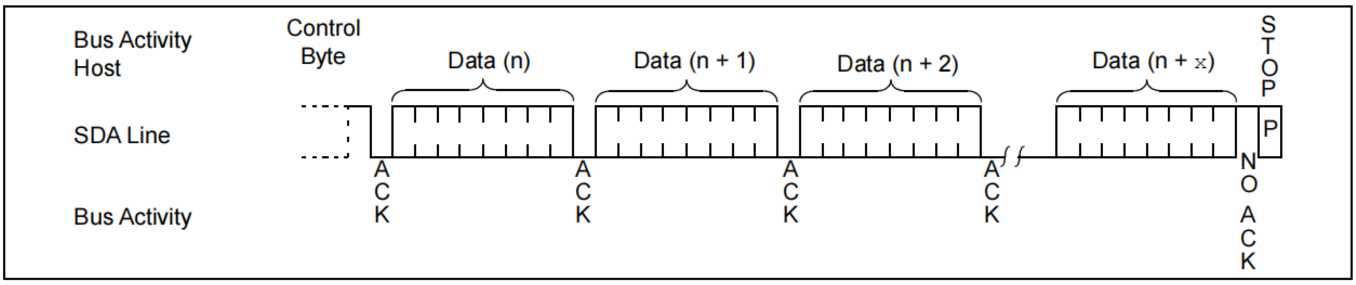


FIGURE 11: SEQUENTIAL READ

Order information

<table>
<tr><th>Order Number</th><th>Package</th><th>Package Quantity</th><th>Marking
On The park</th><th>Temperature</th></tr>
<tr><td>24AA128-I/P-TUDI</td><td>DIP8</td><td>Tube,50,A box of 2000</td><td>24AA128-I/P</td><td rowspan="8">-40°C to +85°C</td></tr>
<tr><td>24AA128T-I/SN-TUDI</td><td>SOP8</td><td>Tape,Reel,4000</td><td>24AA128I/SN</td></tr>
<tr><td rowspan="2">24AA128T-I/ST-TUDI</td><td rowspan="2">TSSOP8</td><td rowspan="2">Tape,Reel,4000</td><td>24AA128</td></tr>
<tr><td>4AC</td></tr>
<tr><td>24LC128-I/P-TUDI</td><td>DIP8</td><td>Tube,50,A box of 2000</td><td>24LC128-I/P</td></tr>
<tr><td>24LC128T-I/SN-TUDI</td><td>SOP8</td><td>Tape,Reel,4000</td><td>24LC128I/SN</td></tr>
<tr><td rowspan="2">24LC128T-I/ST-TUDI</td><td rowspan="2">TSSOP8</td><td rowspan="2">Tape,Reel,4000</td><td>24LC128</td></tr>
<tr><td>4LC</td></tr>
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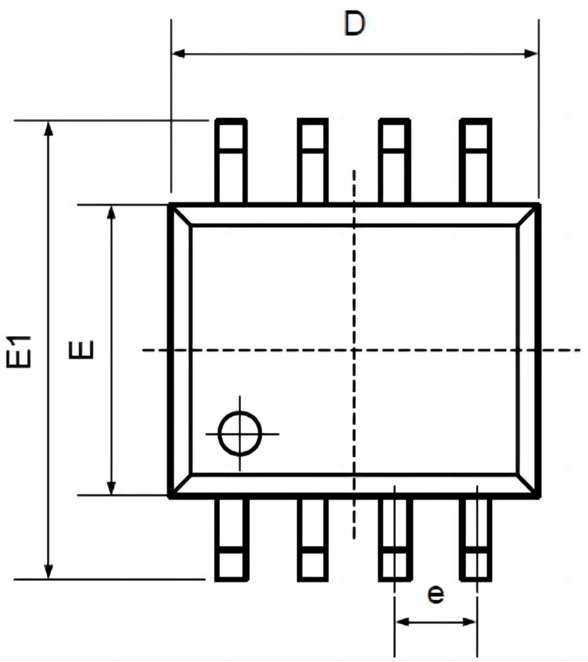
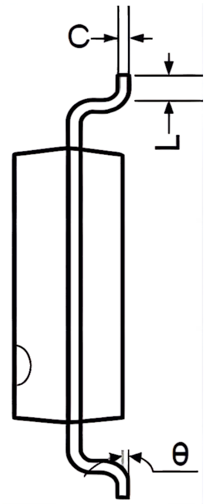
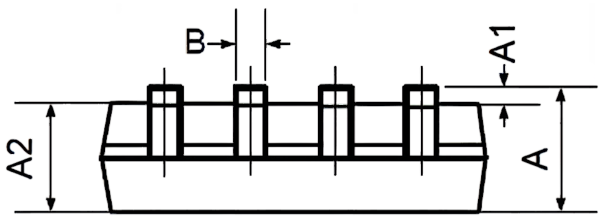
Revision history

	Date	Revision	Page
V1.0	2021/1	New	1-14
V1.1	2024-3	Update model and PDF template	1-20

Package SOP8

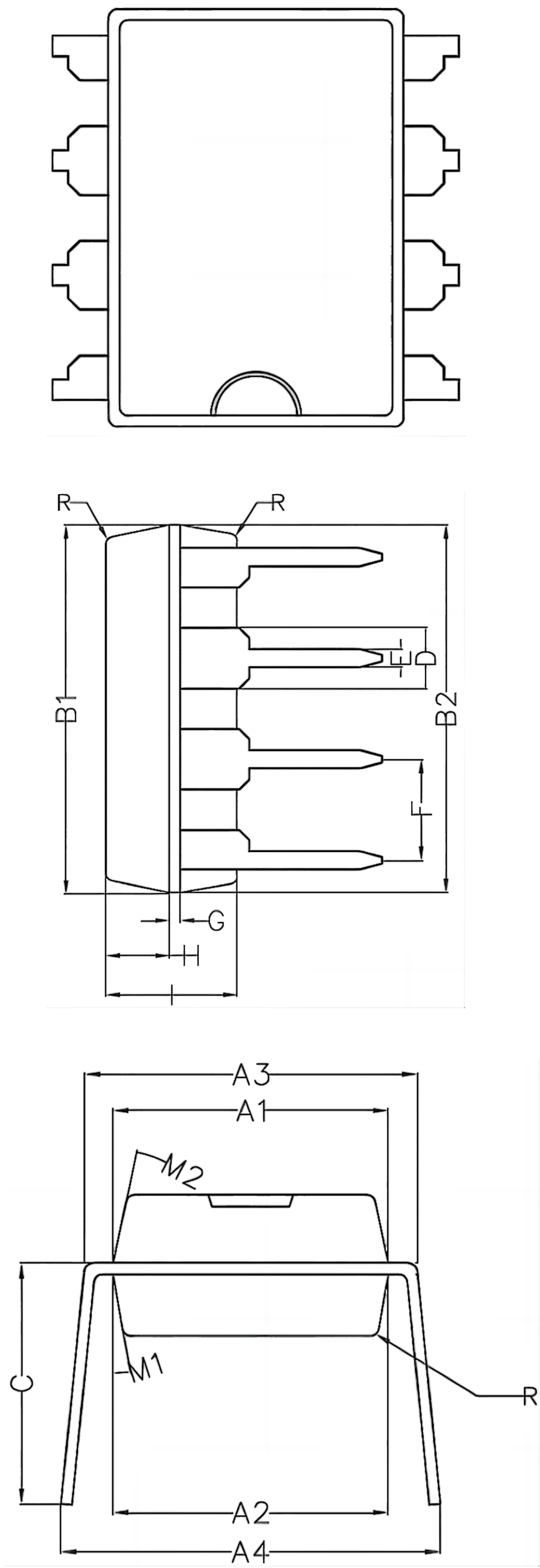






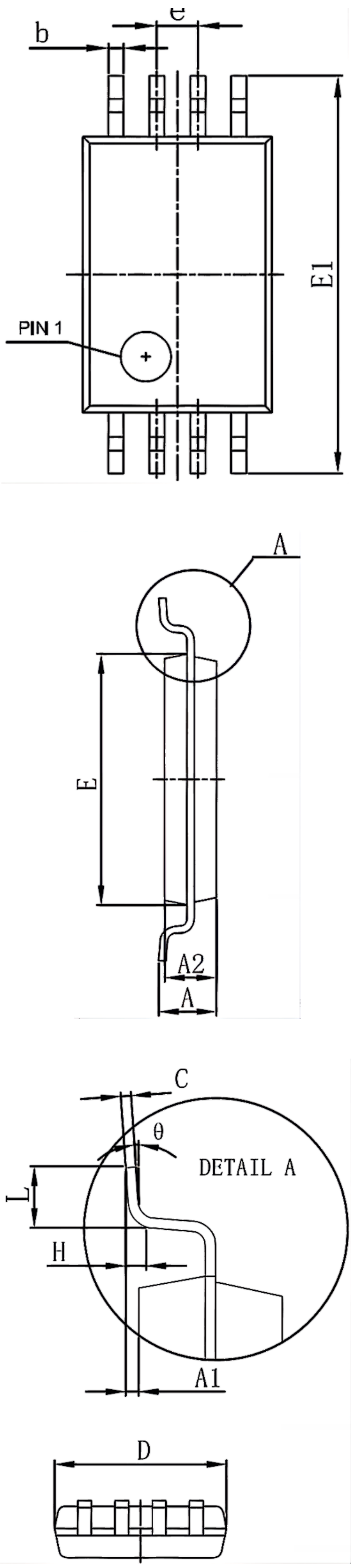
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Package TSSOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

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