钍地半导体
Tudi Semiconductor

Product Specification

TUDI-ADM1485

5 V Low Power EIA RS-485 Transceiver

网址 www.sztdbdt.com

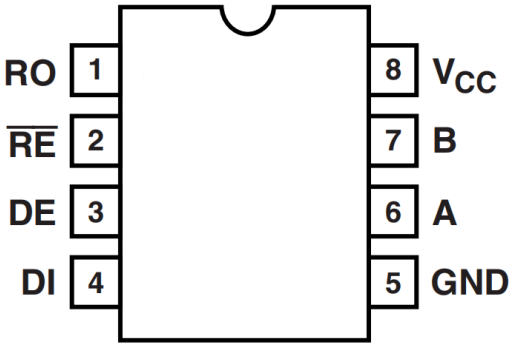
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

FEATURES

- Meets EIA RS-485 Standard
- 30 Mbps Data Rate
- Single 5 V Supply
- –7 V to +12 V Bus Common-Mode
- Range High Speed, Low Power BiCMOS
- Thermal Shutdown Protection
- Short-Circuit Protection
- Driver Propagation Delay: 10 ns
- Receiver Propagation Delay: 15 ns
- High-Z Outputs with Power Off
- Superior Upgrade for LTC1485



DIP8/SOP8/MSOP8

DESCRIPTION

The ADM1485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus trans-mission lines. It is designed for balanced data transmission and complies with both RS-485 and RS-422 EIA Standards. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are three-stated. The ADM1485 operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault condi-tions, a significant temperature increase is detected in the internal driver circuitry. Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM1485 driver features high output impedance when disabled and also when powered down.

This minimizes the loading effect when the transceiver is not being used. The high impedance driver output is maintained over the entire common-mode voltage range from –7 V to +12 V. The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating). The ADM1485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up. The part is fully specified over the commercial and industrial temperature range and is available in PDIP, SOIC, and small MSOP packages. 781/461-3113 2012 ' The ADM1485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at typical data rates of 30 Mbps while low skew minimizes EMI interference.

APPLICATIONS

- Low Power RS-485 Systems
- DTE-DCE Interface
- Packet Switching
- Local Area Networks
- Data Concentration
- Data Multiplexers
- Integrated Services Digital Network (ISDN)

SPECIFICATIONS

(V_{CC} = 5 V 5%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage,V_{OD}			5	V	R=∞,Figure 1
	2.0		5.0	V	V_{CC}=5V,R=50Ω(RS-422),Test Circuit 1
	1.5		5.0	V	R=27Ω(RS-485),Figure 1
V_{OD3}	1.5		5.0	V	V_{TST}=-7V to +12V,Figure 2
|V_{OD}|for Complementary OutputStates			0.2	V	R=27Ω or 50Ω,Figure 1
Common-Mode Output Voltage V_{OC}			3	V	R=27Ω or 50 Ω,Figure 1
|V_{OD}|for Complementary OutputStates			0.2	V	R=27Ω or 50Ω
Output Short-Circuit Current (V_{OUT} =High)	35		250	mA	-7V V_O+12V
Output Short-Circuit Current (V_{OUT}=Low)	35		250	mA	-7V V_O+12V
CMOS Input Logic Threshold Low,VINL			0.8	V	
CMOS Input Logic Threshold High,VINH	2			V	
Logic Input Current(DE,DI)			±1.0	μA	

SPECIFICATIONS (Continued)

(V_{CC} = 5 V 5%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER					
Differential Input Threshold Voltage,V_{TH}	-0.2		+0.2	V	-7V V_{CM} +12V
Input Voltage Hysteresis, V_{TH}		70		mV	V_{CM} =0V
Input Resistance	12			kΩ	-7V V_{CM} +12V
Input Current(A,B)			1	mA	V_{IN} = +12V
			-0.8	mA	V_{IN} = -7V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High,V_{INH}	2			V	
Logic Enable Input Current(RE)			±1	μA	
CMOS Output Voltage Low,V_{OL}			0.4	V	I_{OUT} = +4.0mA
CMOS Output Voltage High,V_{OH}	4			V	I_{OUT} = -4.0 mA
Short-Circuit Output Current	7		85	mA	V_{OUT} =GND or V_{CC}
Three-State Output Leakage Current			±1.0	μ A	0.4V V_{OUT} 2.4V
POWER SUPPLY CURRENT					
I_{CC}(Outputs Enabled)		1.0	2.2	mA	Digital Inputs =GND or V_{CC}
I_{CC}(Outputs Disabled)		1	1	mA	Digital Inputs =GND or V_{CC}

TIMING SPECIFICATIONS

(V_{CC} = 5V±5%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output t_{PLH},t_{PHL}	2	10	15	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100pF,Figure 3
Driver O/P to O/P t_{SKEW}		1	5	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100pF,Figure 3
Driver Rise/Fall Time t_R,t_F		8	15	ns	R_{LDIFF}=54Ω,C_{L1}=C_{L2}=100pF,Figure 3
Driver Enable to Output Valid		10	25	ns	R_L=110Ω,C_L=50 pF,Figure 4
Driver Disable Timing		10	25	ns	R_L=110Ω,C_L=50 pF,Figure 4
Matched Enable Switching		0	2	ns	R_L=110Ω,C_L=50 pF,Figure 4
$\lvert t_{AZH}-t_{BLZ}\rvert$, $\lvert t_{BZH}-t_{AZL}\rvert$					
Matched Disable Switching		0	2	ns	R_L=110Ω,C_L=50 pF,Figure 4
$\lvert t_{AHZ}-t_{BLZ}\rvert$, $\lvert t_{BHZ}-t_{ALZ}\rvert$					
RECEIVER					
Propagation Delay Input to Output t_{PLH},t_{PHL}	8	15	30	ns	C_L=15 pF,Figure 5
Skew $\lvert t_{PLH}-t_{PHL}\rvert$			5	ns	C_L=15 pF,Figure 5
Receiver Enable t_{EN1}		5	20	ns	C_L=15 pF,R_L=1kΩ,Figure 6
Receiver Disable t_{EN2}		5	20	ns	C_L=15 pF,R_L=1kΩ,Figure 6
Tx Pulse Width Distortion		1		ns	
Rx Pulse Width Distortion		1		ns	

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C, unless otherwise noted.)

V_{CC} . . . . . – 0.3 V to +7 V

Inputs

Receiver Inputs (A, B) . . . . . – 9 V to +14 V

Driver Input (DI) . . . . . – 0.3 V to V_{CC} + 0.3 V

Control Inputs (DE, RE) . . . . . – 0.3 V to V_{CC} + 0.3 V

Outputs

Receiver Output . . . . . – 0.5 V to V_{CC} + 0.5 V

Driver Outputs (A, B) . . . . . – 9 V to +14 V

Operating Temperature Range

Commercial (J Version) . . . . . 0°C to 70°C

Industrial (A Version) . . . . . – 40°C to +85°C

Storage Temperature Range . . . . . – 65°C to +150°C

Lead Temperature (Soldering, 10 sec) . . . . . 300°C

Vapor Phase (60 sec) . . . . . 215°C

Infrared (15 sec) . . . . . 220°C

Power Dissipation 8-Lead SOIC . . . . . 450 mW

θ_{JA}, Thermal Impedance . . . . . 170°C/W

Power Dissipation 8-Lead PDIP . . . . . 500 mW

θ_{JA}, Thermal Impedance . . . . . 130°C/W

Power Dissipation 8-Lead MSOP . . . . . 900 mW

θ_{JA},Thermal Impedance . . . . . 206°C/W

Table I. Transmitting

Inputs		Outputs	
DE	DI	B	A
1	1	0	1
1	0	1	0
0	X	Z	Z

Table II. Receiving

RE	InputsA-B	OutputsRO
0	≥+0.2V	1
0	≤-0.2V	0
0	Inputs Open	1
1	X	Z

PIN FUNCTION DESCRIPTIONS

PinNo.	Mnemonic	Function
1	RO	Receiver Output.When enabled if A>B by 200 mV,then RO=High.If A<B by200 mV,then RO=Low.
2	RE	Receiver Output Enable.A low levelenables the receiver output,RO. A highlevel places it in a high impedance state.
3	DE	Driver Output Enable.A high level enables the driver differential outputs,A and B.Alowlevel places it in a high impedancestate.
4	DI	Driver Input.When the driver is enabled,a logic low on DI forces A low and B highwhile a logic high on DI forces A highand B low.
5	GND	Ground Connection,0V.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B
8	Vcc	Power Supply,5V±5%.

Test Circuits

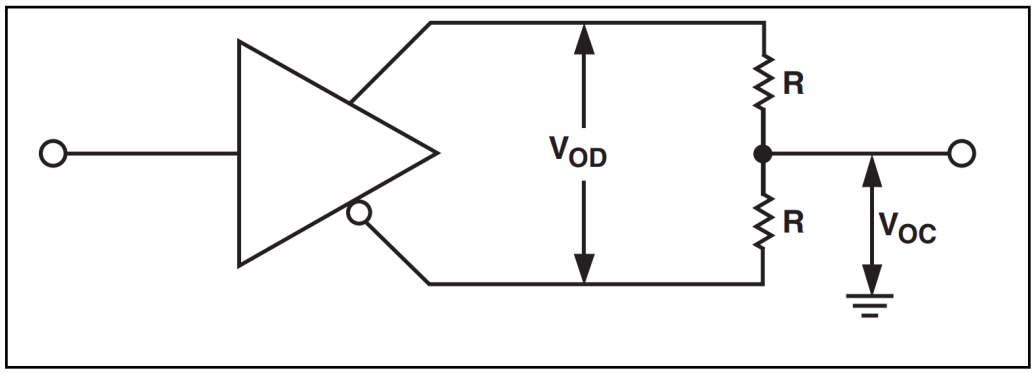


Figure1.Driver Voltage Measurement

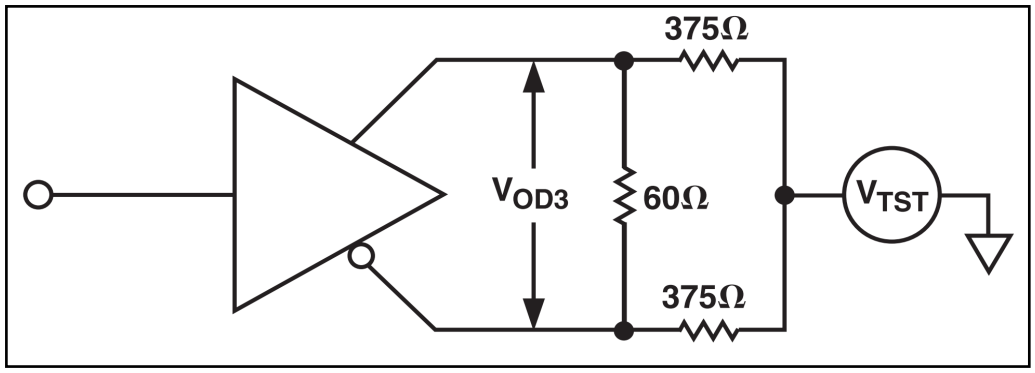


Figure 2. Driver Voltage Measurement

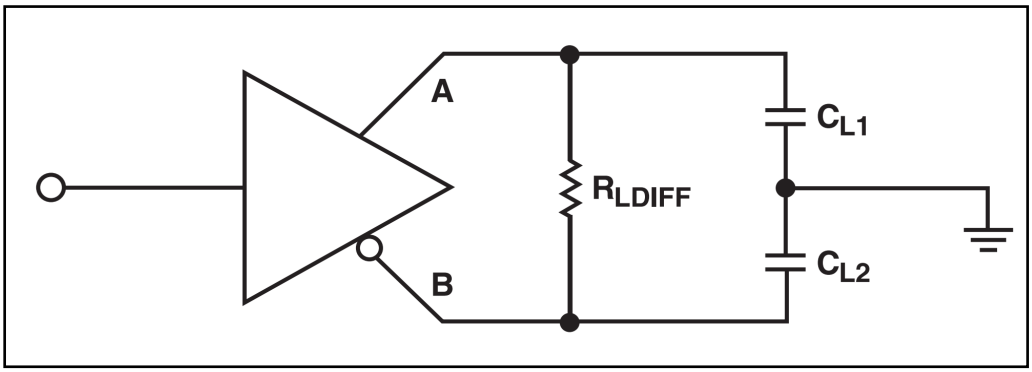


Figure 3. Driver Propagation Delay

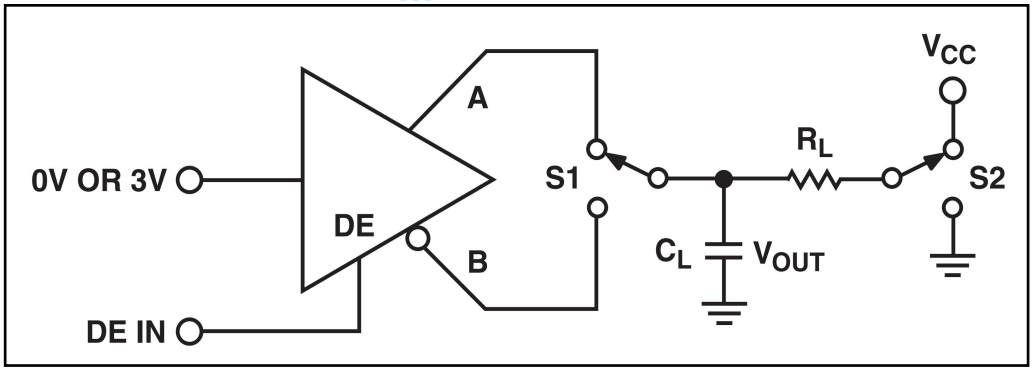


Figure 4. Driver Enable/Disable

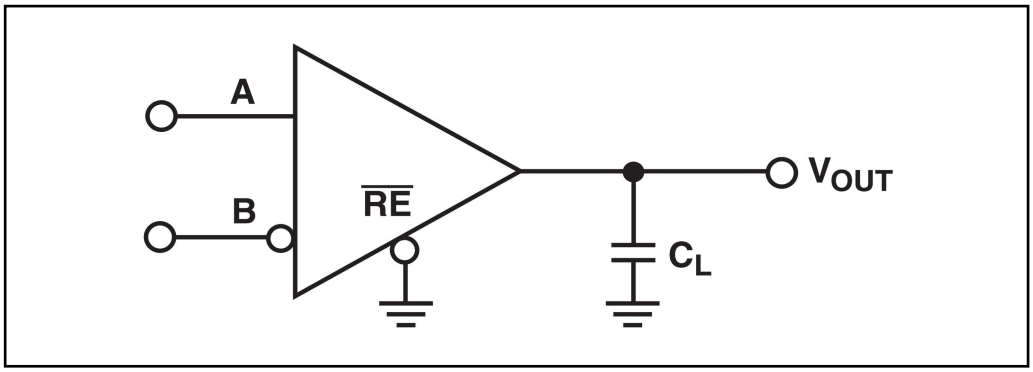


Figure 5. Receiver Propagation Delay

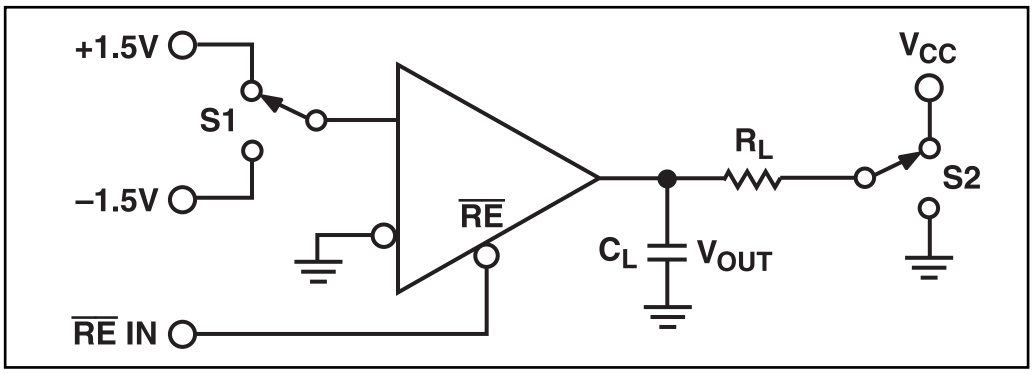


Figure 6. Receiver Enable/Disable

Switching Characteristics

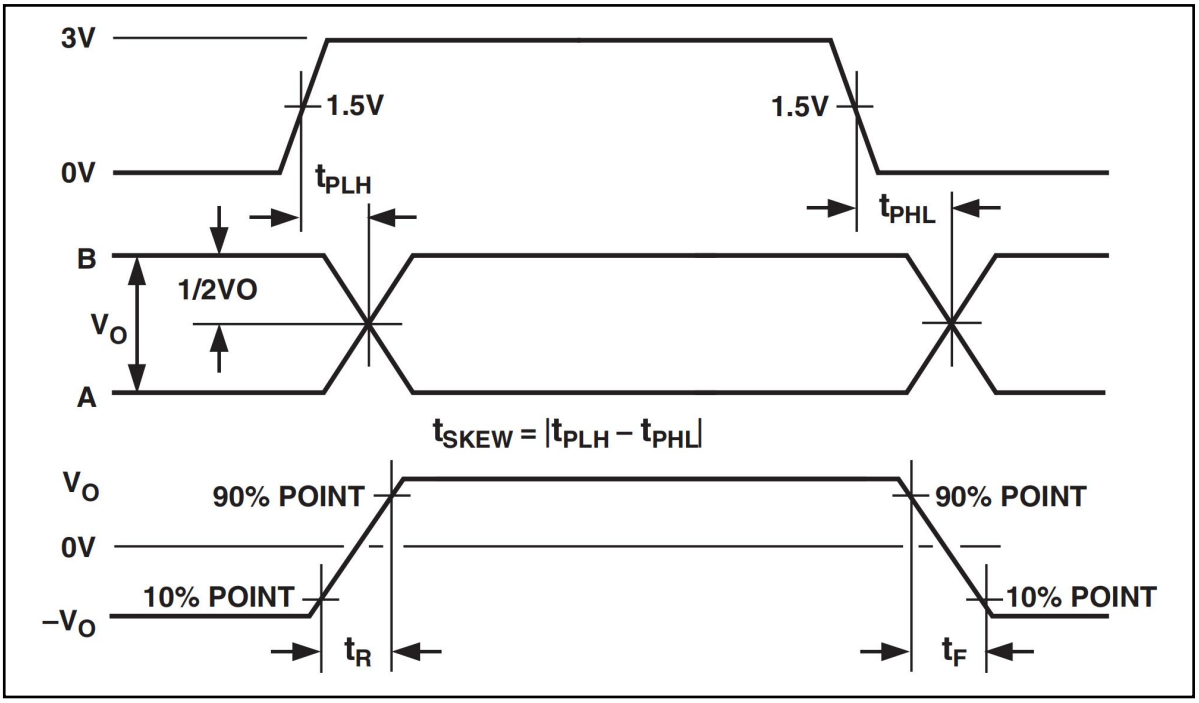


Figure 7. Driver Propagation Delay, Rise/Fall Timing

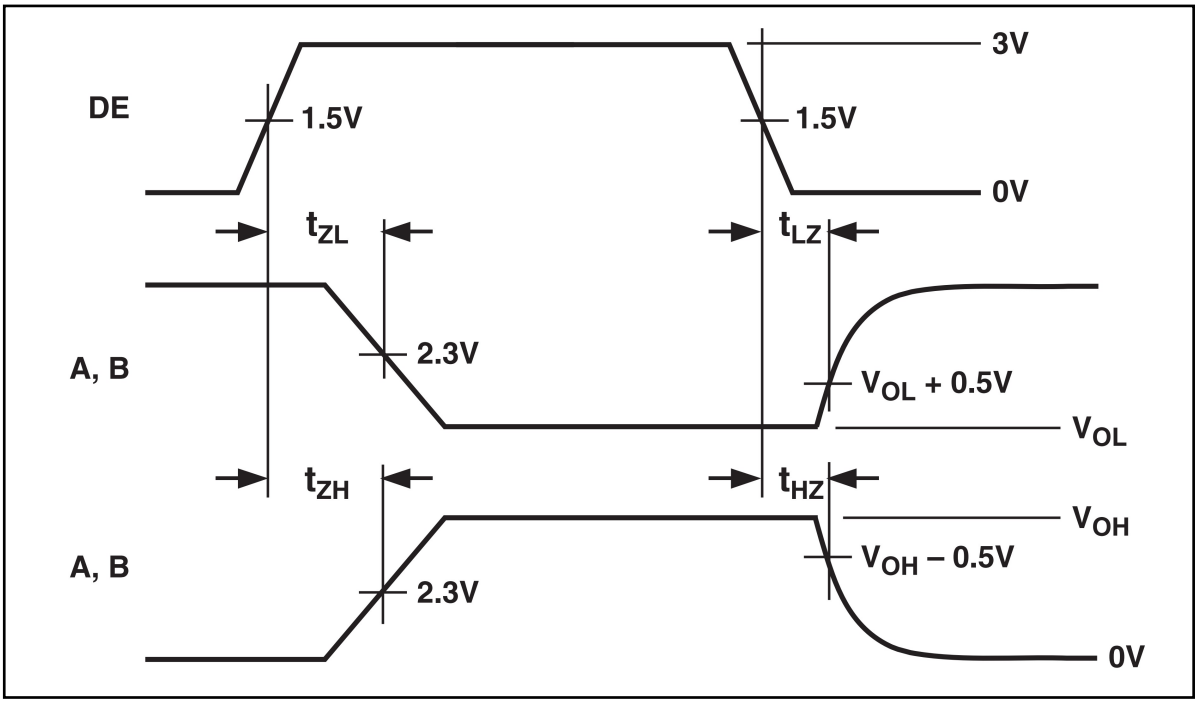


Figure 8. Driver Enable/Disable Timing

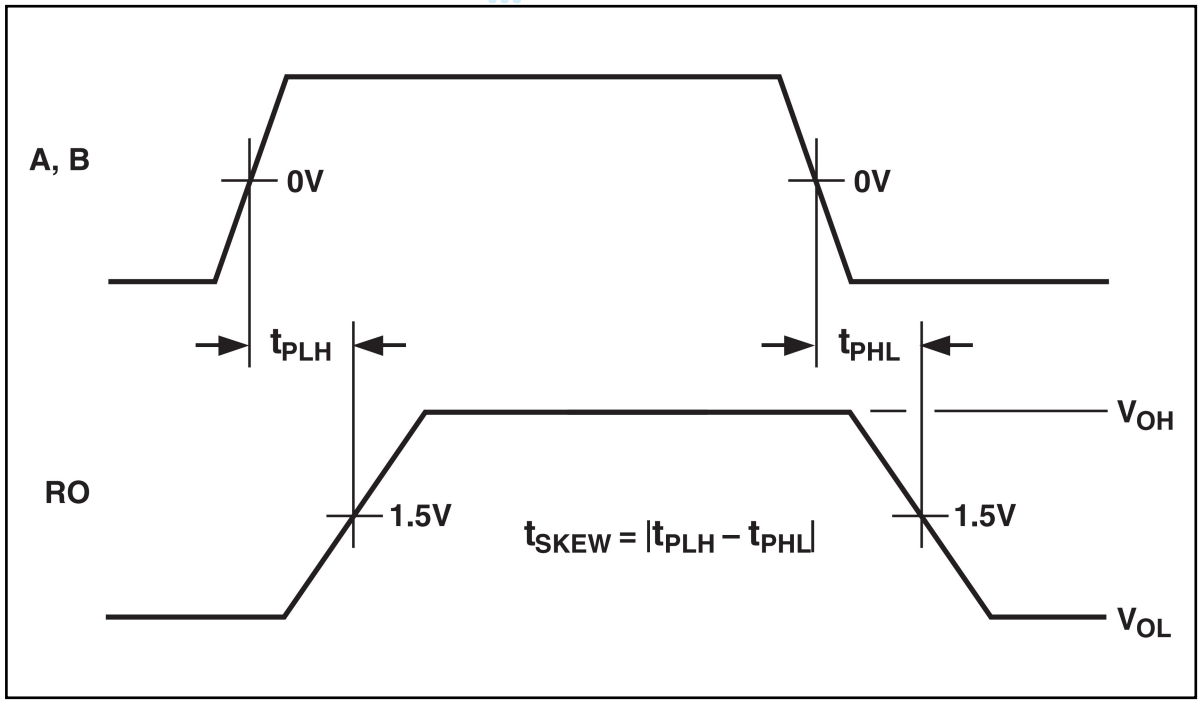


Figure 9. Receiver Propagation Delay

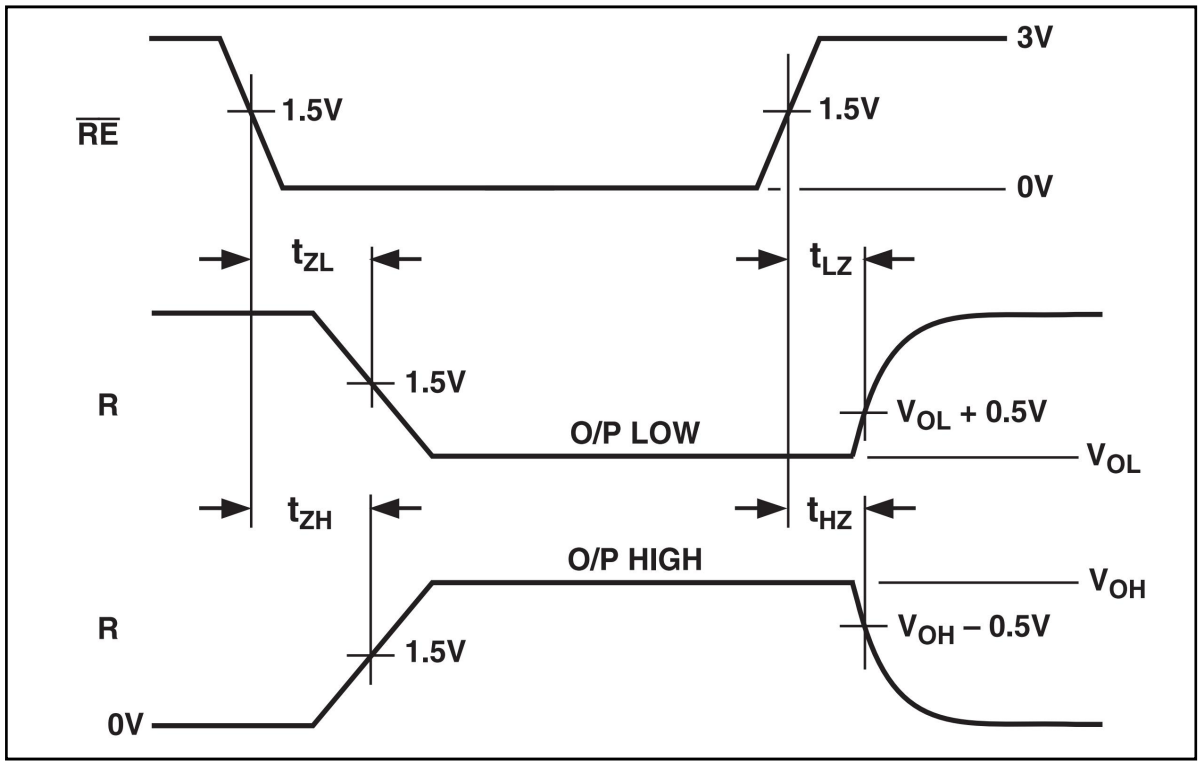


Figure 10. Receiver Enable/Disable Timing

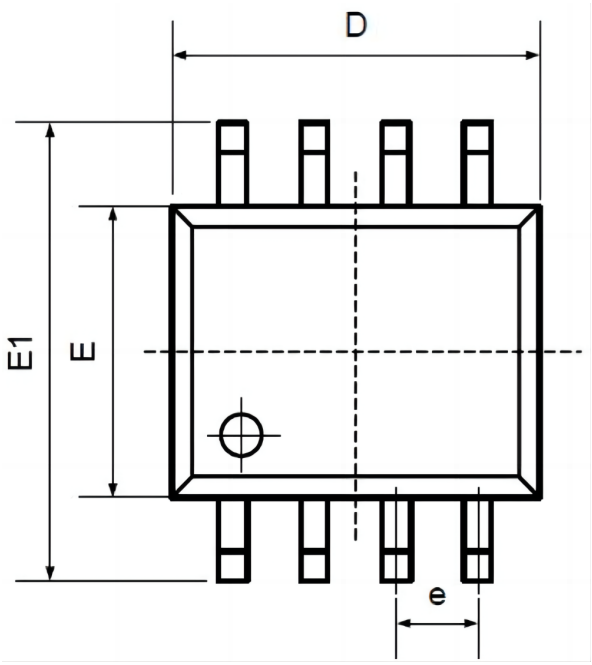
Order information

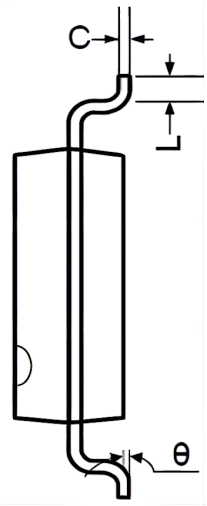
Order Number	Package	Package Quantity	Marking On The park	Temperature
ADM1485JNZ-TUDI	DIP8	Tube,50,A box of 2000	ADM1485J	0°C to 70°C
ADM1485JRZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM485ARZ	
ADM1485ANZ-TUDI	DIP8	Tube,50,A box of 2000	ADM1485A	-40°C to +85°C
ADM1485ARMZ-TUDI	MSOP8	Tape,Reel,4000	1485A	
			M42	
ADM1485ARZ-REEL-TUDI	SOP8	Tape,Reel,4000	ADM1485ARZ	

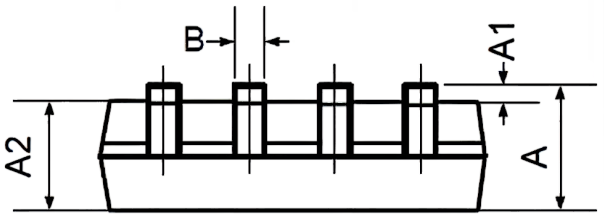
Revision history

	Date	Revision	Page
V1.0	2020/7	New	1-10
V1.1	2025-3	Update model and PDF template	1-16

Package SOP8

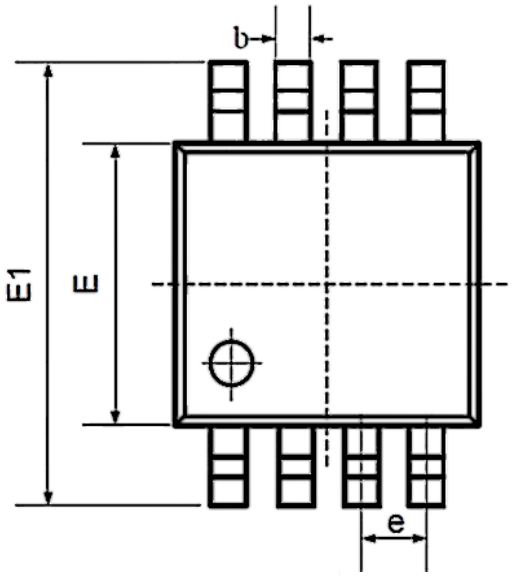


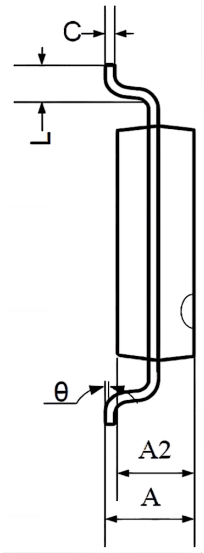


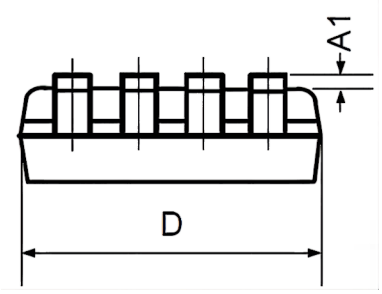


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package MSOP8

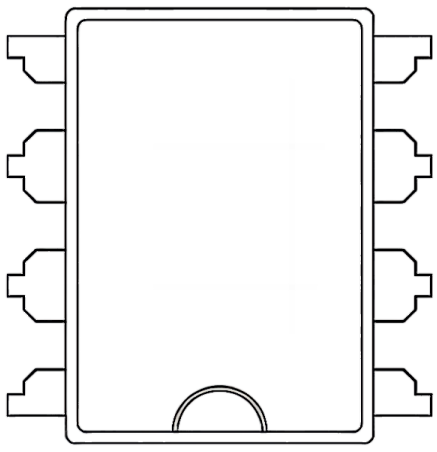


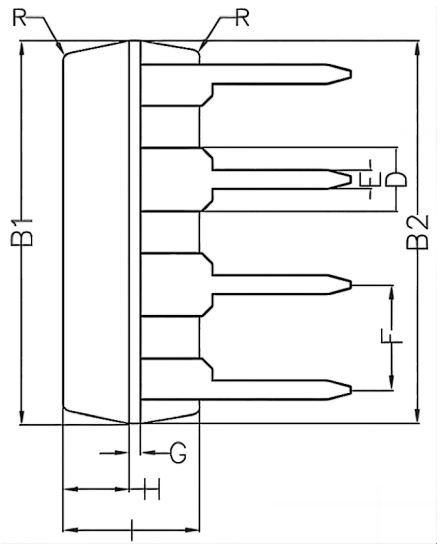


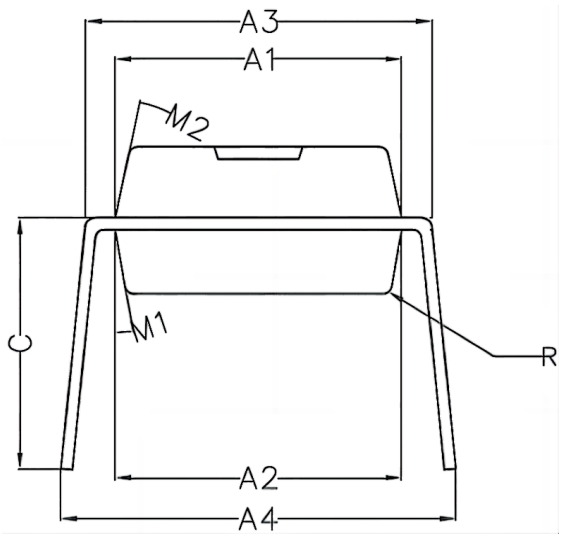


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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