钍地半导体
Tudi Semiconductor

Product Specification

TUDI-24AA64/24LC64

64K I^2C™ Serial EEPROM

网址 www.sztdbdt.com

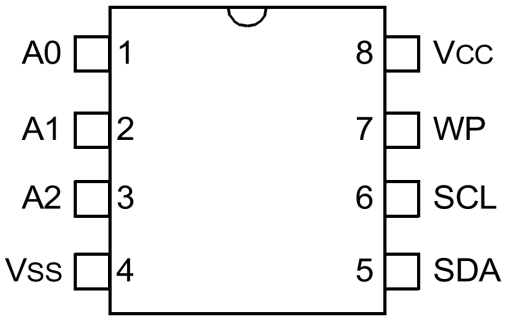
用芯智造·卓越品质

semiconductor device manufacturer

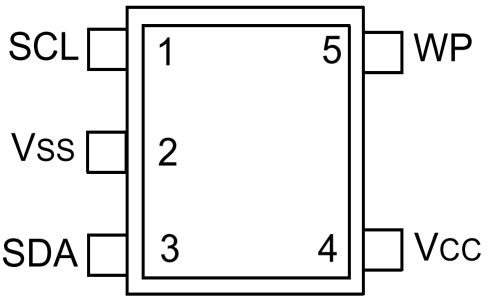
- Design
- research and development
- production
- and sales

Features

- ●Single-Supply with Operation down to 1.7V for 24AA64 Devices, 2.5V for 24LC64 Devices
- ●Low-Power CMOS Technology:
  - Active current 3 mA, max.
  - Standby current 1 µA, max.
- ●2-Wire Serial Interface, I^2C™ Compatible
- ●Packages with 3 Address Pins are Cascadable up to 8 Devices
- ●Schmitt Trigger Inputs for Noise Suppression
- ● Output Slope Control to Eliminate Ground Bounce
- ●100 kHz and 400 kHz Clock Compatibility
- ●1 MHz Clock for FC versions
- ●Page Write Time 5 ms, max.
- ●Self-timed Erase/Write Cycle
- ●32-Byte Page Write Buffer
- ●Hardware Write-Protect
- ●ESD Protection > 4,000V
- ●More than 1 Million Erase/Write Cycles
- ● Data Retention > 200 Years
- ●Factory Programming Available
- ●Packages include 8-lead PDIP, SOIC, TSSOP, X-Rotated TSSOP, SOT-23 or Chip Scale
- ●Pb-Free and RoHS Compliant
- ●Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C



SOP8/DIP8/TSSOP8

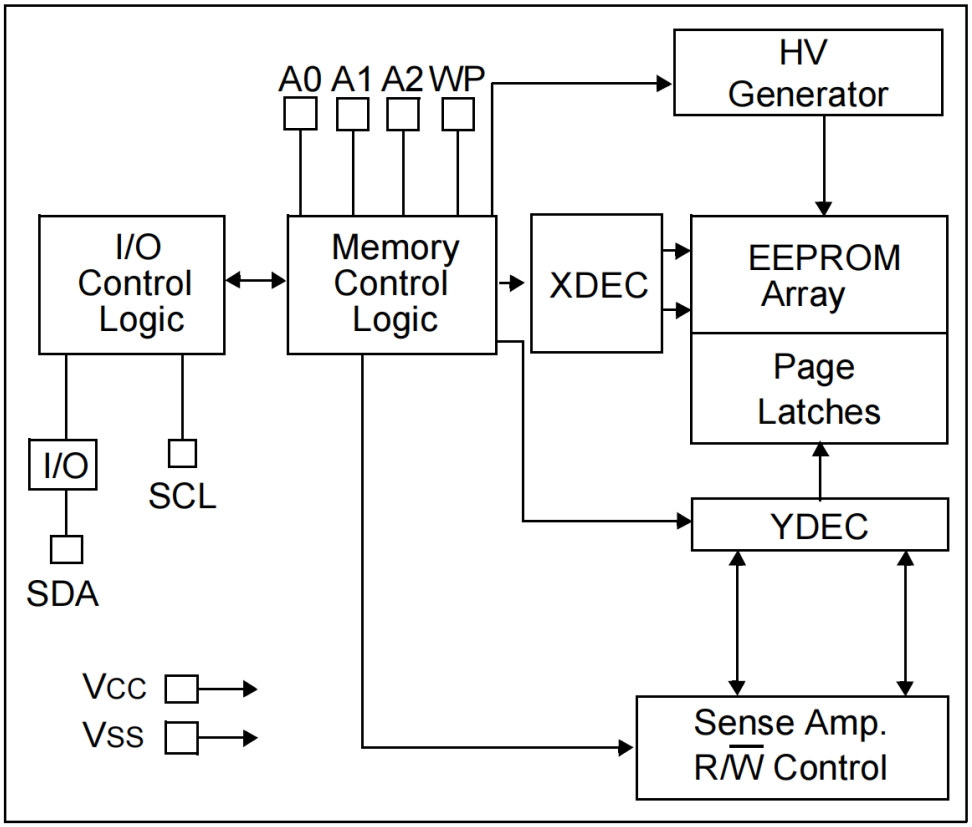


SOT-23

Description

The 24AA64/24LC64 (24XX64*) is a 64 Kbit Electrically ErasablePROM. The device is organized as a single block of 8K x 8-bit memory with a 2 wire serial interface. Low-voltage design permits operation down to 1.7V, with standby and active currents ofonly 1 µA and 3 mA, respectively. It has been developed for advanced, low-power applications such as personal communications or data acquisition. The 24XX64 also has a page write capability for up to 32 bytes of data. Functional address lines allow up to eight devices on the same bus, for up to 512 Kbits address space. The 24XX64 is available in the standard 8-pin PDIP, surface mount SOIC, DIP,TSSOP packages. The 24XX64 is also available in the 5-lead SOT-23, and Chip Scale packages.

Block Diagram



Absolute Maximum Ratings

V_{CC}.....6.5V
All inputs and outputs w.r.t. V_{SS} ..... -0.3V to V_{CC} +1.0V
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-40°C to +125°C
ESD protection on all pins.....4 kV

NOTICE: Stresses above those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA=-40°C to +85°C,Vcc=+1.7V to +5.5V Automotive(E):TA=-40°C to+125°C,Vcc=+1.7V to+5.5V				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
	—	A0,A1,A2,WP,SCL and SDA pins	—	—	—	—	—
D1	V_{IH}	High-level input voltage	0.7 Vcc	—	—	V	—
D2	V_{IL}	Low-level input voltage	—	—	0.3 Vcc 0.2 Vcc	V V	Vcc≥2.5V Vcc<2.5V
D3	V_{HYS}	Hysteresis of Schmitt Trigger inputs (SDA,SCL pins)	0.05 Vcc	—	—	V	Vcc≥2.5V(Note 1)
D4	V_{OL}	Low-level output voltage	—	—	0.40	V	I_{OL}=3.0mA @Vcc=4.5V I_{OL}=2.1mA @Vcc=2.5V
D5	I_{LI}	Input leakage current	—	—	±1	μA	V_{IN} =Vss or Vcc,WP=Vss V_{IN} =Vss or Vcc,WP=Vcc
D6	I_{LO}	Output leakage current	—	—	±1	μA	V_{OUT} =Vss or Vcc
D7	C_{IN}, C_{OUT}	Pin capacitance(all inputs/outputs)	—	—	10	pF	Vcc=5.0V(Note 1 T_A=25°C,F_{CLK}=1 MHz
D8	Icc write	Operating current	—	0.1	3	mA	Vcc=5.5V,SCL=400 kHz
D9	Icc read		—	0.05	400	μA	
D10	Iccs	Standby current	—	0.01	1	μA	Industrial
			—	—	5	μA	Automotive SDA=SCL=Vcc A0,A1,A2,WP=Vss

Note 1: This parameter is periodically sampled and not 100% tested.
2: Typical measurements taken at room temperature.

TABLE 2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics:Industrial (I): Vcc=+1.7V to 5.5V TA=-40°C to +85°CAutomotive (E): Vcc=+1.7V to 5.5V TA=-40°C to 125°C			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
1	FCLK	Clock frequency	— —	100 400	kHz	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
2	THIGH	Clock high time	4000 600	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
3	TLOW	Clock low time	4700 1300	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤ 5.5V
4	TR	SDA and SCL rise time (Note 1)	— —	1000 300	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
5	TF	SDA and SCL fall time (Note 1)	—	300	ns	All except,24FC64
6	THD:STA	Start condition hold time	4000 600	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
7	TSU:STA	Start condition setup time	4700 600	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
8	THD:DAT	Data input hold time	0	—	ns	(Note 2)
9	TSU:DAT	Data input setup time	250 100	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
10	TSU:STO	Stop condition setup time	4000 600	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
11	TSU:WP	WP setup time	4000 600	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V
12	THD:WP	WP hold time	4700 1300	— —	ns	1.7V≤Vcc<2.5V 2.5V≤Vcc≤5.5V

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

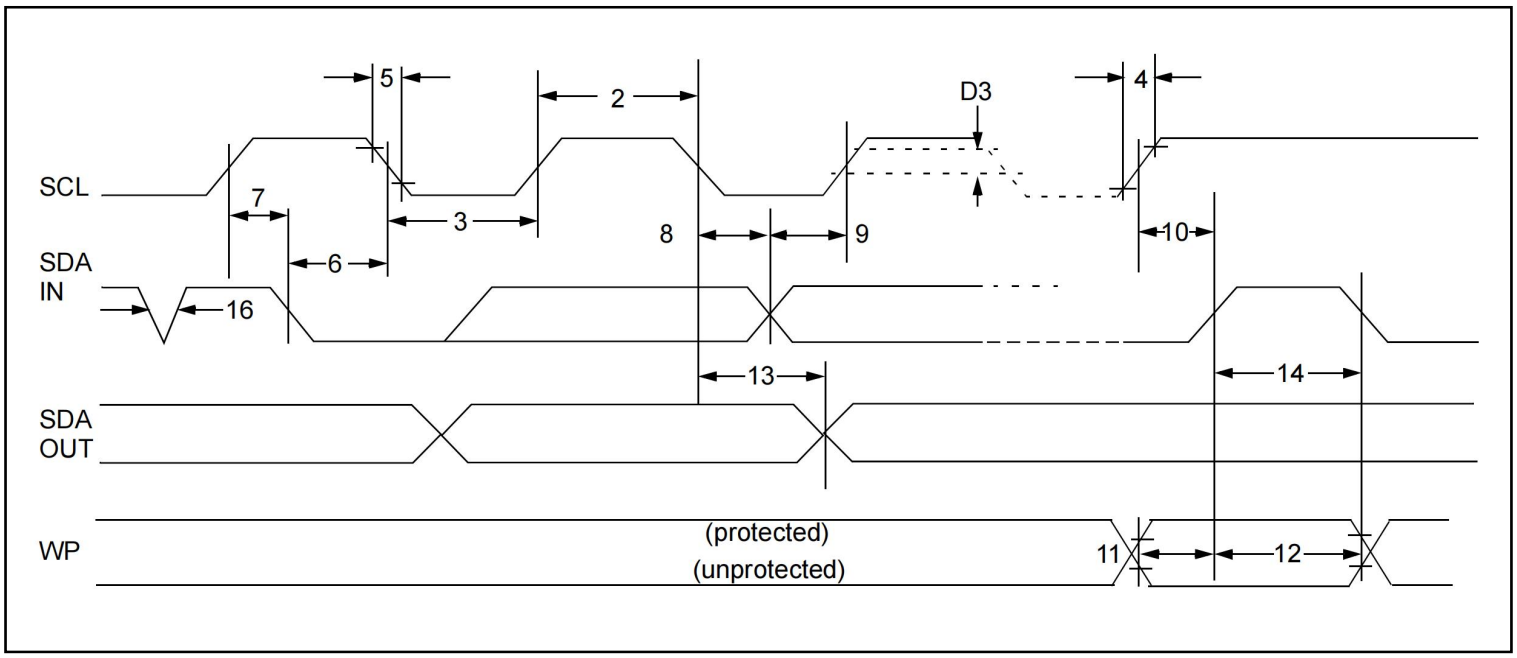


FIGURE 1: BUS TIMING DATA

PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3.

TABLE 3: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	SOT-23	Description
A0	1	1	1	—	Chip Address Input
A1	2	2	2	—	Chip Address Input
A2	3	3	3	—	Chip Address Input
V_{SS}	4	4	4	2	Ground
SDA	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	1	Serial Clock
WP	7	7	7	5	Write-Protect Input
V_{CC}	8	8	8	4	+1.7V to 5.5V Power Supply

A0, A1, A2 Chip Address Inputs :The A0, A1 and A2 inputs are used by the 24XX64 for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.
Up to eight devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either V_{CC} or V_{SS}.
In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic ‘ 0 ’ or logic ‘ 1 ’. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic ‘ 0 ’ or logic ‘ 1 ’ before normal device operation can proceed. Address pins are not available in the SOT-23 or Chip Scal packages.

Serial Data (SDA): SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to V_{CC} (typical 10 kΩ for 100 kHz, 2 kΩfor 400 kHz).
For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

Serial Clock (SCL)：The SCL input is used to synchronize the data transfer from and to the device.

Write-Protect (WP)：This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited but read operations are not affected.

FUNCTIONAL DESCRIPTION

The 24XX64 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX64 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

BUS CHARACTERISTICS：The following bus protocol has been defined:

●Data transfer may be initiated only when the bus is not busy

●During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition

Accordingly, the following bus conditions have been defined (Figure 2).

Bus Not Busy (A)：Both data and clock lines remain high.

Start Data Transfer (B) ：A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

Stop Data Transfer (C)：A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

Data Valid (D)：The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device and is, theoretically, unlimited (although only the last thirty two will be stored when doing a write operation). When an overwrite does occur, it will replace data in a first-in first-out (FIFO) fashion.

Acknowledge：Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX64) will leave the data line high to enable the master to generate the Stop condition.

Note: The 24XX64 does not generate any Acknowledge bits if an internal programming cycle is in progress.

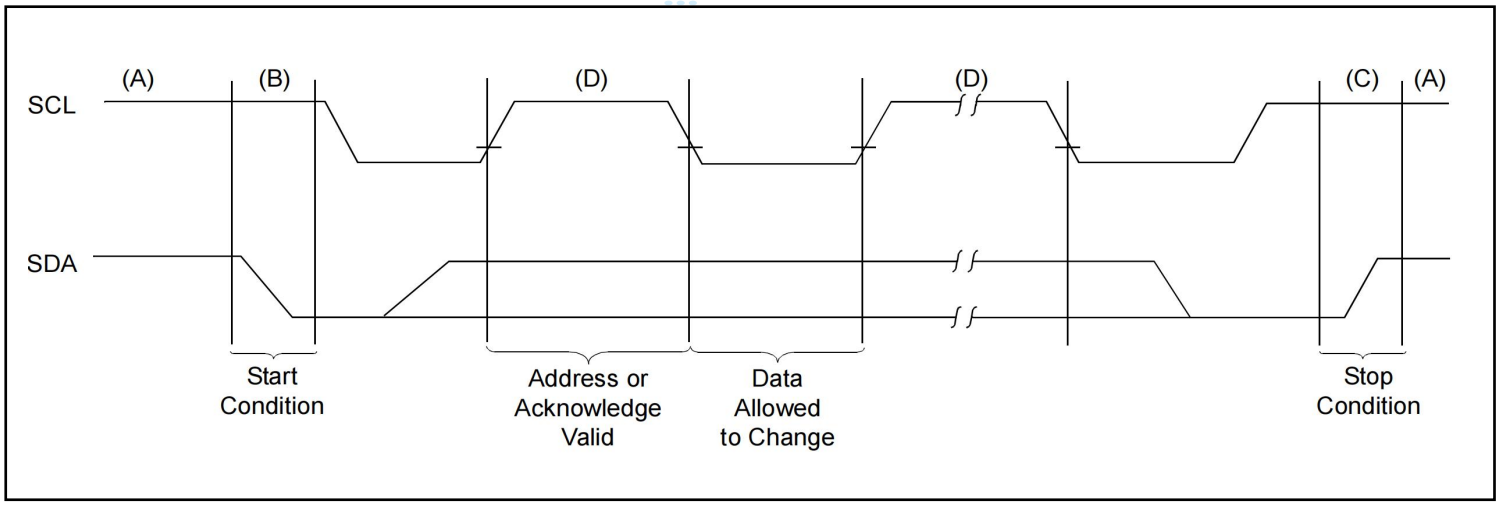


FIGURE 2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 3). The control byte consists of a four-bit control code. For the 24XX64, this is set as ‘1010’ binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX64 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are, in effect, the three Most Significant bits of the word address.
For the SOT-23 and Chip Scale packages, the address pins are not available. During device addressing, the A2,A1 and A0 Chip Select bits (Figure 4) should be set to ‘0’.
The last bit of the control byte defines the operation to be performed. When set to a ‘1’, a read operation is selected. When set to a ‘0’, a write operation is selected. When set to a ‘0’, a write operation is selected. The next two bytes receive ddefine the address of the first data byte (Figure 5-2). Because only A12...A0 are used, the upper-three address bits are “don’t care” bits. The upper-address bits are transferred first, followed by theLess Significant bits.
Following the Start condition, the 24XX64 monitors the SDA bus, checking the device-type identifier being transmitted. Upon receiving a ‘1010’ code and appro-priate device-select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24XX64 will select a read or write operation.

Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24XX64 devices on the same bus. In this case, software can use A0 of the control byte as address bit A13; A1 as address bit A14; and A2 as address bit A15. It is not possible to sequentially read across device boundaries.

The SOT-23 and Chip Scale packages do not support multiple device addressing on the same bus.

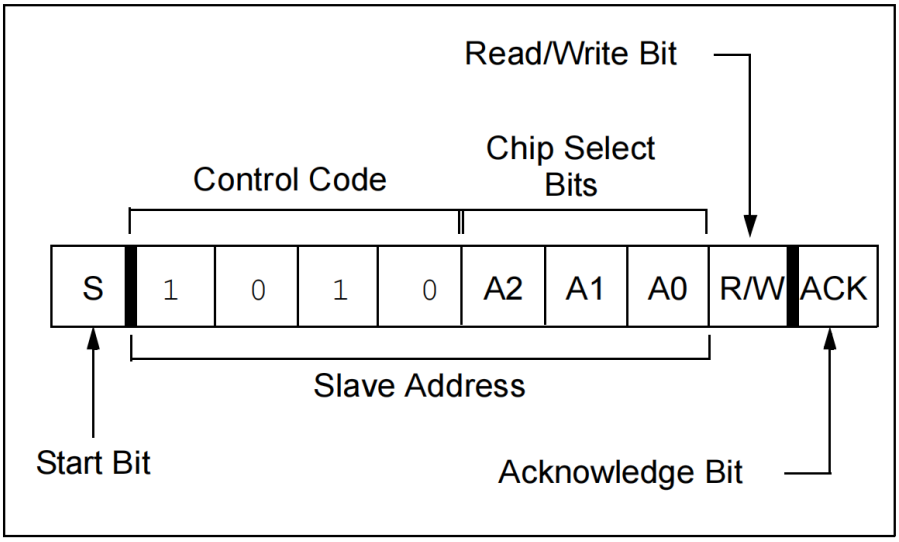


FIGURE 3: CONTROL BYTE FORMAT

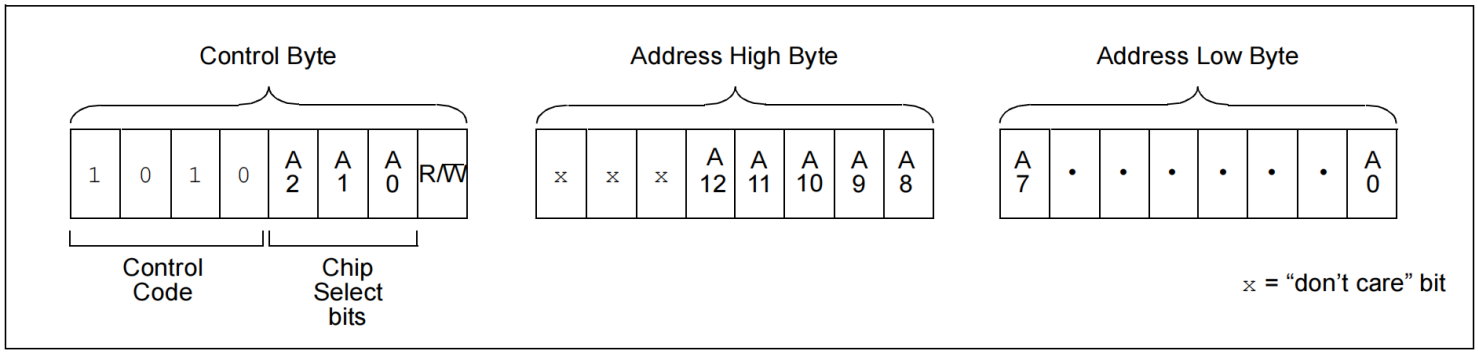


FIGURE 4: ADDRESS SEQUENCE BIT ASSIGNMENTS

Byte Write：Following the Start condition from the master, the control code (four bits), the Chip Select (three bits) and the R/W bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmit-ted by the master is the high-order byte of the word address and will be written into the Address Pointer of the 24XX64. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX64, the master device will transmit the data word to be written into the addressed memory location. The 24XX64 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX64 will not generate Acknowledge signals (Figure 5). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal address coun-ter will point to the address location following the one that was just written.

Note: When doing a write of less than 32 bytes the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page toendure a write cycle, for this reason endurance is specified per page.

Page Write：The write control byte, word address and the first data byte are transmitted to the 24XX64 in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to 31 additional bytes which are temporarily stored in the on-chip page buffer and will be written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the five lower Address Pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation,once the Stop condition is received, an inter-nal write cycle will begin (Figure 6). If an attempt ismade to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written, and the device will immediately accept a new command.

Note: Page write operations are limited to writ-ing bytes within a single physical page,regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘ page size ’) and end at addresses that are integer multiples of [page size － 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

Write Protection：The WP pin allows the user to write-protect the entire array (0000-1FFF) when the pin is tied to Vcc. If tied to Vss the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 2). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

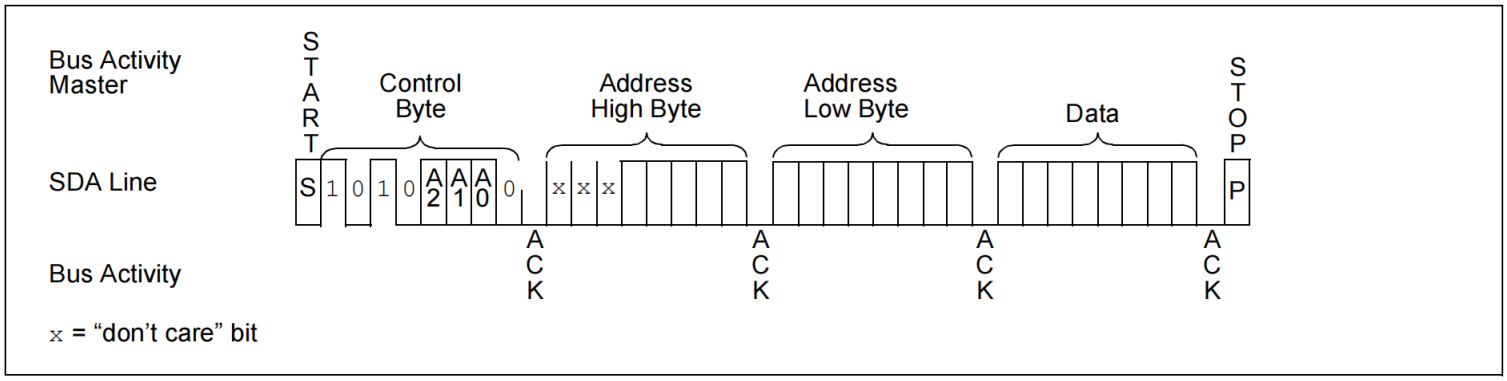


FIGURE 5: BYTE WRITE

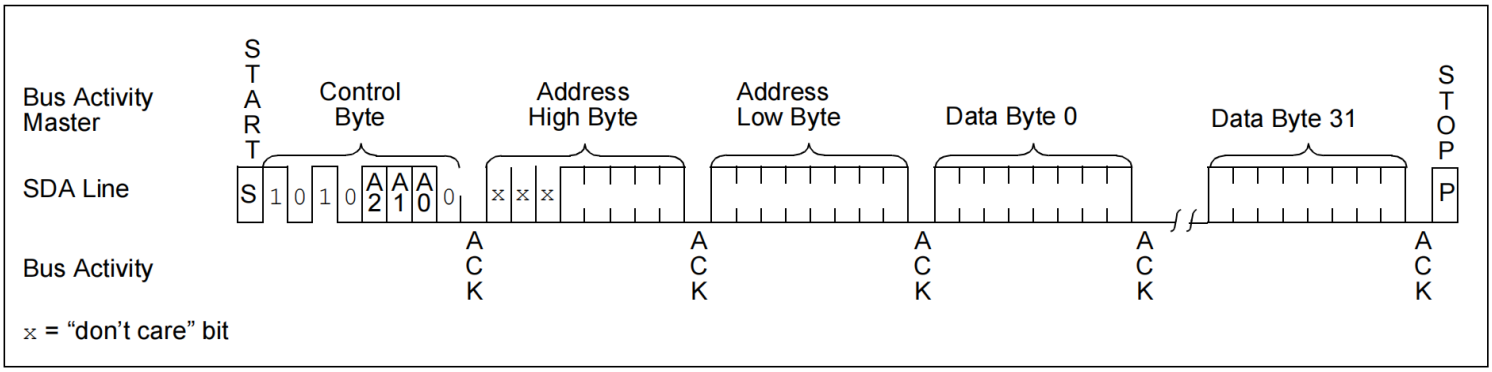


FIGURE 6: PAGE WRITE

ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally -timed write cycle and ACK polling can then be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7 for a flow diagram of this operation.

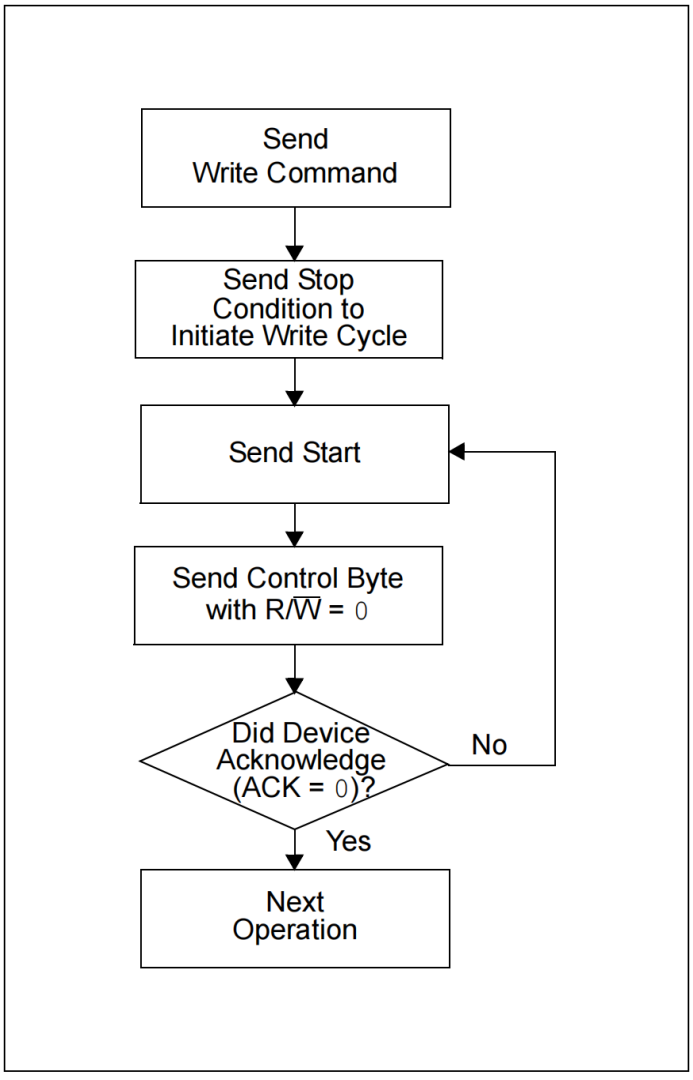


FIGURE 7: ACKNOWLEDGE POLLING FLOW

READ OPERATION: Read operations are initiated in the same way as write operations, with the exception that the R/W bit of the control byte is set to one. There are three basic types of read operations: current address read, random read and sequential read.

Current Address Read： The 24XX64 contains an address counter that main-tains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address ‘ n ’ (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the control byte with R/W bit set to one, the 24XX64 issues an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XX64 discontinues transmission (Figure 8).

Random Read ：Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX64 as part of a write operation (R/W bit set to ‘ 0 ’). Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/W bit set to a one. The 24XX64 will then issue an acknowl-edge and transmit the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition, which causes the 24XX64 to discontinue transmission (Figure 9). After a random Read command, the internal address coun-ter will point to the address location following the one that was just read.

Sequential Read：Sequential reads are initiated in the same way as random reads, except that once the 24XX64 transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX64 to transmit the next sequentially-addressed 8-bit word (Figure 10). Following the final byte being transmitted to the master, the master will NOT generate an acknowledge, but will generate a Stop condition. To provide sequential reads, the 24XX64 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one opera-tion. The internal Address Pointer will automatically roll over from address 1FFF to address 0000 if the master acknowledges the byte received from the array address 1FFF.

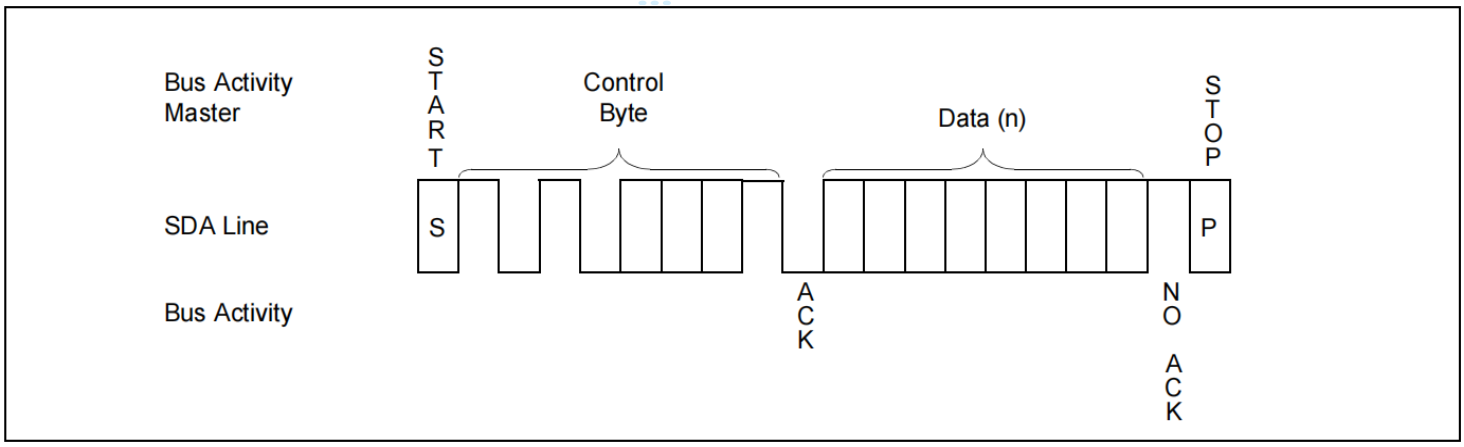


FIGURE 8: CURRENT ADDRESS READ

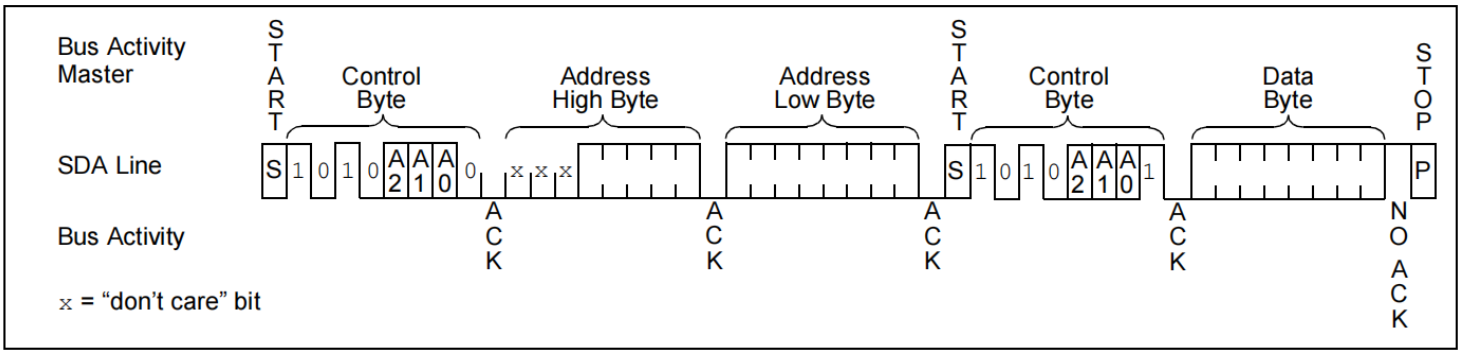


FIGURE 9: RANDOM READ

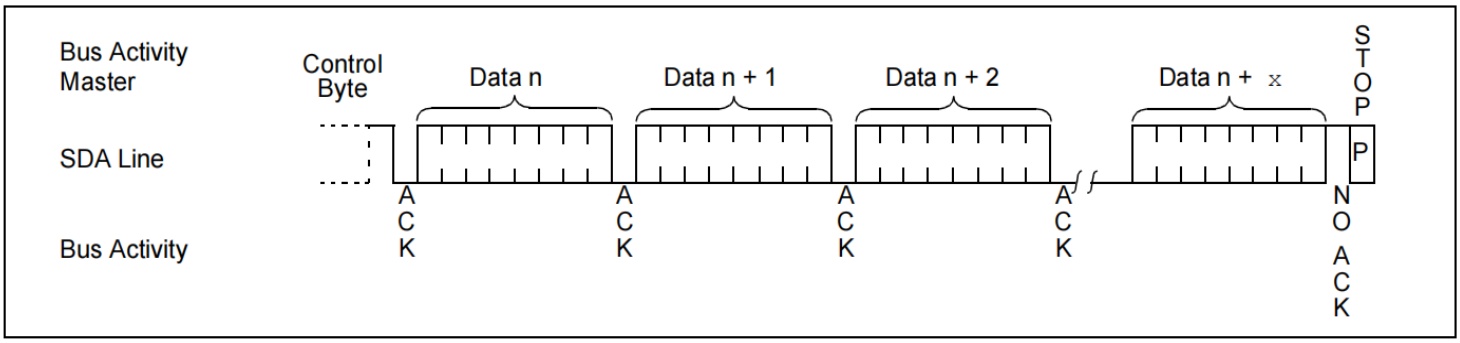


FIGURE 10: SEQUENTIAL READ

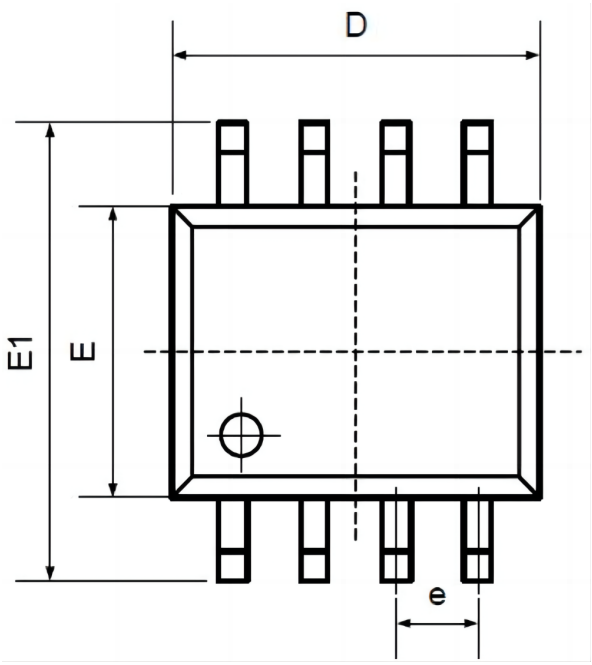
Order information

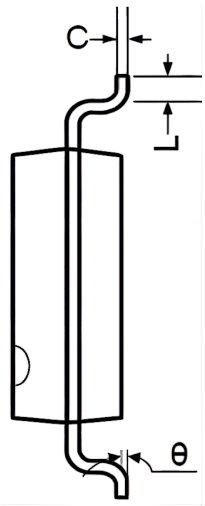
Order Number	Package	Package Quantity	Marking On The park	Temperature
24AA64-I/P-TUDI	DIP8	Tube,50,A box of 2000	24AA32A-I/P	-40C to +85℃
24AA64T-I/SN-TUDI	SOP8	Tape,Reel,4000	24AA64I/SN	
24AA64T-I/ST-TUDI	TSSOP8	Tape,Reel,4000	24AA64	
			4AB	
24AA64T-I/OT-TUDI	SOT23-5	Tape,Reel,3000	7Hxx	
24LC64-I/P-TUDI	DIP8	Tube,50,A box of 2000	24LC64-I/P	
24LC64T-I/SN-TUDI	SOP8	Tape,Reel,4000	24LC64I/SN	
24LC64T-I/ST-TUDI	TSSOP8	Tape,Reel,4000	24LC64	
			4LB	
24LC64T-I/OT-TUDI	SOT23-5	Tape,Reel,3000	7Gxx	
24LC64-E/P-TUDI	DIP8	Tube,50,A box of 2000	24LC64-E/P	-40°C to +125°C
24LC64T-E/OT-TUDI	SOT23-5	Tape,Reel,3000	7Jxx	
24LC64T-E/SN-TUDI	SOP8	Tape,Reel,4000	24LC64E/SN	
24LC64T-E/ST-TUDI	TSSOP8	Tape,Reel,4000	4LB	

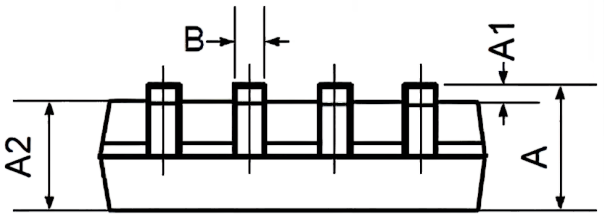
Revision history

	Date	Revision	Page
V1.0	2021/3	New	1-17
V1.1	2025/7	Update model and PDF template	1-21

Package SOP8

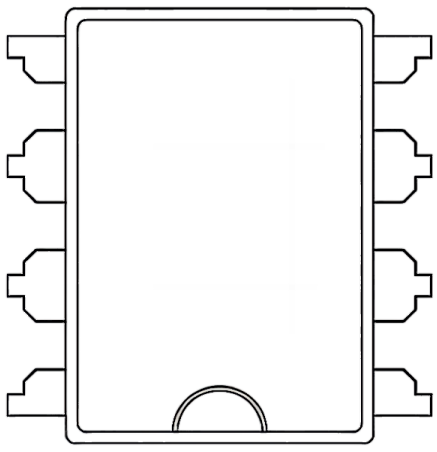


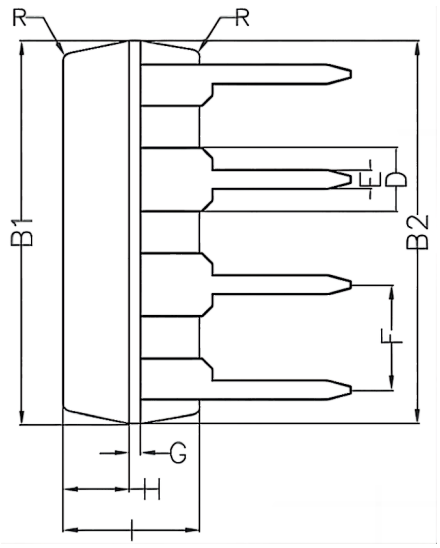


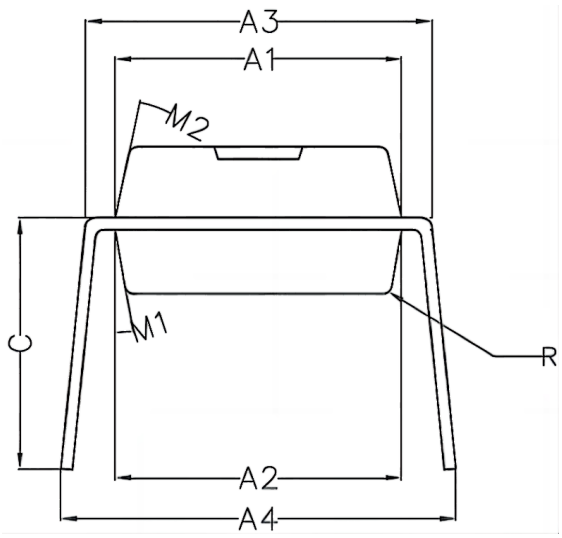


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8

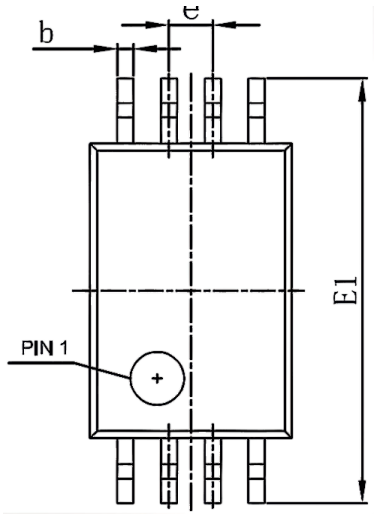


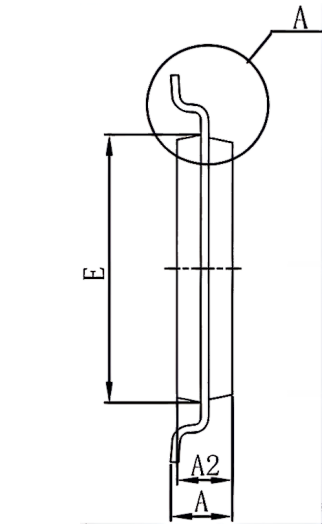


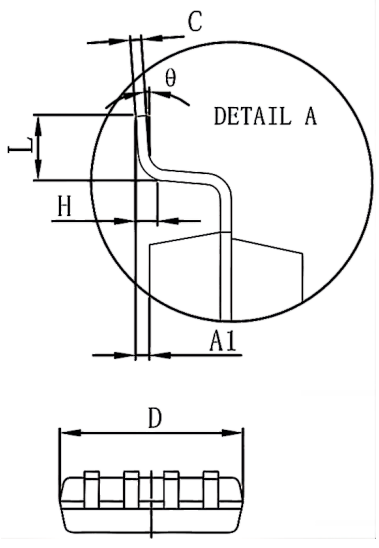


Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Package TSSOP8

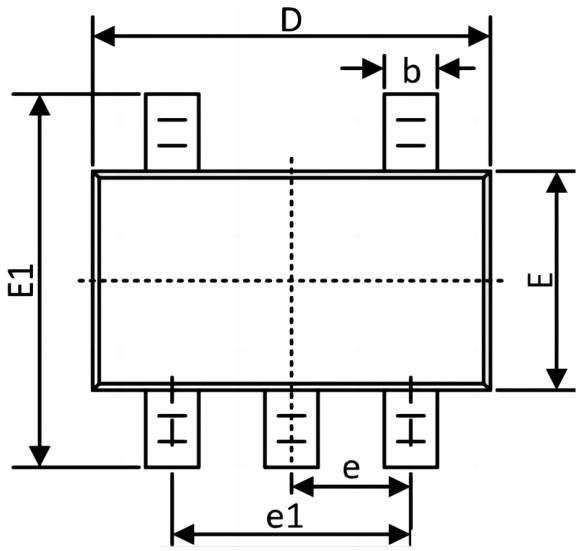


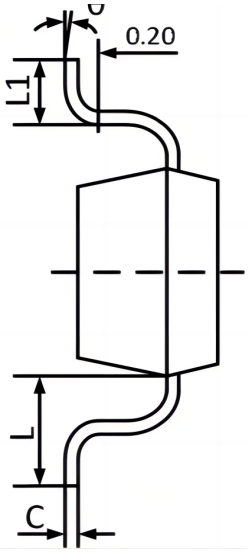


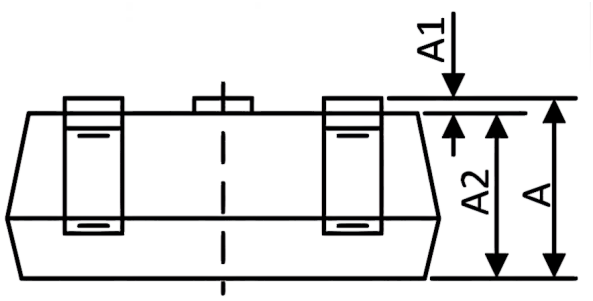


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

Package SOT23-5







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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