钍地半导体
Tudi Semiconductor

Product Specification

TUDI-24AA04/24LC04B

4K I^2C Serial EEPROM

网址 www.sztdbdt.com

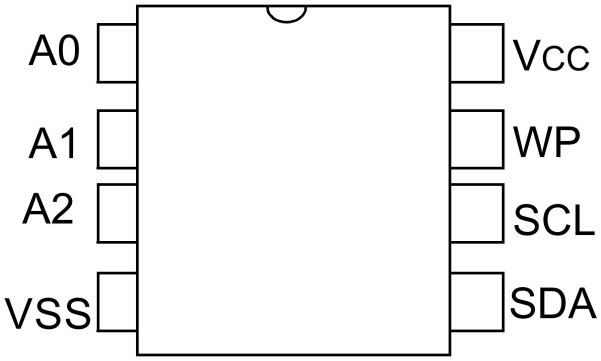
用芯智造·卓越品质

semiconductor device manufacturer

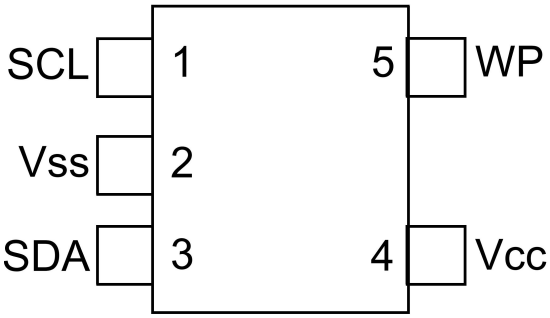
- Design
- research and development
- production
- and sales

Features

- Single Supply with Operation down to 1.7V for 24AA04 Devices, 2.5V for 24LC04B Devices
- Low-Power CMOS Technology:
  - Read current 1 mA, maximum
  - Standby current 1 µA, maximum (I-temp.)
- Two-Wire Serial Interface, I2C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz, 400 kHz and 1 MHz Compatibility
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection >4,000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 Years
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified



SOP8/DIP8/TSSOP8

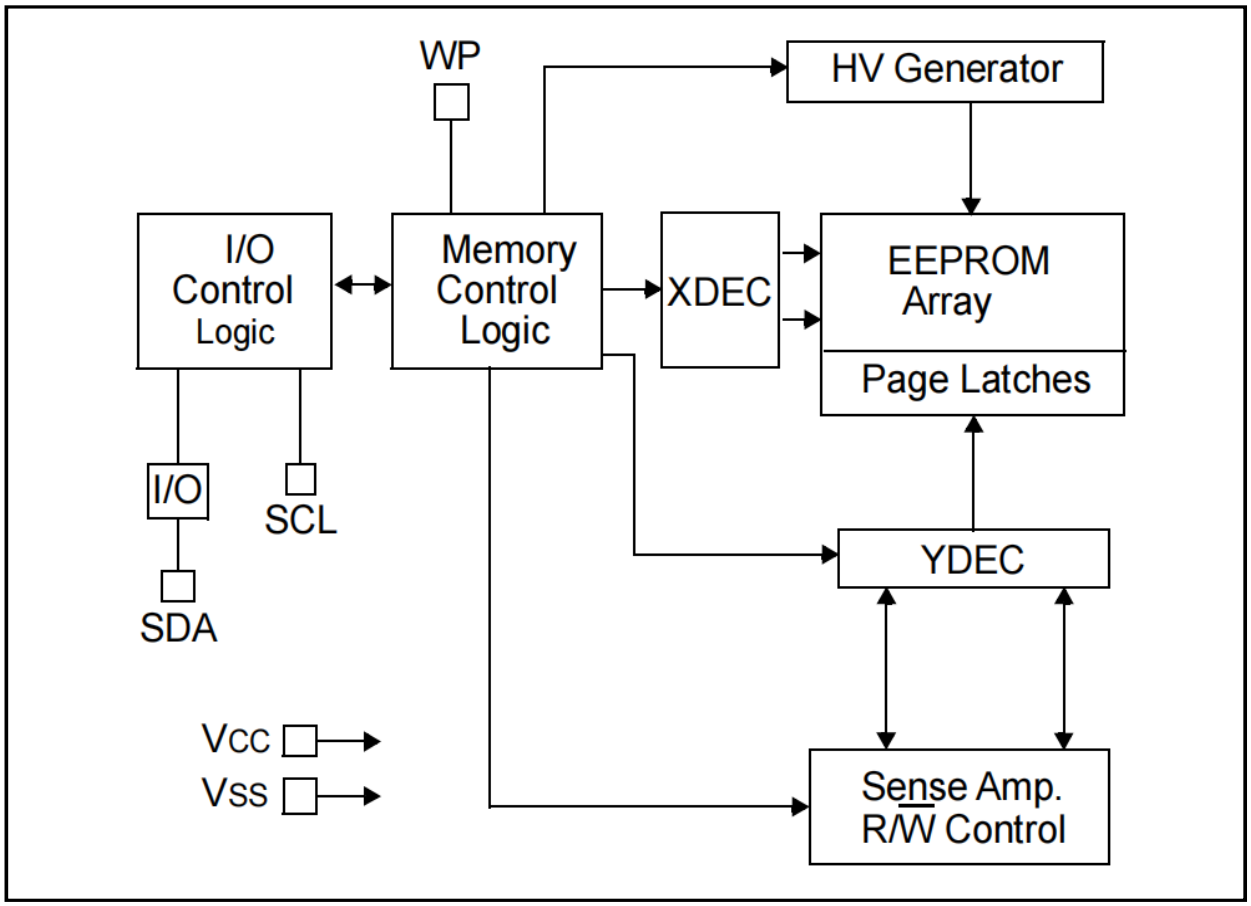


SOT-23

Description

The 24XX04 is a 4-Kbit Electrically Erasable PROM (EEPROM). The device is organized as two blocks of 256 x 8-bit memory with a two-wire serial interface. Its low-voltage design permits operation down to 1.7V with standby and active currents of only 1 µA and 1 mA, respectively. The 24XX04 also has a page write capability for up to 16 bytes of data.

Block Diagram



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{CC}.....6.5V
All inputs and outputs w.r.t. V_{SS} .....-0.3V to V_{CC} +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied..... -40°C to +125°C
ESD protection on all pins .....4 kV

NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial(I):T_A=-40°C to +85°C,V_{CC}=+1.7V to +5.5V Extended(E):T_A=-40°C to+125°C,V_{CC}=+2.5V to+5.5V(24LC04B)				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
D1	V_{IH}	High-Level Input Voltage	0.7 V_{CC}	—	—	V	
D2	V_{IL}	Low-Level Input Voltage	—	—	0.3 V_{CC}	V	
D3	V_{HYS}	Hysteresis of Schmitt Trigger Inputs	0.05 V_{CC}	—	—	V	Note
D4	V_{OL}	Low-Level OutputVoltage	—	—	0.40	V	I_{OL}=3.0 mA,V_{CC}=2.5V
D5	I_{LI}	Input Leakage Current	—	—	± 1	µA	V_{IN}=V_{SS} or V_{CC}
D6	I_{LO}	Output Leakage Current	—	—	±1	µA	V_{OUT} =V_{SS} or V_{CC}
D7	C_{IN}, C_{OUT}	Pin Capacitance(all inputs/outputs)	—	—	10	pF	V_{CC}=5.0V(Note) T_A=25°C,F_{CLK}=1 MHz
D8	$I_{CCWRITE}$	Operating Current	—	—	3	mA	V_{CC}=5.5V,SCL=400 kHz
D9	I_{CCREAD}		—	—	1	mA	V_{CC}=5.5V,SCL=400 kHz
D10	I_{CCS}	Standby Current	—	—	1	µA	SDA=SCL=V_{CC} WP=V_{SS},I-Temp.
			—	—	3	µA	SDA=SCL=V_{CC} WP=V_{SS},E-Temp.
			—	—	5	µA	SDA=SCL=V_{CC} WP=V_{SS},E-Temp. (24LC04B)

Note: This parameter is periodically sampled and not 100% tested.

TABLE 2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial(I):T_A=-40°C to +85°C,V_{CC}=+1.7V to+5.5V Extended(E):T_A=-40°C to+125°C,V_{CC}=+2.5V to+5.5V (24LC04B)				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
1	F_{CLK}	Clock Frequency	—	—	400	kHz	2.5V≤V_{CC}≤5.5V
			—	—	100	kHz	1.7V≤V_{CC}<2.5V(24AA04)
			—	—	1000	kHz	1.7V≤V_{CC}≤5.5V
2	T_{HIGH}	Clock High Time	600	—	—	ns	2.5V≤V_{CC}≤5.5V
			4000	—	—	ns	1.7V≤V_{CC}<2.5V (24AA04)
			260	—	—	ns	1.7V≤V_{CC}≤5.5V
3	T_{LOW}	Clock Low Time	1300	—	—	ns	2.5V≤V_{CC}≤5.5V
			4700	—	—	ns	1.7V≤V_{CC}<2.5V (24AA04)
			500	—	—	ns	1.7V≤V_{CC}≤5.5V
4	T_R	SDA and SCL Rise Time	—	—	300	ns	2.5V≤V_{CC}≤5.5V(Note 1)
			—	—	1000	ns	1.7V≤V_{CC}<2.5V(24AA04) (Note 1)
			—	—	1000	ns	1.7V≤V_{CC}≤5.5V (Note 1)
5	T_F	SDA and SCLF all Time	—	—	300	ns	Note 1
6	$T_{HD:STA}$	Start Condition Hold Time	600	—	—	ns	2.5V≤V_{CC}≤5.5V
			4000	—	—	ns	1.7V≤V_{CC}<2.5V (24AA04)
			250	—	—	ns	1.7V≤V_{CC}≤5.5V
7	$T_{SU:STA}$	Start Condition Setup Time	600	—	—	ns	2.5V≤V_{CC}≤5.5V
			4700	—	—	ns	1.7V≤V_{CC}<2.5V(24AA04)
			250	—	—	ns	1.7V≤V_{CC}≤5.5V

AC CHARACTERISTICS (Continued)			Industrial(I):TA=-40°C to +85°C,Vcc=+1.7V to+5.5V Extended(E):TA=-40°C to+125°C,Vcc=+2.5V to+5.5V (24LC04B)				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
8	$T_{HD:DAT}$	Data Input Hold Time	0	—	—	ns	Note 2
9	$T_{SU:DAT}$	Data Input Setup Time	100	—	—	ns	2.5V≤Vcc≤5.5V
			250	—	—	ns	1.7V≤Vcc<2.5V(24AA04)
			50	—	—	ns	1.7V≤Vcc≤5.5V
10	$T_{SU:STO}$	Stop Condition Setup Time	600	—	—	ns	2.5V≤Vcc≤5.5V
			4000	—	—	ns	1.7V≤Vcc<2.5V(24AA04)
			250	—	—	ns	1.7V≤Vcc≤5.5V
11	$T_{SU:WP}$	WP Setup Time	600	—	—	ns	1.7V≤Vcc≤5.5V
12	$T_{HD:WP}$	WP Hold Time	600	—	—	ns	1.7V≤Vcc≤5.5V
13	T_{AA}	Output Valid from Clock	—	—	900	ns	2.5V≤Vcc≤5.5V(Note 2)
			—	—	3500	ns	1.7V≤Vcc<2.5V(24AA04) (Note 2)
			—	—	450	ns	1.7V≤Vcc≤5.5V (Note 2)
14	T_{BUF}	Bus Free Time:The time the bus must be free before a new transmis-sion can start	1300	—	—	ns	2.5V≤Vcc≤5.5V
			4700	—	—	ns	1.7V≤Vcc<2.5V (24AA04)
			500	—	—	ns	1.7V≤Vcc≤5.5V
15	T_{OF}	Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	$20+0.1C_B$	—	250	ns	2.5V≤Vcc≤5.5V(24LC04B) (Notes 1,2 and 3)
			—	—	250	ns	1.7V≤Vcc<2.5V(24AA04) (Notes 1 and 2)
16	T_{SP}	Input Filter Spike Suppression (SDA and SCL pins)	—	—	50	ns	Note 1

AC CHARACTERISTICS (Continued)			Industrial(I):TA=-40℃ to +85℃,Vcc=+1.7V to+5.5V Extended(E):TA=-40℃ to+125℃,Vcc=+2.5V to+5.5V (24LC04B)				
Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
17	TWC	Write Cycle Time (byte or page)	—	—	5	ms	
18		Endurance	1,000,000	—	—	cycles	+25℃,5.5V,Page Mode (Note 4)

Note 1: Characterized but not 100% tested.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
3: C_B = total capacitance of one bus line in pF.
4: This parameter is not tested but ensured by characterization.

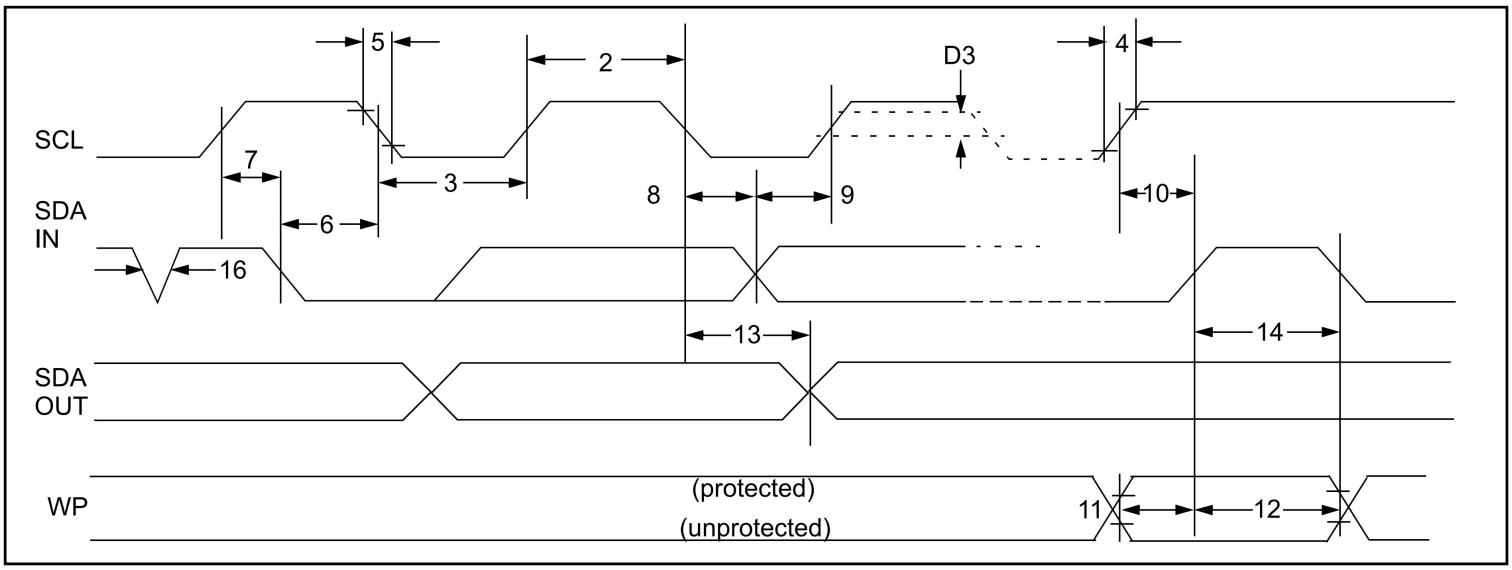


FIGURE 1: BUS TIMING DATA

PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3.

TABLE 3: PIN FUNCTION TABLE

Name	PDIP	SOIC	SOT-23	TSSOP	Description
A0	1	1	—	1	Not Connected
A1	2	2	—	2	Not Connected
A2	3	3	—	3	Not Connected
V_{SS}	4	4	2	4	Ground
SDA	5	5	3	5	Serial Address/Data I/O
SCL	6	6	1	6	Serial Clock
WP	7	7	5	7	Write-Protect Input
V_{CC}	8	8	4	8	Power Supply

A0, A1, A2: The A0, A1 and A2 pins are not used by the 24XX04. They may be left floating or tied to either V_{SS} or V_{CC}.

Serial Address/Data Input/Output (SDA): The SDA input is a bidirectional pin used to transfer addresses and data into and out of the device.Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to V_{CC} (typical 10 kΩ for100 kHz, 2 kΩ for 400 kHz and 1 MHz). For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL Ahigh are reserved for indicating Start and Stop conditions.

Serial Clock (SCL): The SCL input is used to synchronize the data transfer to and from the device.

Write-Protect (WP): This pin must be connected to either V_{SS} or V_{CC}. If tied to V_{SS}, normal memory operation is enabled (read/write the entire memory 000-1FF). If tied to V_{CC},write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

FUNCTIONAL DESCRIPTION

The 24XX04 supports a bidirectional, two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while defining a device receiving data as a receiver. The bus has to be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX04 works as client. Both host and client can operate as transmit-ter or receiver, but the host device determines which mode is activated.

BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 2).

Bus Not Busy (A): Both data and clock lines remain high.

Start Data Transfer (B):A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

Stop Data Transfer (C):A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

Data Valid (D): The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.
The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the host device and is, the-oretically, unlimited (although only the last sixteen will be stored when doing a write operation). When an overwrite does occur, it will replace data based on the First-In First-Out (FIFO) principle.

Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX04) will leave the data line high to enable the host to generate the Stop condition.

Note: The 24XX04 does not generate any Acknowledge bits if an internal programming cycle is in progress.

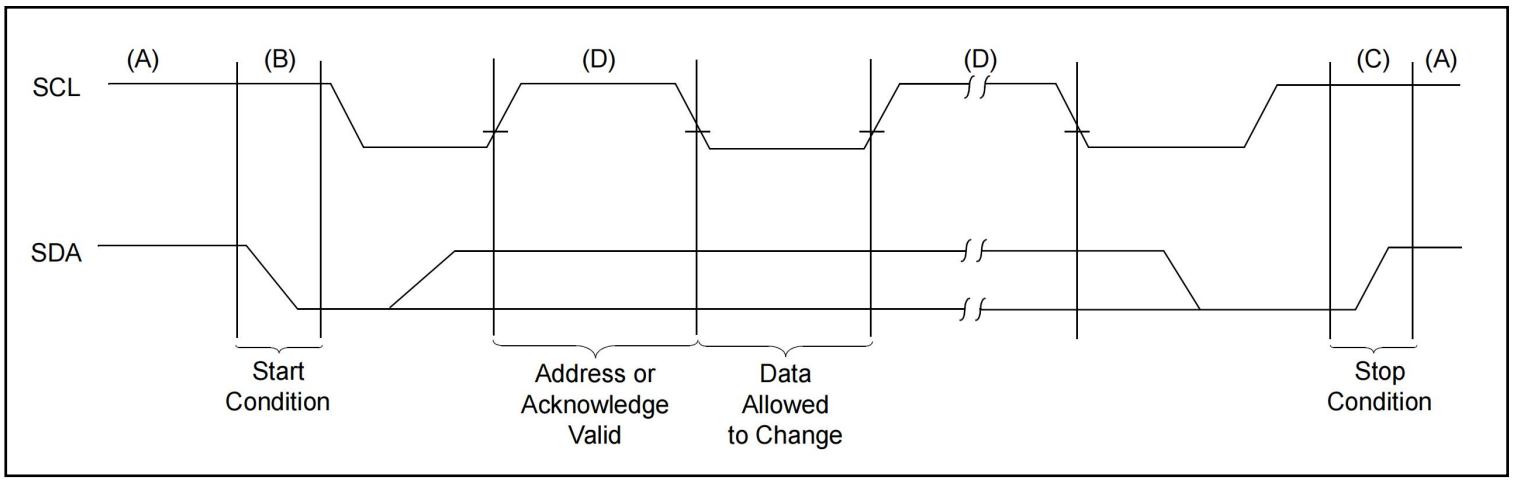


FIGURE 2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a four-bit control code. For the 24XX04, this is set as ‘1010’ binary for read and write operations. The next two bits of the control byte are “don’t cares” for the 24XX04. The last bit, B0, is used by the host device to select which of the two 256-word blocks of memory are to be accessed. This bit is, in effect, the Most Sig-nificant bit of the word address. The combination of the 4-bit control code and the next three bits are called the client address.
The last bit of the control byte is the Read/Write (R/W) bit and it defines the operation to be performed. When set to ‘1’, a read operation is selected. When set to ‘0’, a write operation is selected. Following the Start condition, the 24XX04 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving a valid client address and the R/W bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24XX04 will select a read or write operation.
The next byte received defines the address of the first data byte within the selected block (Figure 4). The word address byte uses all eight bits.

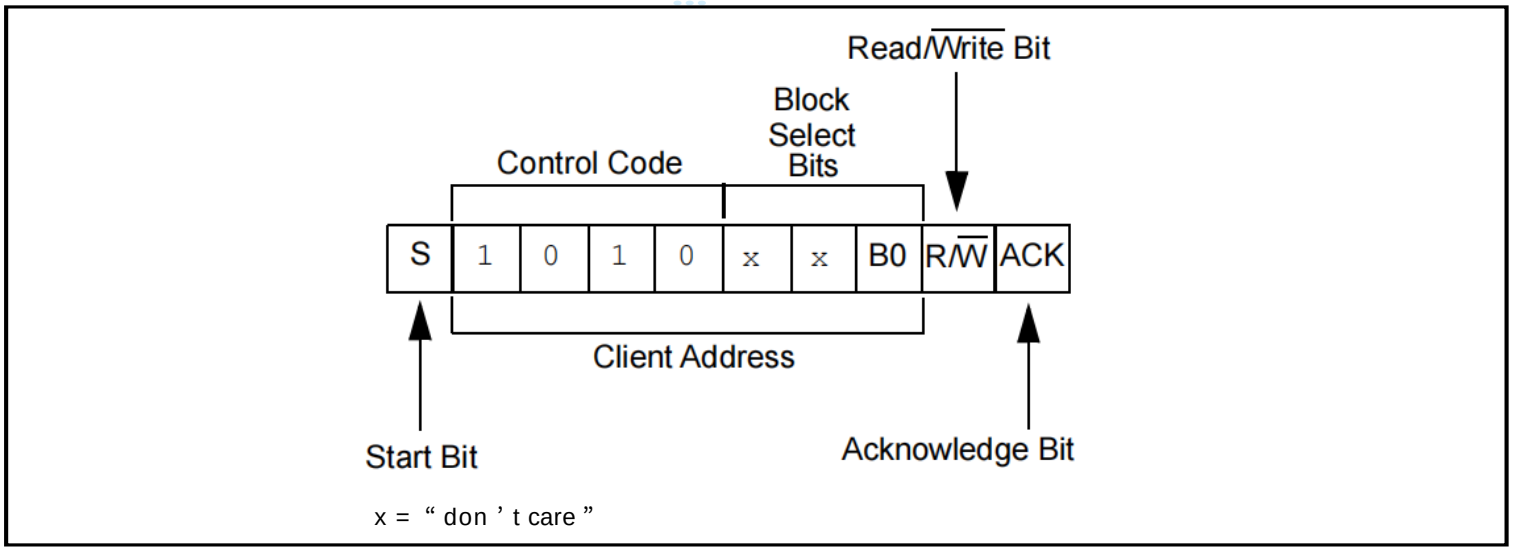


FIGURE 3: CONTROL BYTE ALLOCATION

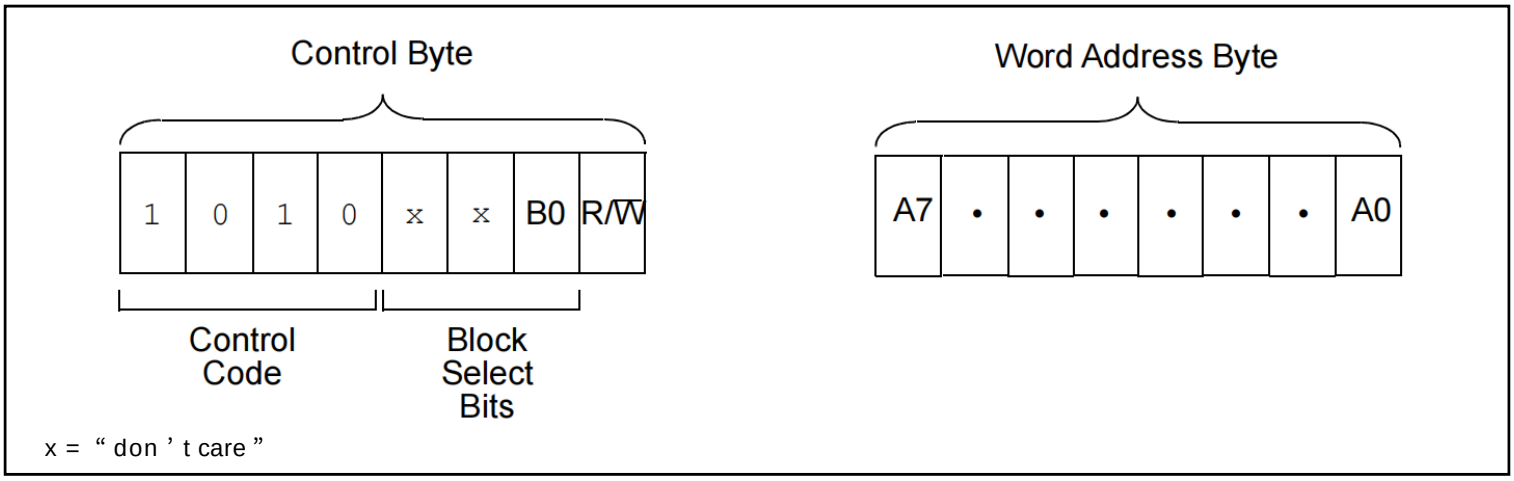


FIGURE 4: ADDRESS SEQUENCE BIT ASSIGNMENTS

Operation	Control Code	Block Select	R/W
Read	1010	Block Address	1
Write	1010	Block Address	0

WRITE OPERATION

Byte Write

Following the Start condition from the host, the device code (4 bits), the block address (2 bits, “ don ’ t care ”, plus B0 bit) and the R/W bit, which is a logic-low, are placed onto the bus by the host transmitter. This indicates to the addressed client receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the word address and will be written into the Address Pointer of the 24XX04. After receiving another Acknowledge signal from the 24XX04, the host device will transmit the data word to be written into the addressed memory location. The 24XX04 acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24XX04 will not generate Acknowledge signals (Figure 5).

Page Write

The write control byte, word address and first data byte are transmitted to the 24XX04 in the same way as in a byte write. However, instead of generating a Stop condition, the host transmits up to 16 data bytes to the 24XX04, which are temporarily stored in the on-chip page buffer and will be written into the memory once the host has transmitted a Stop condition. Upon receipt of each word, the four lower-order Address Pointer bits, which form the byte counter, are internally incremented by one. The higher-order four bits of the word address and bit B0 remain constant. If the host should transmit more than 16 words prior to generating the Stop condi-tion, the Address Pointer will roll over and the previ-ously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6).

Note:
Page write operations are limited to writ-ing bytes within a single physical page regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘ page size ’) and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

Write Protection

The WP pin allows the user to write-protect the entire array (000-1FF) when the pin is tied to V_{CC}. If tied to V_{SS}, the write protection is disabled.

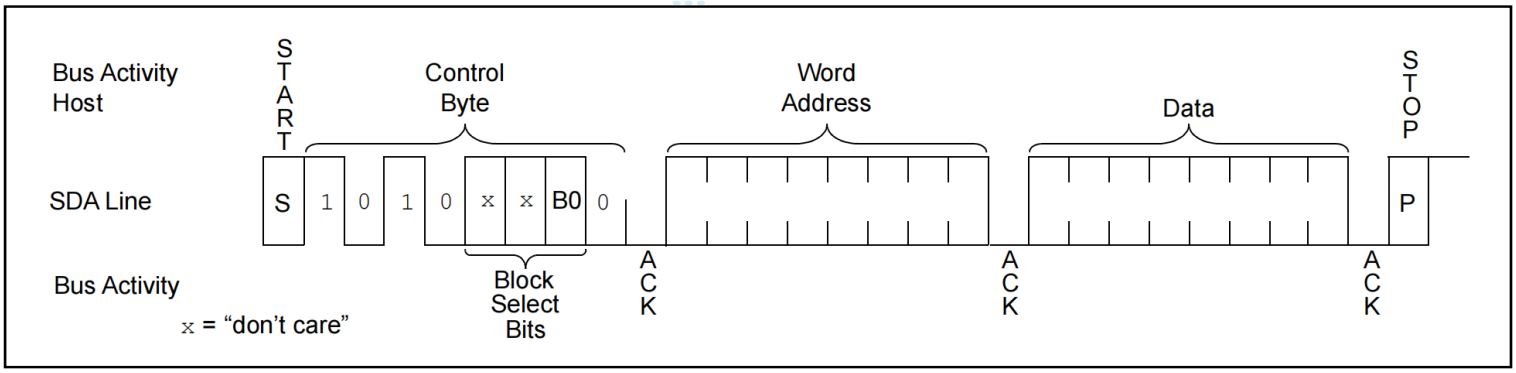


FIGURE 5: BYTE WRITE

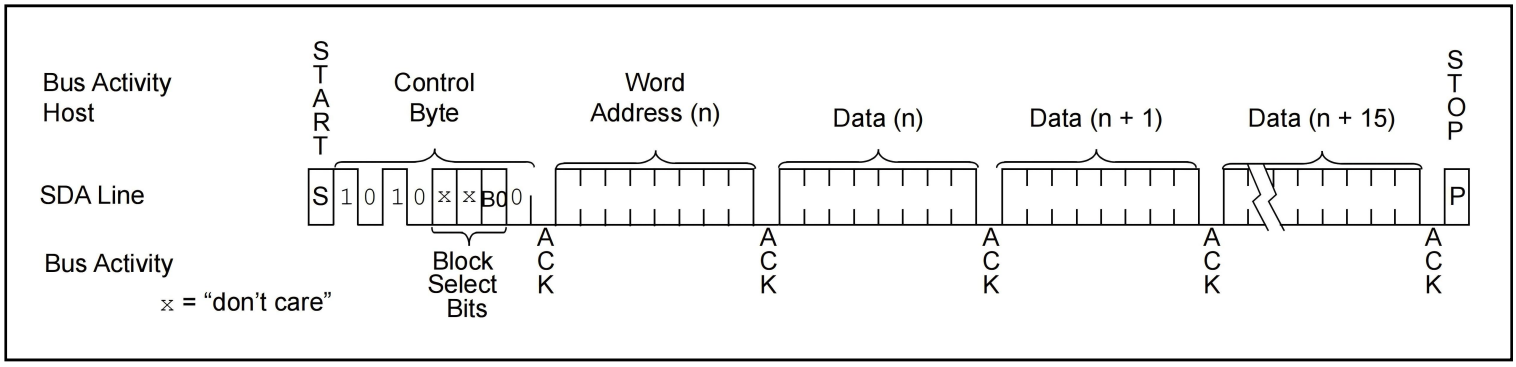


FIGURE 6: PAGE WRITE

ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally-timed write cycle. ACK polling can then be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the host can then proceed with the next read or write operation. See Figure 7 for a flow diagram of this operation.

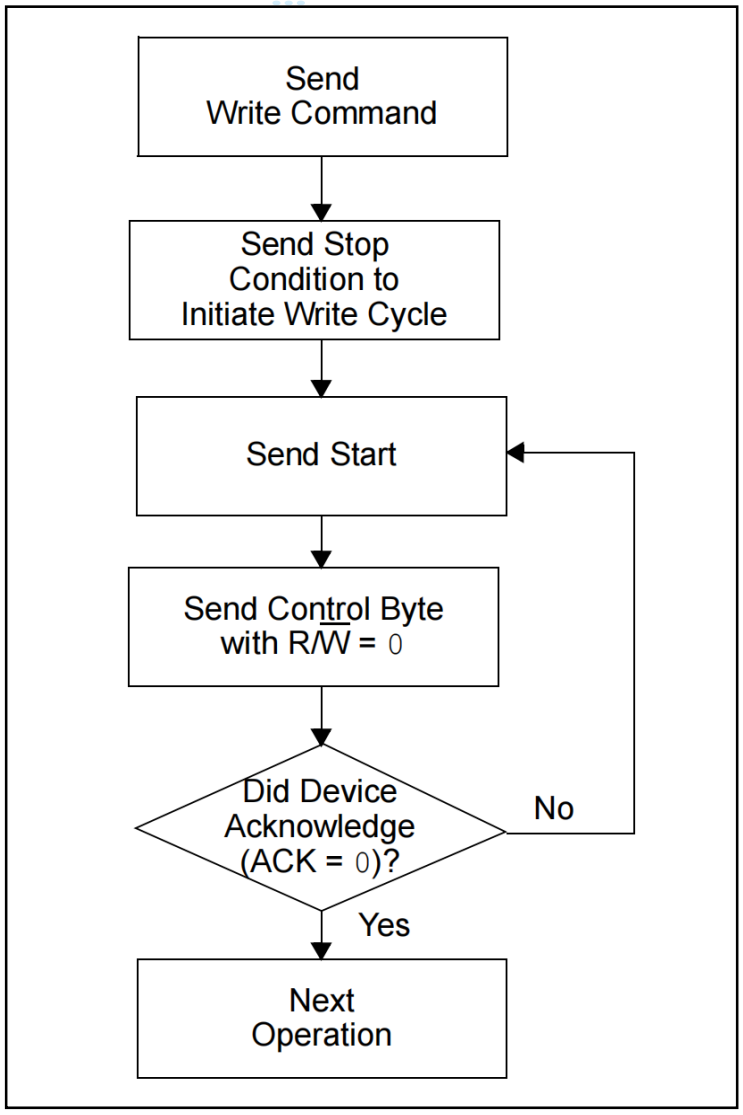


FIGURE 7: ACKNOWLEDGE POLLING FLOW

READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/W bit of the client address is set to ‘1’. There are three basic types of read operations: current address read, random read and sequential read.

Current Address Read

The 24XX04 contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previ-ous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the client address with R/W bit set to ‘1’, the 24XX04 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX04 discontinues transmission (Figure 8).

Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX04 as part of a write operation. Once the word address is sent, the host generates a Start condi-tion following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/W bit set to a ‘1’. The 24XX04 will then issue an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX04 dis-continues transmission (Figure 9).

Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24XX04 transmits the first data byte, the host issues an Acknowledge (as opposed to a Stop condition in a random read). This directs the 24XX04 to transmit the next sequentially addressed 8-bit word (Figure 10).
To provide sequential reads the 24XX04 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

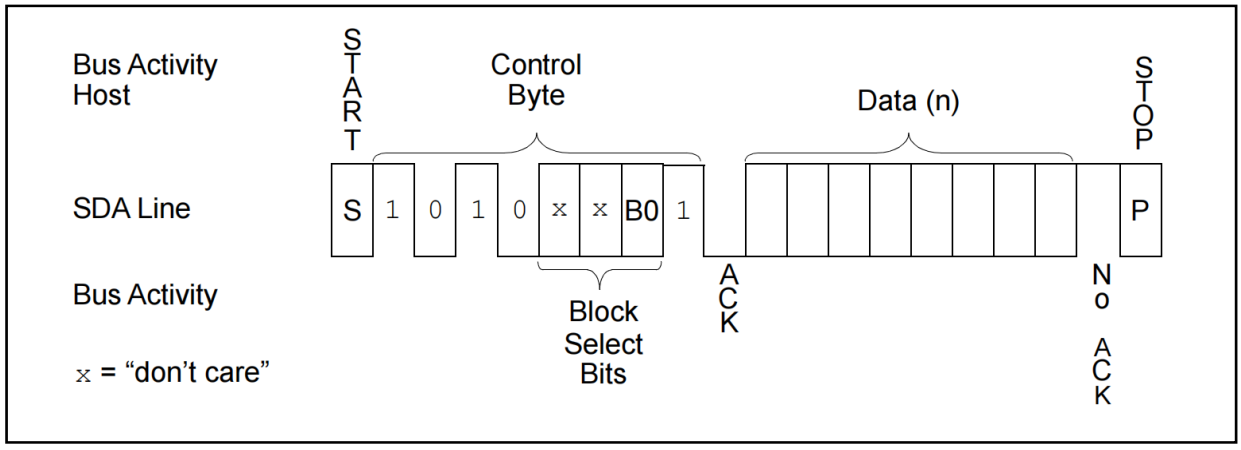


FIGURE 8: CURRENT ADDRESS READ

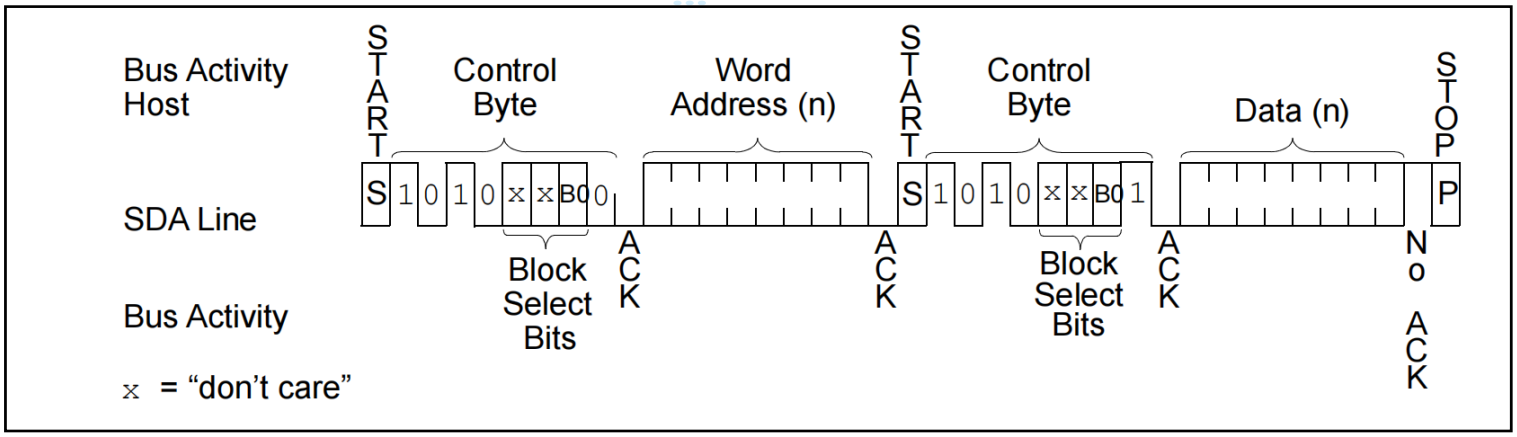


FIGURE 9: RANDOM READ

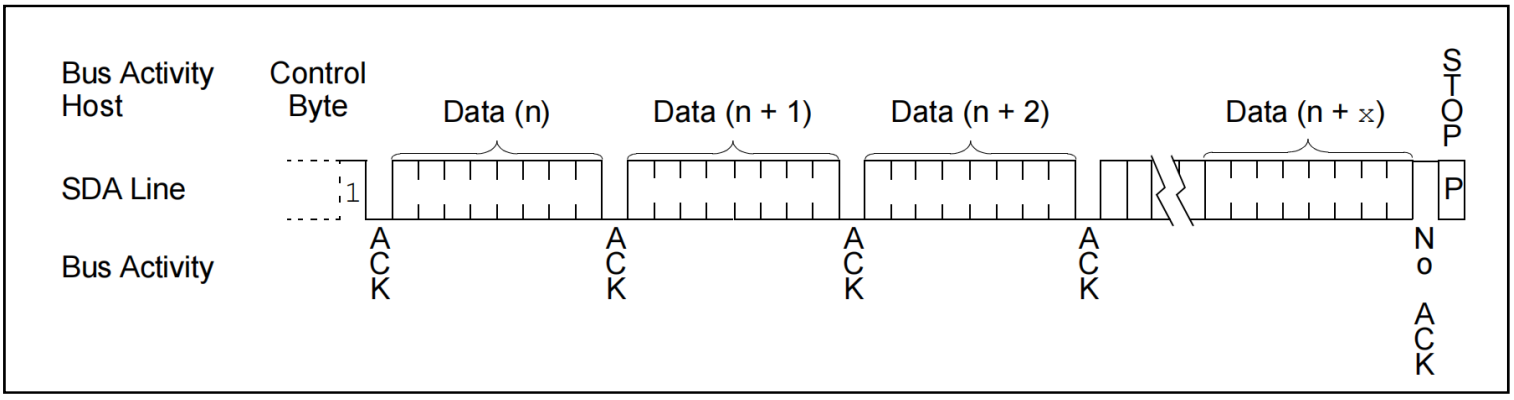


FIGURE 10: SEQUENTIAL READ

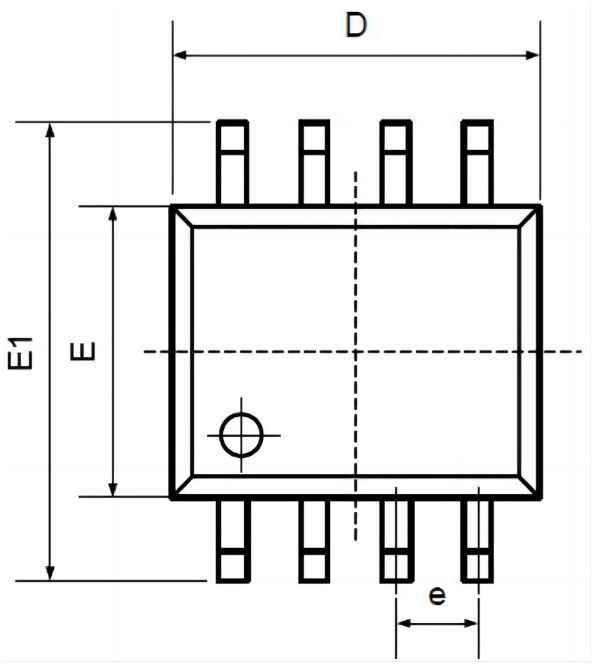
Order information

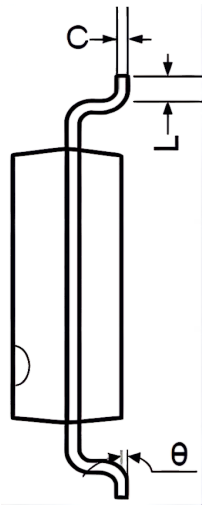
Order Number	Package	Package Quantity	Marking On The park	Temperature
24AA04-I/P-TUDI	DIP8	Tube,50,A box of 2000	24AA04-I/P	-40°C to +85°C
24AA04T-I/SN-TUDI	SOP8	Tape,Reel,4000	24AA04I/SN	
24AA04T-I/ST-TUDI	TSSOP8	Tape,Reel,4000	24AA04	
24AA04T-I/OT-TUDI	SOT23-5	Tape,Reel,3000	B3xx	
24LC04B-I/P-TUDI	DIP8	Tube,50,A box of 2000	24LC04B-I/P	
24LC04BT-I/SN-TUDI	SOP8	Tape,Reel,4000	24LC04BI/SN	
24LC04BT-I/ST-TUDI	TSSOP8	Tape,Reel,4000	24LC04B	
			4L04	
24LC04BT-I/OT-TUDI	SOT23-5	Tape,Reel,3000	M3xx	

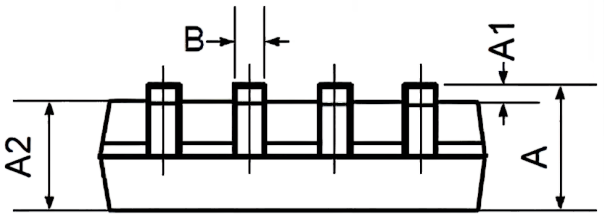
Revision history

	Date	Revision	Page
V1.0	2022/4	New	1-17
V1.1	2024/1	Update model and PDF template	1-22

Package SOP8

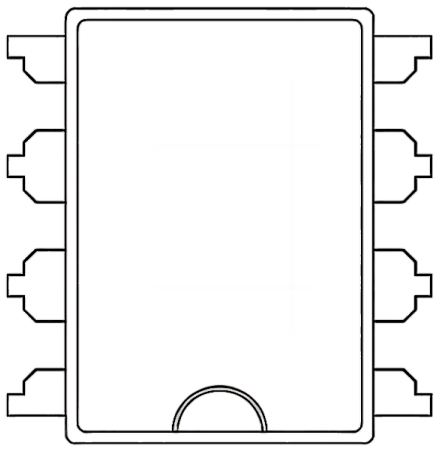


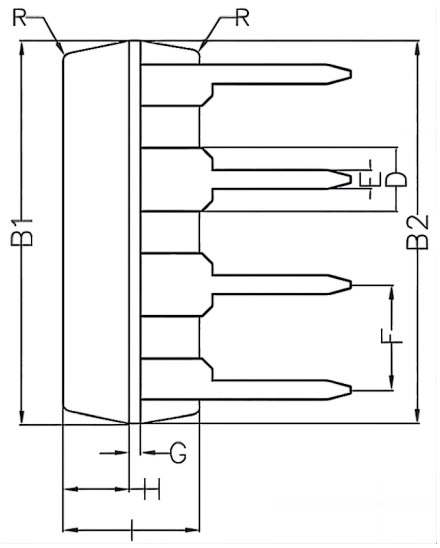


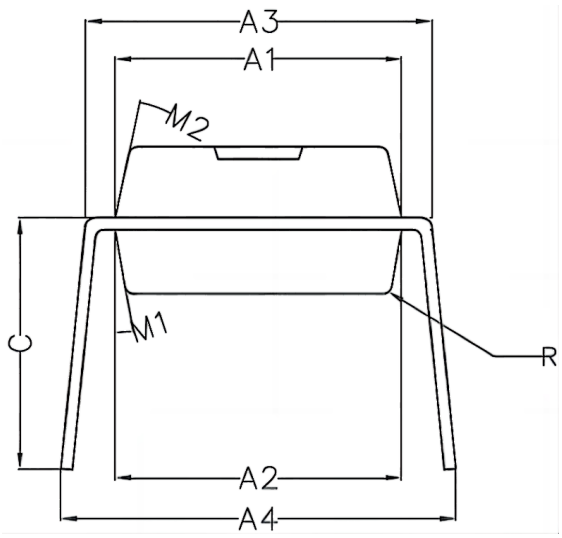


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8

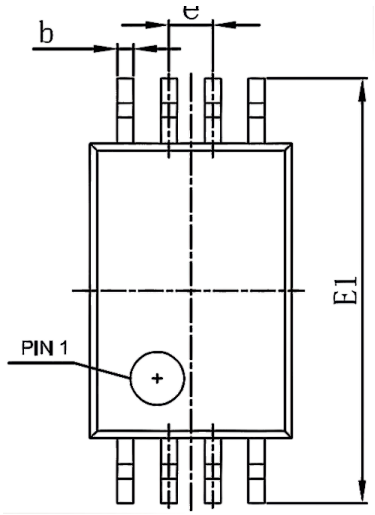


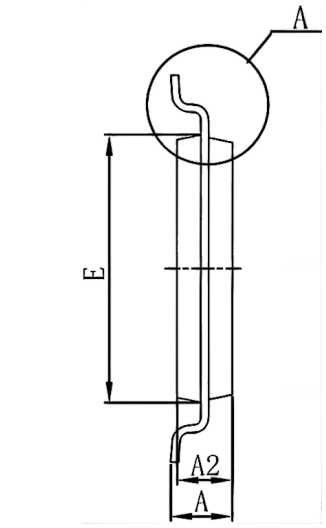


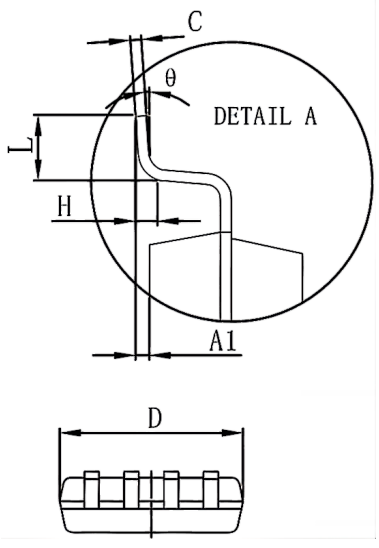


Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Package TSSOP8

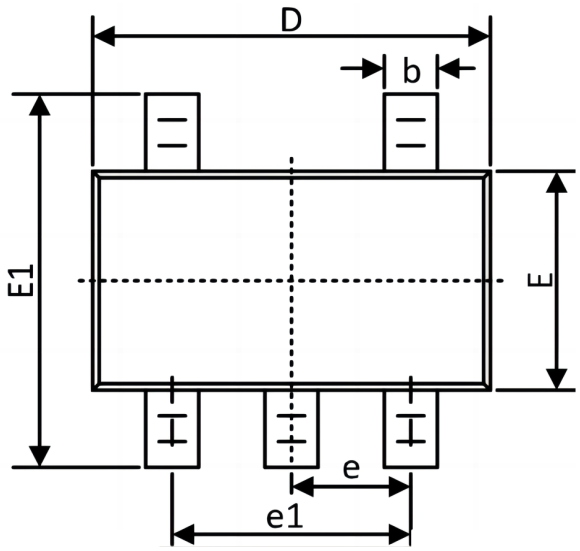


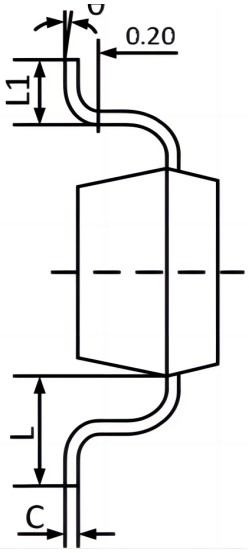


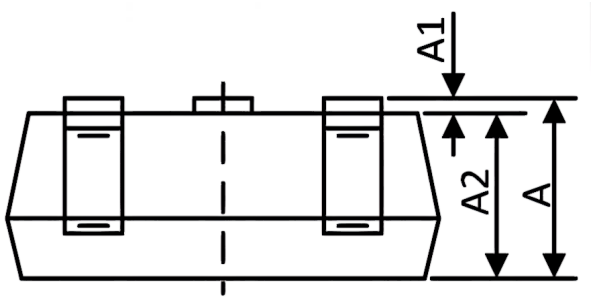


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

Package SOT23-5







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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