



AC101S Datasheet

High Performance and Low Power Mono Audio CODEC

Revision 1.0

Aug, 30, 2018

Declaration

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Revision History

Revision	Date	Author	Description
V1.0	Aug, 30, 2018		Initial Version 1.0

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1. Features

■ ADC

- Mono ADC with 100dB SNR typically(A-weight);
- -80 dB THD+N @ 0 dB gain and 1.0Vpp input;
- Mono Fully-differential analog microphone input with 0dB~31dB boost amplifier gain;
- ADC sample rates supported: 8k, 11.025k, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz;
- Programmable Microphone Bias 1.81V~2.39V;
- Support Automatic Gain Control (AGC) adjusting the ADC recording output;

■ DAC

- Mono DAC with 103dB SNR typically(A-weight);
- -85 dB THD+N @ 0dB line-out gain;
- Mono Fully-differential Line Output with 1.0Vrms maximum output voltage;
- DAC sample rates supported: 8k, 11.025k, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz;
- 3 bands parametric Biquad filter for EQ in DAC path;

■ System

- One TWI control interface up to 400 kHz;
- One 8KHz ~ 48KHz I2S/PCM interface;
- Adjustable 44.1K/48K sample rate without software driver;
- 2 Integrated LDOs, analog LDO output is 1.8V, digital LDO output is 1.2V;
- 3 mm x 3 mm 20-pin QFN Package, pitch 0.4mm;

■ Low Power

- Support single 3.3V power supply;
- < 3mA Mono 48ksps ADC Record with fully-differential analog microphone input;
- < 3mA Mono 48ksps DAC Playback with line-out driver output;

■ Description

The AC101S is a high-performance, low-power, mono audio CODEC optimized for use in portable applications. The device integrates support one fully-differential analog microphone input and mono line output driver.

The mono 24-bit multi-bit sigma delta ADC with digital decimation filters has programmable gain with digital volume control(DVC). Digital audio output word length from 8-24 bits and sampling rates from 8kHz to 48kHz are supported.

A multi-bit sigma delta DAC is used with digital audio input word length from 8-24 bits and sampling rates from 8 to 48kHz. The mono 3-stage biquad filter can be used to provide more flexible filtering of the output signal than can be achieved using the 3-band equalizer. The biquad filters can be used for the implementation of low-pass, high-pass or notch filters.

The AC101S provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK and SDIN/SDOUT pins. These formats are I2S, left justified, right justified, PCM mode.

The AC101S is controlled through TWI (2-wire serial interface). The clock supports up to 400 KHz rate. It works only in the slave mode.

■ Applications

- Portable audio applications
- Digital Cameras and video cameras
- Wireless headset
- Tablets and e-Books

2. Block Diagram

Figure 2-1 shows the block diagram of AC101S CODEC.

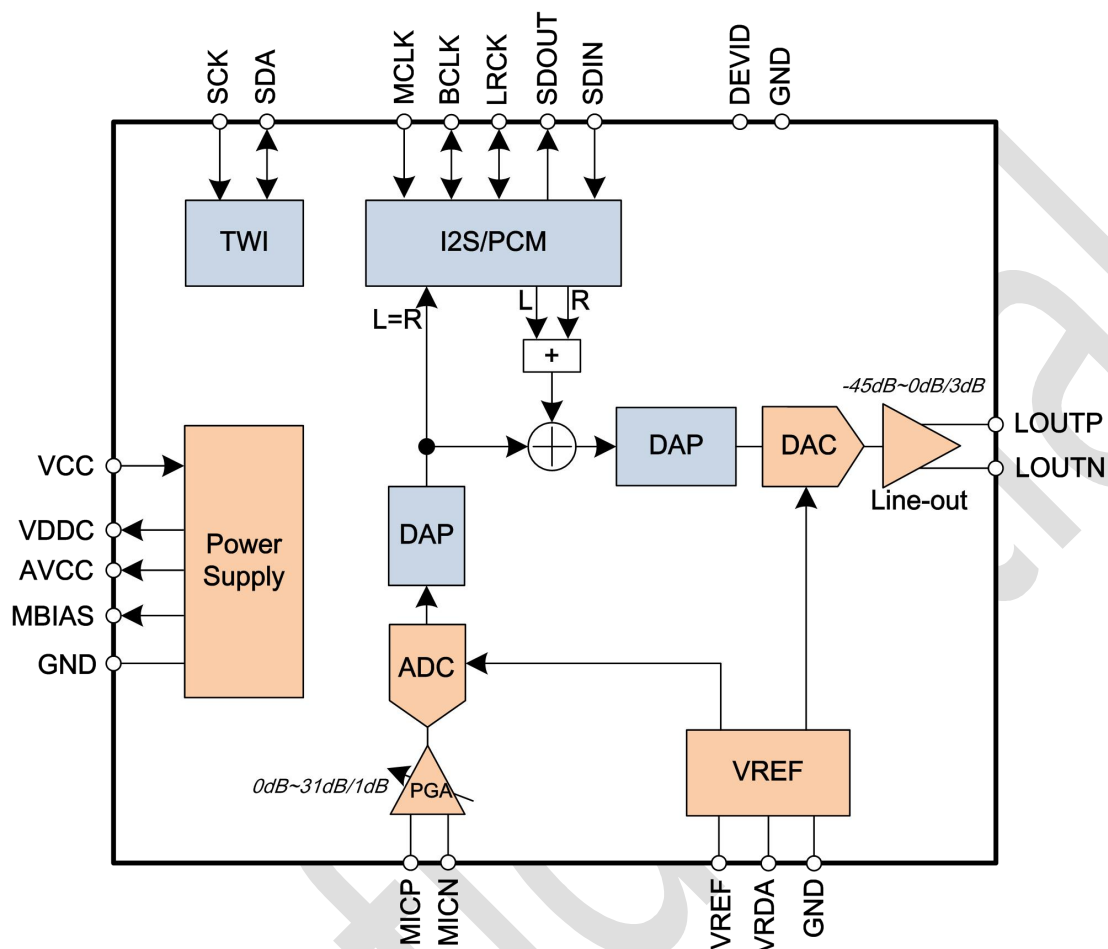


Figure 2-1. AC101S Block Diagram

3. Pin Assignment

Figure 3-1 shows the pin assignment of AC101S CODEC.

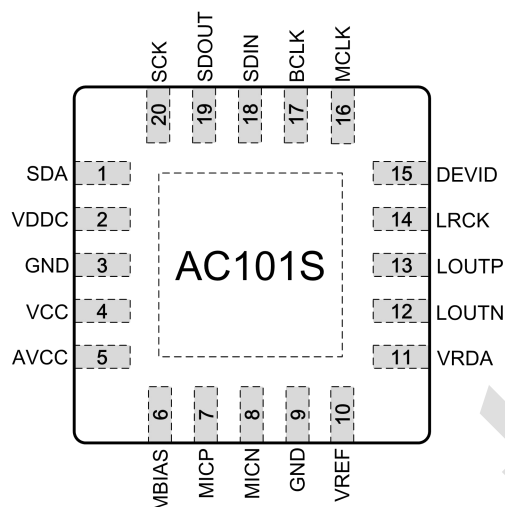


Figure 3-1. Pin Assignment

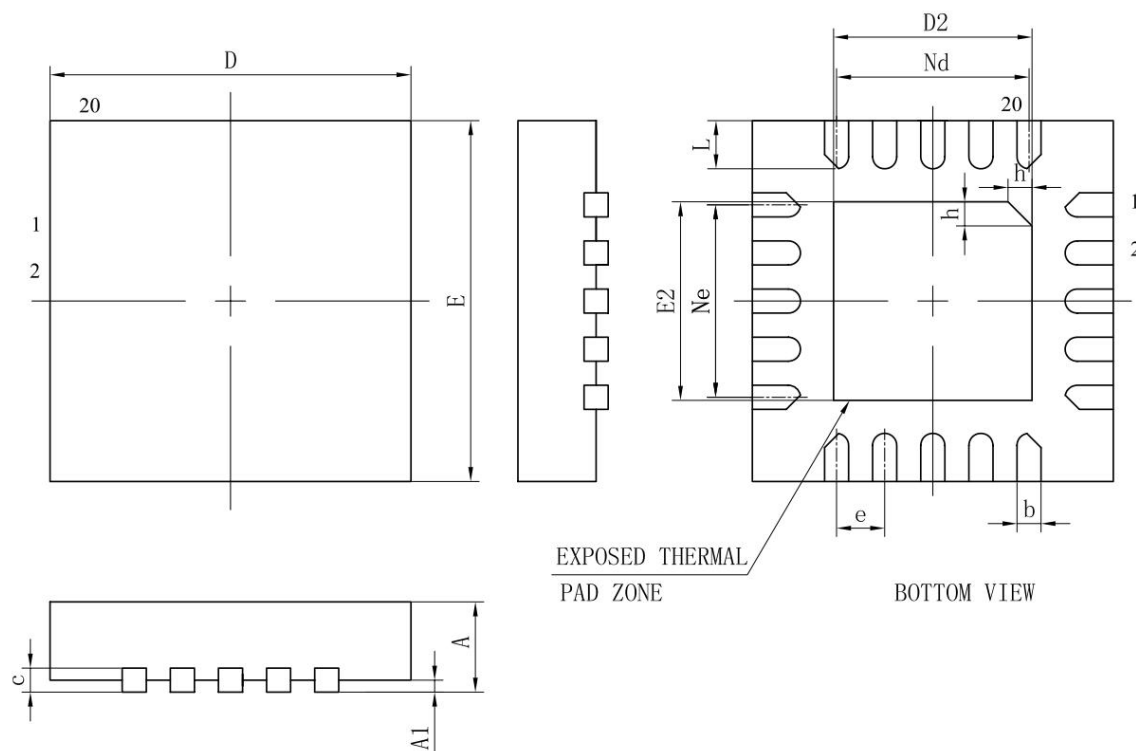
Table 3-1 Pin Function Description

Pin Number	Signal Name	Type	Description
Digital IO Pins (8 pins)			
20	SCK	I	TWI interface serial clock input(Open-drain).
1	SDA	I/O	TWI interface serial data(Open-drain).
14	LRCK	I/O	I2S interface synchronous clock.
15	DEVID	I	TWI interface device ID control.
16	MCLK	I	I2S interface master input clock.
17	BCLK	I/O	I2S interface serial bit clock.
18	SDIN	I	I2S interface serial data input.
19	SDOUT	O	I2S interface serial data output.
Analog IO Pins (6 pins)			
7	MICP	I	Positive differential input for MIC.
8	MICN	I	Negative differential input for MIC.
12	LOUTN	O	Differential negative output to line-out amplifier.
13	LOUTP	O	Differential positive output to line-out amplifier.
10	VREF	O	Internal reference voltage for ADC and DAC.
11	VRDA	O	Internal reference voltage for DAC.
Power/Ground Pins (7 pins)			
2	VDDC	P	The DLDO Power output 1.2V for digital part.
4	VCC	P	The MDLO&DLDO&ALDO Power input, also supply for digital IO.
5	AVCC	P	The ALDO Power output 1.8V for analog part.
6	MBIAS	P	The MLDO output for microphone.
3, 9	GND	G	Chip ground.
21	GND	G	EPAD.

Note: O for output, I for input, I/O for input/output, P for power, and G for ground.

4. Package Dimension

Figure 4-1 shows the package dimension of AC101S CODEC.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30

Figure 4-1. Package Dimension

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices.



CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5- 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Digital power for digital I/O buffer (I2S&TWI) and supply for inner MLDO&DLDO&ALDO.	-0.3	3.63	V
VDDC	Digital power for Audio CODEC, it can be generated by inner DLDO.	-0.3	1.98	V
AVCC	Analog power for Audio CODEC, it can be generated by inner ALDO.	-0.3	1.98	V
MBIAS	Analog power for microphone bias, it can be generated by inner MLDO.	-0.3	3.63	V
T _A	Operating Ambient Temperature.	-40	85	°C
V _{ESD}	Electrostatic Discharge	Human Body Model(HBM) ⁽¹⁾	TBD	V
		Charged Device Model(CDM) ⁽²⁾	TBD	V
I _{Latch-up}	Latch-up I-test performance current-pulse injection on each IO pin ⁽³⁾	TBD		
	Latch-up over-voltage performance voltage injection on each IO pin ⁽⁴⁾	TBD		

(1). Test method: JEDEC JS-001-2012(Class-3A). JEDEC publication JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2). Test method: JESD22-C101F(Class-C1). JEDEC publication JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3). Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

(4). Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

5.2 Recommended Operating Conditions

All AC101S modules are used under the operating conditions contained in Table 5-2.



NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5- 2. Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VCC	Digital power for digital I/O buffer (I2S&TWI).	3.3	3.3	3.63	V
VDDC	Digital power for Audio digital core, it is generated by inner DLDO.	1.08	1.2	1.98	V
AVCC	Analog power for Audio CODEC, it is generated by inner ALDO.	1.62	1.8	1.98	V
MBIAS	Analog power for microphone bias, it can be generate by inner MLDO.	1.8	2.39	2.39	V
GND	Ground reference.	--	0	--	V

5.3 DC Electrical Characteristics

Table 5- 3. DC Electrical Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	--	-0.3	--	VCC+0.3	V
V_{IH}	High Level Input Voltage	VCC=3.3V	2.4	--	3.6	V
V_{IL}	Low Level Input Voltage	VCC=3.3V	-0.3	--	0.7	V
V_{OH}	High Level Input Voltage	VCC=3.3V	2.7	--	NA	V
V_{OL}	Low Level Input Voltage	VCC=3.3V	NA	--	0.4	V
I_{OZ}	Tri-state Output Leakage Current	--	TBD	TBD	TBD	uA
C_{IN}	Input Capacitance	--	NA	NA	5	pF
C_{OUT}	Output Capacitance	--	NA	NA	5	pF

6. Analog Performance Characteristics

Table 6- 1. Absolute Maximum Ratings

	Parameter	Test conditions	Min	Typ	Max	Unit
ADC Input Path Performance	MIC via ADC to I2S, VCC=3.3V, AVCC=1.8V, VDDC=1.2V.					
	SNR(A-weighted)	PGA Gain=0 dB	98	100	102	dB
	THD+N (1.0Vpp 1KHz input)		-80	-80	-82	dB
DAC Output Path Performance	DAC to Line-out on LOU TP and LOU TN, VCC=3.3V, AVCC=1.8V, VDDC=1.2V.					
	Full-Scale Output Level (Fully-differential output)	0dBFS 1KHz input	1.0	1.1	1.15	Vrms
	SNR(A-weighted)	0dBFS 1KHz input	101	103	105	dB
	THD+N	0dBFS 1KHz input	-83	-85	-87	dB

7. Typical Power Consumption

Table 7- 1. Absolute Maximum Ratings

	Parameter	Test conditions	Min	Typ	Max	Unit
Record Path Consumption	MIC via ADC to I2S, VCC=3.3V, ALDO and DLDO enable,AVCC=1.8V, VDDC=1.2V.					
	ADC Record Power consumption	PGA Gain=0 dB	-	2.7	-	mA
Playback Path Consumption	DAC to Line-out on LOU TP and LOU TN, VCC=3.3V, ALDO and DLDO enable,AVCC=1.8V, VDDC=1.2V.					
	DAC Playback Power consumption	0dBFS 1KHz input	-	3.0	-	mA

8. Typical Application Diagram

Figure 8-1 shows the typical application diagram of AC101S CODEC.

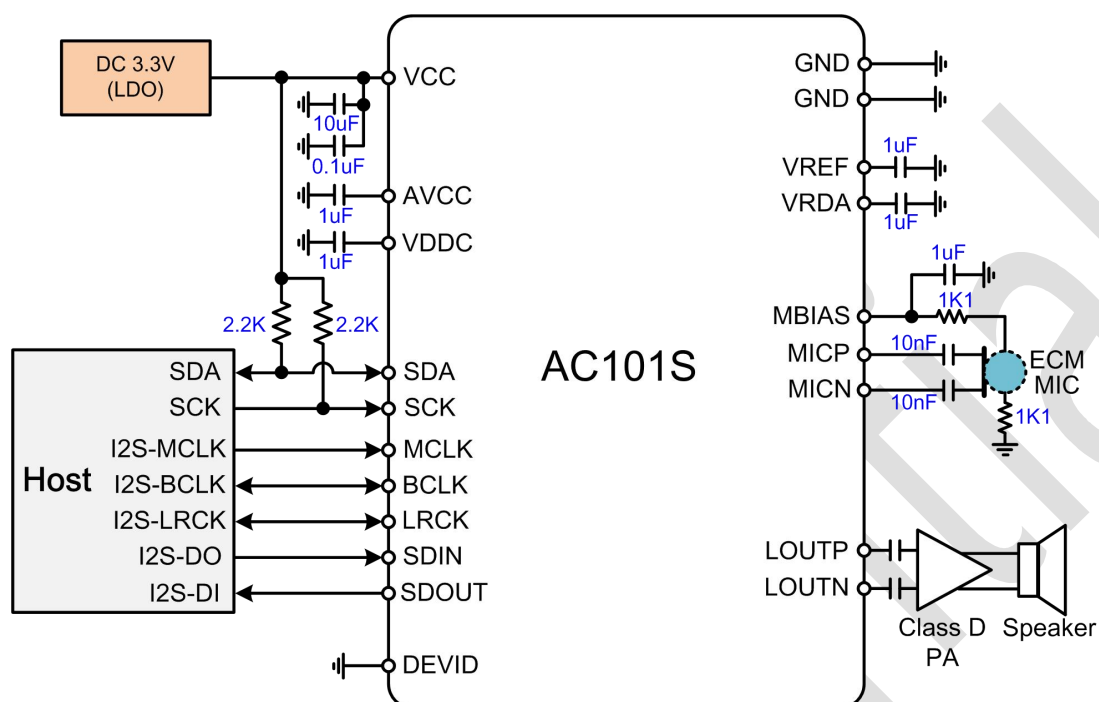


Figure 8-1. Single 3.3V Supply Typical Application Diagram