BUKNS2R0-40MYX8

40 V, 2.0 mΩ, standard level N-channel MOSFET in MLPAK56-WF

3 March 2026 **Product data sheet**

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 25 low-ohmic split-gate technology, for ultra-low $R_{DS(on)}$ capability, housed in a MLPAK56 (SOT8038) package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

Fully automotive qualified to AEC-Q101:

- 175 °C rating suitable for thermally demanding automotive environments

Trench 25 split-gate trench technology:

- Reduced cell-pitch enables enhanced power density resulting in lower conduction losses in same footprint

MLPAK micro-leads with side-wettable flanks:

- Proven board-level reliability during thermal cycling
- Visual (AOI) soldering inspection, no need for expensive X-ray equipment
- Easy solder wetting for good mechanical solder joint

MLPAK copper clip technology:

- Improved reliability, with reduced R_{th}, $R_{DS(on)}$, and package inductance
- Increases maximum current capability and improves current spreading

3. Applications

- 12 V and 24 V automotive systems
- Motor, lighting, and solenoid control
- Ultra high-performance power switching

4. Quick reference data

Table 1. Quick reference data

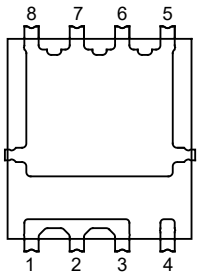
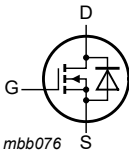
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	175	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		1.6	1.8	2	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	38	46	nC

[1] 175A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 Transparent top view **MLPAK56 (SOT8038-4)**	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUKNS2R0-40MYX8	MLPAK56	Plastic, thermal enhanced surface mounted package with side-wettable flanks (SWF); minileads; 8 terminals; pitch 1.27 mm; 5.6 x 5.15 x 1.0 mm body	SOT8038-4

7. Marking

Table 4. Marking codes

Type number	Marking code
BUKNS2R0-40MYX8	BN2S004 X8MY

8. Limiting values

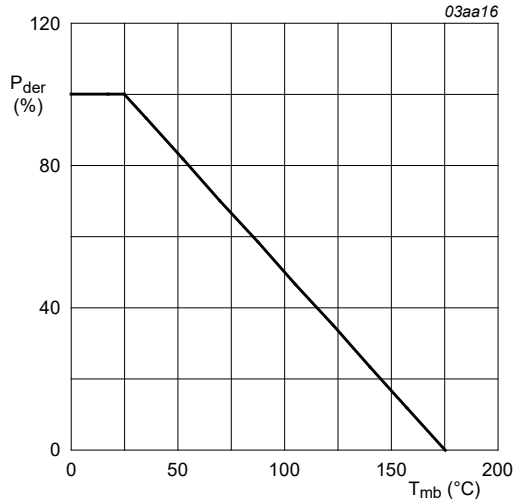
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	142	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	175	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	135	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3	[1]	-	764	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	175	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	764	A

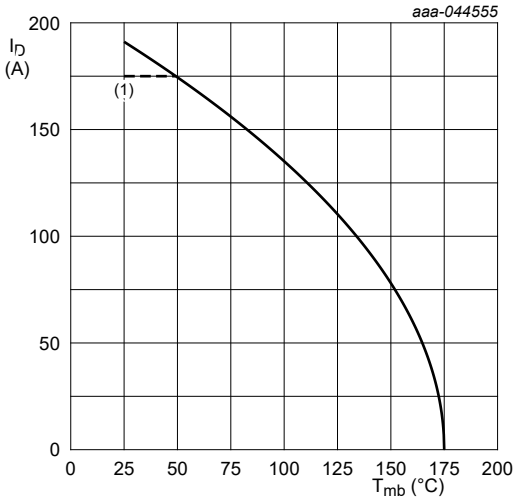
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 62 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 31 µs; Fig. 4	[2] [3]	-	50.7	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[4]	-	62	A

[1] 175A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test.



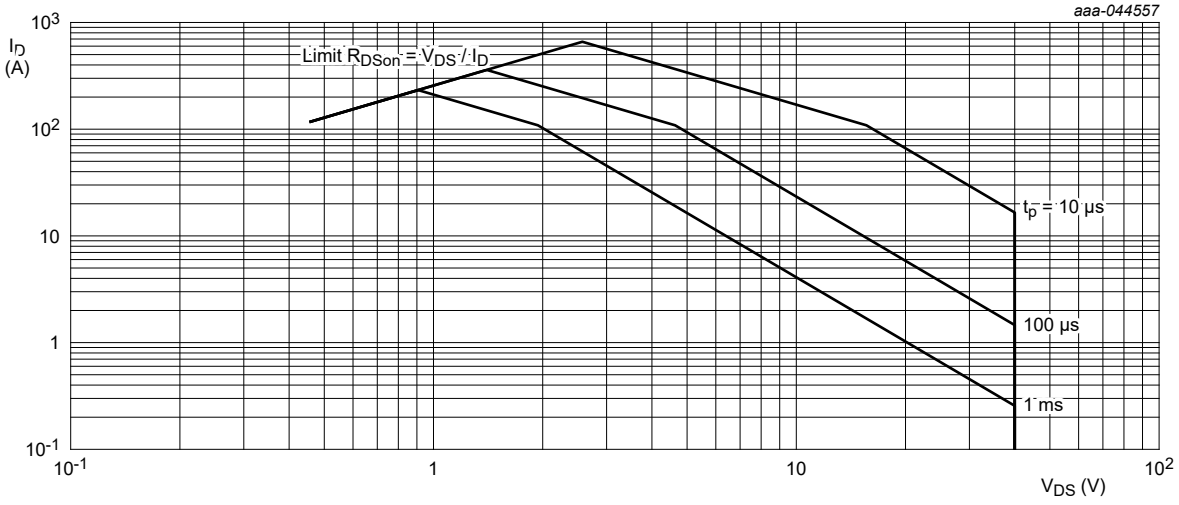
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



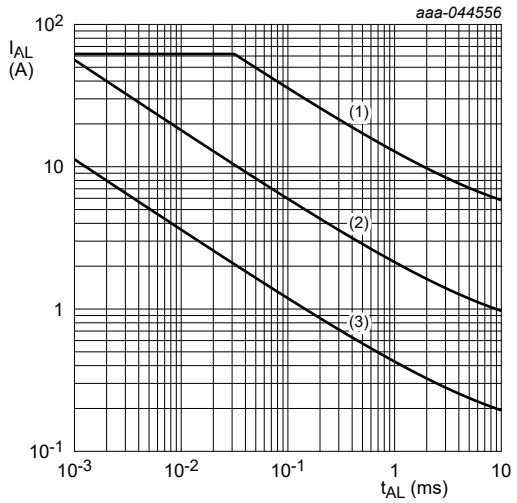
V_{GS} ≥ 10 V
(1) 175A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.81	1.05	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient		[1]	-	24	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

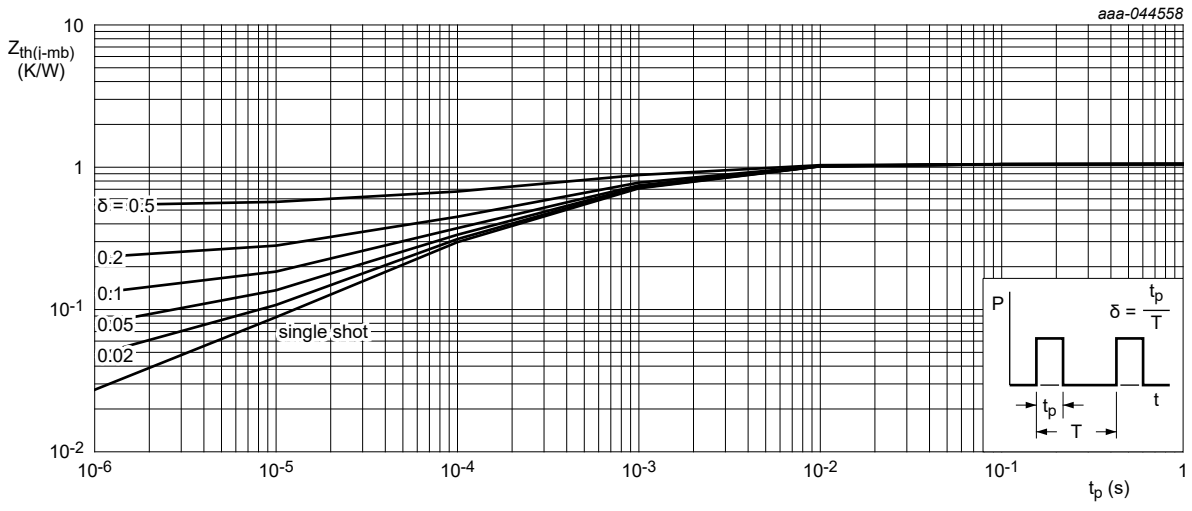


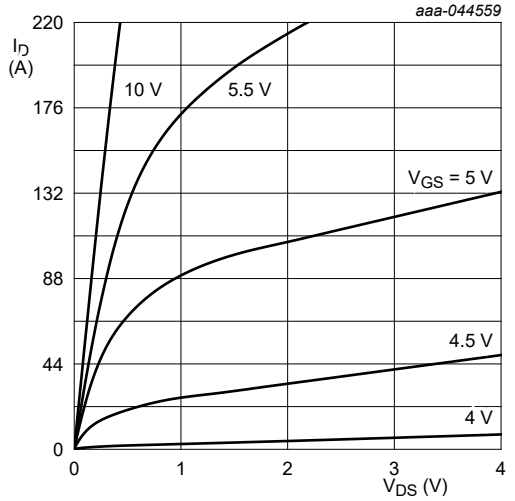
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

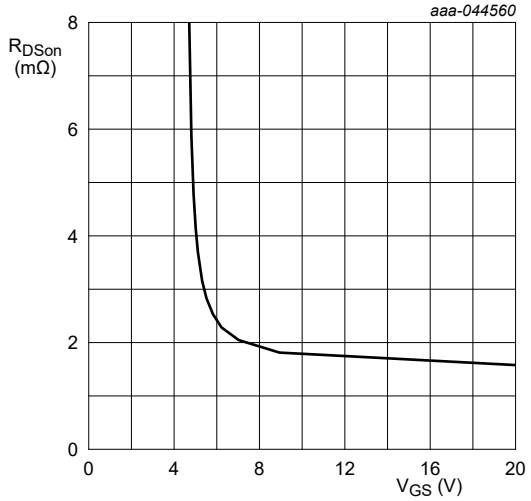
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	44	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	42.8	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	42.5	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.2 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		2	3	4	V
		I_D = 0.2 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10		-	-	4.42	V
		I_D = 0.2 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10		0.7	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.04	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	2	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	80	200	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		1.6	1.8	2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 12		2	2.5	3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 12		2.3	2.76	3.32	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12		2.79	3.3	3.9	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.1	0.4	0.8	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	38	46	nC
Q_{GS}	gate-source charge			-	11	16	nC
Q_{GD}	gate-drain charge			-	7	10	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	2623	3934	pF
C_{oss}	output capacitance			-	730	1095	pF
C_{rss}	reverse transfer capacitance			-	6	9	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 32 V; R_L = 1.3 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	9	-	ns
t_r	rise time			-	8	-	ns
$t_{d(off)}$	turn-off delay time			-	23	-	ns
t_f	fall time			-	10	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.81	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 17		-	33	-	ns
Q_r	recovered charge		[1]	-	20	-	nC

[1] includes capacitive recovery



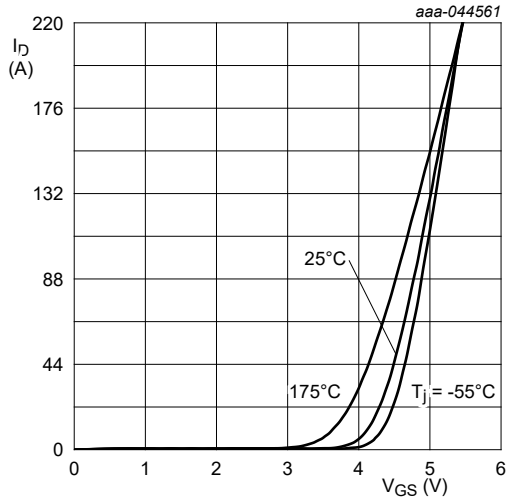
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



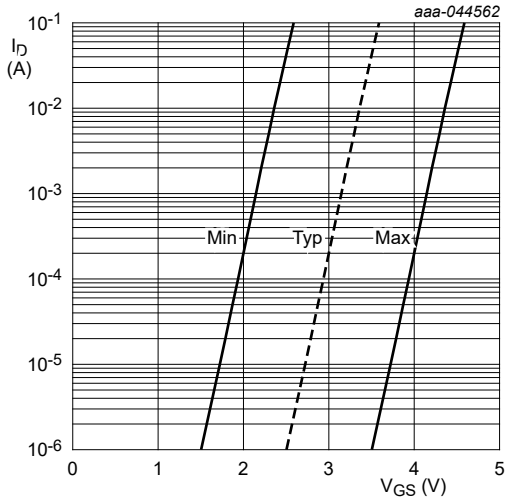
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



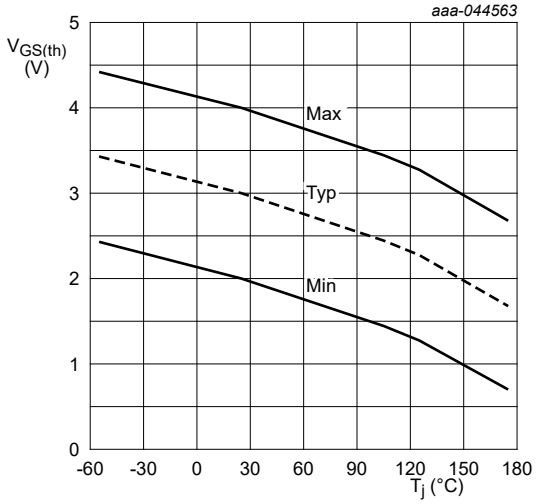
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



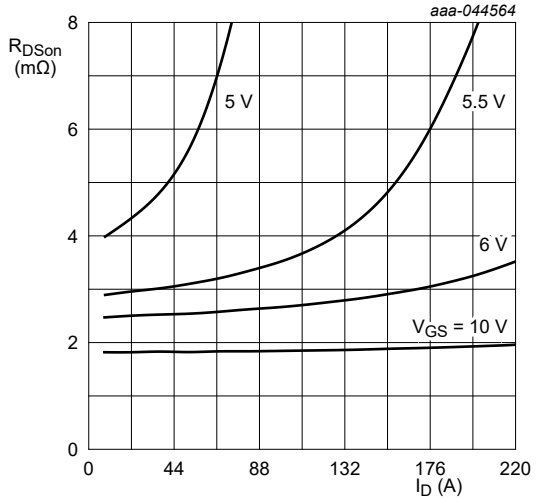
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage



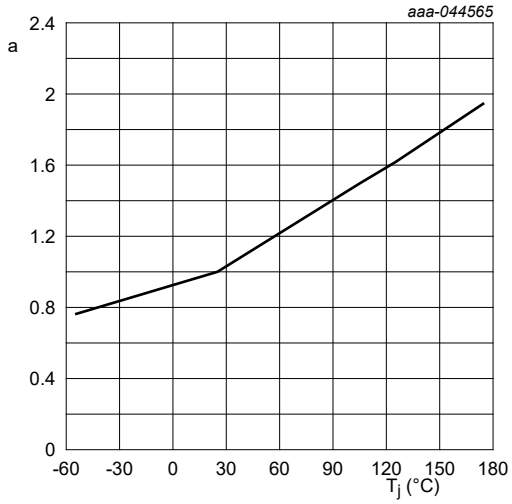
I_D = 0.2 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature



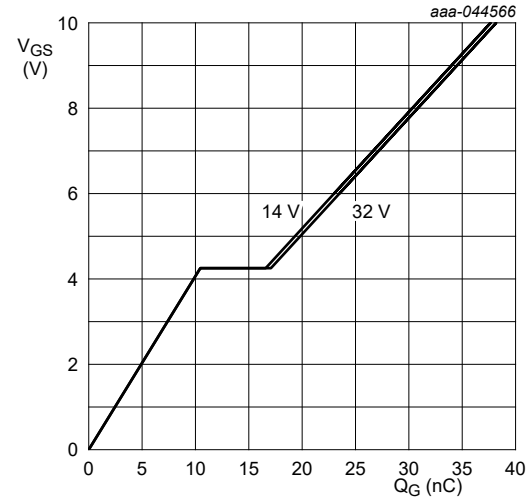
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values

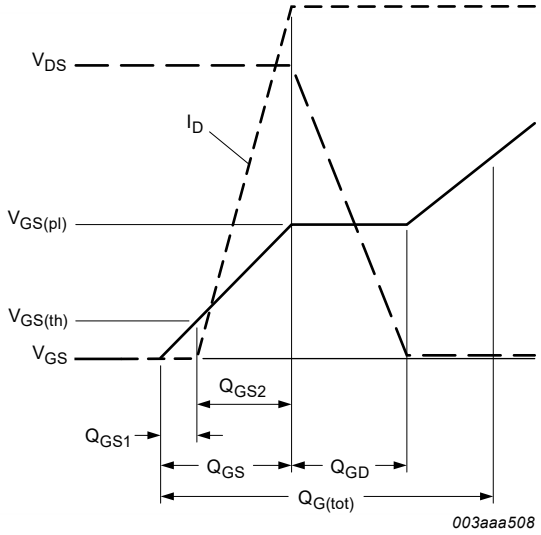
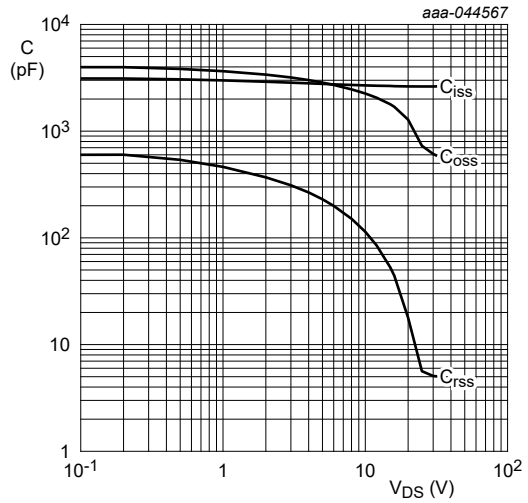
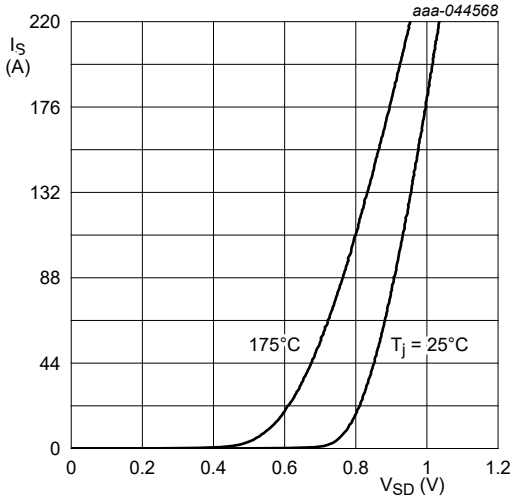


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

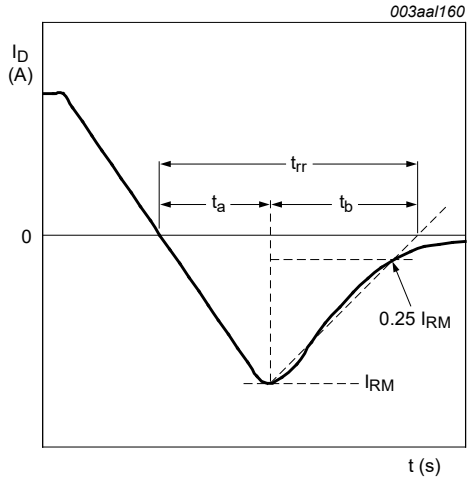
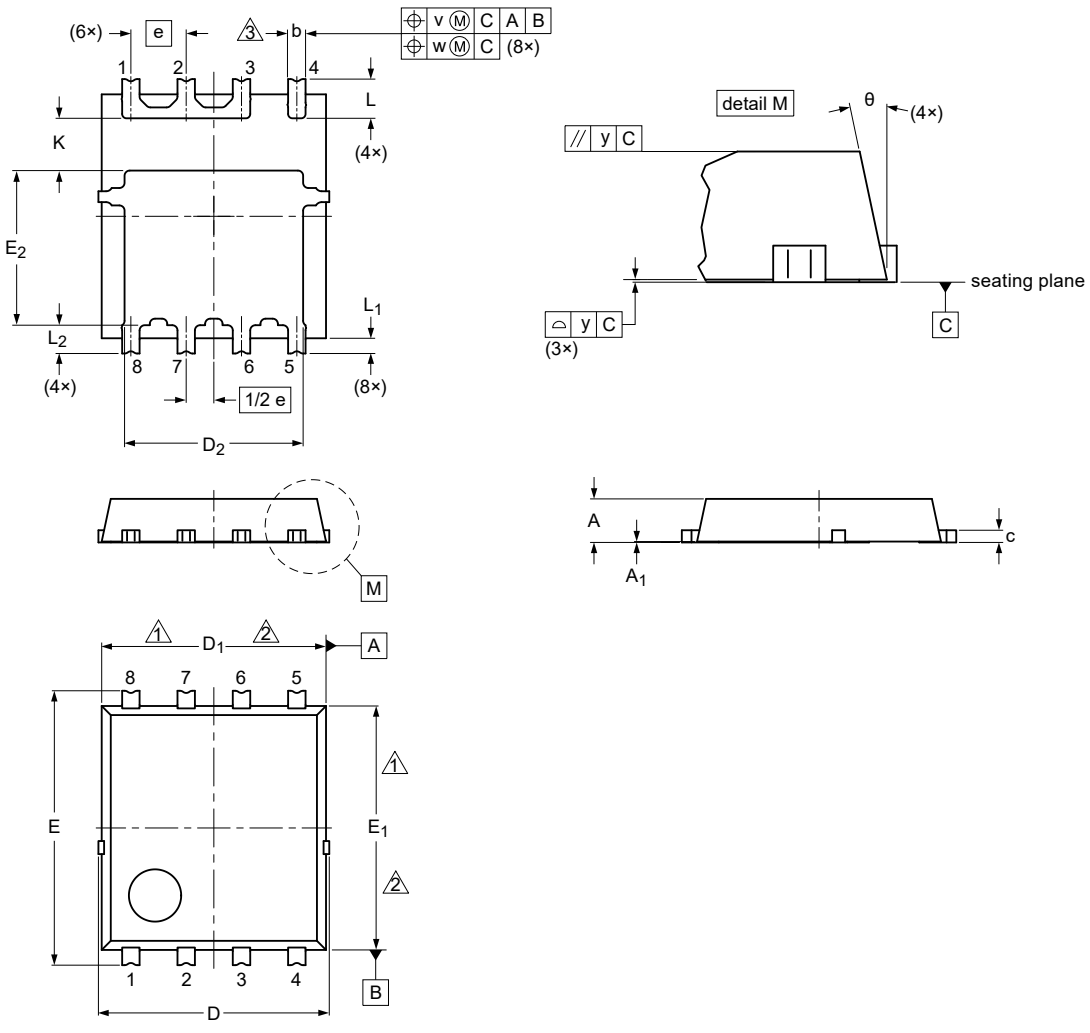


Fig. 17. Reverse recovery timing definition

11. Package outline

MLPAK56: Plastic, thermal enhanced surface mounted package with side-wettable flanks (SWF); minileads; 8 terminals; pitch 1.27 mm; 5.6 x 5.15 x 1.0 mm body **SOT8038-4**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	c	D	D_1	D_2	E	E_1	E_2	e	K	L	L_1	L_2	v	w	y	θ
mm	max	1.1	0.05	0.52	0.33	5.45	5.25	4.25	6.45	5.75	3.65	1.27 BSC	1.2 REF	1.00	0.35 REF	0.75	0.1	0.05	0.1	12°
	nom	1.0			0.28		5.15	4.10	6.30	5.60	3.55			0.90		0.65				
	min	0.9	0	0.34	0.23	5.15	5.05	3.95	6.15	5.45	3.45			0.80		0.55				0°

Note
1. Dimension does not include mold flash, plastic protrusion or gate burrs. These shall not exceed 0.15 mm per end.
2. Dimension does not include interterminal flash or protrusion which shall not exceed 0.25 mm per side.
3. Dimension does not include metal protrusion or burr which shall not exceed 0.075 mm per lead side.

sot8038-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8038-4						24-12-12

Fig. 18. Package outline MLPAK56 (SOT8038-4)

12. Soldering

Footprint information for reflow soldering of MLPAK56 package **SOT8038-4**

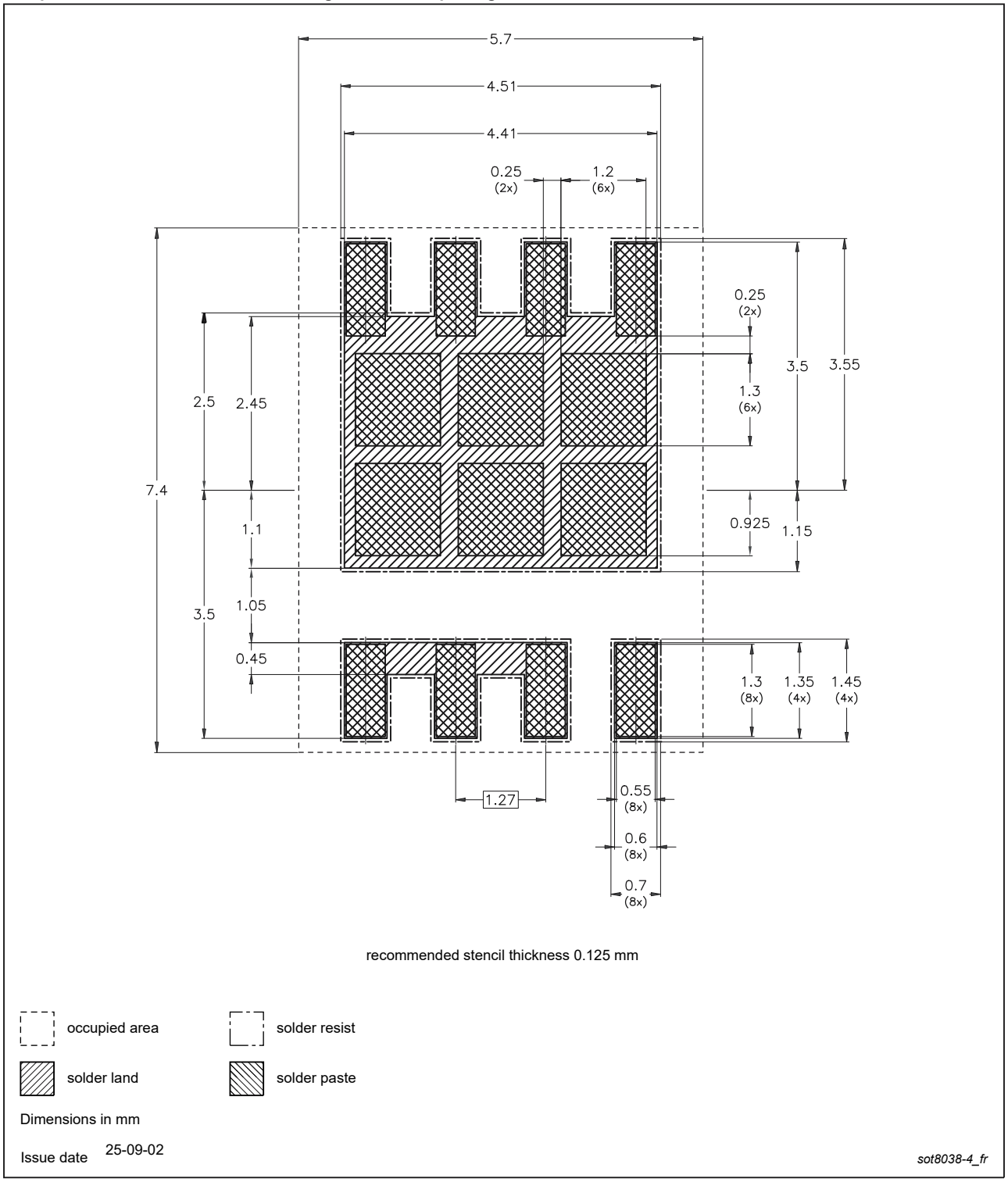


Fig. 19. Reflow soldering footprint for MLPAK56 (SOT8038-4)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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