

AC101B Triple ADC and Stereo DAC Audio CODEC with Headphone Amplifier

1 Features

1. 3 ADC and 2 DAC Audio Codec
2. ADC: SNR 103dB(A), THD -94dB
3. DAC: SNR 117dB(A), THD -90dB
4. Headphone: SNR 117dB(A), THD -80dB
5. Sample Rates Supported: 8kHz~192kHz
6. Low Power Consumption
 - 7uA Low Standby Current
 - 7.124mA Triple Record, 48kHz
 - 7.342mA Stereo Playback, 48kHz
7. Capless Stereo Headphone Driver
 - Integrated charge pump for 0V reference
 - 16mW@1.3V (32Ω)
8. Audio jack insert detection with pop noise free
9. Integrated PLL input clock supports: 400KHz to 24MHz
10. 5mm x 5mm QFN40 Package

2 Applications

1. Smart Voice Assistant Systems
2. Voice Recorders and Players
3. Digital Cameras and video cameras
4. Voice Conferencing System

3 Description

The AC101B is a highly integrated audio codec designed for smart voice assistant systems application. It has one I2S/PCM interface, 3 channel ADC and 2 channel DAC with a capless stereo headphone driver.

An integrated digital PLL supports a large range of input/output frequencies, 400KHz up to 24MHz.

Four analog input paths allow diverse analog audio sources such as two sets of differential microphone, one differential or single-ended line-in or stereo FM input and one Headphone microphone.

One ground-reference headphone output is provided. The output amplifier are powered from an integrated Charge Pump in order to achieve a higher quality, less power consumption in headphone playback, which without any DC blocking capacitor and avoiding unwanted noise.

Two stereo differential speaker output is available by using an external amplifier to drive the loud-speaker.

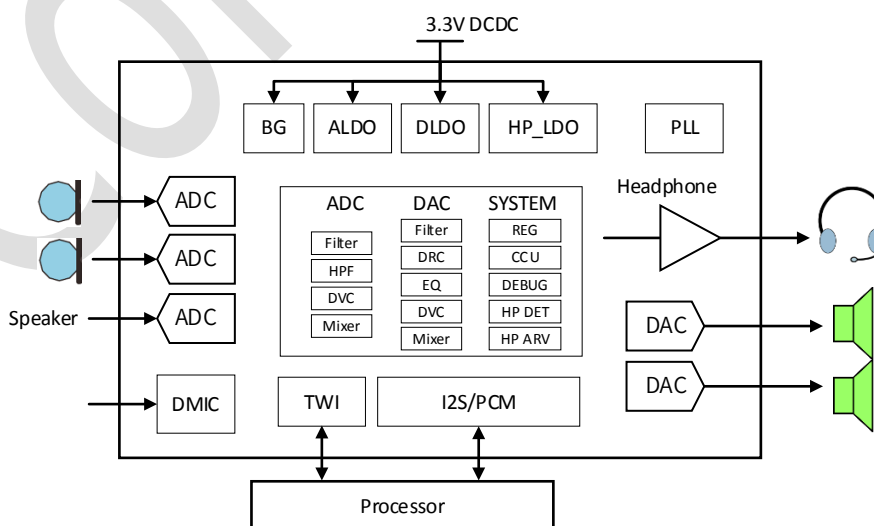
The flexible digital mixers and multiplexers form a varied signal routing to support a complicated application.

AC101B is controlled through TWI (2-wire serial interface). It works only in the slave mode.

The integrated DRC (Dynamic Range Controller) function provide a useful digital sound processing capability in DAC playback path to speaker/headphone. It is used to attenuate the peak signals and boost the low-level signals by adjusting the output signal gain in some conditions

The integrated EQ (Equalizer) consists of 20-band EQ for playback path. Gain, center frequency, and bandwidth of each band EQ can be programmed independently to compensate frequency response of speakers, and to meet various user preferences.

Figure 3-1 Simplified Block Diagram



4 REVISION HISTORY

Revision	Date	Description
V1.0	Apr.30, 2024	Initial release

Confidential

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5 Pin Configuration and Functions

Pin Number	Name	I/O	Description
40	MIC1P	I	Positive differential input for MIC1
1	MIC1N	I	Negative differential input for MIC1
5	AVCC	P	The ALDO Power output for analog part
6	AGND	G	Analog Ground
3	MIC4P	I	Positive differential input for MIC4
4	MIC4N	I	Negative differential input for MIC4
14	MIC2P/ DMICCLK	I	Positive differential input for MIC2/ Digital MIC clock
13	MIC2N/ DMICDAT	I	Negative differential input for MIC2/ Digital MIC data
9	SPORP	O	Differential positive output to speaker2 amplifier
10	SPORN	O	Differential negative output to speaker2 amplifier
11	SPOLP	O	Differential positive output to speaker1 amplifier
12	SPOLN	O	Differential negative output to speaker1 amplifier
15	VCC	P	3.3V power supply
16	VEE	P	Headphone PA negative voltage input
17	HPOUTL	O	Headphone amplifier left channel output
18	HPOUTFB	I	Pseudo differential headphone ground reference
19	HPOUTR	O	Headphone amplifier right channel output
22	CPVDD	P	Analog power for headphone charge pump
23	CPP	IO	Charge pump flying-back capacitor
21	CPN	IO	Charge pump flying-back capacitor
20	CPVEE	P	Charge pump negative decoupling pin
35	HP_DET	I	Audio jack insert detection pin
24	IRQ	O	IRQ for accessory insert and button detect
25	VDD_IO	P	Digital power for digital I/O buffer
26	SDIN	I	I2S interface serial data input
27	SDOUT	O	I2S interface serial data output
28	LRCLK	IO	I2S interface synchronous clock
29	BCLK	IO	I2S interface serial bit clock
30	MCLK	IO	I2S interface master input clock
31	SDA	IO	TWI interface serial data(Open-drain)
32	SCK	I	TWI interface serial clock input(Open-drain)
33	DEVID	IO	TWI interface device ID control
34	VDD_CORE	P	Digital core power
36	RSTN	I	Chip rest pin
8	VRA1	O	Internal reference voltage
7	VRP	O	Internal reference voltage
38	MBIAS	O	Microphone bias voltage output
2	HBIAS	O	Headphone bias voltage output
37	MIC3P	I	Positive differential input for MIC3
39	MIC3N	I	Negative differential input for MIC3
EPAD	GND	G	Digital Ground

Note: O for output, I for input, I/O for input/output, P for power, and G for ground

5.1 Pin Assignment

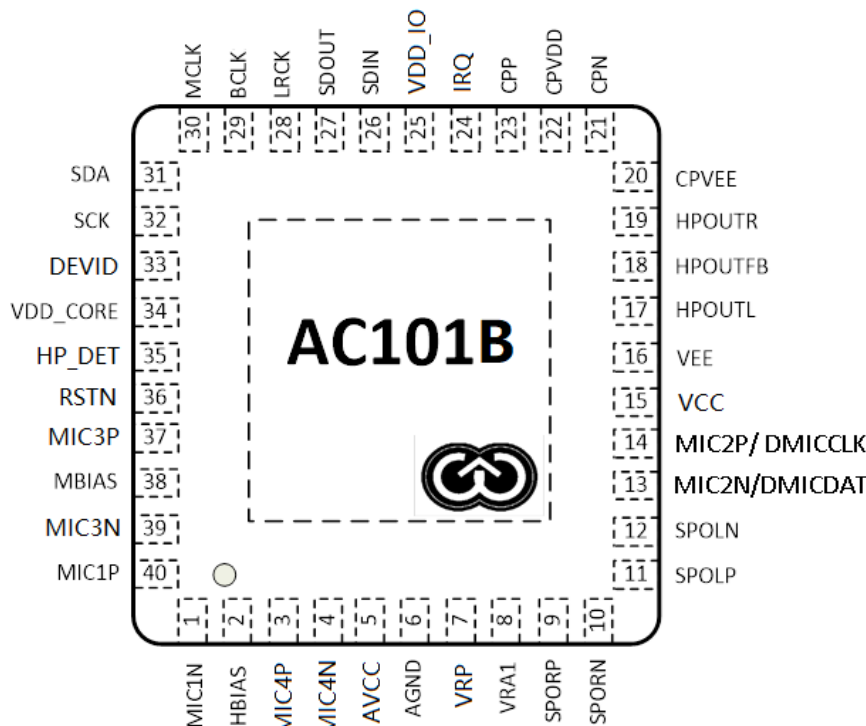


Figure 5-1 AC101B Pin Assignment

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply power	VCC	-0.3	3.9	V
	VDD_IO	-0.3	3.9	V
Integrated power	AVCC	-0.3	3.9	V
	VDD_CORE	-0.3	2.4	V
	CPVDD	-0.3	2.4	V
Digital Input voltage to ground		-0.3	VDD_IO+0.3	V
Analog input voltage to ground		-0.3	AVCC+0.3	V
Operating Temperature, T _A		-40	85	°C
Junction temperature, T _J		-	125	°C
Storage temperature, T _{stg}		-65	150	°C

(1) Current test performance: Pins stressed per JEDEC JESD78D (Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

(2) Over voltage performance: Supplies stressed per JEDEC JESD78D (Class I, Level A) and passed voltage injection as defined in JEDEC.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Human body model(HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 4000	V
	Charged device model(CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows sage manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows sage manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VCC	Chip power supply	3.0	3.3	3.63	V
VDD_IO	Digital power for digital I/O buffer	1.62	3.3	3.63	V
AVCC	Analog power for Audio CODEC, it is generated by inner ALDO	2.396	2.995	3.125	V
VDD_CORE	Digital core power, it is generated by inner DLDO	0.902	1.190	1.895	V
CPVDD	Analog power for headphone charge pump, it is generated by inner HP_LDO	0.8	0.9	1.5	V

6.4 Electrical Characteristics, ADC

At 25°C, VCC = 3.3V, Fs (Audio) = 48 KHz.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
AUDIO ADC(DIFFERENTIAL INPUT)						
Device Setup	AVCC=3.0V、VRP=3.0V、VRA1=1.5V、CPVDD=0.9V、VDD_CORE=1.2V					
Full-Scale input	-	PGA gain = 0dB	-	1	-	Vrms
SNR	Signal-to-Noise Ratio, A-weighted	PGA gain = 0dB	-	103	-	dB
THD+N	Total Harmonic Distortion plus Noise	PGA gain = 0dB 1.0Vpp 1kHz sine input	-	-94	-	dB

6.5 Electrical Characteristics, DAC

At 25°C, VCC = 3.3V, Fs (Audio) = 48 KHz.

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
AUDIO DAC - LINEOUT OUTPUT						
Device Setup	AVCC=3.0V、VRP=3.0V、VRA1=1.5V、CPVDD=0.9V、VDD_CORE=1.2V					
Full-Scale output	-	Line-out gain = 0dB	-	1.8	-	Vrms
SNR	Signal-to-Noise Ratio , A-weighted	Line-out gain = 0dB with auto attenuate	-	123	-	dB
THD+N	Total Harmonic Distortion plus Noise	Line-out gain = 0dB -8.5dBFS 1kHz sine input	-	-91	-	dB
AUDIO DAC - HEADPHONE OUTPUT(R=100k Ω)						
Full-Scale output	-	Line-out gain = 0dB, 100k Ω	-	0.945	-	Vrms
SNR	Signal-to-Noise Ratio , A-weighted	Line-out gain = 0dB with auto attenuate	-	117	-	dB
THD+N	Total Harmonic Distortion plus Noise	Line-out gain = 0dB -8.5dBFS 1kHz sine input	-	-90	-	dB
AUDIO DAC - HEADPHONE OUTPUT(R=16 Ω)						
Full-Scale output	-	Line-out gain = 0dB, 32 Ω	-	0.863	-	Vrms
SNR	Signal-to-Noise Ratio , A-weighted	Line-out gain = 0dB with auto attenuate	-	117	-	dB
THD+N(15mW)	Total Harmonic Distortion plus Noise	Line-out gain = 0dB -8.5dBFS 1kHz sine input	-	-83	-	dB
THD+N(30mW)	Total Harmonic Distortion	Line-out gain = 0dB	-	-80	-	dB

	plus Noise	-8.5dBFS 1kHz sine input				
AUDIO DAC - HEADPHONE OUTPUT(R=32 Ω)						
Full-Scale output	-	Line-out gain = 0dB, 32 Ω	-	0.921	-	Vrms
SNR	Signal-to-Noise Ratio , A-weighted	Line-out gain = 0dB with auto attenuate	-	117	-	dB
THD+N(5mW)	Total Harmonic Distortion plus Noise	Line-out gain = 0dB -8.5dBFS 1kHz sine input	-	-86	-	dB
THD+N(16mW)	Total Harmonic Distortion plus Noise	Line-out gain = 0dB -8.5dBFS 1kHz sine input	-	-80	-	dB

6.6 Electrical Characteristics, Misc.

Parameter	Test Conditions	Min	Typ	Max	Unit
Active Power					
Device Setup	AVCC=3.0V、VRP=3.0V、VRA1=1.5V、CPVDD=0.9V、VDD_CORE=1.2V				
Record path	gain:0dB, 48KHz, ADC 1-3 enable	-	7.124	-	mA
Playback path	DHPL_EN+DACL_EN(0dBFS_1KHz)	-	7.342	-	mA
HEADPHONE	0dBFS_1KHz, 32R, 0dB	-	60.6	-	mA
	0dBFS_1KHz, 16R, 0dB	-	100.60	-	mA
Standby Power					
Standby	Power up, VDD_CORE=1.8V	-	7.15	-	uA
	Lowest power, VDD_CORE=0.9V	-	6.61	-	uA
	Fast power-up, VDD_CORE=1.8V, VRA1 = 1.5V	-	12.17	-	uA
Shut down	Reset	-	0.01	-	uA

7 Detailed Descriptions

7.1 Functional Block Diagram

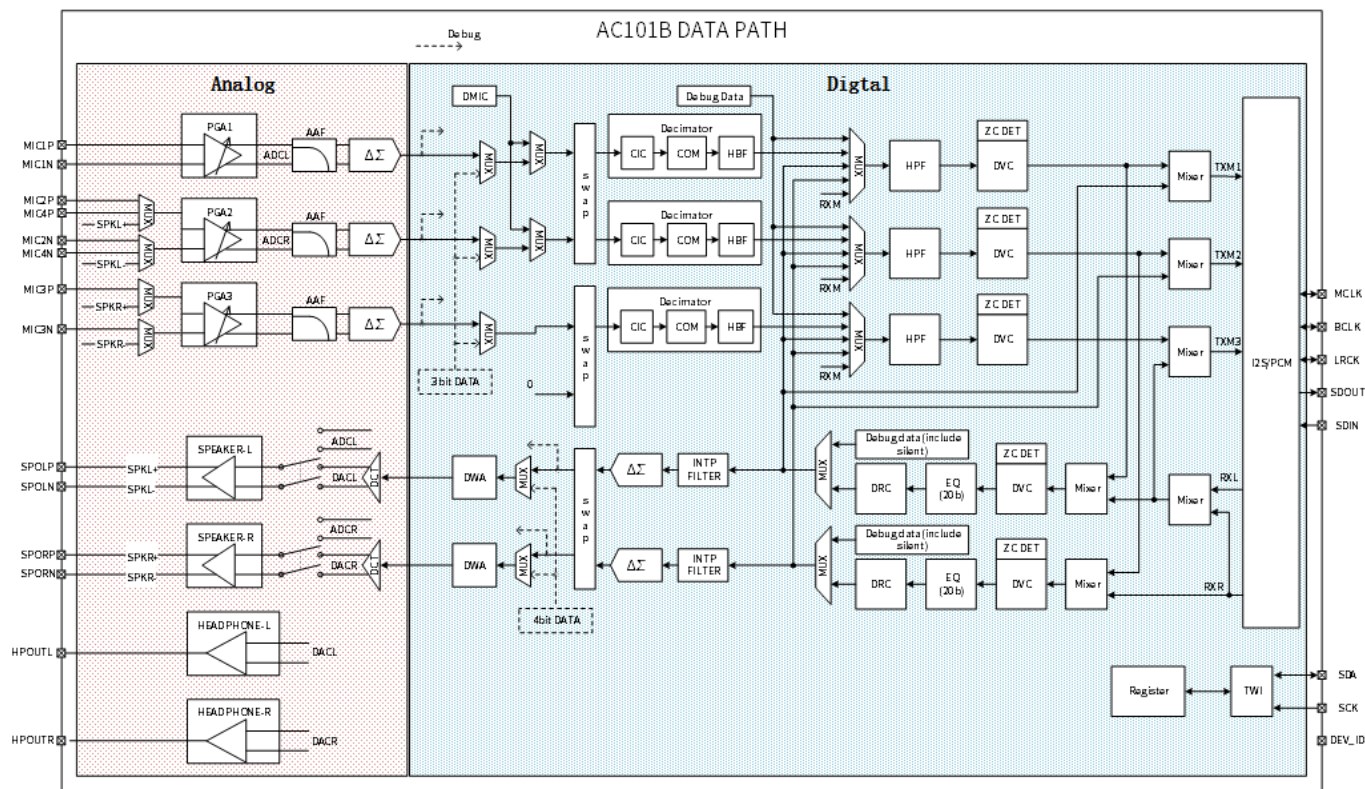


Figure 7-1 Functional Block Diagram

7.2 Feature Description

7.2.1 Power

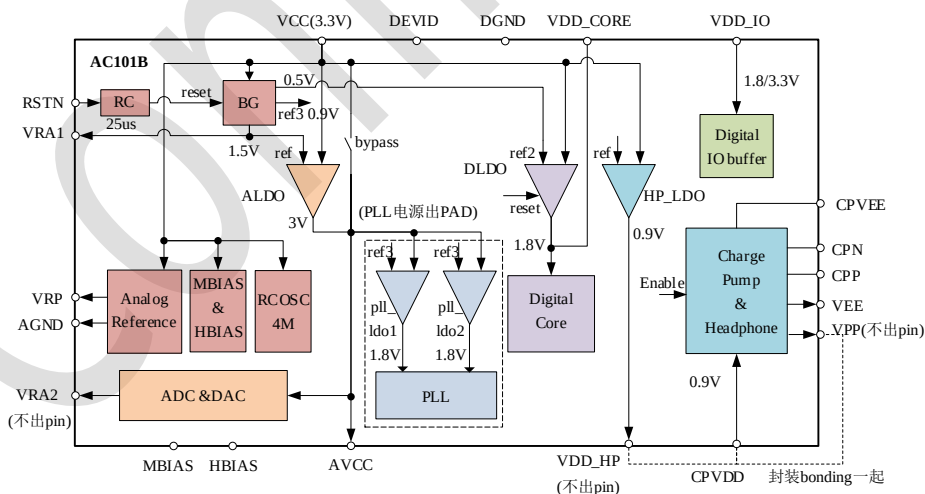


Figure 7-2 Power Management

7.2.2 Reset

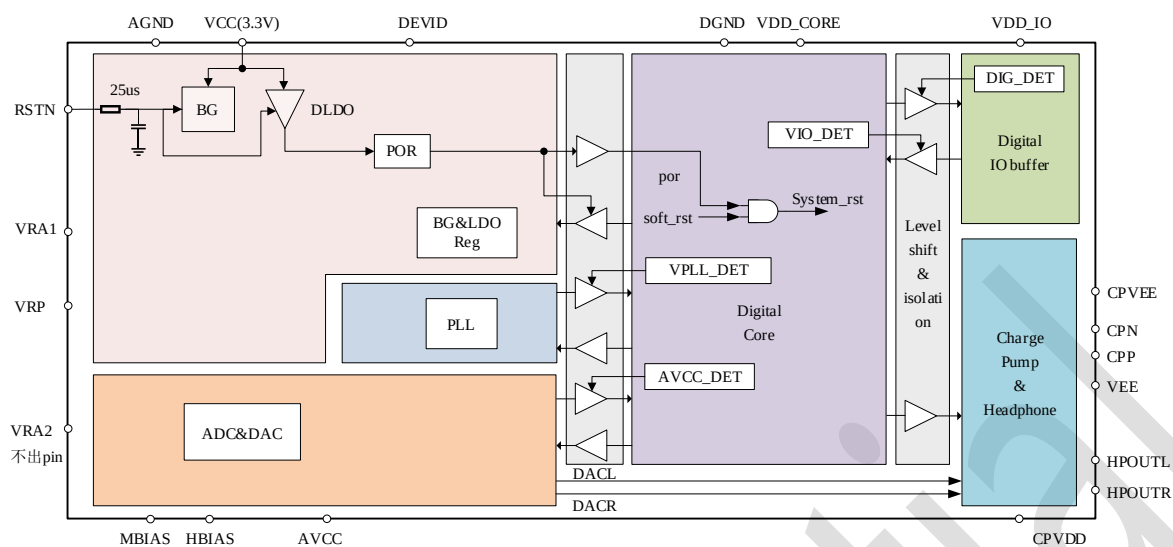


Figure 7-3 Reset Management

7.2.3 Clock

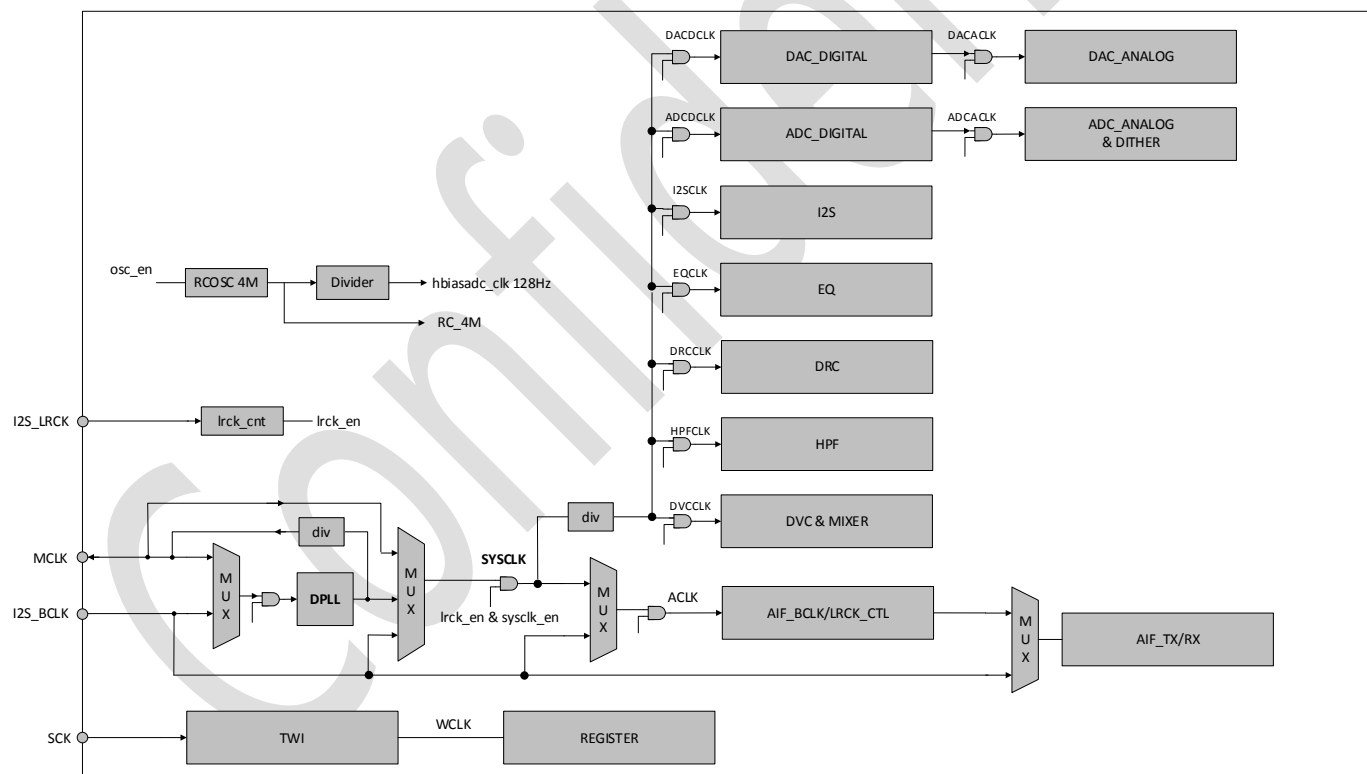


Figure 7-4 Clocking Management

7.2.4 PLL

A Phase-Locked Loop (PLL) is designed to cover a flexible input clock range from 400 KHz to 24MHz. The clock sources of the PLL can be set to MCLK, BCLK by setting register [Reg\[0x20\]](#). The PLL output is always used to provide the system clock (SYSCLK) for AC101B when 24.576MHz or 22.5792MHz cannot be provided from MCLK

and BCLK. The PLL transmit formula as below:

$$F_{OUT} = (F_{IN} * N) / ((M1+1) * (M2+1) * (K1+1) * (K2+1)) ;$$

Table 7-1 clock setting for SYSCLK=24.576MHz

FIN	M1	M2	Fref	N	Fvco	K1	K2	FOUT
400K	0	0	400K	983	393.2M	7	1	24.575M
512K	0	0	512K	960	491.52M	9	1	24.576M
768K	0	0	768K	640	491.52M	9	1	25.576M
800K	0	0	800K	768	614.4M	24	0	24.576M
1.024M	0	0	1.024M	480	491.52M	9	1	24.576M
1.6M	0	0	1.6M	384	614.4M	24	0	24.576M
2.048M	0	0	2.048M	240	491.52M	9	1	24.576M
3.072M	0	0	3.072M	160	491.52M	9	1	24.576M
4.096M	3	0	1.024M	480	491.52M	9	1	24.576M
6M	4	0	1.2M	512	614.4M	24	0	24.576M
12M	9	0	1.2M	512	614.4M	24	0	24.576M
13M	12	0	1M	639	639M	12	1	24.577M
15.36M	9	0	1.536M	320	491.52M	9	1	24.576M
16M	9	0	1.6M	384	614.4M	24	0	24.576M
19.2M	11	0	1.6M	384	614.4M	24	0	24.576M
19.68M	15	1	615K	999	614.385M	24	0	24.575M
24M	9	0	2.4M	256	614.4M	24	0	24.576M
400K	0	0	400K	983	393.2M	7	1	24.575M

Table 7-2 clock setting for SYSCLK=22.5792 MHz

FIN	M1	M2	Fref	N	Fvco	K1	K2	FOUT
400K	0	0	400K	1016	406.4M	8	1	22.5778M
512K	0	0	512K	882	451.584M	9	1	22.5792M
768K	0	0	768K	588	451.584M	9	1	22.5792M
800K	0	0	800K	508	406.4M	8	1	22.5778M
1.024M	0	0	1.024M	441	451.584M	9	1	22.5792M
1.6M	0	0	1.6M	254	406.4M	8	1	22.5778M
2.048M	1	0	1.024M	441	451.584M	9	1	22.5792M
3.072M	2	0	1.024M	441	451.584M	9	1	22.5792M
4.096M	3	0	1.024M	441	451.584M	9	1	22.5792M
6M	5	0	1M	429	429M	18	0	22.5789M
12M	11	0	1M	429	429M	18	0	22.5789M
13M	12	0	1M	429	429M	18	0	22.5789M
15.36M	14	0	1.024M	441	451.584M	9	1	22.5792M
16M	24	0	640K	882	564.48M	24	0	22.5792M
19.2M	4	0	3.84M	147	564.48M	24	0	22.5792M
19.68M	13	1	703K	771	541.9M	23	0	22.5793M
24M	24	0	960K	588	564.48M	24	0	22.5792M
400K	0	0	400K	1016	406.4M	8	1	22.5778M

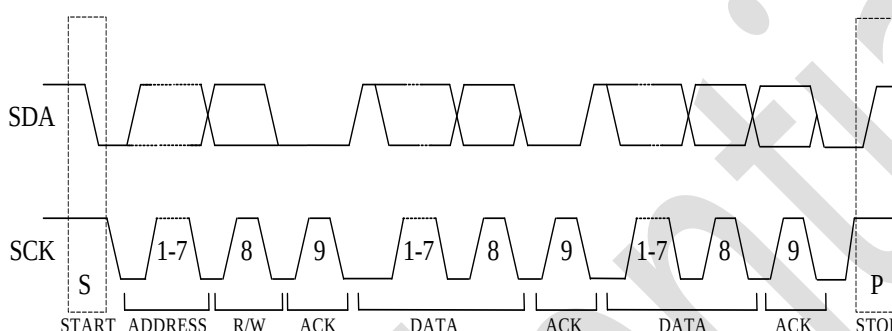
7.2.5 TWI Interface

TWI is a 2-wire (SCK/SDA) half-duplex serial communication interface, supporting only slave mode. SCK is used for clock and SDA is used for data. SCK clock supports up to 400 KHz rate and SDA data is an open drain structure.

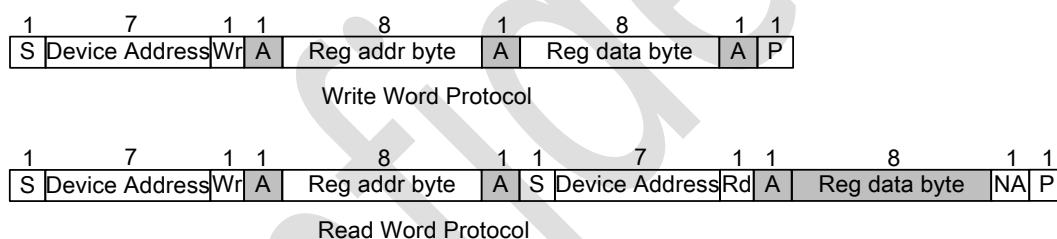
A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave 7-bit address followed by a R/W bit. The 7-bit chip address changed by external two Pins DEV_ID0 and DEV_ID1. The chip address is defined by Table 7-3 below. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCK is high.

Table 7-3 The Chip Slave address

7-bit Address	DEV_ID
0x3D(011 1101)	0
0x3E(011 1110)	1


Figure 7-5 TWI Interface

The formats of “write” and “read” instructions are shown in below.



S: Start Condition
P: Stop Condition
A: 0 for ACK, 1 for NACK
Wr: 0 for Write Command
Rd: 1 for Read Command

Slave Address: 7-bit Device Address
Command Code: 8-bit Register Address
Data Byte: 8-bit Register data
□ : Master-to-Slave
■ : Slave-to-Master

Figure 7-6 TWI Read and Write

7.2.6 I2S/PCM Interface

There are only one I2S/PCM output engine which can be configured as master mode or slave mode in AC101B. The I2S/PCM interfaces provide flexible transit protocol to support varied formats processors.

The serial data is normally driven on negative edge of BCLK. MSB bit of data is normally transmitted first. In the general case, the digital audio interface uses three pins as below:

- BCLK: Bit clock for data synchronization
- LRCK: Left/Right data alignment clock
- SDOUT: output data for ADC1~ADC2 data

I2S audio interface support three different data protocol types below.

- I2S/PCM normal mode
- I2S/PCM TDM mode
- I2S/PCM Encoding mode

I2S/PCM normal mode support four different data format types below. Normal mode is used to transmit 2 channel data on left and right channel simultaneously.

- I2S justified mode
- Left justified mode
- Right justified mode
- PCM short/long frame mode

I2S/PCM TDM mode support four different data format types below. TDM mode is used to transmit up to 16 channel data on timeslot0~timeslot15 when eight AC101B work simultaneously.

- I2S justified TDM mode
- Left justified TDM mode
- Right justified TDM mode
- PCM short/long frame TDM mode

I2S/PCM Encoding mode support four different data format types below. Encoding mode is used to transmit up to 16 channel data using normal I2S format by setting the I2S rate to multi-times of ADC. For example, when the sample rate of ADCs is 16KHz , I2S/PCM Encoding mode can transit 8 channel data by setting I2S LRCK to $16\text{KHz} \times (8/2)$. And the last 4 bits of the sample data indicate the channel number.

- I2S justified Encoding mode
- Left justified Encoding mode
- Right justified Encoding mode
- PCM short/long frame Encoding mode

The timing of I2S in Master mode shows below:

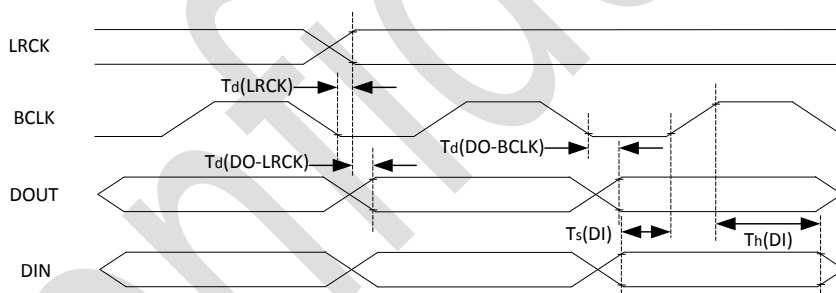
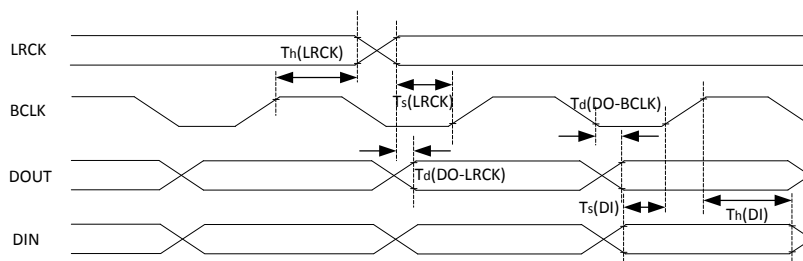


Figure 7-7 I2S Master Mode Timing

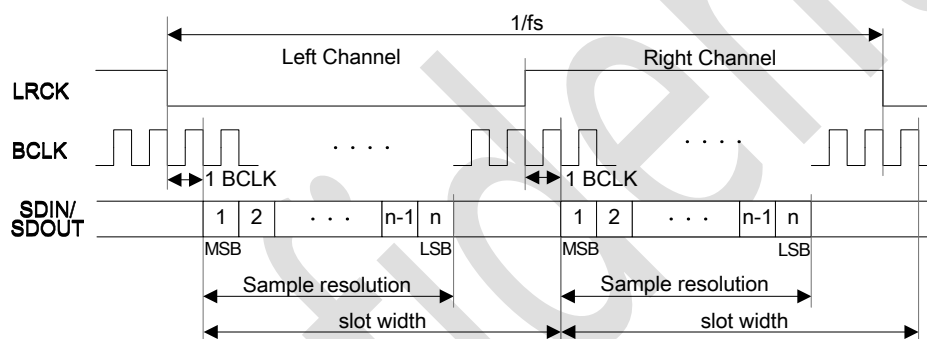
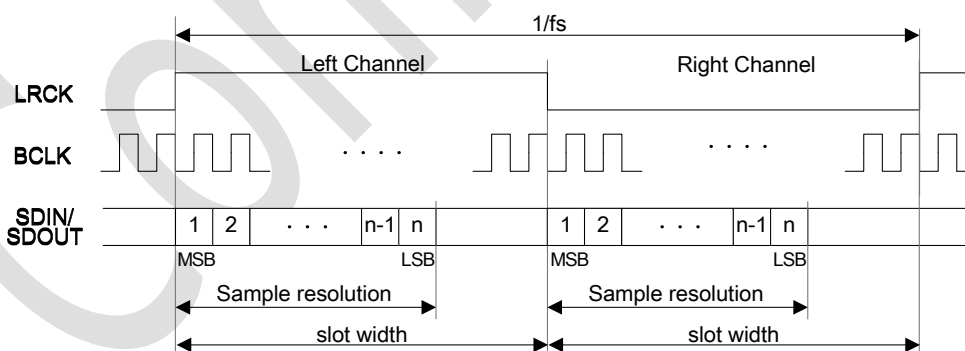
Table 7-4 I2S Timing in Master Mode

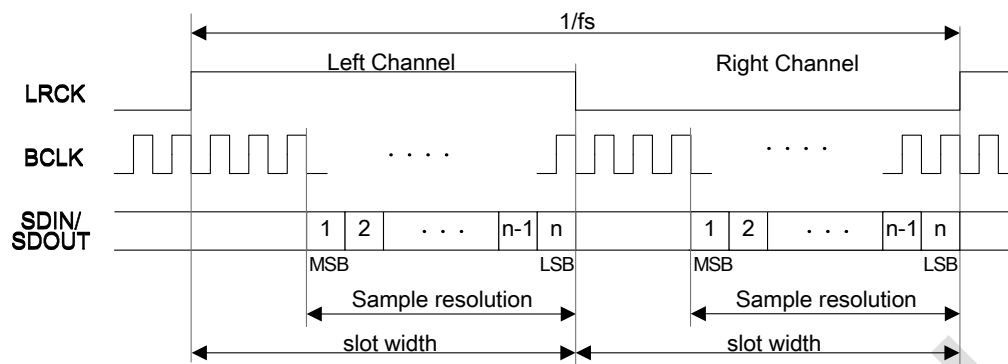
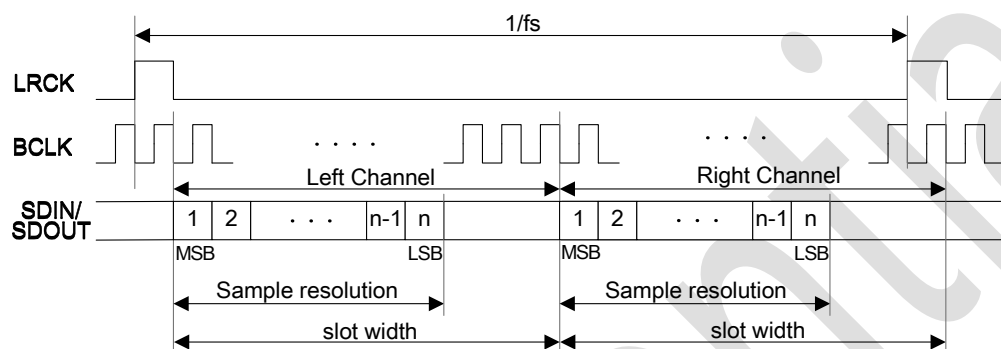
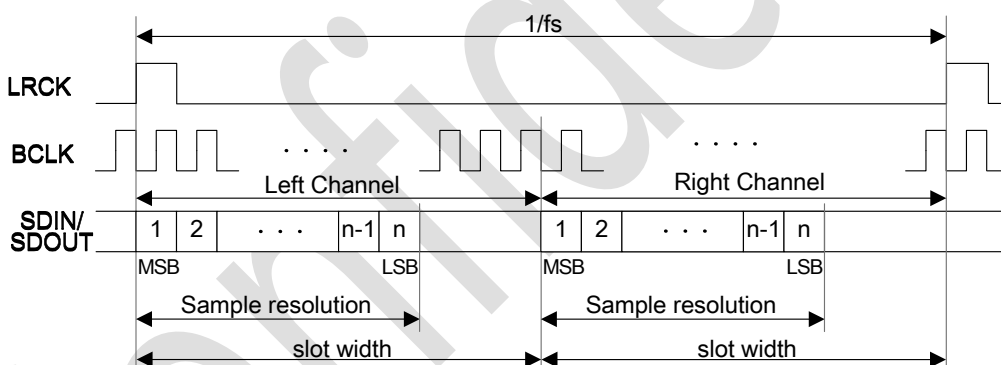
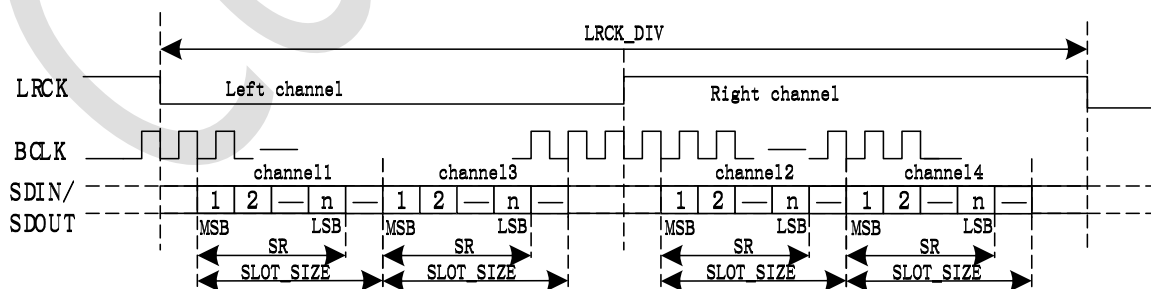
PARAMETER		MIN	MAX	UNITS
Td(LRCK)	LRCK delay	-	10	ns
Td(DO-LRCK)	LRCK to DOUT delay(For LJF)	-	10	ns
Td(DO-BCLK)	BCLK to DOUT delay	-	10	ns
Ts(DI)	DIN setup	4	-	ns
Th(DI)	DIN hold	4	-	ns
Tr	BCLK Rise time	-	8	ns
Tf	BCLK Fall time	-	8	ns

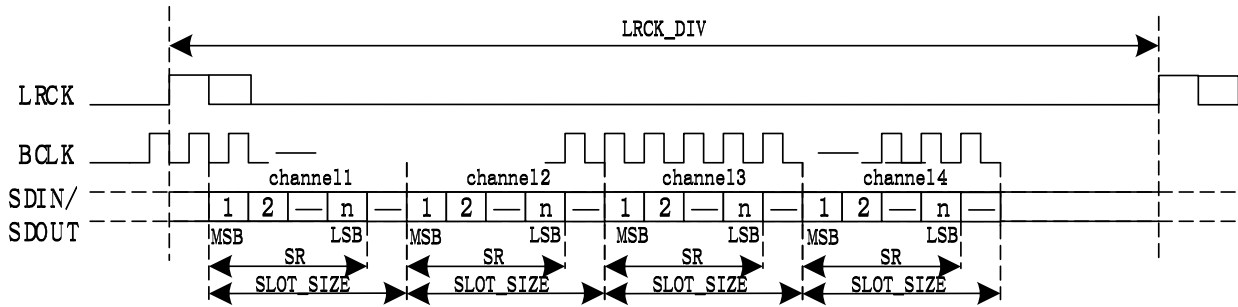
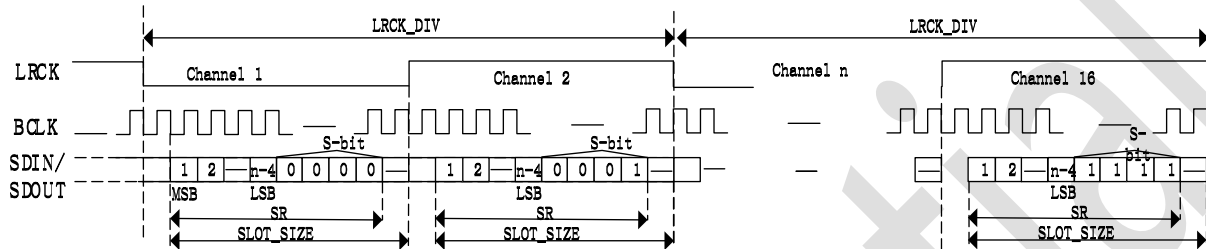
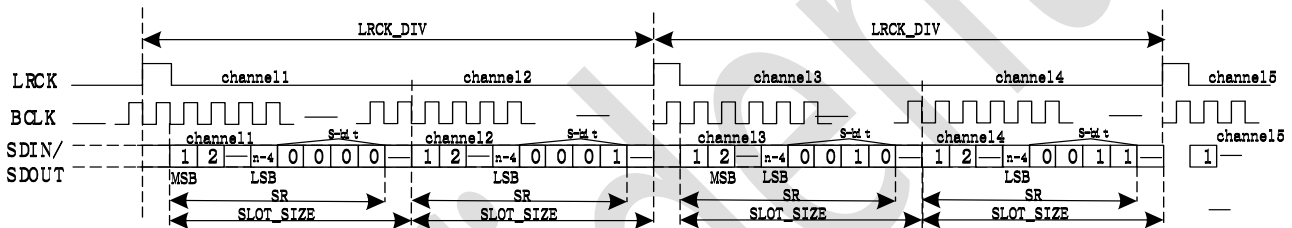
The timing of I2S in slave mode shows below:


Figure 7-8 I2S Slave Mode Timing
Table 7-5 I2S Timing in Slave Mode

PARAMETER		MIN	MAX	UNITS
$T_s(LRCK)$	LRCK setup	4	-	ns
$T_h(LRCK)$	LRCK hold	4	-	ns
$T_d(DO-LRCK)$	LRCK to DOUT delay(For LJF)	-	10	ns
$T_d(DO-BCLK)$	BCLK to DOUT delay	-	10	ns
$T_s(DI)$	DIN setup	4	-	ns
$T_h(DI)$	DIN hold	4	-	ns
T_r	BCLK Rise time	-	4	ns
T_f	BCLK Fall time	-	4	ns


Figure 7-9 I2S Justified mode

Figure 7-10 Left Justified mode


Figure 7-11 Right Justified mode

Figure 7-12 PCM mode A(Offset=1)

Figure 7-13 PCM mode B(Offset=0)

Figure 7-14 I2S TDM mode

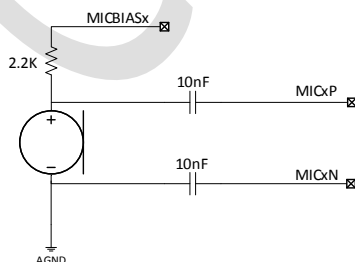
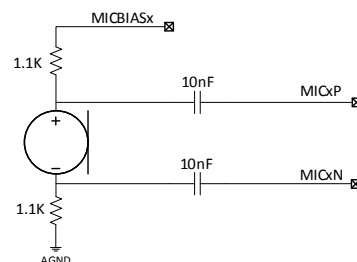

Figure 7-15 PCM TDM mode

Figure 7-16 I2S Encoding mode

Figure 7-17 PCM Encoding mode

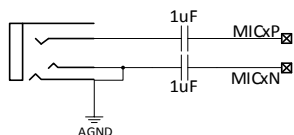
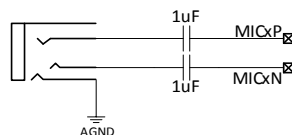
The I2S/PCM management related registers are [Reg\[0x30\]~Reg\[0x44\]](#).

7.2.7 Record Input Path

7.2.7.1 MIC-IN

MIC1P/N, MIC2P/N provide differential input to the ADC1, ADC2 record path. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. There are two independent AAF (Anti-Alias Filter) and PGA (Pre-Gain Amplifier) for the two differential microphone inputs. The gain for each pre-amplifier can be set independently using MIC1BOOST, MIC2BOOST. Two MICBIASx (x=1~2) provide reference voltage for electret condenser type (ECM) microphones.


Figure 7-18 Suggested Single-Ended Mic Input

Figure 7-19 Suggested Differential Mic Input


Figure 7-20 Suggested Single-Ended Line-in

Figure 7-21 Suggested Differential Line-in

7.2.7.2 ADC

The analog ADC data path includes separate programmable Pre-gain amplifier (PGA), anti-aliasing low-pass filter (AAF) and delta-sigma modulator (DSM). The PGA is designed to amplify input signals to the maximum full-scale signal. The AAF is designed to minimize the noise folded down to the audio band by the oversampling ADC, AAF ensure at least 60 dB attenuation at the modulator switching frequency. The DSM oversampling frequency runs at 128fs. The analog ADC data path related registers are [Reg\[0x24\]~Reg\[0x2F\]](#).

7.2.7.3 HPF

A high-pass filter is used in the ADC path to remove any DC components from the incoming audio. This filter operates at all sample rates and can be enabled or disabled. The transfer function for the first order IIR Filter is given by

$$H(z) = \frac{1 - z^{-1}}{1 - az^{-1}}$$

The cutoff frequency of HPF can be changed by setting register [Reg\[0x66\]~Reg\[0x6C\]](#). At $F_s = 48$ kHz, the default corner frequency of this high-pass filter is 1 Hz.

7.2.7.4 DVC

The AC101B includes a digital volume control block with a range from -64dB to +63dB in steps of 0.5dB after HPF. The system controls the volume by setting register [Reg\[0x70\]~Reg\[0x72\]](#). The default digital volume is 0dB (0x81h).

Table 7-6 Digital Volume Control for ADC

Desired Gain(dB)	DVC.Reg(Dec)	DVC.Reg(Hex)
63	255	FF
62.5	254	FE
...	...	...
1	131	83
0.5	130	82
0	129	81
-0.5	128	80
-1	127	7F
...	...	...
-63.5	2	2
-64	1	1
mute	0	0

7.2.7.5 DMIC

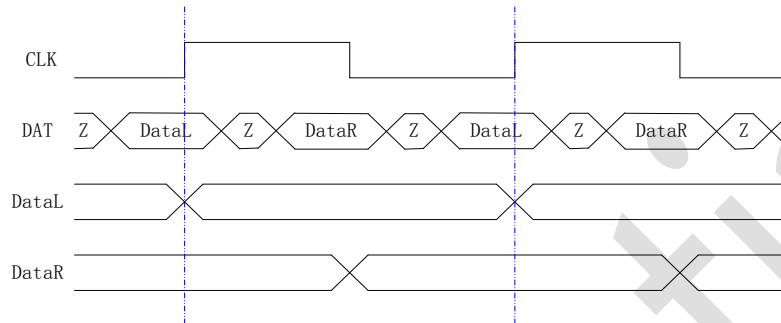
One digital microphone interface is used for dual DMICs. The circuit share decimation filter with audio ADC. DMICCLK can be output 64fs when the DMIC over sample rate is 32kHz~48kHz and 128fs when the DMIC over sample rate is 8kHz~24kHz ($f_s = \text{ADC sample rate}$).

Table 7-7 Digital Microphone Clock

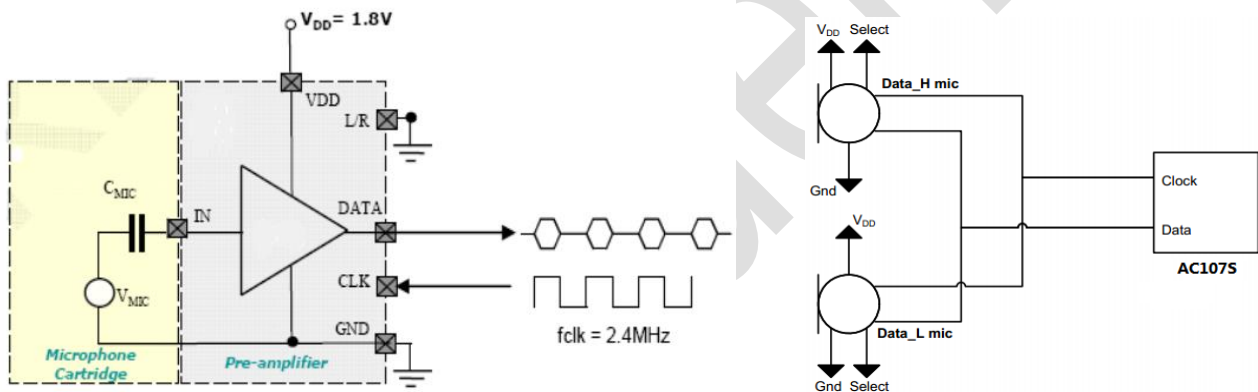
Fs(kHz)	8	12	11.025	16	22.05	24	32	44.1	48
n	128	128	128	128	128	128	64	64	64
Freq(kHz)	1024	1536	1411.2	2048	2822.4	3072	2048	2822.4	3072

Digital Microphone power usually falls between the range 1.6V-3.6V, typical 1.8V. And the Clock frequency is between the ranges 1.024MHz-3.072MHz.

Digital Microphone timing as below:


Figure 7-22 Digital Mixer Path

Digital Microphone application as below:


Figure 7-23 Digital Microphone Application

7.2.8 Playback Output Path

7.2.8.1 EQ

The 20-band parametric Equalizer consists of 20-band EQ for playback path. Gain, center frequency, and bandwidth of each band EQ can be programmed independently to compensate frequency response of speakers, and to meet various user preferences.

Each band EQ can be used for the implementation of low-pass, high-pass or peak filter. The transfer function of each band EQ is given by

$$H(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 + a_1 \cdot z^{-1} + a_2 \cdot z^{-2}}$$

The equalizer register address is located from [Reg\[0x90\]~Reg\[0x9E\]](#). The frequency response for each biquad section with default coefficients is flat at a gain of 0dB.

7.2.8.2 DRC

The dynamic range control (DRC) can be enabled in the digital playback path of AC101B. It automatically adjusts the wide volume gain to flatten volume level.

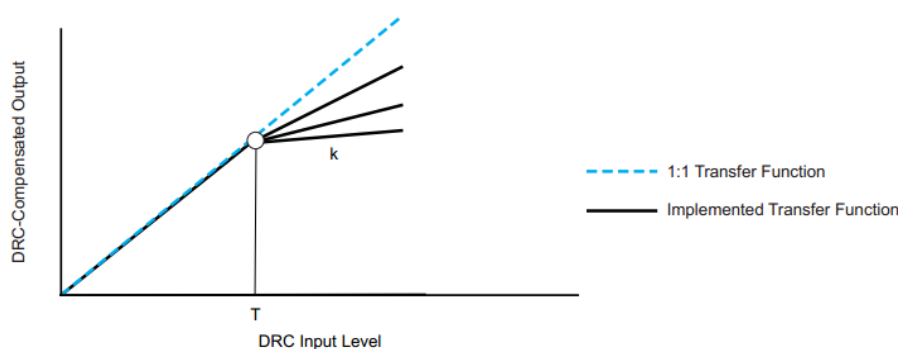


Figure 7-24 DRC Response Characteristic

The DRC supports the main feature below:

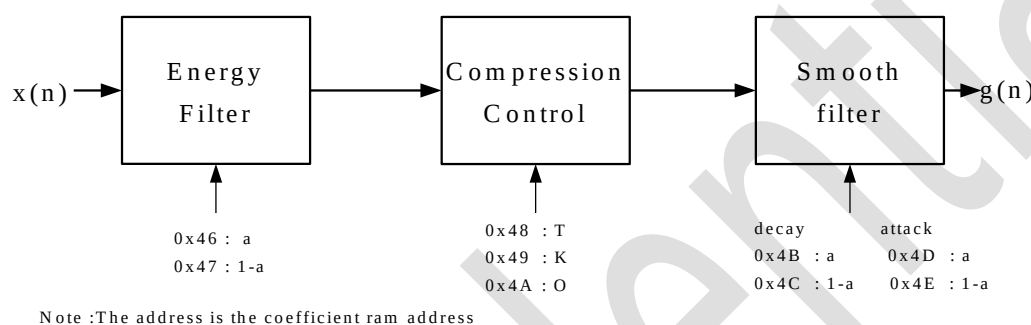


Figure 7-25 DRC Block and Register Control

Adjustable threshold, offset, and compression levels

Programmable energy coefficient, attack, and decay time constants

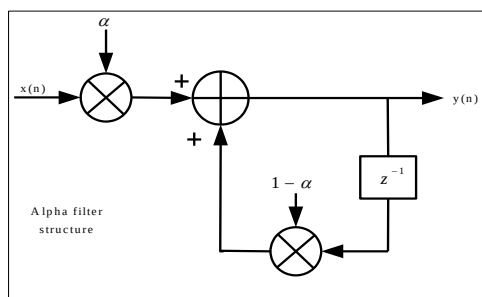
Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

a) DRC parameter setting

Numbers formatted as N.M numbers means that there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 3.24 means that there are 3 bits at the left of the decimal point and 24 bits at the right decimal point.

b) Energy Filter

The Energy Filter is to estimate of the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by $\alpha = 1 - e^{-2.2Ts/ta}$


Figure 7-26 Energy Filter Structure

7.2.8.3 DVC

The AC101B includes a digital volume control block with a range from -64dB to +63dB in steps of 0.5dB after EQ. The system controls the volume by setting register [Reg\[0x85\]~Reg\[0x86\]](#). The default digital volume is 0dB (0x81).

Table 7-8 Digital Volume Control for DAC

Desired Gain(dB)	DVC.Reg(Dec)	DVC.Reg(Hex)
63	255	FF
62.5	254	FE
...	...	...
1	131	83
0.5	130	82
0	129	81
-0.5	128	80
-1	127	7F
...	...	...
-64	1	1
mute	0	0

7.3 Register Maps

7.3.1 Register List

Module Name	7-bit Address	Comments
TWI	0x3D(011 1101)	DEV_ID = 0
	0x3E(011 1110)	DEV_ID = 1

Register Name	Offset	Description
CHIP_SOFT_RST	0x00	Chip Soft Reset
POWER_REG1	0x01	POWER Analog Control Register 1
POWER_REG2	0x02	POWER Analog Control Register 2
POWER_REG3	0x03	POWER Analog Control Register 3
POWER_REG4	0x04	POWER Analog Control Register 4
POWER_REG5	0x05	POWER Analog Control Register 5
POWER_REG6	0x06	POWER Analog Control Register 6
MBIAS_REG	0x07	MBIAS Analog Control Register

HBIAS_REG	0x08	HBIAS Analog Control Register
DAC_REG1	0x09	DAC Analog Control Register 1
DAC_REG2	0x0A	DAC Analog Control Register 2
DAC_REG3	0x0B	DAC Analog Control Register 3
DAC_REG4	0x0C	DAC Analog Control Register 4
PLL_CTRL1	0x10	PLL Configure Control 1 Register
PLL_CTRL2	0x11	PLL Configure Control 2 Register
PLL_CTRL3	0x12	PLL Configure Control 3 Register
PLL_CTRL4	0x13	PLL Configure Control 4 Register
PLL_CTRL5	0x14	PLL Configure Control 5 Register
PLL_CTRL6	0x16	PLL Configure Control 6 Register
PLL_CTRL7	0x17	PLL Configure Control 7 Register
PLL_CTRL8	0x18	PLL Configure Control 8 Register
HP_REG1	0x19	Headphone Analog Control Register 1
HP_REG2	0x1A	Headphone Analog Control Register 2
HP_REG3	0x1B	Headphone Analog Control Register 3
HP_REG4	0x1C	Headphone Analog Control Register 4
HP_REG5	0x1D	Headphone Analog Control Register 5
SYSCLK_CTRL	0x20	System Clock Control Register
ADC1_REG1	0x24	ADC1 Analog Control Register 1
ADC1_REG2	0x25	ADC1 Analog Control Register 2
ADC1_REG3	0x26	ADC1 Analog Control Register 3
ADC1_REG4	0x27	ADC1 Analog Control Register 4
ADC2_REG1	0x28	ADC2 Analog Control Register 1
ADC2_REG2	0x29	ADC2 Analog Control Register 2
ADC2_REG3	0x2A	ADC2 Analog Control Register 3
ADC2_REG4	0x2B	ADC2 Analog Control Register 4
ADC3_REG1	0x2C	ADC3 Analog Control Register 1
ADC3_REG2	0x2D	ADC3 Analog Control Register 2
ADC3_REG3	0x2E	ADC3 Analog Control Register 3
ADC3_REG4	0x2F	ADC3 Analog Control Register 4
I2S_CTRL	0x30	I2S Control Register
I2S_BCLK_CTRL	0x31	I2S BCLK Control Register
I2S_LRCK_CTRL1	0x32	I2S LRCK Control 1 Register
I2S_LRCK_CTRL2	0x33	I2S LRCK Control 2 Register
I2S_FMT_CTRL1	0x34	I2S Format Control 1 Register
I2S_FMT_CTRL2	0x35	I2S Format Control 2 Register
I2S_FMT_CTRL3	0x36	I2S Format Control 3 Register
I2S_TX_CTRL1	0x38	I2S TX Control 1 Register
I2S_TX_CTRL2	0x39	I2S TX Control 2 Register
I2S_TX_CTRL3	0x3A	I2S TX Control 3 Register
I2S_TX_MIX_CTRL	0x3B	I2S TX Mixer Control Register
I2S_TX_CHMP_CTRL1	0x3C	I2S TX Channel Mapping Control 1 Register
I2S_TX_CHMP_CTRL2	0x3D	I2S TX Channel Mapping Control 2 Register
I2S_TX_CHMP_CTRL3	0x3E	I2S TX Channel Mapping Control 3 Register

I2S_TX_CHMP_CTRL4	0x3F	I2S TX Channel Mapping Control 4 Register
I2S_RX_CTRL1	0x40	I2S RX Control 1 Register
I2S_RX_CTRL2	0x41	I2S RX Control 2 Register
I2S_RX_CTRL3	0x42	I2S RX Control 3 Register
I2S_RX_MIX_CTRL	0x43	I2S RX Mixer Control Register
I2S_RX_CHMP_CTRL	0x44	I2S RX Channel Mapping Control Register
DEBUG_CTRL	0x50	Debug Control Register
I2S_PADDRV_CTRL	0x51	I2S Pad Drive Control Register
DEBUG_PADDRV_CTRL	0x52	Debug Pad Drive Control Register
DIG_BYPASS_CTRL	0x53	Digital Bypass Control Register
EFUSE_RD_CTRL	0x54	Efuse Read Control Register
BIST_EN_REG	0x55	BIST Enable Register
BIST_STA_REG	0x56	BIST Status Register
BIST_CTL_REG1	0x57	BIST Control Register 1
BIST_CTL_REG2	0x58	BIST Control Register 2
BIST_CTL_REG3	0x59	BIST Control Register 3
BIST_CTL_REG4	0x5A	BIST Control Register 4
BIST_CTL_REG5	0x5B	BIST Control Register 5
BIST_CTL_REG6	0x5C	BIST Control Register 6
BIST_CTL_REG7	0x5D	BIST Control Register 7
BIST_CTL_REG8	0x5E	BIST Control Register 8
BIST_CTL_REG9	0x5F	BIST Control Register 9
ADDA_FS_CTRL	0x60	ADDA Sample Rate Control Register
ADC_DIG_EN	0x61	ADC Digital Part Enable Register
DMIC_EN	0x62	Digital MIC Enable Register
ADC_DDT_CTRL	0x63	ADC Digital Delay Time Control Register
HPF_EN	0x66	Digital HPF Enable Register
HPF1_COEF_REGH	0x67	High Pass Filter 1 Coef [13:8] Register
HPF1_COEF_REGL	0x68	High Pass Filter 1 Coef [7:0] Register
HPF2_COEF_REGH	0x69	High Pass Filter 2 Coef [13:8] Register
HPF2_COEF_REGL	0x6A	High Pass Filter 2 Coef [7:0] Register
HPF3_COEF_REGH	0x6B	High Pass Filter 3 Coef [13:8] Register
HPF3_COEF_REGL	0x6C	High Pass Filter 3 Coef [7:0] Register
ADC1_MUX_CTRL	0x6D	ADC1 Digital Multiplexer Control Register
ADC2_MUX_CTRL	0x6E	ADC2 Digital Multiplexer Control Register
ADC3_MUX_CTRL	0x6F	ADC3 Digital Multiplexer Control Register
ADC1_DVOL_CTRL	0x70	ADC1 Digital Channel Volume Control Register
ADC2_DVOL_CTRL	0x71	ADC2 Digital Channel Volume Control Register
ADC3_DVOL_CTRL	0x72	ADC3 Digital Channel Volume Control Register
HMIC_DET_CTRL	0x73	HMIC Detect Control Register
HMIC_DET_DBC	0x74	HMIC Detect Debounce Register
HMIC_DET_TH1	0x75	HMIC Detect Threshold 1 Control Register
HMIC_DET_TH2	0x76	HMIC Detect Threshold 2 Control Register
HMIC_DET_DATA	0x77	HMIC Detect ADC Data Register
HP_DET_CTRL	0x78	Headphone Detect Control Register

HP_DET_DBC	0x79	Headphone Detect Debounce Register
HP_DET_IRQ	0x7A	Headphone Detect Interrupt Enable Register
HP_DET_STA	0x7B	Headphone Detect Status Register
ADC_DIG_DEBUG	0x7F	ADC Digital Debug Control Register
DAC_DIG_EN	0x81	DAC Digital Part Enable Register
DAC_DIG_CTRL	0x82	DAC Digital Control Register
DAC_DHP_GAIN_CTRL	0x83	DAC DHP Gain Control Register
DAC_LOUT_CTRL	0x84	DAC LOUT Control Register
DAC_DVC_L	0x85	DAC Left Channel Digital Volume Register
DAC_DVC_R	0x86	DAC Right Channel Digital Volume Register
EQ_CTRL	0x87	EQ Control Register
EQ_COEF_CTRL	0x88	EQ Band-n Coefficient Control Register
DAC_MUX_CTRL	0x89	DAC Digital Multiplexer Control Register
HP_AVR_CTRL	0x8A	Headphone Adaptive Voltage Regulation Control Register
HP_AVR_THH	0x8B	Headphone Adaptive Voltage Regulation Threshold[23:16] Register
HP_AVR_THM	0x8C	Headphone Adaptive Voltage Regulation Threshold[15:8] Register
HP_AVR_THL	0x8D	Headphone Adaptive Voltage Regulation Threshold[7:0] Register
HP_AVR_DBC	0x8E	Headphone Adaptive Voltage Regulation Debounce Register
HP_LOUT_CTRL	0x8F	Headphone LOUT Control Register
EQ_B0_H	0x90	Band-n B0 Coef [20:16] Register
EQ_B0_M	0x91	Band-n B0 Coef [15:8] Register
EQ_B0_L	0x92	Band-n B0 Coef [7:0] Register
EQ_B1_H	0x93	Band-n B1 Coef [20:16] Register
EQ_B1_M	0x94	Band-n B1 Coef [15:8] Register
EQ_B1_L	0x95	Band-n B1 Coef [7:0] Register
EQ_B2_H	0x96	Band-n B2 Coef [20:16] Register
EQ_B2_M	0x97	Band-n B2 Coef [15:8] Register
EQ_B2_L	0x98	Band-n B2 Coef [7:0] Register
EQ_A1_H	0x99	Band-n A1 Coef [20:16] Register
EQ_A1_M	0x9A	Band-n A1 Coef [15:8] Register
EQ_A1_L	0x9B	Band-n A1 Coef [7:0] Register
EQ_A2_H	0x9C	Band-n A2 Coef [20:16] Register
EQ_A2_M	0x9D	Band-n A2 Coef [15:8] Register
EQ_A2_L	0x9E	Band-n A2 Coef [7:0] Register
DRC_ENA	0xA0	DRC Enable Register
DRC_HPFC_1	0xA1	DRC HPF Coef [26:24] Register
DRC_HPFC_2	0xA2	DRC HPF Coef [23:16] Register
DRC_HPFC_3	0xA3	DRC HPF Coef [15:8] Register
DRC_HPFC_4	0xA4	DRC HPF Coef [7:0] Register
DRC_CTRL	0xA5	DRC Control Register
DRC_DLY_CTRL	0xA6	DRC Delay Control Register
DRC_OPT_1	0xA7	DRC Optimum 1 Register
DRC_OPT_2	0xA8	DRC Optimum 2 Register
DRC_LPFAT_1	0xAC	DRC Left Peak Filter Attack Time Coef [26:24] Register
DRC_LPFAT_2	0xAD	DRC Left Peak Filter Attack Time Coef [23:16] Register

DRC_LPFAT_3	0xAE	DRC Left Peak Filter Attack Time Coef [15:8] Register
DRC_LPFAT_4	0xAF	DRC Left Peak Filter Attack Time Coef [7:0] Register
DRC_RPFAT_1	0xB0	DRC Right Peak Filter Attack Time Coef [26:24] Register
DRC_RPFAT_2	0xB1	DRC Right Peak Filter Attack Time Coef [23:16] Register
DRC_RPFAT_3	0xB2	DRC Right Peak Filter Attack Time Coef [15:8] Register
DRC_RPFAT_4	0xB3	DRC Right Peak Filter Attack Time Coef [7:0] Register
DRC_LPFRT_1	0xB4	DRC Left Peak Filter Release Time Coef [26:24] Register
DRC_LPFRT_2	0xB5	DRC Left Peak Filter Release Time Coef [23:16] Register
DRC_LPFRT_3	0xB6	DRC Left Peak Filter Release Time Coef [15:8] Register
DRC_LPFRT_4	0xB7	DRC Left Peak Filter Release Time Coef [7:0] Register
DRC_RPFRT_1	0xB8	DRC Right Peak Filter Release Time Coef [26:24] Register
DRC_RPFRT_2	0xB9	DRC Right Peak Filter Release Time Coef [23:16] Register
DRC_RPFRT_3	0xBA	DRC Right Peak Filter Release Time Coef [15:8] Register
DRC_RPFRT_4	0xBB	DRC Right Peak Filter Release Time Coef [7:0] Register
DRC_LRMSAT_1	0xBC	DRC Left RMS Filter Average Time Coef [26:24] Register
DRC_LRMSAT_2	0xBD	DRC Left RMS Filter Average Time Coef [23:16] Register
DRC_LRMSAT_3	0xBE	DRC Left RMS Filter Average Time Coef [15:8] Register
DRC_LRMSAT_4	0xBF	DRC Left RMS Filter Average Time Coef [7:0] Register
DRC_RRMSAT_1	0xC0	DRC Right RMS Filter Average Time Coef [26:24] Register
DRC_RRMSAT_2	0xC1	DRC Right RMS Filter Average Time Coef [23:16] Register
DRC_RRMSAT_3	0xC2	DRC Right RMS Filter Average Time Coef [15:8] Register
DRC_RRMSAT_4	0xC3	DRC Right RMS Filter Average Time Coef [7:0] Register
DRC_CT_1	0xC4	DRC Compressor Threshold Setting [31:24] Register
DRC_CT_2	0xC5	DRC Compressor Threshold Setting [23:16] Register
DRC_CT_3	0xC6	DRC Compressor Threshold Setting [15:8] Register
DRC_CT_4	0xC7	DRC Compressor Threshold Setting [7:0] Register
DRC_KC_1	0xC8	DRC Compressor Slope Setting [31:24] Register
DRC_KC_2	0xC9	DRC Compressor Slope Setting [23:16] Register
DRC_KC_3	0xCA	DRC Compressor Slope Setting [15:8] Register
DRC_KC_4	0xCB	DRC Compressor Slope Setting [7:0] Register
DRC_OPC_1	0xCC	DRC Compressor Output at Compressor Threshold [31:24] Register
DRC_OPC_2	0xCD	DRC Compressor Output at Compressor Threshold [23:16] Register
DRC_OPC_3	0xCE	DRC Compressor Output at Compressor Threshold [15:8] Register
DRC_OPC_4	0xCF	DRC Compressor Output at Compressor Threshold [7:0] Register
DRC_LT_1	0xD0	DRC Limiter Threshold Setting [31:24] Register
DRC_LT_2	0xD1	DRC Limiter Threshold Setting [23:16] Register
DRC_LT_3	0xD2	DRC Limiter Threshold Setting [15:8] Register
DRC_LT_4	0xD3	DRC Limiter Threshold Setting [7:0] Register
DRC_KL_1	0xD4	DRC Limiter Slope Setting [31:24] Register
DRC_KL_2	0xD5	DRC Limiter Slope Setting [23:16] Register
DRC_KL_3	0xD6	DRC Limiter Slope Setting [15:8] Register
DRC_KL_4	0xD7	DRC Limiter Slope Setting [7:0] Register
DRC_OPL_1	0xD8	DRC Limiter Output at Limiter Threshold [31:24] Register
DRC_OPL_2	0xD9	DRC Limiter Output at Limiter Threshold [23:16] Register
DRC_OPL_3	0xDA	DRC Limiter Output at Limiter Threshold [15:8] Register

DRC_OPL_4	0xDB	DRC Limiter Output at Limiter Threshold [7:0] Register
DRC_ET_1	0xDC	DRC Expander Threshold Setting [31:24] Register
DRC_ET_2	0xDD	DRC Expander Threshold Setting [23:16] Register
DRC_ET_3	0xDE	DRC Expander Threshold Setting [15:8] Register
DRC_ET_4	0xDF	DRC Expander Threshold Setting [7:0] Register
DRC_KE_1	0xE0	DRC Expander Slope Setting [31:24] Register
DRC_KE_2	0xE1	DRC Expander Slope Setting [23:16] Register
DRC_KE_3	0xE2	DRC Expander Slope Setting [15:8] Register
DRC_KE_4	0xE3	DRC Expander Slope Setting [7:0] Register
DRC_OPE_1	0xE4	DRC Expander Output at Expander Threshold [31:24] Register
DRC_OPE_2	0xE5	DRC Expander Output at Expander Threshold [23:16] Register
DRC_OPE_3	0xE6	DRC Expander Output at Expander Threshold [15:8] Register
DRC_OPE_4	0xE7	DRC Expander Output at Expander Threshold [7:0] Register
DRC_KN_1	0xE8	DRC Linear Slope Setting [31:24] Register
DRC_KN_2	0xE9	DRC Linear Slope Setting [23:16] Register
DRC_KN_3	0xEA	DRC Linear Slope Setting [15:8] Register
DRC_KN_4	0xEB	DRC Linear Slope Setting [7:0] Register
DRC_SFAT_1	0xEC	DRC Smooth filter Gain Attack Time Coef [26:24] Register
DRC_SFAT_2	0xED	DRC Smooth filter Gain Attack Time Coef [23:16] Register
DRC_SFAT_3	0xEE	DRC Smooth filter Gain Attack Time Coef [15:8] Register
DRC_SFAT_4	0xEF	DRC Smooth filter Gain Attack Time Coef [7:0] Register
DRC_SFRT_1	0xF0	DRC Smooth filter Gain Release Time Coef [26:24] Register
DRC_SFRT_2	0xF1	DRC Smooth filter Gain Release Time Coef [23:16] Register
DRC_SFRT_3	0xF2	DRC Smooth filter Gain Release Time Coef [15:8] Register
DRC_SFRT_4	0xF3	DRC Smooth filter Gain Release Time Coef [7:0] Register
DRC_MXGS_1	0xF4	DRC MAX Gain Setting [31:24] Register
DRC_MXGS_2	0xF5	DRC MAX Gain Setting [23:16] Register
DRC_MXGS_3	0xF6	DRC MAX Gain Setting [15:8] Register
DRC_MXGS_4	0xF7	DRC MAX Gain Setting [7:0] Register
DRC_MNGS_1	0xF8	DRC MIN Gain Setting [31:24] Register
DRC_MNGS_2	0xF9	DRC MIN Gain Setting [23:16] Register
DRC_MNGS_3	0xFA	DRC MIN Gain Setting [15:8] Register
DRC_MNGS_4	0xFB	DRC MIN Gain Setting [7:0] Register
DRC_EPSC_1	0xFC	DRC Expander Smooth Time Coef [26:24] Register
DRC_EPSC_2	0xFD	DRC Expander Smooth Time Coef [23:16] Register
DRC_EPSC_3	0xFE	DRC Expander Smooth Time Coef [15:8] Register
DRC_EPSC_4	0xFF	DRC Expander Smooth Time Coef [7:0] Register

7.3.2 Register Description

7.3.2.1 数字系统软复位

Reg 00h Chip Soft Reset Register (Default Value: 0x17)

Offset: 0x00			Register Name: CHIP_SOFT_RST
Bit	R/W	Default	Description

7:0	R/W	0x17	SOFT_RESET Writing (0x34) to this register resets all registers and all digital modules to their default state. Reading from this register will indicate device type and version.
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7.3.2.2 Power 控制寄存器

Reg 01h POWER Analog Control Register 1 (Default Value:0x00)

Offset: 0x01			Register Name: POWER_REG1
Bit	R/W	Default	Description
7	R/W	0x0	VRA1_SPEEDUP_DISABLE VRA1 speedup disable control 0: VRA1 speedup open 1: VRA1 speedup finish
6	R/W	0x0	BG_BUFEN BG Output Buffer Enable For Vra1 0: Disable 1: Enable
5:4	R/W	0x0	BG_VSEL BG Output Voltage Sel For Vra1 00: 1.5V 01: 1.35V 10: 1.1V 11: 0.9V
3:0	R/W	0x0	BG_TRIM BG Output Voltage Trimming For Vra1 0000: 1.50V 1000: 1.42V 0001: 1.51V 1001: 1.43V 0010: 1.52V 1010: 1.44V 0011: 1.53V 1011: 1.45V 0100: 1.54V 1100: 1.46V 0101: 1.55V 1101: 1.47V 0110: 1.56V 1110: 1.48V 0111: 1.57V 1111: 1.49V when POWER_REG1<5:4>=00

Reg 02h POWER Analog Control Register 2 (Default Value:0x04)

Offset: 0x02			Register Name: POWER_REG2
Bit	R/W	Default	Description
7	R/W	0x0	CURRENT_TEST_SELECT Internal Current Sink Test Enable (from MICIN1P pin) 0: Normal 1: For Debug
6:4	R/W	0x0	BG_Current_TRIM Bandgap Output Current Trimming According to MICIN1P Test 000: 5.00uA 100: 4.82uA 001: 5.05uA 101: 4.87uA

			010: 5.10uA 110: 4.91uA 011: 5.15uA 111: 4.96uA
3	R/W	0x0	OSC_EN Internal Oscillator Enable Control for 4MHz Clock 0: Disable 1: Enable
2:0	R/W	0x4	OSC_CLOCK_TRIM Internal Oscillator Output 4MHz Clock Frequency Trimming 000: 3.30MHz 100: 3.92MHz 001: 3.47MHz 101: 4.05MHz 010: 3.62MHz 110: 4.20MHz 011: 3.77MHz 111: 4.33MHz

Reg 03h POWER Analog Control Register 3 (Default Value:0x1C)

Offset: 0x03			Register Name: POWER_REG3
Bit	R/W	Default	Description
7	R/W	0x0	VRP_BYPASS VRP Output Voltage Bypass 0: Normal 1: Bypass to VDD33
6	R/W	0x0	DLDO_LQ DLDO Static Low Power Disable Control 0: Low Power Mode 1: Normal Mode
5	R/W	0x0	VRP_NOCAP_EN VRP PIN NO CAP IN PCB Enable 0: Need CAP 1: No CAP
4:0	R/W	0x1C	DLDO_VSEL DLDO Output Voltage Control 00000: 0.902V 10000: 1.415V 00001: 0.934V 10001: 1.447V 00010: 0.966V 10010: 1.479V 00011: 0.998V 10011: 1.511V 00100: 1.031V 10100: 1.543V 00101: 1.062V 10101: 1.575V 00110: 1.094V 10110: 1.607V 00111: 1.126V 10111: 1.639V 01000: 1.158V 11000: 1.671V 01001: 1.190V 11001: 1.703V 01010: 1.223V 11010: 1.735V 01011: 1.255V 11011: 1.767V 01100: 1.287V 11100: 1.799V 01101: 1.319V 11101: 1.831V 01110: 1.351V 11110: 1.863V 01111: 1.383V 11111: 1.895V

Reg 04h POWER Analog Control Register 4 (Default Value:0x10)

Offset: 0x04			Register Name: POWER_REG4
Bit	R/W	Default	Description
7	R/W	0x0	ALDO_EN ALDO Enable Control 0: Disable 1: Enable
6:4	R/W	0x1	ALDO_VSEL ALDO Output Voltage Select 000: 3.125V 100: 2.662V 001: 2.995V 101: 2.567V 010: 2.875V 110: 2.479V 011: 2.765V 111: 2.396V
3	R/W	0x0	ALDO_BYPASS ALDO Output Voltage Bypass 0: Normal 1: Bypass to VDD33
2	R/W	0x0	Reserved
1	R	0x0	AVCC_POR The flag of ALDO power on 0: AVCC is power off 1: AVCC is power on
0	R/W	0x0	ADDA_BIASEN ADDA Current Bias Enable 0: Disable 1: Enable

Reg 05h POWER Analog Control Register 5 (Default Value:0x11)

Offset: 0x05			Register Name: POWER_REG5
Bit	R/W	Default	Description
7	R/W	0x0	HPLDO_EN HPLDO Enable Control 0: Disable 1: Enable
6:4	R/W	0x1	HPLDO_VSEL HPLDO Output Voltage Select 000: 0.8V 100: 1.2V 001: 0.9V 101: 1.3V 010: 1.0V 110: 1.4V 011: 1.1V 111: 1.5V
3	R/W	0x0	VRP_EN VRP Output Voltage Enable Control 0: Disable 1: Enable
2:0	R/W	0x1	VRP_VSEL

			VRP Output Voltage Select
			000: 3.125V 100: 2.662V
			001: 2.995V 101: 2.567V
			010: 2.875V 110: 2.479V
			011: 2.765V 111: 2.396V

Reg 06h POWER Analog Control Register 6 (Default Value:0x55)

Offset: 0x06			Register Name: POWER_REG6
Bit	R/W	Default	Description
7:6	R/W	0x1	IOPDRVS Headphone Driver Bias Current Control 0: 6uA 1: 7uA 2: 8uA 3: 9uA
5:4	R/W	0x1	IOPVRS OPVR Bias Current Control 0: 6uA 1: 7uA 2: 8uA 3: 9uA
3:2	R/W	0x1	IOPDACS DAC OP Bias Current Control 0: 6uA 1: 7uA 2: 8uA 3: 9uA
1:0	R/W	0x1	ISPKS Speaker Output OP Bias Current Control 0: 6uA 1: 7uA 2: 8uA 3: 9uA

Reg 07h MBIAS Analog Control Register (Default Value:0x30)

Offset: 0x07			Register Name: MBIAS_REG
Bit	R/W	Default	Description
7	R/W	0x0	MBIAS_EN Microphone Bias Enable 0: Disable 1: Enable
6:5	R/W	0x1	MBIAS_VOL_SEL MMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V

			11: 2.50V
4	R/W	0x1	MBIAS chopper enable 0: Disable 1: Enable
3:2	R/W	0x0	MBIAS chopper clock select 00: 250KHz 01: 500KHz 10: 1MHz 11: 2MHz
1:0	R/W	0x0	Reserved

Reg 08h HBIAS Analog Control Register (Default Value:0x10)

Offset: 0x08			Register Name: HBIAS_REG
Bit	R/W	Default	Description
7:6	R/W	0x0	Reserved
5:4	R/W	0x1	HBIAS_VOL_SEL HMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V
3	R/W	0x0	Reserved
2	R/W	0x0	HBIAS_MODE HBIAS&ADC Working Mode 0: Hbias is enabled only when with load 1: Hbias is enabled when HBIASEN write 1
1	R/W	0x0	HBIAS_EN Headset Microphone Bias Enable 0: Disable 1: Enable
0	R/W	0x0	HBIASADC_EN Headset Microphone Bias Current sensor & ADC Enable 0: Disable 1: Enable

7.3.2.3 DAC 模拟控制器寄存器
Reg 09h DAC Analog Control Register 1 (Default Value:0x00)

Offset: 0x09			Register Name: DAC_REG1
Bit	R/W	Default	Description
7	R/W	0x0	DACL_EN DACL Enable 0: Disable 1: Enable
6	R/W	0x0	DACR_EN DACR Enable

			0: Disable 1: Enable
5:4	R/W	0x0	CKDAC_DELAY_SET clock delay time after CKADC 0: min 3: max
3:0	R/W	0x0	Reserved

Reg 0Ah DAC Analog Control Register 2 (Default Value:0x00)

Offset: 0x0A			Register Name: DAC_REG2
Bit	R/W	Default	Description
7	R/W	0x0	DAC_CHOPPER_ENABLE DAC chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	DAC_CHOPPER_NOL_ENABLE DAC chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
5:4	R/W	0x0	DAC_CHOPPER_CKSET DAC chopper clock frequency Fs:3.072MHz/2.048MHz 0=384kHz/256kHz 1=192kHz/128kHz 2=96kHz/64kHz 3=48kHz/32kHz
3:2	R/W	0x0	DAC_CHOPPER_DELAY_SET Control DAC chopper clock delay time after CKDAC 0: min 3: max
1:0	R/W	0x0	DAC_CHOPPER_NOL_DELAY_SET Control DAC chopper clock non-overlapping time 0: min when DAC_CHOPPER_NOL_ENABLE=1 3: max when DAC_CHOPPER_NOL_ENABLE=1

Reg 0Bh DAC Analog Control Register 3 (Default Value:0x00)

Offset: 0x0B			Register Name: DAC_REG3
Bit	R/W	Default	Description
7	R/W	0x0	SPKL_EN Left Differential Speakerout Enable 0: Disable 1: Enable
6	R/W	0x0	SPKR_EN Right Differential Speakerout Enable 0: Disable 1: Enable

5	R/W	0x0	SPK_SELPGA_EN Differential Speaker Input Select PGA Output 0: Disable 1: Enable
4:1	R/W	0x0	Reserved
0	R/W	0x0	SPK_CH_OUT_EDGE Differential Speakerout Chopper Clock Edge Control 0: in phase with ckdac 1: out of phase with ckdac

Reg 0Ch DAC Analog Control Register 4 (Default Value:0x00)

Offset: 0x0C			Register Name: DAC_REG4
Bit	R/W	Default	Description
7	R/W	0x0	SPK_CHOPPER_ENABLE SPK chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	SPK_CHOPPER_NOL_ENABLE SPK chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
5:4	R/W	0x0	SPK_CHOPPER_CKSET SPK chopper clock frequency Fs:3.072MHz/2.048MHz 0=384kHz/256kHz 1=192kHz/128kHz 2=96kHz/64kHz 3=48kHz/32kHz
3:2	R/W	0x0	SPK_CHOPPER_DELAY_SET Control SPK chopper clock delay time after CKDAC 0: min 3: max
1:0	R/W	0x0	SPK_CHOPPER_NOL_DELAY_SET Control SPK chopper clock non-overlapping time 0: min when DAC_CHOPPER_NOL_ENABLE=1 3: max when DAC_CHOPPER_NOL_ENABLE=1

7.3.2.4 PLL 配置寄存器

Reg 10h PLL Configure Control 1 Register (Default Value: 0x48)

Offset: 0x10			Register Name: PLL_CTRL1
Bit	R/W	Default	Description
7	/	/	/
6:4	R/W	0x4	PLL_IBIAS PLL internal bias current tuning 0: min

			... 7: max
3	R/W	0x1	PLL_NDET PLL loop divider factor detection 0: Disable 1: Enable
2	R	0x0	PLL Locked status 0: Not locked or not enabled 1: Enabled and locked
1	R/W	0x0	PLL_COM_EN PLL Common voltage Enable 0: Disable 1: Enable
0	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL output $F_{OUT} = F_{IN} * N / ((M1+1) * (M2+1) * (K1+1) * (K2+1))$;

Reg 11h PLL Configure Control 2 Register (Default Value: 0x00)

Offset: 0x11			Register Name: PLL_CTRL2
Bit	R/W	Default	Description
7:6	/	/	/
5	R/W	0x0	PLL_PREDIV2 PLL pre-divider factor M2 Factor=0, M2=0 Factor=1, M2=1
4:0	R/W	0x0	PLL_PREDIV1 PLL pre-divider factor M1 Factor=0, M1=0 Factor=1, M1=1 ... Factor=31, M1=31

Reg 12h PLL Configure Control 3 Register (Default Value: 0x03)

Offset: 0x12			Register Name: PLL_CTRL3
Bit	R/W	Default	Description
7:2	/	/	/
1:0	R/W	0x3	PLL_LOOPDIV_MSB The 2-High Bit of PLL Loop Divider Factor N. Factor=0, N=0 Factor=1, N=1 ... Factor=1023, N=1023 Factor N is equal to [PLL_LOOPDIV_MSB, PLL_LOOPDIV_LSB]

Reg 13h PLL Configure Control 4 Register (Default Value: 0x0D)

Offset: 0x13			Register Name: PLL_CTRL4
Bit	R/W	Default	Description
7:0	R/W	0x0D	PLL_LOOPDIV_LSB The 8-Low Bit of PLL PLL Loop Divider Factor N. Factor=0, N=0 Factor=1, N=1 ... Factor=1023, N=1023 Factor N is equal to [PLL_LOOPDIV_MSB, PLL_LOOPDIV_LSB]

Reg 14h PLL Configure Control 5 Register (Default Value: 0x00)

Offset: 0x14			Register Name: PLL_CTRL5
Bit	R/W	Default	Description
7:6	/	/	/
5	R/W	0x0	PLL_POSTDIV2 PLL post-divider factor K2 Factor=0, K2=0 Factor=1, K2=1
4:0	R/W	0x0	PLL_POSTDIV1 PLL post-divider factor K1 Factor=0, K1=0 Factor=1, K1=1 ... Factor=31, K1=31

Reg 16h PLL Configure Control 6 Register (Default Value: 0x04)

Offset: 0x16			Register Name: PLL_CTRL6
Bit	R/W	Default	Description
7:6	R/W	0x0	PLL_LDO PLL internal ldo voltage tuning 0: 1.8V 1: 2.0V 2: Reserved 3: Reserved
5	R/W	0x0	Reserved
4:0	R/W	0x4	PLL_CP PLL cp current tuning 0x0: 2uA 0x1: 4uA 0x2: 6uA;{(fref/((M1+1)(M2+1))):0.4MHz~0.8MHz} 0x3: 8uA;{(fref/((M1+1)(M2+1))):0.81MHz~1.59MHz} 0x4: 10uA;{(fref/((M1+1)(M2+1))):1.6MHz~4.096MHz} ... 0xF: 32uA

			...
			0x1E: 62uA
			0x1F: 64uA

Reg 17h PLL Configure Control 7 Register (Default Value: 0xD0)

Offset: 0x17			Register Name: PLL_CTRL7
Bit	R/W	Default	Description
7:6	R/W	0x3	PLL_CAP PLL loop filter capacitance tuning 0x0: min ... 0x3: max
5:4	R/W	0x1	PLL_RES PLL loop filter resistance tuning 0x0: min 0x1: {(fref/((M1+1)(M2+1))):1.6MHz~4.096MHz} 0x2: {(fref/((M1+1)(M2+1))):0.81MHz~1.59MHz} 0x3: max, {(fref/((M1+1)(M2+1))):0.4MHz~0.8MHz}
3:0	/	/	/

Reg 18h PLL Configure Control 8 Register (Default Value: 0x00)

Offset: 0x18			Register Name: PLL_LOCK_CTRL
Bit	R/W	Default	Description
7	/	/	/
6:4	R/W	0x0	HOLD_TIME SYSCLK hold time T T=0, Bypass T=1, 1 LRCK width ... T=7, 7 LRCK width
3:2	R/W	0x0	LOCK_LEVEL1 PLL lock level1 00: 21-29 clock cycles 01: 22-28 clock cycles 1x: 20-30 clock cycles
1	R/W	0x0	LOCK_LEVEL2 PLL lock level2 0: 24-26 clock cycles 1: 23-27 clock cycles
0	R/W	0x0	PLL_LOCK_EN PLL clk lock enable 0: Disable 1: Enable

7.3.2.5 Headphone 模拟控制寄存器

Reg 19h Headphone Analog Control Register 1 (Default Value:0x01)

Offset: 0x19			Register Name: HP_REG1
Bit	R/W	Default	Description
7	R/W	0x0	HPPA_EN Right & Left Headphone PA Enable 0: Disable 1: Enable
6	R/W	0x0	CP_EN Charge Pump Clock Enable 0: Disable 1: Enable
5	R/W	0x0	HPOUT_EN Headphone out enable 0: Disable 1: Enable
4:2	R/W	0x0	Reserved
1:0	R/W	0x1	CP_CLKS Charge pump clock select 00: 250k 01: 333k 10: 666k 11: 1000k

Reg 1Ah Headphone Analog Control Register 2 (Default Value:0x00)

Offset: 0x1A			Register Name: HP_REG2
Bit	R/W	Default	Description
7	R/W	0x0	HP_CHOPPER_ENABLE HP chopper enable 0: Disable 1: Enable
6	R/W	0x0	HP_CHOPPER_NOL_ENABLE HP chopper non-overlapping clock enable 0: Disable 1: Enable
5:4	R/W	0x0	HP_CHOPPER_CKSET Control HP chopper clock frequency Fs: 6.144MHz 0: 384kHz 1: 192kHz 2: 96kHz 3: 48kHz
3:2	R/W	0x0	HP_CHOPPER_DELAY_SET Control HP chopper clock delay time after CKDAC

			0: min 3: max
1:0	R/W	0x0	HP_CHOPPER_NOL_DELAY_SET Control HP chopper clock non-overlapping time 0: min when HP_CHOPPER_NOL_ENABLE=1 3: max when HP_CHOPPER_NOL_ENABLE=1

Reg 1Bh Headphone Analog Control Register 3 (Default Value:0x80)

Offset: 0x1B			Register Name: HP_REG3
Bit	R/W	Default	Description
7:0	R/W	0x80	Reserved

Reg 1Ch Headphone Analog Control Register 4 (Default Value:0x80)

Offset: 0x1C			Register Name: HP_REG4
Bit	R/W	Default	Description
7:0	R/W	0x80	Reserved

Reg 1Dh Headphone Analog Control Register 5 (Default Value:0x10)

Offset: 0x1D			Register Name: HP_REG5
Bit	R/W	Default	Description
7:6	R/W	0x0	Reserved
5:4	R/W	0x1	OPDRV_CUR OPDRV output stage current setting 00: 6uA 01: 7uA 10: 8uA 11: 9uA
3	R/W	0x0	Reserved
2:0	R/W	0x0	HEADPHONE_GAIN 000: 0dB 001: -6dB 010: -12dB 011: -18dB 100: -24dB 101: -30dB 110: -36dB 111: -42dB

Reg 20h System Clock Control Register (Default Value: 0x00)

Offset: 0x20			Register Name: SYSCLK_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	PLLCLK_EN PLLCLK Enable 0: Disable 1: Enable

6:5	/	/	/
4	R/W	0x0	PLLCLK_SRC PLL Clock Source Select 0: MCLK 1: BCLK
3:2	R/W	0x0	SYSClk_SRC System Clock Source Select 0: MCLK 1: BCLK 2: PLL 3: Reserved
1	R/W	0x0	MCLKDIV MCLK Divide Ratio from SYSClk 0: Divide by 1 1: Divide by 2
0	R/W	0x0	SYSClk_EN SYSClk Enable 0: Disable 1: Enable

7.3.2.6 ADC 模拟控制寄存器

Reg 24h ADC1 Analog Control Register 1 (Default Value:0x00)

Offset: 0x24			Register Name: ADC1_REG1
Bit	R/W	Default	Description
7	R/W	0x0	ADC1_EN ADC1 Channel Global Enable 0: ADC(PGA&DSM) Disable 1: ADC(PGA) Enable
6	R/W	0x0	ADC1_DSM_DIS ADC1 DSM Disable Control, enable/disable Only DSM 0: normal operation 1: disable DSM modulator
5:4	R/W	0x0	ADC1_DSM_OTA_CTRL Op number control for ADC1 DSM 0: max 3: min
3	R/W	0x0	ADC_DSM_EN_DITHER 0: Dither Off 1: Dither On
2:0	R/W	0x0	ADC_DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 000: Min Level 111: Max Level

Reg 25h ADC1 Analog Control Register 2 (Default Value:0x0B)

Offset: 0x25			Register Name: ADC1_REG2
Bit	R/W	Default	Description
7	R/W	0x0	ADC1/2/3_PGA_CHOPPER_EDGE ADC1/2/3 PGA Chopper Clock Edge Control 0: in phase with ckadc 1: out of phase with ckadc
6:4	R/W	0x0	ADC1_DSM_OTA_IB_SEL Control bias current for DSM integrator op-amps 0: 6.0uA 4: 4.0uA 1: 6.5uA 5: 4.5uA 2: 7.0uA 6: 5.0uA 3: 7.5uA 7: 5.5uA
3:2	R/W	0x2	ADC1_DSM_OP_BIAS_CTRL Control ADC1 DSM op-amp Bias CMOS Size 0: 4 parallel CMOS unit enabled 1: 5 parallel CMOS unit enabled 2: 6 parallel CMOS unit enabled 3: 7 parallel CMOS unit enabled
1:0	R/W	0x3	ADC1_PGA_OP_BIAS_CTRL Control ADC1 PGA op-amp Bias CMOS Size 0: 1 parallel CMOS unit enabled 1: 3 parallel CMOS unit enabled 2: 5 parallel CMOS unit enabled 3: 7 parallel CMOS unit enabled

Reg 26h ADC1 Analog Control Register 3 (Default Value:0xC0)

Offset: 0x26			Register Name: ADC1_REG3
Bit	R/W	Default	Description
7:5	R/W	0x6	ADC1_PGA_OTA_IB_SEL Control bias current of OTA for PGA 0: 1 uA 4: 5 uA 1: 2 uA 5: 6 uA 2: 3 uA 6: 7 uA 3: 4 uA 7: 8 uA
4:0	R/W	0x0	ADC1_PGA_GAIN_CTRL ADC1 PGA Gain Setting for MIC-IN: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB

			0x8: 13 dB 0x18: 29 dB
			0x9: 14 dB 0x19: 30 dB
			0xA: 15 dB 0x1A: 31 dB
			0xB: 16 dB 0x1B: 32 dB
			0xC: 17 dB 0x1C: 33 dB
			0xD: 18 dB 0x1D: 34 dB
			0xE: 19 dB 0x1E: 35 dB
			0xF: 20 dB 0x1F: 36 dB

Reg 27h ADC1 Analog Control Register 4 (Default Value:0x00)

Offset: 0x27			Register Name: ADC1_REG4
Bit	R/W	Default	Description
7	R/W	0x0	ADC1_PGA_CHOPPER_ENABLE ADC1 PGA chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	ADC1_PGA_CHOPPER_NOL_ENABLE ADC1 PGA chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
5:4	R/W	0x0	ADC1_PGA_CHOPPER_CKSET Control ADC1 PGA chopper clock frequency Fs:3.072MHz/2.048MHz 0=384kHz/256kHz 1=192kHz/128kHz 2=96kHz/64kHz 3=48kHz/32kHz
3:2	R/W	0x0	ADC1_PGA_CHOPPER_DELAY_SET Control ADC1 PGA chopper clock delay time after CKADC 0: min 3: max
1:0	R/W	0x0	ADC1_PGA_CHOPPER_NOL_DELAY_SET Control ADC1 PGA chopper clock non-overlapping time 0: min when ADC1_PGA_CHOPPER_NOL_ENABLE=1 3: max when ADC1_PGA_CHOPPER_NOL_ENABLE=1

Reg 28h ADC2 Analog Control Register 1 (Default Value:0x00)

Offset: 0x28			Register Name: ADC2_REG1
Bit	R/W	Default	Description
7	R/W	0x0	ADC2_EN ADC2 Channel Global Enable 0: ADC(PGA&DSM) Disable 1: ADC(PGA) Enable
6	R/W	0x0	ADC2_DSM_DIS ADC2 DSM Disable Control, enable/disable Only DSM 0: normal operation

			1: disable DSM modulator
5:4	R/W	0x0	ADC2_DSM_OTA_CTRL Op number control for ADC1 DSM 0: max 3: min
3	R/W	0x0	ADC2_DSM_DEMOFF ADC2 DEM Control 0: enable DEM 1: disable DEM
2	R/W	0x0	ADC2_EN_CROSSTALK_AVOIDANCE ADC2 crosstalk avoidance enable 0: Disable 1: Enable
1:0	R/W	0x0	ADC2_MIC_MIX_MUX2 ADC2 INPUT CHOOSE MIC or SPKOUTL 00: MIC2 01: MIC4 10: SPKOUTL 11: illegal operation

Reg 29h ADC2 Analog Control Register 2 (Default Value:0x0B)

Offset: 0x29			Register Name: ADC2_REG2
Bit	R/W	Default	Description
7	R/W	0x0	ADC2_DSM_SEL_OUT_EDGE ADC2 clock edge 0: DSM output is clocked on falling edge of input clock 1: DSM output is clocked on rising edge of input clock
6:4	R/W	0x0	ADC2_DSM_OTA_IB_SEL Control bias current for DSM integrator op-amps 0: 6.0uA 4: 4.0uA 1: 6.5uA 5: 4.5uA 2: 7.0uA 6: 5.0uA 3: 7.5uA 7: 5.5uA
3:2	R/W	0x2	ADC2_DSM_OP_BIAS_CTRL Control ADC2 DSM op-amp Bias CMOS Size 0: 4 parallel CMOS unit enabled 1: 5 parallel CMOS unit enabled 2: 6 parallel CMOS unit enabled 3: 7 parallel CMOS unit enabled
1:0	R/W	0x3	ADC2_PGA_OP_BIAS_CTRL Control ADC2 PGA op-amp Bias CMOS Size 0: 1 parallel CMOS unit enabled 1: 3 parallel CMOS unit enabled 2: 5 parallel CMOS unit enabled 3: 7 parallel CMOS unit enabled

Reg 2Ah ADC2 Analog Control Register 3 (Default Value:0xC0)

Offset: 0x2A			Register Name: ADC2_REG3
Bit	R/W	Default	Description
7:5	R/W	0x6	ADC2_PGA_OTA_IB_SEL Control bias current of OTA for PGA 0: 1 uA 4: 5 uA 1: 2 uA 5: 6 uA 2: 3 uA 6: 7 uA 3: 4 uA 7: 8 uA
4:0	R/W	0x0	ADC2_PGA_GAIN_CTRL ADC2 PGA Gain Setting for MIC-IN: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB

Reg 2Bh ADC2 Analog Control Register 4 (Default Value:0x00)

Offset: 0x2B			Register Name: ADC2_REG4
Bit	R/W	Default	Description
7	R/W	0x0	ADC2_PGA_CHOPPER_ENABLE ADC2 PGA chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	ADC2_PGA_CHOPPER_NOL_ENABLE ADC2 PGA chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
5:4	R/W	0x0	ADC2_PGA_CHOPPER_CKSET Control ADC2 PGA chopper clock frequency Fs:3.072MHz/2.048MHz 0=384kHz/256kHz 1=192kHz/128kHz 2=96kHz/64kHz

			3=48kHz/32kHz
3:2	R/W	0x0	ADC2_PGA_CHOPPER_DELAY_SET Control ADC2 PGA chopper clock delay time after CKADC 0: min 3: max
1:0	R/W	0x0	ADC2_PGA_CHOPPER_NOL_DELAY_SET Control ADC2 PGA chopper clock non-overlapping time 0: min when ADC2_PGA_CHOPPER_NOL_ENABLE=1 3: max when ADC2_PGA_CHOPPER_NOL_ENABLE=1

Reg 2Ch ADC3 Analog Control Register 1 (Default Value:0x00)

Offset: 0x2C			Register Name: ADC3_REG1
Bit	R/W	Default	Description
7	R/W	0x0	ADC3_EN ADC3 Channel Global Enable 0: ADC(PGA&DSM) Disable 1: ADC(PGA) Enable
6	R/W	0x0	ADC3_DSM_DIS ADC3 DSM Disable Control, enable/disable Only DSM 0: normal operation 1: disable DSM modulator
5:4	R/W	0x0	ADC3_DSM_OTA_CTRL Op number control for ADC1 DSM 0: max 3: min
3	R/W	0x0	ADC3_DSM_DEMOFF ADC3 DEM Control 0: enable DEM 1: disable DEM
2	R/W	0x0	ADC1_DSM_DEMOFF ADC1 DEM Control 0: enable DEM 1: disable DEM
1	R/W	0x0	ADC3_MIC_MIX ADC3 INPUT CHOOSE MIC or SPKOUTR 0: MIC 1: SPKOUTR
0	R/W	0x0	ADC1_DSM_SEL_OUT_EDGE ADC1 clock edge 0: DSM output is clocked on falling edge of input clock 1: DSM output is clocked on rising edge of input clock

Reg 2Dh ADC3 Analog Control Register 2 (Default Value:0x0B)

Offset: 0x2D			Register Name: ADC3_REG2
Bit	R/W	Default	Description
7	R/W	0x0	ADC3_DSM_SEL_OUT_EDGE

			ADC3 clock edge 0: DSM output is clocked on falling edge of input clock 1: DSM output is clocked on rising edge of input clock
6:4	R/W	0x0	ADC3_DSM_OTA_IB_SEL Control bias current for DSM integrator op-amps 0: 6.0uA 4: 4.0uA 1: 6.5uA 5: 4.5uA 2: 7.0uA 6: 5.0uA 3: 7.5uA 7: 5.5uA
3:2	R/W	0x2	ADC3_DSM_OP_BIAS_CTRL Control ADC3 DSM op-amp Bias CMOS Size 0: 4 parallel CMOS unit enabled 1: 5 parallel CMOS unit enabled 2: 6 parallel CMOS unit enabled 3: 7 parallel CMOS unit enabled
1:0	R/W	0x3	ADC3_PGA_OP_BIAS_CTRL Control ADC3 PGA op-amp Bias CMOS Size 0: 1 parallel CMOS unit enabled 1: 3 parallel CMOS unit enabled 2: 5 parallel CMOS unit enabled 3: 7 parallel CMOS unit enabled

Reg 2Eh ADC3 Analog Control Register 3 (Default Value:0xC0)

Offset: 0x2E			Register Name: ADC3_REG3
Bit	R/W	Default	Description
7:5	R/W	0x6	ADC3_PGA_OTA_IB_SEL Control bias current of OTA for PGA 0: 1 uA 4: 5 uA 1: 2 uA 5: 6 uA 2: 3 uA 6: 7 uA 3: 4 uA 7: 8 uA
4:0	R/W	0x0	ADC3_PGA_GAIN_CTRL ADC3 PGA Gain Setting for MIC-IN: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB

			0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
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Reg 2Fh ADC3 Analog Control Register 4 (Default Value:0x00)

Offset: 0x2F			Register Name: ADC3_REG4
Bit	R/W	Default	Description
7	R/W	0x0	ADC3_PGA_CHOPPER_ENABLE ADC3 PGA chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	ADC3_PGA_CHOPPER_NOL_ENABLE ADC3 PGA chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
5:4	R/W	0x0	ADC3_PGA_CHOPPER_CKSET Control ADC3 PGA chopper clock frequency Fs:3.072MHz/2.048MHz 0=384kHz/256kHz 1=192kHz/128kHz 2=96kHz/64kHz 3=48kHz/32kHz
3:2	R/W	0x0	ADC3_PGA_CHOPPER_DELAY_SET Control ADC3 PGA chopper clock delay time after CKADC 0: min 3: max
1:0	R/W	0x0	ADC3_PGA_CHOPPER_NOL_DELAY_SET Control ADC3 PGA chopper clock non-overlapping time 0: min when ADC3_PGA_CHOPPER_NOL_ENABLE=1 3: max when ADC3_PGA_CHOPPER_NOL_ENABLE=1

7.3.2.7 I2S 控制寄存器
Reg 30h I2S Control Register (Default Value: 0x00)

Offset: 0x30			Register Name: I2S_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	BCLK_IOEN 0: input (slave) 1: output (master)
6	R/W	0x0	LRCK_IOEN 0: input (slave) 1: output (master)
5	R/W	0x0	MCLK_IOEN 0: Input 1: Output PLL_CLK
4	R/W	0x0	SDO_EN

			0: Disable, SDOUT pin is Hi-Z state 1: Enable
3	R/W	0x0	OUT Mute 0: normal transfer 1: force SDOUT to output 0
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	I2SGEN I2S Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

Reg 31h I2S BCLK Control Register (Default Value: 0x00)

Offset: 0x31			Register Name: I2S_BCLK_CTRL
Bit	R/W	Default	Description
7:6	/	/	/
5	R/W	0x0	EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the same BCLK edge BCLK_POLARITY = 0, use negative edge drive BCLK_POLARITY = 1, use positive edge drive
4	R/W	0x0	BCLK_POLARITY 0: normal mode, negative edge drive and positive edge sample 1: invert mode, positive edge drive and negative edge sample
3:0	R/W	0x0	BCLKDIV BCLK Divide Ratio from SYSCLK 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96

			13: Divide by 128 14: Divide by 176 15: Divide by 192 This bit is only used in master mode
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Reg 32h I2S LRCK Control 1 Register (Default Value: 0x00)

Offset: 0x32			Register Name: I2S_LRCK_CTRL1
Bit	R/W	Default	Description
7:6	/	/	/
5	R/W	0x0	LRCK_WIDTH LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame) (this bit is only used in PCM mode)
4	R/W	0x0	LRCK_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
3:2	/	/	/
1:0	R/W	0x0	LRCK_PERIODH The 2-High bit of LRCK period value. It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width ... n = 1023: 1024 BCLKs width This bit is must be configured in master and slave mode

Reg 33h I2S LRCK Control 2 Register (Default Value: 0x00)

Offset: 0x33			Register Name: I2S_LRCK_CTRL2
Bit	R/W	Default	Description
7:0	R/W	0x00	LRCK_PERIODL The 8-Low bit of LRCK period value. It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example:

			n = 7: 8 BCLK width ... n = 1023: 1024 BCLKs width This bit is must be configured in master and slave mode
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Reg 34h I2S Format Control 1 Register (Default Value: 0x15)

Offset: 0x34			Register Name: I2S_FMT_CTRL1
Bit	R/W	Default	Description
7	R/W	0x0	ENCD_FMT Encoding Mode coding format Selection 0: 0,1,...,N-1 1: 1,2,...,N N is the channel (slot) number
6	R/W	0x0	ENCD_SEL Encoding Mode Selection 0: disable 1: enable
5:4	R/W	0x1	MODE_SEL Mode Selection 0: PCM mode (Offset 0: PCM_B; Offset 1: PCM_A) 1: Left mode (Offset 0: LJ mode; Offset 1: I2S mode) 2: Right-Justified mode 3: Reserved
3	/	/	/
2	R/W	0x1	OFFSET Offset tune, TX and RX data offset to LRCK 0: no offset 1: data is offset by 1 BCLKs to LRCK
1	R/W	0x0	TX_SLOT_HIZ 0: normal mode for the last half cycle of BCLK in the slot 1: turn to hi-z state for the last half cycle of BCLK in the slot
0	R/W	0x1	TX_STATE 0: transfer level 0 when not transferring slot 1: turn to hi-z state (TDM) when not transferring slot

Reg 35h I2S Format Control 2 Register (Default Value: 0x33)

Offset: 0x35			Register Name: I2S_FMT_CTRL2
Bit	R/W	Default	Description
7	/	/	/
6:4	R/W	0x3	SW Slot Width Select 0: Reserved 1: Reserved 2: Reserved 3: 16-bit 4: 20-bit

			5: 24-bit 6: 28-bit 7: 32-bit
3	/	/	/
2:0	R/W	0x3	SR Sample Resolution 0: Reserved 1: Reserved 2: Reserved 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit

Reg 36h I2S Format Control 3 Register (Default Value: 0x30)

Offset: 0x36			Register Name: I2S_FMT_CTRL3
Bit	R/W	Default	Description
7	R/W	0x0	RX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in slot [sample resolution < slot size] 0: Zeros at LSB position 1: Sign extension at MSB position 2: Reserved 3: Transfer 0 after each sample in each slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law (this bit is only used in PCM mode)
1:0	R/W	0x0	TX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law (this bit is only used in PCM mode)

Reg 38h I2S TX Control 1 Register (Default Value: 0x00)

Offset: 0x38			Register Name: I2S_TX_CTRL1
Bit	Read/Write	Default	Description
7:4	/	/	/
3:0	R/W	0x0	TX_CHSEL TX Channel (slot) number Select for each output 0: 1 channel / slot ... 7: 8 channels / slots 8: 9 channels / slots ... 15: 16 channels / slots

Reg 39h I2S TX Control 2 Register (Default Value: 0x00)

Offset: 0x39			Register Name: I2S_TX_CTRL2
Bit	Read/Write	Default	Description
7:0	R/W	0x0	TX_CHEN_LOW TX Channel1 ~Channel8 (slot) enable, bit[7:0] refer to slot [8:1]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable

Reg 3Ah I2S TX Control 3 Register (Default Value: 0x00)

Offset: 0x3A			Register Name: I2S_TX_CTRL3
Bit	Read/Write	Default	Description
7:0	R/W	0x0	TX_CHEN_HIGH TX Channel9 ~Channel16(slot) enable, bit[7:0] refer to slot [16:9]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable

Reg 3Bh I2S TX Mixer Control Register (Default Value: 0x00)

Offset: 0x3B			Register Name: I2S_TX_MIX_CTRL
Bit	R/W	Default	Description
7:6	/	/	/
5:4	R/W	0x0	TX_MIX3 Output data is TXM3 00: RECD_DAT3 01: RXM1 10: RXM1 + RECD_DAT3 11: (RXM1 + RECD_DAT3) / 2
3:2	R/W	0x0	TX_MIX2 Output data is TXM2 00: RECD_DAT2 01: PLAY_DAT2

			10: PLAY_DAT2 + RECD_DAT2 11: (PLAY_DAT2 + RECD_DAT2) / 2
1:0	R/W	0x0	TX_MIX1 Output data is TXM1 00: RECD_DAT1 01: PLAY_DAT1 10: PLAY_DAT1 + RECD_DAT1 11: (PLAY_DAT1 + RECD_DAT1) / 2

Reg 3Ch I2S TX Channel Mapping Control 1 Register (Default Value: 0x00)

Offset: 0x3C			Register Name: I2S_TX_CHMP_CTRL1
Bit	Read/Write	Default	Description
7:6	R/W	0x0	TX_CH4_MAP TX Channel4 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
5:4	R/W	0x0	TX_CH3_MAP TX Channel3 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
3:2	R/W	0x0	TX_CH2_MAP TX Channel2 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
1:0	R/W	0x0	TX_CH1_MAP TX Channel1 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved

Reg 3Dh I2S TX Channel Mapping Control 2 Register (Default Value: 0x00)

Offset: 0x3D			Register Name: I2S_TX_CHMP_CTRL2
Bit	Read/Write	Default	Description
7:6	R/W	0x0	TX_CH8_MAP TX Channel8 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved

5:4	R/W	0x0	TX_CH7_MAP TX Channel7 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
3:2	R/W	0x0	TX_CH6_MAP TX Channel6 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
1:0	R/W	0x0	TX_CH5_MAP TX Channel5 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved

Reg 3Eh I2S TX Channel Mapping Control 3 Register (Default Value: 0x00)

Offset: 0x3E			Register Name: I2S_TX_CHMP_CTRL3
Bit	Read/Write	Default	Description
7:6	R/W	0x0	TX_CH12_MAP TX Channel12 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
5:4	R/W	0x0	TX_CH11_MAP TX Channel11 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
3:2	R/W	0x0	TX_CH10_MAP TX Channel10 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
1:0	R/W	0x0	TX_CH9_MAP TX Channel9 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved

Reg 3Fh I2S TX Channel Mapping Control 4 Register (Default Value: 0x00)

Offset: 0x3F			Register Name: I2S_TX_CHMP_CTRL4
Bit	Read/Write	Default	Description
7:6	R/W	0x0	TX_CH16_MAP TX Channel16 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
5:4	R/W	0x0	TX_CH15_MAP TX Channel15 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
3:2	R/W	0x0	TX_CH14_MAP TX Channel14 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved
1:0	R/W	0x0	TX_CH13_MAP TX Channel13 Mapping 0: TXM1 1: TXM2 2: TXM3 3: Reserved

Reg 40h I2S RX Control 1 Register (Default Value: 0x00)

Offset: 0x40			Register Name: I2S_RX_CTRL1
Bit	Read/Write	Default	Description
7:4	/	/	/
3:0	R/W	0x0	RX_CHSEL RX Channel (slot) number Select for each input 0: 1 channel / slot ... 7: 8 channels / slots 8: 9 channels / slots ... 15: 16 channels / slots

Reg 41h I2S RX Control 2 Register (Default Value: 0x03)

Offset: 0x41			Register Name: I2S_RX_CTRL2
Bit	Read/Write	Default	Description
7:0	R/W	0x3	RX_CHEN_LOW

			RX Channel1 ~Channel8 (slot) enable, bit[7:0] refer to slot [8:1]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: Disable 1: Enable
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Reg 42h I2S RX Control 3 Register (Default Value: 0x00)

Offset: 0x42			Register Name: I2S_RX_CTRL3
Bit	Read/Write	Default	Description
7:0	R/W	0x0	RX_CHEN_HIGH RX Channel9 ~Channel16(slot) enable, bit[7:0] refer to slot [16:9]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: Disable 1: Enable

Reg 43h I2S RX Mixer Control Register (Default Value: 0x00)

Offset: 0x43			Register Name: I2S_RX_MIX_CTRL
Bit	R/W	Default	Description
7:6	/	/	/
5:4	R/W	0x0	RX_MIX3 Output data is RXM3 00: RXR 01: RECD_DAT2 10: RXR+RECD_DAT2 11: (RXR+RECD_DAT2) / 2
3:2	R/W	0x0	RX_MIX2 Output data is RXM2 00: RXM1 01: RECD_DAT1 10: RXM1+RECD_DAT1 11: (RXM1+RECD_DAT1) / 2
1:0	R/W	0x0	RX_MIX1 Output data is RXM1 00: RXL 01: RXR 10: RXL+RXR 11: (RXL+RXR) / 2

Reg 44h I2S RX Channel Mapping Control Register (Default Value: 0x10)

Offset: 0x44			Register Name: I2S_RX_CHMP_CTRL
Bit	Read/Write	Default	Description
7:4	R/W	0x1	RXR_MAP RXR Channel Mapping 0: 1 st channel / slot ... 7: 8 th channels / slots 8: 9 th channels / slots

			... 15: 16 th channels / slots
3:0	R/W	0x0	RXL_MAP RXL Channel Mapping 0: 1 st channel / slot ... 7: 8 th channels / slots 8: 9 th channels / slots ... 15: 16 th channels / slots

7.3.2.8 DEBUG 控制寄存器

Reg 50h Debug Control Register (Default Value: 0x00)

Offset: 0x50			Register Name: DEBUG_CTRL
Bit	Read/Write	Default	Description
7:4	/	/	/
3:0	R/W	0x0	ADDA_DEBUG_MODE ADC/DAC Debug Mode Select 0x0: Func mode 0x1: Reserved 0x2: ADC1 analog debug 0x3: ADC2 analog debug 0x4: ADC3 analog debug 0x5: ADC1 digital debug 0x6: ADC2 digital debug 0x7: ADC3 digital debug 0x8: DAC1 analog debug 0x9: DAC2 analog debug 0xA: DAC1 debug 0xB: DAC2 debug 0xC: ADC1 debug 0xD: ADC2 debug 0xE: ADC3 debug 0xF: Reserved

Reg 51h I2S Pad Drive Control Register (Default Value: 0x55)

Offset: 0x51			Register Name: I2S_PADDRV_CTRL
Bit	Read/Write	Default	Description
7:6	R/W	0x1	PAD Programmable Drive Control for MCLK 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PAD Programmable Drive Control for BCLK 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3:2	R/W	0x1	PAD Programmable Drive Control for LRCK 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PAD Programmable Drive Control for SDOUT/SDIN 00: Level 0 01: Level 1 10: Level 2 11: Level 3

Reg 52h Debug Pad Drive Control Register (Default Value: 0x55)

Offset: 0x52			Register Name: DEBUG_PADDRV_CTRL
Bit	Read/Write	Default	Description
7:6	R/W	0x1	PAD Programmable Drive Control for IRQ 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PAD Programmable Drive Control for DEVID 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PAD Programmable Drive Control for HP_DET 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PAD Programmable Drive Control for DMIC CLK 00: Level 0 01: Level 1 10: Level 2 11: Level 3

Reg 53h Digital Bypass Control Register (Default Value: 0x00)

Offset: 0x53			Register Name: DIG_BYPASS_CTRL
Bit	Read/Write	Default	Description
7:3	R/W	0x0	Reserved
2	R/W	0x0	Dither_EN 0: Disable 1: Enable
1	R/W	0x0	HP_AUTO_CLEAR HP_PULLOUT_PENDING auto clear when plug in, HP_PLUGIN_PENDING auto clear when pull out 0: auto clear 1: don't clear
0	R/W	0x0	ADC HPF improvement bypass 0: Disable 1: Enable

Reg 54h Efuse Read Control Register (Default Value: 0x00)

Offset: 0x54			Register Name: EFUSE_RD_CTRL
Bit	Read/Write	Default	Description
7:4	R	0x0	Efuse read value
3:1	/	/	/
0	R/W	0x0	Efuse read enable 0: Disable

			1: Enable
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Reg 55h BIST Enable Register (Default Value: 0x00)

Offset: 0x55			Register Name: BIST_EN_REG
Bit	Read/Write	Default	Description
7:2	/	/	/
1			
0	R/W	0x0	BIST_EN SRAM BIST Enable 0: SRAM BIST disable 1: SRAM BIST enable

Reg 56h BIST Status Register (Default Value: 0x02)

Offset: 0x56			Register Name: BIST_STA_REG
Bit	Read/Write	Default	Description
7	R	0x0	BIST_ERR_STA. BIST Error Status. 0: No effect 1: Error
6:4	R	0x0	BIST_ERR_PAT. BIST Error Pattern.
3:2	R	0x0	BIST_ERR_CYC. BIST Error Cycle.
1	R	0x1	BIST_STOP. BIST Stop. 0: Running 1: Stop
0	R	0x0	BIST_BUSY. BIST Busy. 0: Idle 1: Busy

Reg 57h BIST Control Register 1 (Default Value: 0x00)

Offset: 0x57			Register Name: BIST_CTL_REG1
Bit	Read/Write	Default	Description
7:5	R/W	0x0	BIST_REG_SEL. BIST Register Select.
4	R/W	0x0	BIST_ADDR_MODE_SEL. BIST Address Mode Select. 0: Memory address change as 0123 1: Memory address change as 0132
3:1	R/W	0x0	BIST_WDATA_PAT. BIST Write Data Pattern. 000: 0x00000000 001: 0x55555555

			010: 0x33333333 011: 0x0F0F0F0F 100: 0x00FF00FF 101: 0x0000FFFF Others: /
0	R/W	0x0	BIST_EN. BIST Enable. A positive edge will trigger the BIST to start.

Reg 58h BIST Control Register 2 (Default Value: 0x00)

Offset: 0x58			Register Name: BIST_CTL_REG2
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_START_ADDR_L. BIST Start Address Low bit(addr[7:0])

Reg 59h BIST Control Register 3 (Default Value: 0x00)

Offset: 0x59			Register Name: BIST_CTL_REG3
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_START_ADDR_H. BIST Start Address High bit(addr[15:8])

Reg 5Ah BIST Control Register 4 (Default Value: 0x00)

Offset: 0x5A			Register Name: BIST_CTL_REG4
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_END_ADDR_L. BIST End Address High bit(addr[7:0])

Reg 5Bh BIST Control Register 5 (Default Value: 0x00)

Offset: 0x5B			Register Name: BIST_CTL_REG5
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_END_ADDR_H. BIST End Address High bit(addr[15:8])

Reg 5Ch BIST Control Register 6 (Default Value: 0x00)

Offset: 0x5C			Register Name: BIST_CTL_REG6
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_DATA_MASK1. BIST Data Mask for data[7:0],for any bit: 0: Unmask 1: Mask Mask 表示屏蔽相关的位不进行测试

Reg 5Dh BIST Control Register 7 (Default Value: 0x00)

Offset: 0x5D			Register Name: BIST_CTL_REG7
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_DATA_MASK2.

			BIST Data Mask for data[15:8],for any bit: 0: Unmask 1: Mask Mask 表示屏蔽相关的位不进行测试
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Reg 5Eh BIST Control Register 8 (Default Value: 0x00)

Offset: 0x5E			Register Name: BIST_CTL_REG8
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_DATA_MASK3. BIST Data Mask for data[23:16],for any bit: 0: Unmask 1: Mask Mask 表示屏蔽相关的位不进行测试

Reg 5Fh BIST Control Register 9 (Default Value: 0x00)

Offset: 0x5F			Register Name: BIST_CTL_REG9
Bit	Read/Write	Default	Description
7:0	R/W	0x0	BIST_DATA_MASK4. BIST Data Mask for data[31:24],for any bit: 0: Unmask 1: Mask Mask 表示屏蔽相关的位不进行测试

Reg 60h ADDA Sample Rate Control Register (Default Value: 0x08)

Offset: 0x60			Register Name: ADDA_FS_CTRL
Bit	Read/Write	Default	Description
7:4	/	/	/
3:0	R/W	0x8	ADDA_FS_DIV ADC/DAC Clock Divide, 128*fs, SYSCLK=24.576MHz 0:div1 (192KHz) 1:div2 (96KHz) 2:div3 (64KHz) 3:div4 (48KHz) 4:div6 (32KHz) 5:div8 (24KHz) 6:div12 (16KHz) 7:div16 (12KHz) 8:div24 (8KHz) Other: Reserved $ADC\ Clock = SYSCLK / (ADDA_FS_DIV + 1) / (2^{ADC_OSR})$ ADC_OSR: Reg63h bit[6:5] $DAC\ Clock = SYSCLK / (ADDA_FS_DIV + 1) / (2^{DAC_OSR})$ DAC_OSR: Reg82h bit[1:0]

7.3.2.9 ADC 通路寄存器

Reg 61h ADC Digital Part Enable Register (Default Value: 0x80)

Offset: 0x61			Register Name: ADC_DIG_EN
Bit	Read/Write	Default	Description
7:4	R/W	0x8	REQ_WIDTH 0:min ... 15:max
3	R/W	0x0	ADC_EN Digital part globe enable 0: Disable 1: Enable
2	R/W	0x0	ENAD3 ADC3 digital part enable 0: Disable 1: Enable
1	R/W	0x0	ENAD2 ADC2 digital part enable 0: Disable 1: Enable
0	R/W	0x0	ENAD1 ADC1 digital part enable 0: Disable 1: Enable

Reg 62h Digital MIC Enable Register (Default Value: 0x00)

Offset: 0x62			Register Name: DMIC_EN
Bit	Read/Write	Default	Description
7:6	/	/	/
5	R/W	0x0	MIC_O_SWP_2 MIC3 output data swap with MIC4(amic4=0) output data enable 0: Disable 1: Enable
4	R/W	0x0	MIC_O_SWP_1 MIC1 output data swap with MIC2 output data enable 0: Disable 1: Enable
3	R/W	0x0	DMIC_VOL_FIX DMIC volume up to 6dB 0: Disable 1: Enable
2	R/W	0x0	ADC2_SRC_SEL ADC Channel 2 Digital Decimation Filter Source Selection 0: AMIC

			1: DMIC
1	R/W	0x0	ADC1_SRC_SEL ADC Channel 1 Digital Decimation Filter Source Selection 0: AMIC 1: DMIC
0	R/W	0x0	DMIC_EN DMIC enable 0: Disable 1: Enable

Reg 63h ADC Digital Delay Time Control Register (Default Value: 0x80)

Offset: 0x63			Register Name: ADC_DDT_CTRL
Bit	Read/Write	Default	Description
7	R/W	0x1	ADC_DVC_ZCD_EN ADC DVC Zero Cross Detect Enable 0: Disable 1: Enable
6:5	R/W	0x0	ADC_OSR 00:128 01:64 10:32 11:reserved
4:3	R/W	0x0	ADC_DLY_MODE ADC Delay Mode For Transmitting Data after ENAD 00: no delay 01: no data is sent during the delay 10: write 0 to each channel during the delay period 11: reserved
2:0	R/W	0x0	ADC_DTS ADC Delay Time For Transmitting Data after ENAD (Fs=48KHz) 000:1.7ms 001:3.3ms 010:5ms 011:6.7ms 100:8.3ms 101:10ms 110:20ms

			111:30ms (Fs=16KHz) 000:5ms 001:10ms 010:15ms 011:20ms 100:25ms 101:30ms 110:60ms 111:90ms
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Reg 66h Digital HPF Enable Register (Default Value: 0x07)

Offset: 0x66			Register Name: HPF_EN
Bit	Read/Write	Default	Description
7:3	/	/	/
2	R/W	0x1	DIG_ADC3_HPF_EN Digital ADC3 channel HPF enable 0: Disable 1: Enable
1	R/W	0x1	DIG_ADC2_HPF_EN Digital ADC2 channel HPF enable 0: Disable 1: Enable
0	R/W	0x1	DIG_ADC1_HPF_EN Digital ADC1 channel HPF enable 0: Disable 1: Enable

Reg 67h High Pass Filter 1 Coef [13:8] Register (Default Value: 0x20)

Offset: 0x67			Register Name: HPF1_COEF_REGH
Bit	Read/Write	Default	Description
7:6	/	/	/
5:0	R/W	0x20	HPF1_COEF_HIGH[13:8] $\alpha=-0.999345715621208$, Fpass=5Hz

Reg 68h High Pass Filter 1 Coef [7:0] Register (Default Value: 0x05)

Offset: 0x68			Register Name: HPF1_COEF_REGL
Bit	Read/Write	Default	Description
7:0	R/W	0x05	HPF1_COEF_LOW[7:0] $\alpha=-0.999345715621208$, Fpass=5Hz

Reg 69h High Pass Filter 2 Coef [13:8] Register (Default Value: 0x20)

Offset: 0x69			Register Name: HPF2_COEF_REGH
Bit	Read/Write	Default	Description
7:6	/	/	/
5:0	R/W	0x20	HPF2_COEF_HIGH[13:8] $\alpha=-0.999345715621208$, Fpass=5Hz

Reg 6Ah High Pass Filter 2 Coef [7:0] Register (Default Value: 0x05)

Offset: 0x6A			Register Name: HPF2_COEF_REGL
Bit	Read/Write	Default	Description
7:0	R/W	0x05	HPF2_COEF_LOW[7:0] $\alpha=-0.999345715621208$, Fpass=5Hz

Reg 6Bh High Pass Filter 3 Coef [13:8] Register (Default Value: 0x20)

Offset: 0x6B			Register Name: HPF3_COEF_REGH
Bit	Read/Write	Default	Description
7:6	/	/	/
5:0	R/W	0x20	HPF3_COEF_HIGH[13:8] $\alpha=-0.999345715621208$, Fpass=5Hz

Reg 6Ch High Pass Filter 3 Coef [7:0] Register (Default Value: 0x05)

Offset: 0x6C			Register Name: HPF3_COEF_REGL
Bit	Read/Write	Default	Description
7:0	R/W	0x05	HPF3_COEF_LOW[7:0] $\alpha=-0.999345715621208$, Fpass=5Hz

Reg 6Dh ADC1 Digital Multiplexer Control Register (Default Value: 0x01)

Offset: 0x6D			Register Name: ADC1_MUX_CTRL
Bit	Read/Write	Default	Description
7:3	/	/	/
2:0	R/W	0x01	DIG_ADC1_MUX ADC1 Digital Multiplexer Source Select 0x00: Debug data 0x01: ADC1 data 0x02: DAC1 data 0x03: DAC2 data 0x04: RXM1 Others: reserved

Reg 6Eh ADC2 Digital Multiplexer Control Register (Default Value: 0x01)

Offset: 0x6E			Register Name: ADC2_MUX_CTRL
Bit	Read/Write	Default	Description
7:3	/	/	/
2:0	R/W	0x01	DIG_ADC2_MUX ADC2 Digital Multiplexer Source Select

			0x00: Debug data 0x01: ADC2 data 0x02: DAC1 data 0x03: DAC2 data 0x04: RXM1 Others: reserved
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Reg 6Fh ADC3 Digital Multiplexer Control Register (Default Value: 0x01)

Offset: 0x6F			Register Name: ADC3_MUX_CTRL
Bit	Read/Write	Default	Description
7:3	/	/	/
2:0	R/W	0x01	DIG_ADC3_MUX ADC3 Digital Multiplexer Source Select 0x00: Debug data 0x01: ADC3 data 0x02: DAC1 data 0x03: DAC2 data 0x04: RXM1 Others: reserved

Reg 70h ADC1 Digital Channel Volume Control Register (Default Value: 0x81)

Offset: 0x70			Register Name: ADC1_DVOL_CTRL
Bit	Read/Write	Default	Description
7:0	R/W	0x81	DIG_ADC1_VOL ADC1 Digital channel volume Control (-64dB To 63dB, 0.5dB/Step) 0x00: Mute 0x01: -64dB 0x80 = -0.5dB 0x81 = 0dB 0x82 = 0.5dB 0xFF = 63dB

Reg 71h ADC2 Digital Channel Volume Control Register (Default Value: 0x81)

Offset: 0x71			Register Name: ADC2_DVOL_CTRL
Bit	Read/Write	Default	Description
7:0	R/W	0x81	DIG_ADC2_VOL ADC2 Digital channel volume Control (-64dB To 63dB, 0.5dB/Step) 0x00: Mute 0x01: -64dB 0x80 = -0.5dB 0x81 = 0dB

			0x82 = 0.5dB 0xFF = 63dB
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Reg 72h ADC3 Digital Channel Volume Control Register (Default Value: 0x81)

Offset: 0x72			Register Name: ADC3_DVOL_CTRL
Bit	Read/Write	Default	Description
7:0	R/W	0x81	DIG_ADC3_VOL ADC3 Digital channel volume Control (-64dB To 63dB, 0.5dB/Step) 0x00: Mute 0x01: -64dB 0x80 = -0.5dB 0x81 = 0dB 0x82 = 0.5dB 0xFF = 63dB

Reg 73h HMIC Detect Control Register (Default Value: 0x00)

Offset: 0x73			Register Name: HMIC_DET_CTRL
Bit	R/W	Default	Description
7:6	/	/	/
5	R/W	0x0	KEYUP_CLEAR Key Up Irq Pending bit auto clear when Key Down Irq 0: don't clear 1: auto clear
4	R/W	0x0	HMIC_DATA_IRQ_MODE Hmic Data Irq Mode Select 0: Hmic data irq once after key down 1: Hmic data irq from key down, util key up
3:2	R/W	0x0	HMIC_SF Hmic Smooth Filter setting 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8
1:0	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11: Down by 8, 16Hz

Reg 74h HMIC Detect Debounce Register (Default Value: 0x00)

Offset: 0x74			Register Name: HMIC_DET_DBC
Bit	R/W	Default	Description

7:4	R/W	0x0	HMIC_M Debounce when key down or key up
3:0	R/W	0x0	HMIC_N Debounce when earphone plug in or pull out

Reg 75h HMIC Detect Threshold 1 Control Register (Default Value: 0x00)

Offset: 0x75			Register Name: HMIC_DET_TH1
Bit	R/W	Default	Description
7	/	/	/
6:5	R/W	0x0	HMIC_TH1_HYSTERESIS Hmic Hysteresis Threshold1 00: no Hysteresis 01: Pull Out when Data <= (Hmic_th1-1) 10: Pull Out when Data <= (Hmic_th1-2) 11: Pull Out when Data <= (Hmic_th1-3)
4:0	R/W	0x0	HMIC_TH1 Hmic_th1[4:0], detecting eraphone plug in or pull out.

Reg 76h HMIC Detect Threshold 2 Control Register (Default Value: 0x00)

Offset: 0x76			Register Name: HMIC_DET_TH2
Bit	R/W	Default	Description
7:6	/	/	/
5	R/W	0x0	HMIC_TH2_HYSTERESIS Hmic Hysteresis Threshold2 0: no Hysteresis 1: Key Up when Data <= (Hmic_th2-1)
4:0	R/W	0x0	HMIC_TH2 Hmic_th2[4:0] for detecting Key down or Key up.

Reg 77h HMIC Detect ADC Data Register (Default Value: 0x00)

Offset: 0x77			Register Name: HMIC_DET_DATA
Bit	R/W	Default	Description
7:5	/	/	/
4:0	R	0x0	HMIC_DATA HMIC Average Data

Reg 78h Headphone Detect Control Register (Default Value: 0x10)

Offset: 0x78			Register Name: HP_DET_CTRL
Bit	R/W	Default	Description
7:5	/	/	/
4	R	0x1	HP_DET Headphone detect value from HP_DET pin
3	R/W	0x0	HMIC_DET_AUTO_DIS HBIASEN & HBIASADCEN is automatically disable after pull out 0: Disable

			1: Enable
2	R/W	0x0	HMIC_DET_AUTO_EN HBIASEN & HBIASADCEN is automatically enable after plug in 0: Disable 1: Enable
1	R/W	0x0	DET_POLY Detect polarity 0: Low is plug in 1: High is plug in
0	R/W	0x0	HP_DET_EN Headphone detect enable 0: Disable 1: Enable

Reg 79h Headphone Detect Debounce Register (Default Value: 0x33)

Offset: 0x79			Register Name: HP_DET_DBC
Bit	R/W	Default	Description
7	/	/	/
6:4	R/W	0x3	PULL_OUT_DBC Debounce gear of pull out 0x0: 0.1ms 0x1: 0.2ms 0x2: 0.5ms 0x3: 1ms 0x4: 2ms 0x5: 5ms 0x6: 10ms 0x7: Reserved
3	/	/	/
2:0	R/W	0x3	PLUG_IN_DBC Debounce gear of plug in 0x0: 0.1ms 0x1: 0.2ms 0x2: 0.5ms 0x3: 1ms 0x4: 2ms 0x5: 5ms 0x6: 10ms 0x7: Reserved

Reg 7Ah Headphone Detect Interrupt Enable Register (Default Value: 0x00)

Offset: 0x7A			Register Name: HP_DET_IRQ
Bit	R/W	Default	Description
7	/	/	/
6	R/W	0x0	HP_PULLOUT_IRQ

			Headphone out Irq Enable 0: Disable 1: Enable
5	R/W	0x0	HP_PLUGIN_IRQ Headphone Plug in Irq Enable 0: Disable 1: Enable
4	R/W	0x0	HMIC_PULLOUT_IRQ Hmic Earphone Pull out Irq Enable 0: Disable 1: Enable
3	R/W	0x0	HMIC_PLUGIN_IRQ Hmic Earphone Plug in Irq Enable 0: Disable 1: Enable
2	R/W	0x0	HMIC_KEYUP_IRQ Hmic Key Up Irq Enable 0: Disable 1: Enable
1	R/W	0x0	HMIC_KEYDOWN_IRQ Hmic Key Down Irq Enable 0: Disable 1: Enable
0	R/W	0x0	HMIC_DATA_IRQ_EN Hmic Data Irq Enable 0: Disable 1: Enable

Reg 7Bh Headphone Detect Status Register (Default Value: 0x00)

Offset: 0x7B			Register Name: HP_DET_STA
Bit	R/W	Default	Description
7	/	/	/
6	R/W1C	0x0	HP_PULLOUT_PENDING Headphone Pull out Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Pull out Irq Pending Interrupt
5	R/W1C	0x0	HP_PLUGIN_PENDING Headphone Plug in Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Plug in Irq Pending Interrupt
4	R/W1C	0x0	HMIC_PULLOUT_PENDING Hmic Earphone Pull out Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Pull out Irq Pending Interrupt
3	R/W1C	0x0	HMIC_PLUGIN_PENDING Hmic Earphone Plug in Irq pending bit, write 1 to clear

			0: No Pending Interrupt 1: Plug in Irq Pending Interrupt
2	R/W1C	0x0	HMIC_KEYUP_PENDING Hmic Key Up Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key up Irq Pending Interrupt
1	R/W1C	0x0	HMIC_KEYDOWN_PENDING Hmic Key Down Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key down Irq Pending Interrupt
0	R/W1C	0x0	HMIC_DATA_PENDING Hmic Data Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Data Irq Pending Interrupt

Reg 7Fh ADC Digital Debug Control Register (Default Value: 0x00)

Offset: 0x7F			Register Name: ADC_DIG_DEBUG
Bit	Read/Write	Default	Description
7:6	/	/	/
5:4	R/W	0x0	DSM_DITHER_CTRL Control of the input pin: dsm_dither_sign and dsm_dither_data 00: single-stage shaped pseudorandom dither signal 01: original pseudorandom dither signal 10: offset voltage of the positive direction 11: offset voltage of the negative direction
3	R/W	0x0	I2S_LPB_DEBUG RX-> TXdata loopback 0: Disable 1: Enable
2:0	R/W	0x0	ADC_PTN_SEL ADC Pattern Select 000: Normal 001: 0x5A5A5A(24-bit) 010: 0x123456 (24-bit) 011: Zero data 1xx: I2S_RX data When this bit selected, the digital path data source will be changed to internal rom data

7.3.2.10 DAC 通路寄存器
Reg 81h DAC Digital Part Enable Register (Default Value: 0x00)

Offset: 0x81			Register Name: DAC_DIG_EN
Bit	Read/Write	Default	Description
7:3	/	/	/
2	R/W	0x0	DAC_EN

			Digital part globe enable 0: Disable 1: Enable
1	R/W	0x0	ENDAL DAC Left Channel digital part enable 0: Disable 1: Enable
0	R/W	0x0	ENDAR DAC Right Channel digital part enable 0: Disable 1: Enable

Reg 82h DAC Digital Control Register (Default Value: 0xC0)

Offset: 0x82			Register Name: DAC_DIG_CTRL
Bit	R/W	Default	Description
7	R/W	0x1	DVCZCDEN DVC Zero Cross Detect Enable 0: Disable 1: Enable
6:4	R/W	0x4	Dither_SGM Dither sigma 000: Reserved 001: 1/2 010: 1/2 ² 011: 1/2 ³ 100: 1/2 ⁴ 101: 1/2 ⁵ 110: 1/2 ⁶ 111: Reserved
3	/	/	/
2	R/W	0x0	DAC_SWP DACL filter output data swap with DACR filter output data enable 0: Disable 1: Enable
1:0	R/W	0x0	DAC_OSR 00:128 01:64 10:32 11:reserved

Reg 83h DAC DHP Gain Control Register (Default Value: 0x30)

Offset: 0x83			Register Name: DAC_DHP_GAIN_CTRL
Bit	R/W	Default	Description
7	/	/	/
6:4	R/W	0x3	DAC Playback Mute detection in time: @1/fs 000: 16

			001: 32 010: 64 011: 128 100: 256 101: 512 110: 1024 111: 2048
3	/	/	/
2:0	R/W	0x0	DHP_Output Gain DHP Output Gain Control, Total 8level, from 0dB to -42dB, 6dB/step。 000: 0dB 001: -6dB 010: -12dB 011: -18dB 100: -24dB 101: -30dB 110: -36dB 111: -42dB

Reg 84h DAC LOUT Control Register (Default Value: 0x05)

Offset: 0x84			Register Name: DAC_LOUT_CTRL
Bit	R/W	Default	Description
7:6	/	/	/
5:4	R/W	0x0	ATT_STEP auto attenuate time step setting 00: 128 samples 01: 32 samples 10: 16 samples 11: 1 samples
3	/	/	/
2	R/W	0x1	LOUT_AUTO_ATT Lineout auto attenuate enable 0: Disable 1: Enable
1	R/W	0x0	LOUT_AUTO_MUTE Lineout auto mute enable Only if LOUT_AUTO_ATT set 1, Lineout auto mute enable can take effect 0: Disable 1: Enable
0	R/W	0x1	DHP_GAIN_ZC_DEN DHP Gain Zero Cross Detect Enable 0: Disable 1: Enable

Reg 85h DAC Left Channel Digital Volume Register (Default Value: 0x81)

Offset: 0x85	Register Name: DAC_DVC_L
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Bit	R/W	Default	Description
7:0	R/W	0x81	DAC_DVC_L DAC Left Channel Digital Volume (-64dB To 63dB, 0.5dB/Step) 0x00: Mute 0x01: -64dB 0x80 = -0.5dB 0x81 = 0dB 0x82 = 0.5dB 0xFF = 63dB

Reg 86h DAC Right Channel Digital Volume Register (Default Value: 0x81)

Offset: 0x86			Register Name: DAC_DVC_R
Bit	R/W	Default	Description
7:0	R/W	0x81	DAC_DVC_R DAC Right Channel Digital Volume (-64dB To 63dB, 0.5dB/Step) 0x00: Mute 0x01: -64dB 0x80 = -0.5dB 0x81 = 0dB 0x82 = 0.5dB 0xFF = 63dB

Reg 87h EQ Control Register (Default Value: 0x00)

Offset: 0x87			Register Name: EQ_CTRL
Bit	R/W	Default	Description
7:4	R/W	0x0	EQ Left Channel Enable Control 0: Disable(and bypass) 1: Enable BIT3: Band 16~20 BIT2: Band 11~15 BIT1: Band 6~10 BIT0: Band 1~5
3:0	R/W	0x0	EQ Right Channel Enable Control 0: Disable(and bypass) 1: Enable BIT3: Band 16~20 BIT2: Band 11~15 BIT1: Band 6~10 BIT0: Band 1~5

Reg 88h EQ Band-n Coefficient Control Register (Default Value: 0x00)

Offset: 0x88			Register Name: EQ_COEF_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	EQ Coefficient Register Configuration Channel Selection 0: EQ Left Channel 1: EQ Right Channel
6:5	/	/	/
4:0	R/W	0x0	Band Coefficient(B0, B1, B2, A1, A2) Register(0x90~0x9E) Control 0: Band 1 configuration 1: Band 2 configuration 2: Band 3 configuration ... n-1: Band n configuration(n=1~20) Other: Reserve

Reg 89h DAC Digital Multiplexer Control Register (Default Value: 0x00)

Offset: 0x89			Register Name: DAC_MUX_CTRL
Bit	Read/Write	Default	Description
7:6	/	/	/
5:4	R/W	0x0	DIG_DAC2_MUX DAC2 Digital Multiplexer Source Select 0x0: Normal data(Audio sample from DRC) 0x1: -6 dB sin wave 0x2: -60 dB sin wave 0x3: Zero data
3:2	/	/	/
1:0	R/W	0x0	DIG_DAC1_MUX DAC1 Digital Multiplexer Source Select 0x00: Normal data(Audio sample from DRC) 0x1: -6 dB sin wave 0x2: -60 dB sin wave 0x3: Zero data

Reg 8Ah Headphone Adaptive Voltage Regulation Control Register (Default Value: 0x51)

Offset: 0x8A			Register Name: HP_AVR_CTRL
Bit	Read/Write	Default	Description
7	R/W	0x0	HP_AVR_DEN Headphone Adaptive Voltage Regulation Detect Enable 0: Disable 1: Enable
6:4	R/W	0x5	HVH HPLDO High voltage 000: 0.8V 100: 1.2V 001: 0.9V 101: 1.3V 010: 1.0V 110: 1.4V

			011: 1.1V 111: 1.5V
3	/	/	/
2:0	R/W	0x1	HVL HPLDO low voltage 000: 0.8V 100: 1.2V 001: 0.9V 101: 1.3V 010: 1.0V 110: 1.4V 011: 1.1V 111: 1.5V

Reg 8Bh Headphone Adaptive Voltage Regulation Threshold[23:16] Register (Default Value: 0x00)

Offset: 0x8B			Register Name: HP_AVR_THH
Bit	Read/Write	Default	Description
7:0	R/W	0x00	THH Headphone Adaptive Voltage Regulation Threshold

Reg 8Ch Headphone Adaptive Voltage Regulation Threshold[15:8] Register (Default Value: 0x00)

Offset: 0x8C			Register Name: HP_AVR_THM
Bit	Read/Write	Default	Description
7:0	R/W	0x00	THM Headphone Adaptive Voltage Regulation Threshold

Reg 8Dh Headphone Adaptive Voltage Regulation Threshold[7:0] Register (Default Value: 0x00)

Offset: 0x8D			Register Name: HP_AVR_THL
Bit	Read/Write	Default	Description
7:0	R/W	0x00	THL Headphone Adaptive Voltage Regulation Threshold

Reg 8Eh Headphone Adaptive Voltage Regulation Debounce Register (Default Value: 0x01)

Offset: 0x8E			Register Name: HP_AVR_DBC
Bit	Read/Write	Default	Description
7:4	/	/	/
3:0	R/W	0x1	HV_DBC HVH to HVL debounce time 0x0: Not debounce 0x1: 1024/fs 0x2: 2048/fs 0x3: 4096/fs 0x4: 8192/fs 0x5: 16384/fs 0x6: 32768/fs 0x7: 65536/fs 0x8: 131072/fs 0x9: 262144/fs Other: Reserved

Reg 8Fh Headphone LOUT Control Register (Default Value: 0x05)

Offset: 0x8F			Register Name: HP_LOUT_CTRL
Bit	R/W	Default	Description
7:6	/	/	/
5:4	R/W	0x0	HP_ATT_STEP Headphone auto attenuate time step setting 00: 128 samples 01: 32 samples 10: 16 samples 11: 1 samples
3	/	/	/
2	R/W	0x1	HP_LOUT_AUTO_ATT Headphone lineout auto attenuate enable 0: Disable 1: Enable
1	/	/	/
0	R/W	0x1	HP_GAIN_ZC_DEN Headphone Gain Zero Cross Detect Enable 0: Disable 1: Enable

7.3.2.11 EQ 系数复用寄存器
Reg 90h Band-n B0 Coef [20:16] Register (Default Value: 0x01)

Offset: 0x90			Register Name: EQ_B0_H
Bit	R/W	Default	Description
7:5	/	/	/
4:0	R/W	0x01	EQ n, b0 coefficient high 5-bit (2's complement in 5.16 format)

Reg 91h Band-n B0 Coef [15:8] Register (Default Value: 0x00)

Offset: 0x91			Register Name: EQ_B0_M
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n, b0 coefficient middle 8-bit (2's complement in 5.16 format)

Reg 92h Band-n B0 Coef [7:0] Register (Default Value: 0x00)

Offset: 0x92			Register Name: EQ_B0_L
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n, b0 coefficient low 8-bit (2's complement in 5.16 format)

Reg 93h Band-n B1 Coef [20:16] Register (Default Value: 0x00)

Offset: 0x93			Register Name: EQ_B1_H
Bit	R/W	Default	Description
7:5	/	/	/
4:0	R/W	0x00	EQ n, b1 coefficient high 5-bit (2's complement in 5.16 format)

Reg 94h Band-n B1 Coef [15:8] Register (Default Value: 0x00)

Offset: 0x94			Register Name: EQ_B1_M
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , b1 coefficient middle 8-bit (2's complement in 5.16 format)

Reg 95h Band-n B1 Coef [7:0] Register (Default Value: 0x00)

Offset: 0x95			Register Name: EQ_B1_L
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , b1 coefficient low 8-bit (2's complement in 3.16 format)

Reg 96h Band-n B2 Coef [20:16] Register (Default Value: 0x00)

Offset: 0x96			Register Name: EQ_B2_H
Bit	R/W	Default	Description
7:5	/	/	/
4:0	R/W	0x00	EQ n , b2 coefficient high 5-bit (2's complement in 5.16 format)

Reg 97h Band-n B2 Coef [15:8] Register (Default Value: 0x00)

Offset: 0x97			Register Name: EQ_B2_M
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , b2 coefficient middle 8-bit (2's complement in 5.16 format)

Reg 98h Band-n B2 Coef [7:0] Register (Default Value: 0x00)

Offset: 0x98			Register Name: EQ_B2_L
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , b2 coefficient low 8-bit (2's complement in 5.16 format)

Reg 99h Band-n A1 Coef [20:16] Register (Default Value: 0x00)

Offset: 0x99			Register Name: EQ_A1_H
Bit	R/W	Default	Description
7:5	/	/	/
4:0	R/W	0x00	EQ n , a1 coefficient high 5-bit (2's complement in 5.16 format)

Reg 9Ah Band-n A1 Coef [15:8] Register (Default Value: 0x00)

Offset: 0x9A			Register Name: EQ_A1_M
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , a1 coefficient middle 8-bit (2's complement in 5.16 format)

Reg 9Bh Band-n A1 Coef [7:0] Register (Default Value: 0x00)

Offset: 0x9B			Register Name: EQ_A1_L
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , a1 coefficient low 8-bit (2's complement in 5.16 format)

Reg 9Ch Band-n A2 Coef [20:16] Register (Default Value: 0x00)

Offset: 0x9C			Register Name: EQ_A2_H
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Bit	R/W	Default	Description
7:5	/	/	/
4:0	R/W	0x00	EQ n , a2 coefficient high 5-bit (2's complement in 5.16 format)

Reg 9Dh Band-n A2 Coef [15:8] Register (Default Value: 0x00)

Offset: 0x9D			Register Name: EQ_A2_M
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , a2 coefficient middle 8-bit (2's complement in 5.16 format)

Reg 9Eh Band-n A2 Coef [7:0] Register (Default Value: 0x00)

Offset: 0x9E			Register Name: EQ_A2_L
Bit	R/W	Default	Description
7:0	R/W	0x00	EQ n , a2 coefficient low 8-bit (2's complement in 5.16 format)

7.3.2.12 DRC 控制寄存器
Reg A0h DRC Enable Register (Default Value: 0x00)

Offset: 0xA0			Register Name: DRC_ENA
Bit	R/W	Default	Description
7:2	/	/	/
1	R/W	0x0	DRC_CAL_ENA DRC Calculation Enable 0: Disable 1: Enable
0	R/W	0x0	DRC_HPF_ENA DRC HPF function Enable 0: Disable 1: Enable

Reg A1h DRC HPF Coef [26:24] Register (Default Value: 0x00)

Offset: 0xA1			Register Name: DRC_HPFC_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	HPF coefficient bit[26:24] setting and the data is 3.24 format

Reg A2h DRC HPF Coef [23:16] Register (Default Value: 0xFF)

Offset: 0xA2			Register Name: DRC_HPFC_2
Bit	R/W	Default	Description
7:0	R/W	0xFF	HPF coefficient bit[23:16] setting and the data is 3.24 format

Reg A3h DRC HPF Coef [15:8] Register (Default Value: 0xFA)

Offset: 0xA3			Register Name: DRC_HPFC_3
Bit	R/W	Default	Description
7:0	R/W	0xFA	HPF coefficient bit[15:8] setting and the data is 3.24 format

Reg A4h DRC HPF Coef [7:0] Register (Default Value: 0xC1)

Offset: 0xA4			Register Name: DRC_HPFC_4
Bit	R/W	Default	Description
7:0	R/W	0xC1	HPF coefficient bit[7:0] setting and the data is 3.24 format

Reg A5h DRC Control Register (Default Value: 0x00)

Offset: 0xA5			Register Name: DRC_CTRL
Bit	R/W	Default	Description
7	/	/	/
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable
5	R/W	0x0	DRC gain min limit enable. when this function enable, it will overwrite the noise detect function. 0: Disable 1: Enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0: Disable 1: Enable
3	R/W	0x0	Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused. (AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT/AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0: Disable 1: Enable When the Delay function enable is disable, the Signal delay time is unused.
1	R/W	0x0	DRC LT Enable 0: Disable 1: Enable When the DRC LT is disable the LT, KI and OPL parameter is unused
0	R/W	0x0	DRC ET Enable 0: Disable 1: Enable When the DRC ET is disable the ET, Ke and OPE parameter is unused

Reg A6h DRC Delay Control Register (Default Value: 0x00)

Offset: 0xA6			Register Name: DRC_DLY_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	The delay buffer use or not when the drc disable and the drc buffer data output

			completely 0 : Don't use the buffer 1 : Use the buffer
6	R	0x0	1-Band DRC delay buffer data output state when drc delay function is enable and the drc function disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0; 0 : not complete 1 : is complete
5:0	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ----- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused.

Reg A7h DRC Optimum 1 Register (Default Value: 0x00)

Offset: 0xA7			Register Name: DRC_OPT_1
Bit	R/W	Default	Description
7	/	/	/
6	R/W	0x0	DRC data output when DRC disable and DRC delay data output complete. 0 : the output is the input music data 1 : the output is 0
5	R/W	0x0	DRC gain default value setting 0: The default gain is 1 1: The default gain is 0
4:0	R/W	0x0	The hysteresis of the gain smooth filter to use the decay time coefficient or the attack time coefficient. When in the decay time state, if $g(n-1)-g(n)>\text{hysteresis}$, then the state will change to attack time state, and when in the attack time, if $g(n)-g(n-1)>\text{hysteresis}$, then the state will change to decay time state. Note the hysteresis of 0x00 and 0x04 is the same. 00000: 2^{-16} 00001: 2^{-19} 00010: 2^{-18} 00011: 2^{-17} 00100: 2^{-16} -----

			10011: 2^{-1} 10100 ~11111: 1 hysteresis = 2^{n-20} , except n=0x00, and n less 0x14.
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Reg A8h DRC Optimum 2 Register (Default Value: 0x00)

Offset: 0xA8			Register Name: DRC_OPT_2
Bit	R/W	Default	Description
7:4	/	/	/
3	R/W	0x0	The gain smooth use the expander coefficient when the energy in expander range 0 : use the normal smooth coefficient 1 : use the expander coefficient
2	R/W	0x0	The gain normal smooth coefficient selection mode set 0 : both release and attack coefficient use hysteresis; 1 : only the attack coefficient use hysteresis;
1	R/W	0x0	The min of energy set in Peak detect mode 0 : -120dB 1 : -210dB
0	R/W	0x0	The energy mode select in rms detect mode 0 : the energy is RMS 1 : the energy is square of RMS

Reg ACh DRC Left Peak Filter Attack Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xAC			Register Name: DRC_LPFAT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg ADh DRC Left Peak Filter Attack Time Coef [23:16] Register (Default Value: 0x0B)

Offset: 0xAD			Register Name: DRC_LPFAT_2
Bit	R/W	Default	Description
7:0	R/W	0x0B	The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg AEh DRC Left Peak Filter Attack Time Coef [15:8] Register (Default Value: 0x77)

Offset: 0xAE			Register Name: DRC_LPFAT_3
Bit	R/W	Default	Description
7:0	R/W	0x77	The left peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg AFh DRC Left Peak Filter Attack Time Coef [7:0] Register (Default Value: 0xBF)

Offset: 0xAF			Register Name: DRC_LPFAT_4
Bit	R/W	Default	Description
7:0	R/W	0xBF	The left peak filter attack time parameter setting, which determine by the equation that

			AT = $1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)
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Reg B0h DRC Right Peak Filter Attack Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xB0			Register Name: DRC_RPFAT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The right peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg B1h DRC Right Peak Filter Attack Time Coef [23:16] Register (Default Value: 0x0B)

Offset: 0xB1			Register Name: DRC_RPFAT_2
Bit	R/W	Default	Description
7:0	R/W	0x0B	The right peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg B2h DRC Right Peak Filter Attack Time Coef [15:8] Register (Default Value: 0x77)

Offset: 0xB2			Register Name: DRC_RPFAT_3
Bit	R/W	Default	Description
7:0	R/W	0x77	The right peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg B3h DRC Right Peak Filter Attack Time Coef [7:0] Register (Default Value: 0xBF)

Offset: 0xB3			Register Name: DRC_RPFAT_4
Bit	R/W	Default	Description
7:0	R/W	0xBF	The right peak filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/t_a)$. The format is 3.24. (1ms)

Reg B4h DRC Left Peak Filter Release Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xB4			Register Name: DRC_LPFRT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2T_s/t_r)$. The format is 3.24. (100ms)

Reg B5h DRC Left Peak Filter Release Time Coef [23:16] Register (Default Value: 0xFF)

Offset: 0xB5			Register Name: DRC_LPFRT_2
Bit	R/W	Default	Description
7:0	R/W	0xFF	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2T_s/t_r)$. The format is 3.24. (100ms)

Reg B6h DRC Left Peak Filter Release Time Coef [15:8] Register (Default Value: 0xE1)

Offset: 0xB6			Register Name: DRC_LPFRT_3
Bit	R/W	Default	Description
7:0	R/W	0xE1	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2T_s/t_r)$. The format is 3.24. (100ms)

Reg B7h DRC Left Peak Filter Release Time Coef [7:0] Register (Default Value: 0xF8)

Offset: 0xB7			Register Name: DRC_LPFRT_4
Bit	R/W	Default	Description
7:0	R/W	0xF8	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg B8h DRC Right Peak Filter Release Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xB8			Register Name: DRC_RPFRT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg B9h DRC Right Peak Filter Release Time Coef [23:16] Register (Default Value: 0xFF)

Offset: 0xB9			Register Name: DRC_RPFRT_2
Bit	R/W	Default	Description
7:0	R/W	0xFF	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg BAh DRC Right Peak Filter Release Time Coef [15:8] Register (Default Value: 0xE1)

Offset: 0xBA			Register Name: DRC_RPFRT_3
Bit	R/W	Default	Description
7:0	R/W	0xE1	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg BBh DRC Right Peak Filter Release Time Coef [7:0] Register (Default Value: 0xF8)

Offset: 0xBB			Register Name: DRC_RPFRT_4
Bit	R/W	Default	Description
7:0	R/W	0xF8	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg BCh DRC Left RMS Filter Average Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xBC			Register Name: DRC_LRMSAT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg BDh DRC Left RMS Filter Average Time Coef [23:16] Register (Default Value: 0x01)

Offset: 0xBD			Register Name: DRC_LRMSAT_2
Bit	R/W	Default	Description
7:0	R/W	0x01	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg BEh DRC Left RMS Filter Average Time Coef [15:8] Register (Default Value: 0x2B)

Offset: 0xBE			Register Name: DRC_LRMSAT_3
Bit	R/W	Default	Description
7:0	R/W	0x2B	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg BFh DRC Left RMS Filter Average Time Coef [7:0] Register (Default Value: 0xAF)

Offset: 0xBF			Register Name: DRC_LRMSAT_4
Bit	R/W	Default	Description
7:0	R/W	0xAF	The left peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg C0h DRC Right RMS Filter Average Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xC0			Register Name: DRC_RRMSAT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg C1h DRC Right RMS Filter Average Time Coef [23:16] Register (Default Value: 0x01)

Offset: 0xC1			Register Name: DRC_RRMSAT_2
Bit	R/W	Default	Description
7:0	R/W	0x01	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg C2h DRC Right RMS Filter Average Time Coef [15:8] Register (Default Value: 0x2B)

Offset: 0xC2			Register Name: DRC_RRMSAT_3
Bit	R/W	Default	Description
7:0	R/W	0x2B	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg C3h DRC Right RMS Filter Average Time Coef [7:0] Register (Default Value: 0xAF)

Offset: 0xC3			Register Name: DRC_RRMSAT_4
Bit	R/W	Default	Description
7:0	R/W	0xAF	The right peak filter release time parameter setting, which determine by the equation that $RT = \exp(-2.2Ts/tr)$. The format is 3.24. (100ms)

Reg C4h DRC Compressor Threshold Setting [31:24] Register (Default Value: 0x06)

Offset: 0xC4			Register Name: DRC_CT_1
Bit	R/W	Default	Description
7:0	R/W	0x06	The compressor threshold setting, which set by the equation that $CTin = -CT/6.0206$. The format is 8.24 (-40dB)

Reg C5h DRC Compressor Threshold Setting [23:16] Register (Default Value: 0xA4)

Offset: 0xC5			Register Name: DRC_CT_2
Bit	R/W	Default	Description
7:0	R/W	0xA4	The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB)

Reg C6h DRC Compressor Threshold Setting [15:8] Register (Default Value: 0xD3)

Offset: 0xC6			Register Name: DRC_CT_3
Bit	R/W	Default	Description
7:0	R/W	0xD3	The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB)

Reg C7h DRC Compressor Threshold Setting [7:0] Register (Default Value: 0xC0)

Offset: 0xC7			Register Name: DRC_CT_4
Bit	R/W	Default	Description
7:0	R/W	0xC0	The compressor threshold setting, which set by the equation that $CT_{in} = -CT/6.0206$. The format is 8.24 (-40dB)

Reg C8h DRC Compressor Slope Setting [31:24] Register (Default Value: 0x00)

Offset: 0xC8			Register Name: DRC_KC_1
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (2 : 1)

Reg C9h DRC Compressor Slope Setting [23:16] Register (Default Value: 0x80)

Offset: 0xC9			Register Name: DRC_KC_2
Bit	R/W	Default	Description
7:0	R/W	0x80	The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (2 : 1)

Reg CAh DRC Compressor Slope Setting [15:8] Register (Default Value: 0x00)

Offset: 0xCA			Register Name: DRC_KC_3
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (2 : 1)

Reg CBh DRC Compressor Slope Setting [7:0] Register (Default Value: 0x00)

Offset: 0xCB			Register Name: DRC_KC_4
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the compressor which determine by the equation that $K_c = 1/R$, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (2 : 1)

Reg CCh DRC Compressor Output at Compressor Threshold [31:24] Register (Default Value: 0xF9)

Offset: 0xCC			Register Name: DRC_OPC_1
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Bit	R/W	Default	Description
7:0	R/W	0xF9	The output of the compressor which determine by the equation $OPC/6.0206$ The format is 8.24 (-40dB)

Reg CDh DRC Compressor Output at Compressor Threshold [23:16] Register (Default Value: 0x5B)

Offset: 0xCD			Register Name: DRC_OPC_2
Bit	R/W	Default	Description
7:0	R/W	0x5B	The output of the compressor which determine by the equation $OPC/6.0206$ The format is 8.24 (-40dB)

Reg CEh DRC Compressor Output at Compressor Threshold [15:8] Register (Default Value: 0x2C)

Offset: 0xCE			Register Name: DRC_OPC_3
Bit	R/W	Default	Description
7:0	R/W	0x2C	The output of the compressor which determine by the equation $OPC/6.0206$ The format is 8.24 (-40dB)

Reg CFh DRC Compressor Output at Compressor Threshold [7:0] Register (Default Value: 0x3F)

Offset: 0xCF			Register Name: DRC_OPC_4
Bit	R/W	Default	Description
7:0	R/W	0x3F	The output of the compressor which determine by the equation $OPC/6.0206$ The format is 8.24 (-40dB)

Reg D0h DRC Limiter Threshold Setting [31:24] Register (Default Value: 0x01)

Offset: 0xD0			Register Name: DRC_LT_1
Bit	R/W	Default	Description
7:0	R/W	0x01	The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB)

Reg D1h DRC Limiter Threshold Setting [23:16] Register (Default Value: 0xA9)

Offset: 0xD1			Register Name: DRC_LT_2
Bit	R/W	Default	Description
7:0	R/W	0xA9	The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB)

Reg D2h DRC Limiter Threshold Setting [15:8] Register (Default Value: 0x34)

Offset: 0xD2			Register Name: DRC_LT_3
Bit	R/W	Default	Description
7:0	R/W	0x34	The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB)

Reg D3h DRC Limiter Threshold Setting [7:0] Register (Default Value: 0xF0)

Offset: 0xD3			Register Name: DRC_LT_4
Bit	R/W	Default	Description
7:0	R/W	0xF0	The limiter threshold setting, which set by the equation that $LT_{in} = -LT/6.0206$, The format is 8.24. (-10dB)

Reg D4h DRC Limiter Slope Setting [31:24] Register (Default Value: 0x00)

Offset: 0xD4			Register Name: DRC_KL_1
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (50 :1)

Reg D5h DRC Limiter Slope Setting [23:16] Register (Default Value: 0x05)

Offset: 0xD5			Register Name: DRC_KL_2
Bit	R/W	Default	Description
7:0	R/W	0x05	The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (50 :1)

Reg D6h DRC Limiter Slope Setting [15:8] Register (Default Value: 0x1E)

Offset: 0xD6			Register Name: DRC_KL_3
Bit	R/W	Default	Description
7:0	R/W	0x1E	The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (50 :1)

Reg D7h DRC Limiter Slope Setting [7:0] Register (Default Value: 0xB8)

Offset: 0xD7			Register Name: DRC_KL_4
Bit	R/W	Default	Description
7:0	R/W	0xB8	The slope of the limiter which determine by the equation that $KI = 1/R$, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (50 :1)

Reg D8h DRC Limiter Output at Limiter Threshold [31:24] Register (Default Value: 0xFB)

Offset: 0xD8			Register Name: DRC_OPL_1
Bit	R/W	Default	Description
7:0	R/W	0xFB	The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB)

Reg D9h DRC Limiter Output at Limiter Threshold [23:16] Register (Default Value: 0xD8)

Offset: 0xD9			Register Name: DRC_OPL_2
Bit	R/W	Default	Description
7:0	R/W	0xD8	The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB)

Reg DAh DRC Limiter Output at Limiter Threshold [15:8] Register (Default Value: 0xFB)

Offset: 0xDA			Register Name: DRC_OPL_3
Bit	R/W	Default	Description
7:0	R/W	0xFB	The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB)

Reg DBh DRC Limiter Output at Limiter Threshold [7:0] Register (Default Value: 0xA7)

Offset: 0xDB			Register Name: DRC_OPL_4
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Bit	R/W	Default	Description
7:0	R/W	0xA7	The output of the limiter which determine by equation $OPT/6.0206$. The format is 8.24 (-25dB)

Reg DCh DRC Expander Threshold Setting [31:24] Register (Default Value: 0x0B)

Offset: 0xDC			Register Name: DRC_ET_1
Bit	R/W	Default	Description
7:0	R/W	0x0B	The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB)

Reg DDh DRC Expander Threshold Setting [23:16] Register (Default Value: 0xA0)

Offset: 0xDD			Register Name: DRC_ET_2
Bit	R/W	Default	Description
7:0	R/W	0xA0	The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB)

Reg DEh DRC Expander Threshold Setting [15:8] Register (Default Value: 0x72)

Offset: 0xDE			Register Name: DRC_ET_3
Bit	R/W	Default	Description
7:0	R/W	0x72	The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB)

Reg DFh DRC Expander Threshold Setting [7:0] Register (Default Value: 0x91)

Offset: 0xDF			Register Name: DRC_ET_4
Bit	R/W	Default	Description
7:0	R/W	0x91	The expander threshold setting, which set by the equation that $ETin = -ET/6.0206$, The format is 8.24. (-70dB)

Reg E0h DRC Expander Slope Setting [31:24] Register (Default Value: 0x05)

Offset: 0xE0			Register Name: DRC_KE_1
Bit	R/W	Default	Description
7:0	R/W	0x05	The slope of the expander which determine by the equation that $Ke = 1/R$, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (1:5)

Reg E1h DRC Expander Slope Setting [23:16] Register (Default Value: 0x00)

Offset: 0xE1			Register Name: DRC_KE_2
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the expander which determine by the equation that $Ke = 1/R$, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (1:5)

Reg E2h DRC Expander Slope Setting [15:8] Register (Default Value: 0x00)

Offset: 0xE2			Register Name: DRC_KE_3
Bit	R/W	Default	Description

7:0	R/W	0x00	The slope of the expander which determine by the equation that $K_e = 1/R$, there, R is the ratio of the expander, which always is integer and the k_e must larger than 50. The format is 8.24. (1:5)
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Reg E3h DRC Expander Slope Setting [7:0] Register (Default Value: 0x00)

Offset: 0xE3			Register Name: DRC_KE_4
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the expander which determine by the equation that $K_e = 1/R$, there, R is the ratio of the expander, which always is integer and the k_e must larger than 50. The format is 8.24. (1:5)

Reg E4h DRC Expander Output at Expander Threshold [31:24] Register (Default Value: 0xF4)

Offset: 0xE4			Register Name: DRC_OPE_1
Bit	R/W	Default	Description
7:0	R/W	0xF4	The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB)

Reg E5h DRC Expander Output at Expander Threshold [23:16] Register (Default Value: 0x5F)

Offset: 0xE5			Register Name: DRC_OPE_2
Bit	R/W	Default	Description
7:0	R/W	0x5F	The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB)

Reg E6h DRC Expander Output at Expander Threshold [15:8] Register (Default Value: 0x8D)

Offset: 0xE6			Register Name: DRC_OPE_3
Bit	R/W	Default	Description
7:0	R/W	0x8D	The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB)

Reg E7h DRC Expander Output at Expander Threshold [7:0] Register (Default Value: 0x6E)

Offset: 0xE7			Register Name: DRC_OPE_4
Bit	R/W	Default	Description
7:0	R/W	0x6E	The output of the expander which determine by equation $OPE/6.0206$. The format is 8.24 (-70dB)

Reg E8h DRC Linear Slope Setting [31:24] Register (Default Value: 0x01)

Offset: 0xE8			Register Name: DRC_KN_1
Bit	R/W	Default	Description
7:0	R/W	0x01	The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is integer . The format is 8.24. (1:1)

Reg E9h DRC Linear Slope Setting [23:16] Register (Default Value: 0x00)

Offset: 0xE9			Register Name: DRC_KN_2
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the

			ratio of the linear, which always is integer . The format is 8.24. (1:1)
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Reg EAh DRC Linear Slope Setting [15:8] Register (Default Value: 0x00)

Offset: 0xEA			Register Name: DRC_KN_3
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is integer . The format is 8.24. (1:1)

Reg EBh DRC Linear Slope Setting [7:0] Register (Default Value: 0x00)

Offset: 0xEB			Register Name: DRC_KN_4
Bit	R/W	Default	Description
7:0	R/W	0x00	The slope of the linear which determine by the equation that $K_n = 1/R$, there, R is the ratio of the linear, which always is integer . The format is 8.24. (1:1)

Reg ECh DRC Smooth filter Gain Attack Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xEC			Register Name: DRC_SFAT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms)

Reg EDh DRC Smooth filter Gain Attack Time Coef [23:16] Register (Default Value: 0x02)

Offset: 0xED			Register Name: DRC_SFAT_2
Bit	R/W	Default	Description
7:0	R/W	0x02	The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms)

Reg EEh DRC Smooth filter Gain Attack Time Coef [15:8] Register (Default Value: 0x56)

Offset: 0xEE			Register Name: DRC_SFAT_3
Bit	R/W	Default	Description
7:0	R/W	0x56	The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms)

Reg EFh DRC Smooth filter Gain Attack Time Coef [7:0] Register (Default Value: 0x00)

Offset: 0xEF			Register Name: DRC_SFAT_4
Bit	R/W	Default	Description
7:0	R/W	0x00	The smooth filter attack time parameter setting, which determine by the equation that $AT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (5ms)

Reg F0h DRC Smooth filter Gain Release Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xF0			Register Name: DRC_SFRT_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (200ms)

Reg F1h DRC Smooth filter Gain Release Time Coef [23:16] Register (Default Value: 0x00)

Offset: 0xF1			Register Name: DRC_SFRT_2
Bit	R/W	Default	Description
7:0	R/W	0x00	The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (200ms)

Reg F2h DRC Smooth filter Gain Release Time Coef [15:8] Register (Default Value: 0x0F)

Offset: 0xF2			Register Name: DRC_SFRT_3
Bit	R/W	Default	Description
7:0	R/W	0x0F	The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (200ms)

Reg F3h DRC Smooth filter Gain Release Time Coef [7:0] Register (Default Value: 0x04)

Offset: 0xF3			Register Name: DRC_SFRT_4
Bit	R/W	Default	Description
7:0	R/W	0x04	The gain smooth filter release time parameter setting, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (200ms)

Reg F4h DRC MAX Gain Setting [31:24] Register (Default Value: 0xFE)

Offset: 0xF4			Register Name: DRC_MXGS_1
Bit	R/W	Default	Description
7:0	R/W	0xFE	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must $-20dB < MXG < 30dB$ (-10dB)

Reg F5h DRC MAX Gain Setting [23:16] Register (Default Value: 0x56)

Offset: 0xF5			Register Name: DRC_MXGS_2
Bit	R/W	Default	Description
7:0	R/W	0x56	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must $-20dB < MXG < 30dB$ (-10dB)

Reg F6h DRC MAX Gain Setting [15:8] Register (Default Value: 0xCB)

Offset: 0xF6			Register Name: DRC_MXGS_3
Bit	R/W	Default	Description
7:0	R/W	0xCB	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must $-20dB < MXG < 30dB$ (-10dB)

Reg F7h DRC MAX Gain Setting [7:0] Register (Default Value: 0x0F)

Offset: 0xF7			Register Name: DRC_MXGS_4
Bit	R/W	Default	Description
7:0	R/W	0x0F	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must $-20dB < MXG < 30dB$ (-10dB)

Reg F8h DRC MIN Gain Setting [31:24] Register (Default Value: 0xF9)

Offset: 0xF8			Register Name: DRC_MNGS_1
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Bit	R/W	Default	Description
7:0	R/W	0xF9	The min gain setting which determine by equation $MNG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB)

Reg F9h DRC MIN Gain Setting [23:16] Register (Default Value: 0x5B)

Offset: 0xF9			Register Name: DRC_MNGS_2
Bit	R/W	Default	Description
7:0	R/W	0x5B	The min gain setting which determine by equation $MNG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB)

Reg FAh DRC MIN Gain Setting [15:8] Register (Default Value: 0x2C)

Offset: 0xFA			Register Name: DRC_MNGS_3
Bit	R/W	Default	Description
7:0	R/W	0x2C	The min gain setting which determine by equation $MNG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB)

Reg FBh DRC MIN Gain Setting [7:0] Register (Default Value: 0x3F)

Offset: 0xFB			Register Name: DRC_MNGS_4
Bit	R/W	Default	Description
7:0	R/W	0x3F	The min gain setting which determine by equation $MNG/6.0206$. The format is 8.24 and must $-60dB \leq MNG \leq -30dB$ (-40dB)

Reg FCh DRC Expander Smooth Time Coef [26:24] Register (Default Value: 0x00)

Offset: 0xFC			Register Name: DRC_EPSC_1
Bit	R/W	Default	Description
7:3	/	/	/
2:0	R/W	0x00	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms)

Reg FDh DRC Expander Smooth Time Coef [23:16] Register (Default Value: 0x00)

Offset: 0xFD			Register Name: DRC_EPSC_2
Bit	R/W	Default	Description
7:0	R/W	0x00	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms)

Reg FEh DRC Expander Smooth Time Coef [15:8] Register (Default Value: 0x64)

Offset: 0xFE			Register Name: DRC_EPSC_3
Bit	R/W	Default	Description
7:0	R/W	0x64	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that $RT = 1 - \exp(-2.2Ts/tr)$. The format is 3.24. (30ms)

Reg FFh DRC Expander Smooth Time Coef [7:0] Register (Default Value: 0x0C)

Offset: 0xFF			Register Name: DRC_EPSC_4
Bit	R/W	Default	Description
7:0	R/W	0x0C	The gain smooth filter release and attack time parameter setting in expander region,

			which determine by the equation that $RT = 1 - \exp(-2.2T_s/tr)$. The format is 3.24. (30ms)
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8 APPLICATION INFORMATION

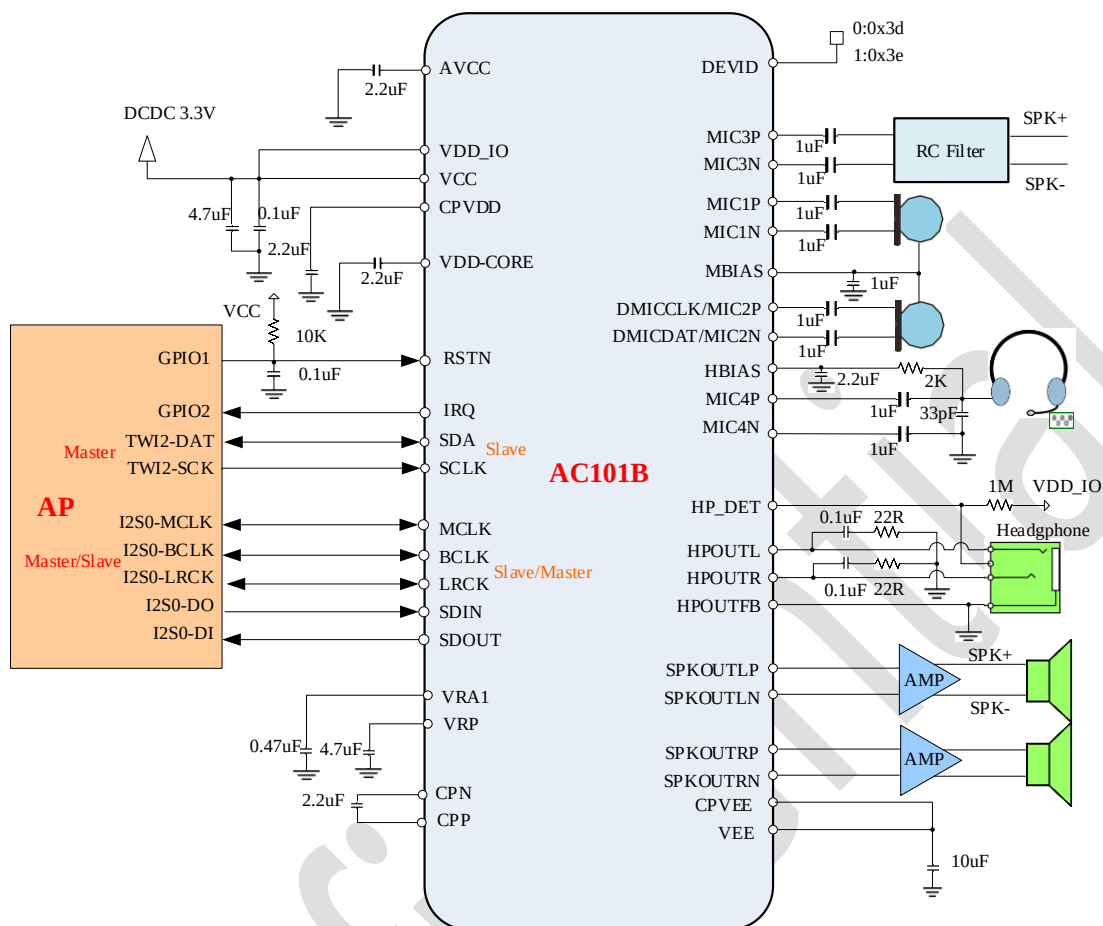


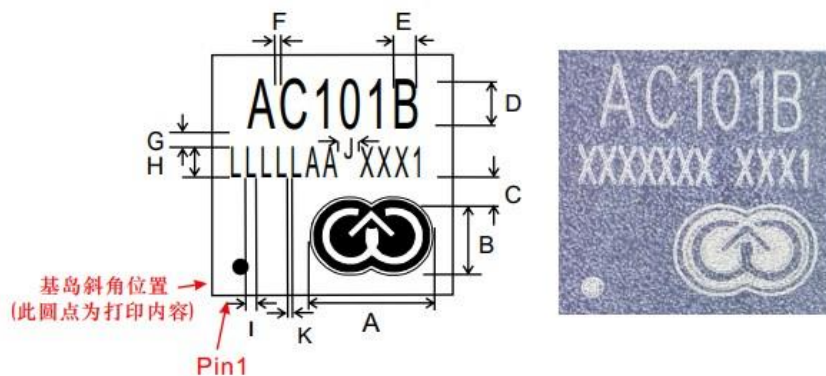
Figure 8-1. Typical Application Diagram

9 PCB Layout Guidelines

Each system design and PCB layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the AC101B performance:

1. The decoupling capacitors for the power supplies must be placed close to the device terminals. Figure 8-1 shows the recommended decoupling capacitors for the AC101B.
2. For analog differential audio signals, they must be routed differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to avoid undesirable crosstalk.
3. Analog and digital grounds must be separated to prevent possible digital noise from affecting the analog performance of the board.

10.2 Marking Information



A	B	C	D	E	F	G	H	I	J	K
2.54	1.62	0.38	1.07	0.50	0.11	0.36	0.64	0.26	0.51	0.07

注:字体:Swis721 LtCn BT

“LLLLLAA XXX1” 其中“LLLLL”为内部批号前五位,“AA”“1”固定不变,
“XXX”为Date Code; “内部批号前五位”、“Date Code”以用户在订单中指定为准.

单位:mm 公差:±0.1mm 印章整体上下左右居中对称

Figure 10-2 AC101B Marking

Table 10-1 AC101B Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AC101B	Product name	Fixed
2	LLLLLAA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

11 REFLOW PROFILE

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

The figure shows the typical reflow profile of AC101B device sample.

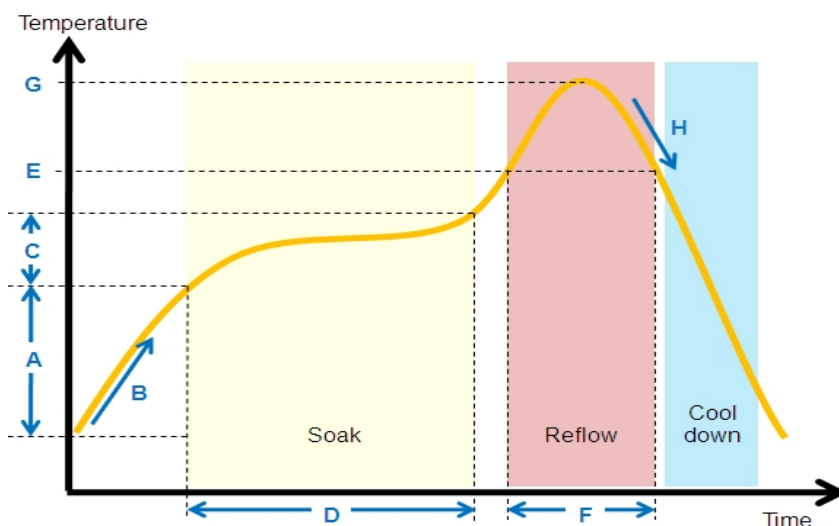


Figure 11-11-1 AC101B Typical Reflow Profile

Reflow profile conditions of AC101B device sample is given in Table 11-1.

Table 11-1 AC101B Reflow Profile Conditions

QTI typical SMT reflow profile conditions (for reference only)		
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C/sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C/sec

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