



# MPQ4263

## 36V, 140W Buck-Boost with Integrated LS-FETs, Supports High-Side Current Sense and I<sup>2</sup>C Interface for Automotive, AEC-Q100

### DESCRIPTION

The MPQ4263 is a buck-boost converter with two integrated low-side MOSFETs (LS-FETs). The device can deliver up to 140W of peak output power ( $P_{OUT}$ ) at certain input voltage ( $V_{IN}$ ) supply ranges with excellent efficiency.

The MPQ4263 is well-suited for USB power delivery (PD) applications, and it can work with an external USB PD controller through the I<sup>2</sup>C interface.

The I<sup>2</sup>C interface and one-time programmable (OTP) memory provide flexibility for the configurable features.

Fault condition protection includes CC current limiting with high-side (HS) current-sensing, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MPQ4263 requires a minimal number of readily available, standard external components, and is available in a QFN-20 (3mmx5mm) package. It is available in AEC-Q100 Grade 1.

### FEATURES

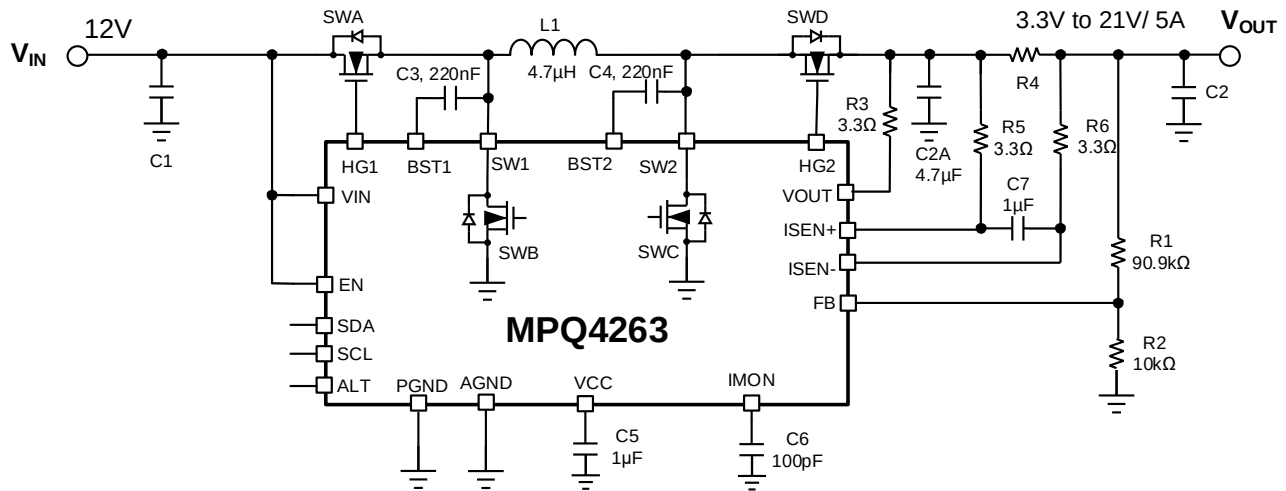
- 140W Buck-Boost Converter with Integrated Low-Side MOSFETs (LS-FETs)
- Integrated Gate Driver for High-Side MOSFETs (HS-FETs)
- Configurable Input Under-Voltage Lockout (UVLO)
- 3.6V to 36V Start-Up Input Voltage ( $V_{IN}$ ) Range
- 1V to 36V Output Voltage ( $V_{OUT}$ ) Range
- Supports 2.8V Falling  $V_{IN}$  When  $V_{OUT} > 3.5V$
- Up to 98% Peak Efficiency
- I<sup>2</sup>C-Configurable Reference Voltage ( $V_{REF}$ ) Range: 0.1V to 2.147V with 1mV Resolution
- Accurate Output CC Current Limit:  $\pm 5\%$ , Supports High-Side Current Sense
- Accurate Output Current ( $I_{OUT}$ ) Monitor (IMON) Function
- Meets USB PD 3.1, EPR AVS, and PPS Specification
- Selectable 280kHz, 420kHz, and 580kHz Switching Frequency ( $f_{SW}$ )
- Selectable Forced PWM Mode or Auto-PFM/PWM Mode
- Output Bias  $V_{CC}$  LDO for Higher Efficiency
- Line Drop Compensation via  $R_{SENS}$
- I<sup>2</sup>C, Alert, and One-Time Programmable (OTP) Memory
- EN Shutdown Passive Discharge
- Output Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Thermal Shutdown Protection
- Available in a QFN-20 (3mmx5mm) Package
- Available in AEC-Q100 in Grade 1

### APPLICATIONS

- USB PD Hubs
- USB PD Charging Ports
- Automotive DC Power Supplies
- Wireless Charging

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## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number*            | Package          | Top Marking | MSL |
|-------------------------|------------------|-------------|-----|
| MPQ4263GQVE-0000-AEC1   | QFN-20 (3mmx5mm) | See Below   | 1   |
| MPQ4263GQVE-0001-AEC1   |                  |             |     |
| MPQ4263GQVE-0002-AEC1   |                  |             |     |
| MPQ4263GQVE-xxxx-AEC1** |                  |             |     |
| EVKT-MPQ4263            | Evaluation kit   |             |     |

\* For Tape & Reel, add suffix -Z (e.g. MPQ4263GQVE-xxxx- AEC1-Z).

\*\* “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. “xxxx” and “0000” are already preconfigured by the MPS factory; the user cannot reconfigure the OTP. The default code is “0000”. The “0001” code is for 60W PD applications with a 420kHz frequency. The “0002” code is for 100W PD applications with a 280kHz frequency.

## TOP MARKING

**MPYW**

**4263**

**LLL**

**E**

MP: MPS prefix  
Y: Year code  
W: Week code  
4263: Part number  
LLL: Lot number  
E: Wettable flank

## EVALUATION KIT (EVKT-MPQ4263)

EVKT-MPQ4263 kit contents (items below can be ordered separately):

| # | Part Number           | Item                                                                                          | Quantity |
|---|-----------------------|-----------------------------------------------------------------------------------------------|----------|
| 1 | EVQ4263-QVE-00A       | MPQ4263 evaluation board                                                                      | 1        |
| 2 | EVKT-USBi2C-02 bag    | Includes USB-to-I <sup>2</sup> C communication interface, one USB cable, and one ribbon cable | 1        |
| 3 | MPQ4263GQVE-0000-AEC1 | IC with default configuration                                                                 | 2        |
| 4 | Online resources      | Include GUI and supplemental files                                                            | -        |

Order directly from [MonolithicPower.com](https://www.monolithicpower.com) or our distributors.

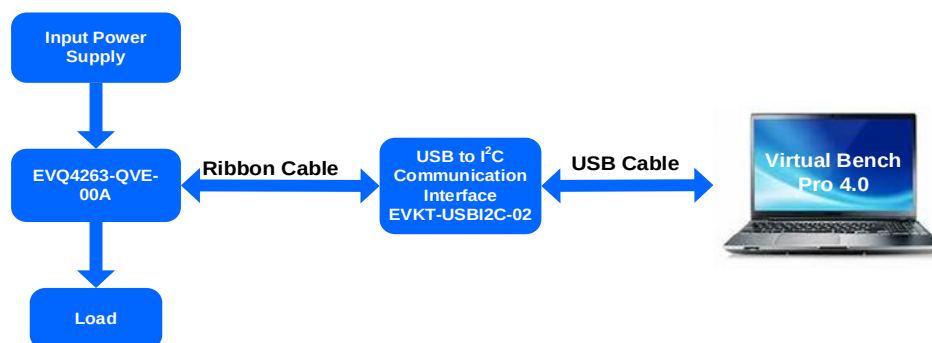
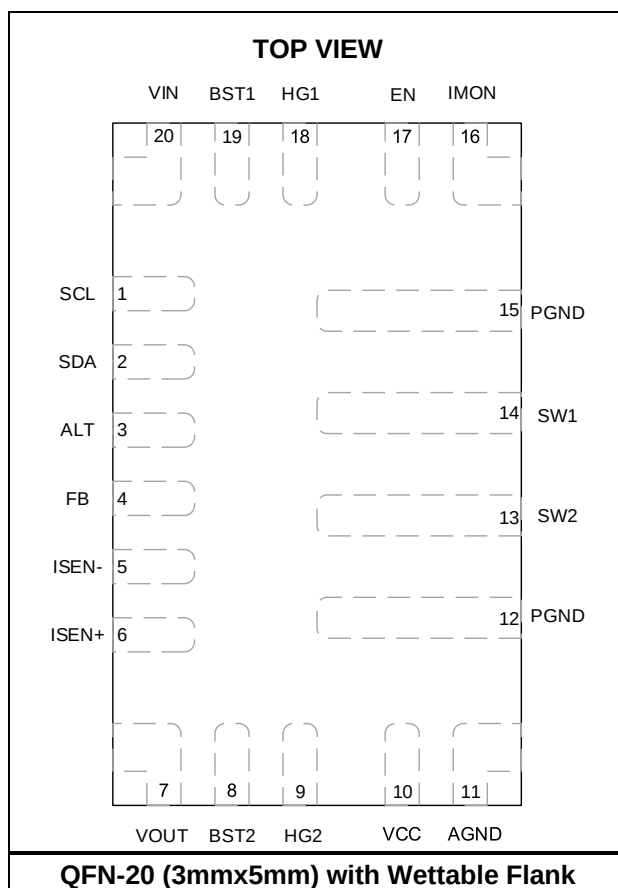


Figure 1: EVKT-MPQ4263 Evaluation Kit Set-Up

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #  | Name  | Description                                                                                                                                                                                                                  |
|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1      | SCL   | I <sup>2</sup> C clock signal input.                                                                                                                                                                                         |
| 2      | SDA   | I <sup>2</sup> C data line.                                                                                                                                                                                                  |
| 3      | ALT   | I <sup>2</sup> C alert pin. The ALT pin is an open-drain output, active low.                                                                                                                                                 |
| 4      | FB    | <b>Feedback pin.</b> Connect the FB pin to the tap of an external resistor divider, connected from the output to AGND, to set the output voltage (V <sub>OUT</sub> ).                                                        |
| 5      | ISEN- | <b>Negative node of the current-sense signal input.</b> Place a current-sense resistor should between ISEN+ and ISEN-.                                                                                                       |
| 6      | ISEN+ | <b>Positive node of the current-sense signal input.</b> Place a current-sense resistor should between ISEN+ and ISEN-.                                                                                                       |
| 7      | VOUT  | <b>Output voltage sense input.</b> The VOUT pin provides the VCC supply at certain V <sub>OUT</sub> conditions.                                                                                                              |
| 8      | BST2  | <b>Bootstrap.</b> A 0.22μF capacitor is connected between SW2 and BST2 to form a floating supply across the high-side switch driver.                                                                                         |
| 9      | HG2   | <b>High-side 2 gate drive output for the boost high-side switch (SWD).</b>                                                                                                                                                   |
| 10     | VCC   | <b>Internal 5V LDO regulator output.</b> Decouple the VCC pin with a 0.47μF to 1μF capacitor.                                                                                                                                |
| 11     | AGND  | <b>Analog ground.</b> Connect AGND to PGND. Connect the AGND pin to the VCC capacitor's ground node.                                                                                                                         |
| 12, 15 | PGND  | <b>Power ground.</b> The PGND pin requires extra care during PCB layout. Connect the PGND pin to ground with copper traces and vias.                                                                                         |
| 13     | SW2   | <b>Switch 2 node of the buck-boost.</b> Connect SW1 to SW2 with a power inductor. Use a wide PCB trace to make the connection.                                                                                               |
| 14     | SW1   | <b>Switch 1 node of the buck-boost.</b> Connect SW1 to SW2 with a power inductor. Use a wide PCB trace to make the connection.                                                                                               |
| 16     | IMON  | <b>Current monitor output.</b> The IMON pin represents the signal between ISEN+ and ISEN-.                                                                                                                                   |
| 17     | EN    | <b>EN input.</b> Apply high logic to the EN pin to enable the chip.                                                                                                                                                          |
| 18     | HG1   | <b>High-side 1 gate drive output for the buck high-side switch (SWA).</b>                                                                                                                                                    |
| 19     | BST1  | <b>Bootstrap.</b> A 0.22μF capacitor is connected between SW1 and BST1 to form a floating supply across the high-side switch driver.                                                                                         |
| 20     | VIN   | <b>Supply voltage for the internal logic circuitry but not the power MOSFETs.</b> Kelvin connect the VIN pin to the SWA MOSFET's drain with a wide PCB trace. This connection cannot be shared with another DC/DC converter. |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                         |                                                                           |
|-------------------------------------------------------------------------|---------------------------------------------------------------------------|
| Input voltage (V <sub>IN</sub> )                                        | .....-0.4V to +40V                                                        |
| V <sub>SW1</sub>                                                        | .....-0.3V (-8V for <10ns)<br>to V <sub>IN</sub> + 0.3V (+43V for <10ns)  |
| V <sub>SW2</sub>                                                        | .....-0.3V (-8V for <10ns)<br>to V <sub>OUT</sub> + 0.3V (+43V for <10ns) |
| V <sub>BST1</sub> /BST2/HG1/HG2                                         | ..... V <sub>SW1</sub> /SW2 + 6V                                          |
| V <sub>OUT</sub> /ISEN+/ISEN-                                           | .....-0.3V to +40V                                                        |
| V <sub>EN</sub>                                                         | .....-0.3V to +40V                                                        |
| All other pins                                                          | .....-0.3V to +6V                                                         |
| Continuous power dissipation (T <sub>A</sub> = 25°C) <sup>(2) (5)</sup> |                                                                           |
| QFN-20 (3mmx5mm)                                                        | ..... 6W                                                                  |
| Junction temperature (T <sub>J</sub> )                                  | .....150°C                                                                |
| Lead temperature                                                        | .....260°C                                                                |
| Storage temperature                                                     | ..... -65°C to +150°C                                                     |

## ESD Ratings <sup>(3)</sup>

|                            |                     |
|----------------------------|---------------------|
| Human body model (HBM)     |                     |
| SW1, HG1, and BST1         | .....-2kV to +1.8kV |
| All other pins             | .....±2kV           |
| Charged-device model (CDM) | .....±750V          |

## Recommended Operating Conditions <sup>(4)</sup>

|                                              |                      |
|----------------------------------------------|----------------------|
| Operating input voltage (V <sub>IN</sub> )   | .....3.6V to 36V     |
| Operating output voltage (V <sub>OUT</sub> ) | .....1V to 36V       |
| Output current (I <sub>OUT</sub> )           | ..... 7A             |
| Output power (P <sub>OUT</sub> )             | .....140W            |
| Operating junction temp (T <sub>J</sub> )    | .... -40°C to +150°C |

## Thermal Resistance

 $\theta_{JA}$      $\theta_{JC}$ 

|                                 |                          |
|---------------------------------|--------------------------|
| EVQ4263-QVE- 00A <sup>(5)</sup> | .....20.7...2.4...°C/W   |
| QFN-20 (3mmx5mm) <sup>(6)</sup> | .....39.1.....2.5...°C/W |

### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature, T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
- 4) The device is not guaranteed to function outside of its operating conditions. The output power can reach 140W for V<sub>IN</sub> ≥ 19V applications. Thermal derating must be considered for different SWA/SWD selections and PCB size.
- 5) Measured on an EVQ4263-QVE-00A, 4-layer PCB, 64mmx64mm.
- 6) Measured on a JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 5V, T<sub>J</sub> = -40°C to +150°C, typical value is tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                     | Symbol                       | Condition                                                                                  | Min   | Typ   | Max   | Units           |
|---------------------------------------------------------------|------------------------------|--------------------------------------------------------------------------------------------|-------|-------|-------|-----------------|
| Supply current (shutdown)                                     | I <sub>Q_STD</sub>           | V <sub>EN</sub> =0V                                                                        |       | 1     | 10    | μA              |
| Supply current (quiescent)                                    | I <sub>Q1</sub>              | No switching, I <sup>2</sup> C set OPERATION to on, EN on, PFM mode, T <sub>J</sub> = 25°C |       | 775   | 1500  | μA              |
|                                                               | I <sub>Q2</sub>              | I <sup>2</sup> C set OPERATION = off, EN on, T <sub>J</sub> = 25°C                         |       | 135   | 300   | μA              |
| EN rising threshold                                           | V <sub>EN_RISING</sub>       | EN to enable switching                                                                     | -5%   | +1.22 | +5%   | V               |
| EN hysteresis                                                 | V <sub>EN_HYS</sub>          |                                                                                            |       | 200   |       | mV              |
| EN pull-down resistor                                         | R <sub>EN</sub>              | EN = 2V                                                                                    |       | 1.9   | 3     | MΩ              |
| Thermal shutdown <sup>(7)</sup>                               | T <sub>STD</sub>             |                                                                                            |       | 160   |       | °C              |
| Thermal hysteresis <sup>(7)</sup>                             | T <sub>STD_HYS</sub>         |                                                                                            |       | 20    |       | °C              |
| VCC regulator                                                 | V <sub>CC</sub>              |                                                                                            | 4.85  | 5.15  | 5.45  | V               |
| VCC load regulation                                           | V <sub>CC_LOG</sub>          | I <sub>CC</sub> = 50mA                                                                     |       | 2     | 5     | %               |
| VCC power source change threshold                             | V <sub>CC_VTH</sub>          | V <sub>IN</sub> = 12V, ramp V <sub>OUT</sub> from 5V to 10V                                | 6.4   | 6.8   | 7.2   | V               |
| V <sub>CC</sub> under-voltage lockout (UVLO) rising threshold | V <sub>CC_UVLO_R</sub>       |                                                                                            | 3.15  | 3.35  | 3.55  | V               |
| V <sub>CC</sub> UVLO threshold hysteresis                     | V <sub>CC_UVLO_HYS</sub>     |                                                                                            |       | 150   |       | mV              |
| Input voltage (V <sub>IN</sub> ) UVLO falling threshold       | V <sub>UVLO_VIN</sub>        |                                                                                            | 2.35  | 2.56  | 2.75  | V               |
| <b>Buck-Boost Converter</b>                                   |                              |                                                                                            |       |       |       |                 |
| Switch B (SW) on resistance                                   | R <sub>DS_ON_B</sub>         |                                                                                            |       | 20    | 45    | mΩ              |
| Switch C (SWC) on resistance                                  | R <sub>DS_ON_C</sub>         |                                                                                            |       | 14    | 35    | mΩ              |
| Feedback voltage                                              | V <sub>FB1</sub>             |                                                                                            | -3%   | +330  | +3%   | mV              |
|                                                               | V <sub>FB2</sub>             |                                                                                            | -2%   | +500  | +2%   | mV              |
|                                                               | V <sub>FB3</sub>             |                                                                                            | -1.5% | +2    | +1.5% | V               |
| Output absolute over-voltage protection (OVP) rising          | V <sub>OUT_OVP_ABS</sub>     | Trim option 1                                                                              | 24.5  | 26.5  | 28.5  | V               |
|                                                               |                              | Trim option 2                                                                              | 37    | 39    | 41    | V               |
| Output absolute OVP hysteresis                                | V <sub>OUT_OVP_ABS_HYS</sub> | Trim option 1                                                                              |       | 670   |       | mV              |
|                                                               |                              | Trim option 2                                                                              |       | 920   |       | mV              |
| Output OVP rising threshold                                   | V <sub>OUT_OVP_R</sub>       |                                                                                            | 114%  | 120%  | 126%  | V <sub>FB</sub> |
| Output OVP hysteresis                                         | V <sub>OUT_OVP_HYS</sub>     |                                                                                            |       | 10%   |       | V <sub>FB</sub> |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 5V, T<sub>J</sub> = -40°C to +150°C, typical value is tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                          | Symbol                     | Condition                                                                                                             | Min  | Typ   | Max  | Units |
|--------------------------------------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------|------|-------|------|-------|
| Switch leakage                                                     | SW <sub>LKG</sub>          | V <sub>EN</sub> = 0V, V <sub>SW1</sub> = 36V, V <sub>SW2</sub> = 36V, T <sub>J</sub> = 25°C                           |      |       | 1    | μA    |
|                                                                    |                            | V <sub>EN</sub> = 0V, V <sub>SW1</sub> = 36V, V <sub>SW2</sub> = 36V, T <sub>J</sub> = -40°C to +125°C <sup>(7)</sup> |      |       | 15   |       |
| Oscillator frequency                                               | f <sub>SW1</sub>           | T <sub>J</sub> = 25°C                                                                                                 | 220  | 280   | 340  | kHz   |
|                                                                    | f <sub>SW2</sub>           | T <sub>J</sub> = 25°C                                                                                                 | 340  | 420   | 500  |       |
|                                                                    | f <sub>SW3</sub>           | T <sub>J</sub> = 25°C                                                                                                 | 480  | 580   | 680  |       |
| Frequency dithering span                                           | f <sub>SRANGE</sub>        | 2kHz triangle modulation                                                                                              |      | ±8    |      | %     |
| Hiccup off timer <sup>(7)</sup>                                    | t <sub>HICCUP</sub>        | V <sub>REF</sub> = 0.5V                                                                                               |      | 50    |      | ms    |
| Soft-start time                                                    | t <sub>SS</sub>            | Output from 10% to 90%, V <sub>OUT</sub> = 5V, constant slew rate for other V <sub>REF</sub>                          |      | 1     |      | ms    |
| Minimum on time <sup>(7)</sup>                                     | t <sub>ON_MIN_BT</sub>     | Boost SWC                                                                                                             |      | 180   |      | ns    |
| Minimum off time <sup>(7)</sup>                                    | t <sub>OFF_MIN</sub>       | Buck SWB                                                                                                              |      | 180   |      | ns    |
| ISENS over-current (OC) threshold                                  | I <sub>OC1</sub>           | OC threshold = 1A, R <sub>SENS</sub> = 5mΩ, T <sub>J</sub> = -40°C to +125°C                                          | 4.25 | 5     | 5.75 | mV    |
|                                                                    | I <sub>OC2</sub>           | OC threshold = 3A, R <sub>SENS</sub> = 5mΩ, T <sub>J</sub> = -40°C to +125°C                                          | -5%  | +15   | +5%  | mV    |
|                                                                    | I <sub>OC3</sub>           | OC threshold = 5A, R <sub>SENS</sub> = 5mΩ, T <sub>J</sub> = -40°C to +125°C                                          | -5%  | +25   | +5%  | mV    |
| SWB valley limit <sup>(7)</sup>                                    | I <sub>LIMIT2</sub>        | SWB, VALLEY_CL = 01b, T <sub>J</sub> = -40°C to +125°C                                                                |      | 9     |      | A     |
| SWC current limit <sup>(7)</sup>                                   | I <sub>LIMIT3</sub>        | SWC, PEAK_CL = 01b, T <sub>J</sub> = -40°C to +125°C                                                                  |      | 12    |      | A     |
| V <sub>OUT</sub> under-voltage (UV) threshold to enter hiccup mode | V <sub>OUT_UV_HICCUP</sub> |                                                                                                                       | -5%  | +2.93 | +5%  | V     |
| Line drop compensation                                             | V <sub>DROP</sub>          | I <sub>OUT</sub> = 1A                                                                                                 |      | 100   |      | mV    |
| Output discharge resistor                                          | R <sub>DISCHG</sub>        |                                                                                                                       |      | 65    |      | Ω     |
| <b>Mode Transition Threshold</b>                                   |                            |                                                                                                                       |      |       |      |       |
| Buck-boost to buck transition threshold <sup>(7)</sup>             | V <sub>MODE_TH2</sub>      | V <sub>IN</sub> / V <sub>OUT</sub>                                                                                    |      | 120   |      | %     |
| Buck-boost to boost transition threshold <sup>(7)</sup>            | V <sub>MODE_HYS2</sub>     | V <sub>IN</sub> / V <sub>OUT</sub>                                                                                    |      | 82    |      | %     |
| <b>High-Side Gate Driver</b>                                       |                            |                                                                                                                       |      |       |      |       |
| Gate source current capability <sup>(7)</sup>                      | I <sub>DR1H_SRC</sub>      | V <sub>BST-SW</sub> = 5.2V, 4.7nF load                                                                                |      | 0.8   |      | A     |
|                                                                    | I <sub>DR2H_SRC</sub>      | V <sub>BST-SW</sub> = 5.2V, 4.7nF load                                                                                |      | 1.2   |      | A     |
| Gate source resistance                                             | R <sub>DR1H_SRC</sub>      | V <sub>BST-SW</sub> = 5.2V                                                                                            |      | 3     | 5    | Ω     |
|                                                                    | R <sub>DR2H_SRC</sub>      | V <sub>BST-SW</sub> = 5.2V                                                                                            |      | 2     | 3    | Ω     |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 5V, T<sub>J</sub> = -40°C to +150°C, typical value is tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                     | Symbol                        | Condition                              | Min   | Typ   | Max   | Units           |
|---------------------------------------------------------------|-------------------------------|----------------------------------------|-------|-------|-------|-----------------|
| Gate sink current capability <sup>(7)</sup>                   | I <sub>DR1H_SIN</sub>         | V <sub>BST-SW</sub> = 5.2V, 4.7nF load |       | 1.8   |       | A               |
|                                                               | I <sub>DR2H_SIN</sub>         | V <sub>BST-SW</sub> = 5.2V, 4.7nF load |       | 3.3   |       | A               |
| Gate sink resistance                                          | R <sub>DR1H_SIN</sub>         |                                        |       | 1     | 2     | Ω               |
|                                                               | R <sub>DR2H_SIN</sub>         |                                        |       | 1     | 2     | Ω               |
| Dead time of two edges <sup>(7)</sup>                         | t <sub>DLS1_HS1_RISING</sub>  | SWB body diode freewheeling duration   |       | 12    |       | ns              |
|                                                               | t <sub>DHS2_LS2_FALLING</sub> | SWD body diode freewheeling duration   |       | 20    |       | ns              |
| ALT pin leakage                                               | I <sub>ALT_LKG</sub>          | V <sub>ALT</sub> = 5V                  |       | 0.1   |       | μA              |
| ALT pin pull-low resistance                                   | R <sub>ALT</sub>              |                                        |       |       | 20    | Ω               |
| <b>I<sup>2</sup>C Interface Specifications <sup>(7)</sup></b> |                               |                                        |       |       |       |                 |
| Input logic high                                              | V <sub>IH</sub>               |                                        | 1.35  |       |       | V               |
| Input logic low                                               | V <sub>IL</sub>               |                                        |       |       | 0.9   | V               |
| Output voltage logic low                                      | V <sub>OUT_L</sub>            |                                        |       |       | 0.4   | V               |
| SCL clock frequency                                           | f <sub>SCL</sub>              |                                        |       | 400   | 1000  | kHz             |
| SCL high time                                                 | t <sub>HIGH</sub>             |                                        | 60    |       |       | ns              |
| SCL low time                                                  | t <sub>LOW</sub>              |                                        | 160   |       |       | ns              |
| Data set-up time                                              | t <sub>SU_DAT</sub>           |                                        | 10    |       |       | ns              |
| Data hold time                                                | t <sub>HD_DAT</sub>           |                                        | 0     | 60    |       | ns              |
| Set-up time for (repeated) start command                      | t <sub>SU_STA</sub>           |                                        | 160   |       |       | ns              |
| Hold time for (repeated) start command                        | t <sub>HD_STA</sub>           |                                        | 160   |       |       | ns              |
| Bus free time between a start and a stop command              | t <sub>BUF</sub>              |                                        | 160   |       |       | ns              |
| Set-up time for stop command                                  | t <sub>SU_STO</sub>           |                                        | 160   |       |       | ns              |
| Rising time for SCL and SDA                                   | t <sub>R</sub>                |                                        | 10    |       | 300   | ns              |
| Falling time for SCL and SDA                                  | t <sub>F</sub>                |                                        | 10    |       | 300   | ns              |
| Pulse width of suppressed spike                               | t <sub>SP</sub>               |                                        | 0     |       | 50    | ns              |
| Capacitance for each bus line                                 | C <sub>B</sub>                |                                        |       |       | 400   | pF              |
| <b>Power Good (PG) Indication</b>                             |                               |                                        |       |       |       |                 |
| PG lower rising threshold                                     | V <sub>PG_R_L</sub>           | PG switches high                       | 88.5% | 93%   | 98.5% | V <sub>FB</sub> |
| PG lower falling threshold                                    | V <sub>PG_F_L</sub>           | PG switches low                        | 77%   | 82.5% | 88%   | V <sub>FB</sub> |
| PG upper rising threshold                                     | V <sub>PG_R_H</sub>           | PG switches low                        | 115%  | 120%  | 126%  | V <sub>FB</sub> |
| PG upper falling threshold                                    | V <sub>PG_F_H</sub>           | PG switches high                       | 105%  | 110%  | 115%  | V <sub>FB</sub> |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 5V, T<sub>J</sub> = -40°C to +150° C, typical value is tested at T<sub>J</sub> = 25°C, unless otherwise noted.

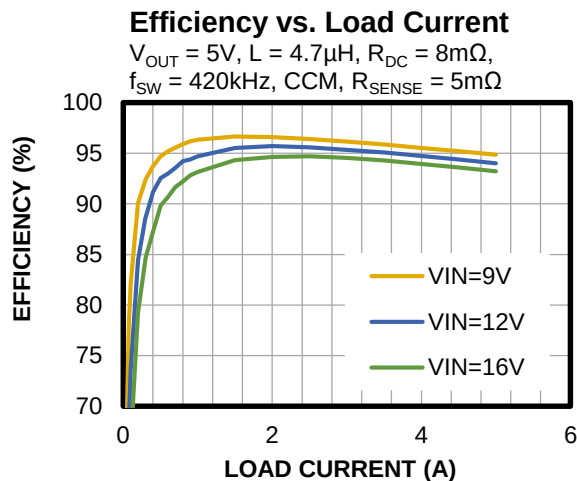
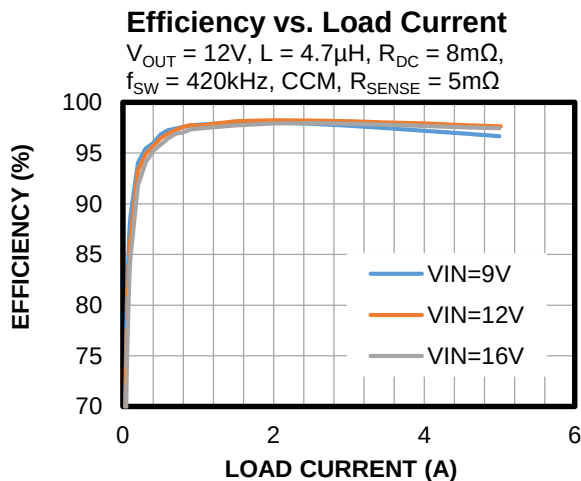
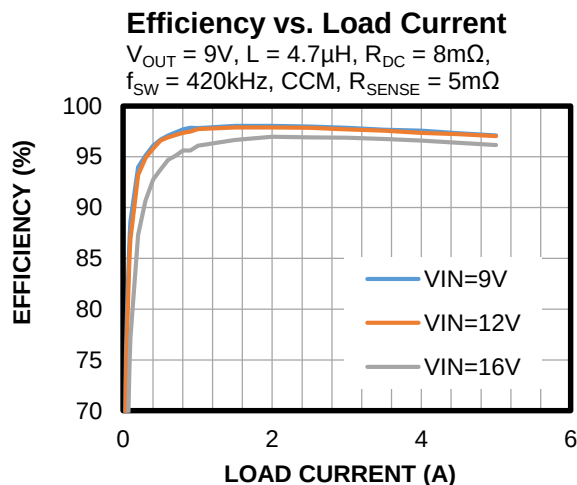
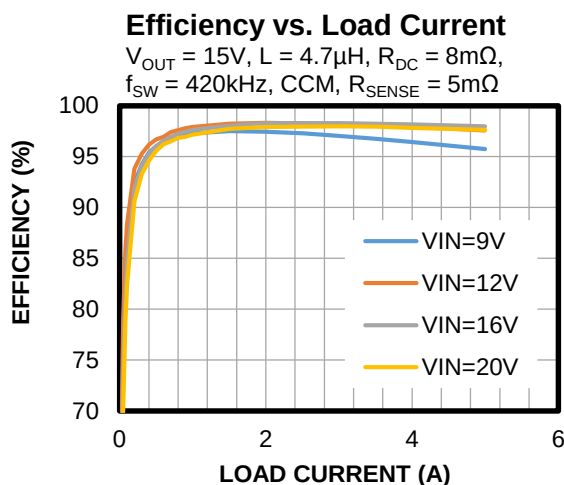
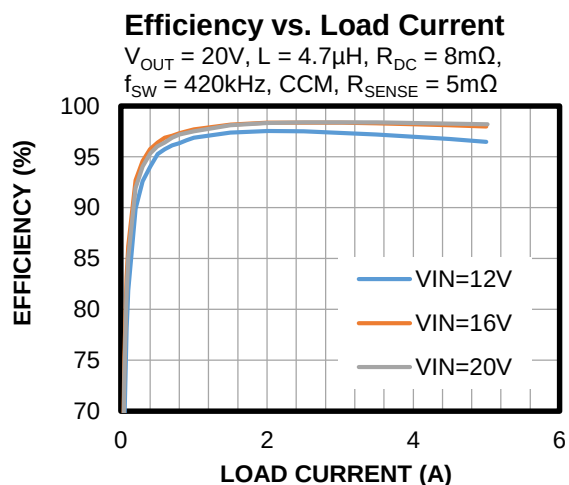
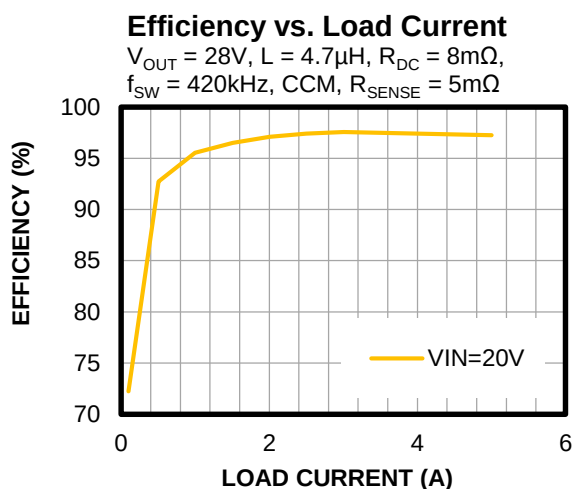
| Parameter                       | Symbol             | Condition                                                                                | Min | Typ | Max | Units |
|---------------------------------|--------------------|------------------------------------------------------------------------------------------|-----|-----|-----|-------|
| <b>Current Monitor Function</b> |                    |                                                                                          |     |     |     |       |
| IMON output voltage gain        | G <sub>IMON1</sub> | I <sup>2</sup> C set R <sub>SENS</sub> = 5mΩ, 25mV sense voltage, T <sub>J</sub> = 25°C  | -3% | +68 | +3% | V/V   |
| IMON output voltage gain        | G <sub>IMON2</sub> | I <sup>2</sup> C set R <sub>SENS</sub> = 10mΩ, 50mV sense voltage, T <sub>J</sub> = 25°C | -3% | +34 | +3% | V/V   |

**Note:**

7) Guaranteed by characterization.

# TYPICAL CHARACTERISTICS

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

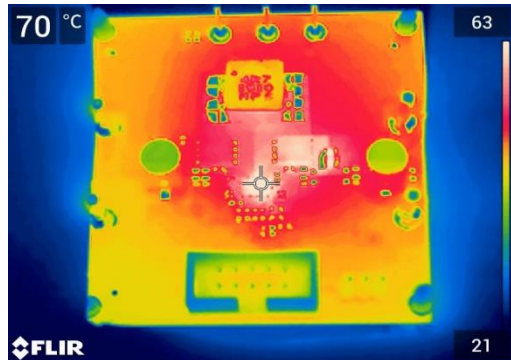


## TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{SW} = 420kHz$ , forced PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

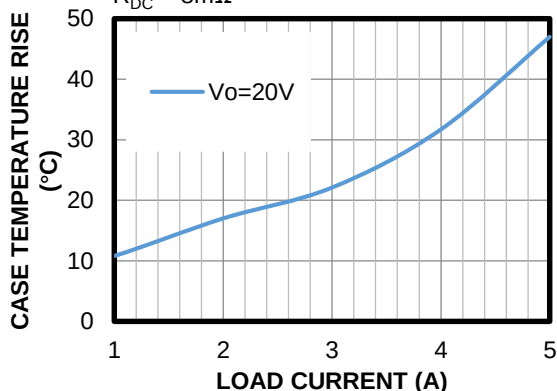
### Case Temperature

$V_{IN} = 20V$ ,  $V_{OUT} = 28V$ ,  $I_{OUT} = 5A$



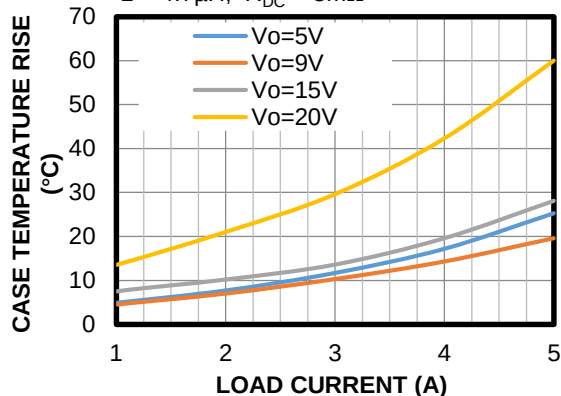
### Case Temperature Rise

$V_{IN} = 12V$ ,  $V_{OUT} = 20V$ ,  $f_{SW} = 280kHz$ , based on 6cmx6cm board,  $L = 6.8\mu H$ ,  $R_{DC} = 8m\Omega$



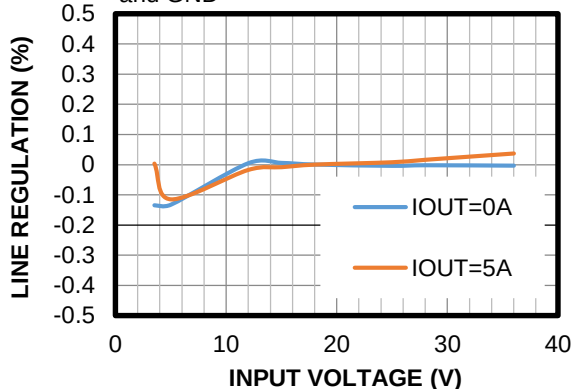
### Case Temperature Rise

$V_{IN} = 12V$ ,  $V_{OUT} = 5V/9V/15V/20V$ ,  $f_{SW} = 420kHz$ , based on 6cmx6cm board,  $L = 4.7\mu H$ ,  $R_{DC} = 8m\Omega$



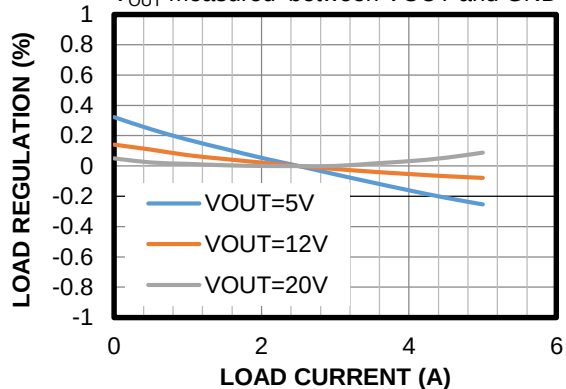
### Line Regulation

$V_{OUT} = 5V$ ,  $V_{OUT}$  measured between VOUT and GND

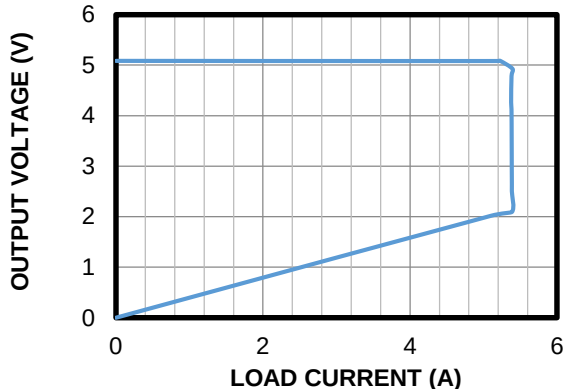


### Load Regulation

$R_{SENSE} = 5m\Omega$ , no line drop compensation,  $V_{OUT}$  measured between VOUT and GND

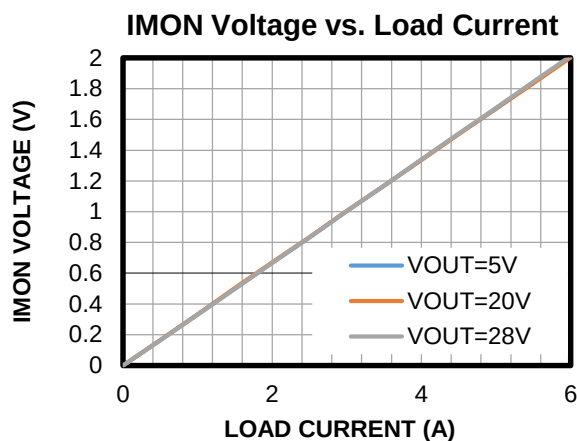
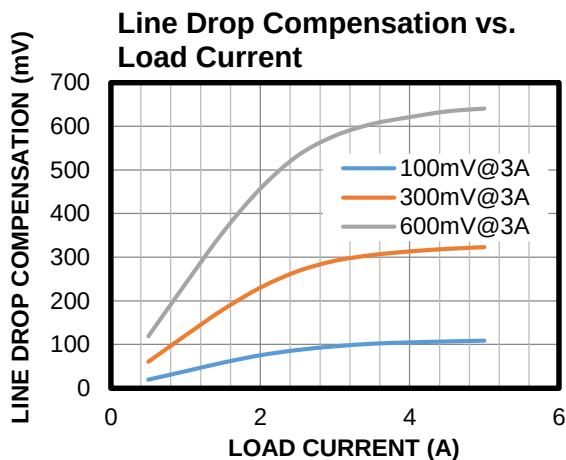
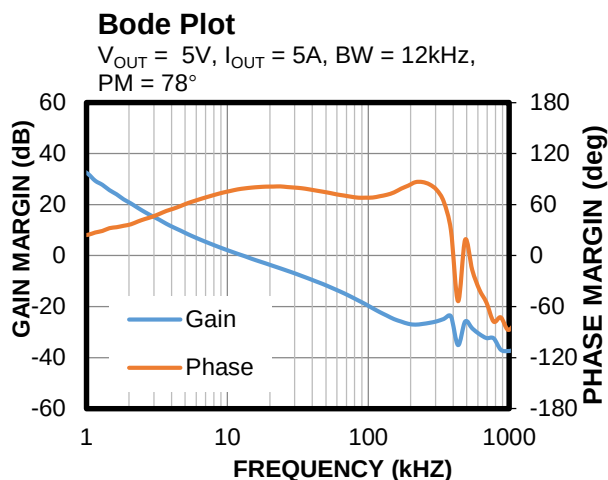
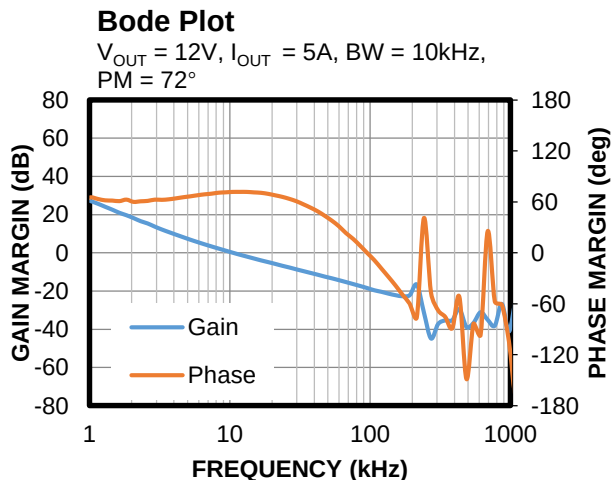
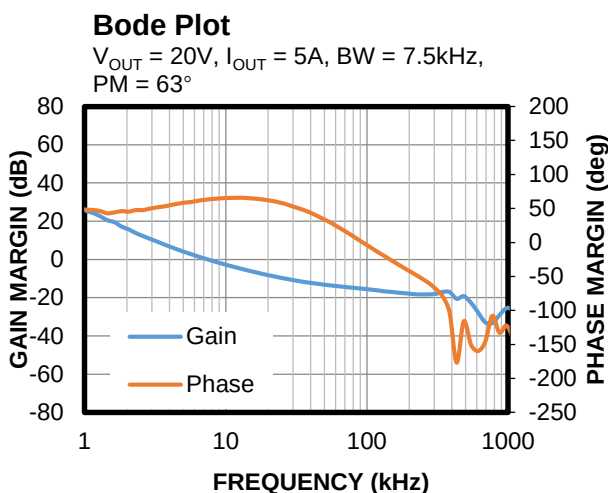


### CC/CV Curve



## TYPICAL CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

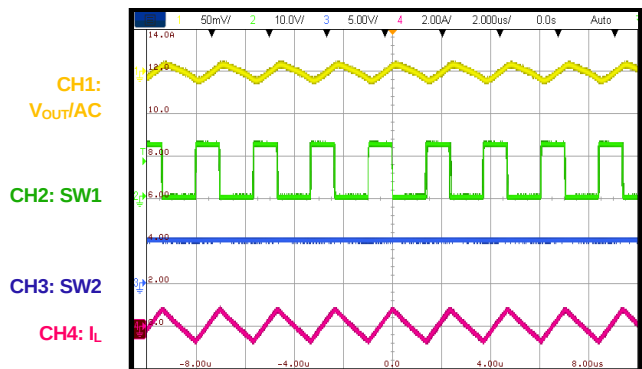


# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $f_{SW} = 420kHz$ , forced PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

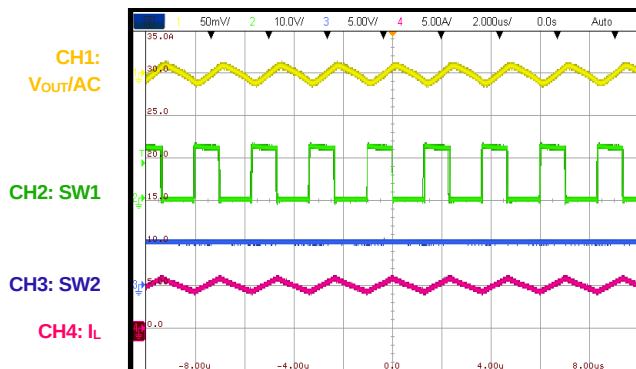
## Output Voltage Ripple

$V_{OUT} = 5V$ , load = 0A



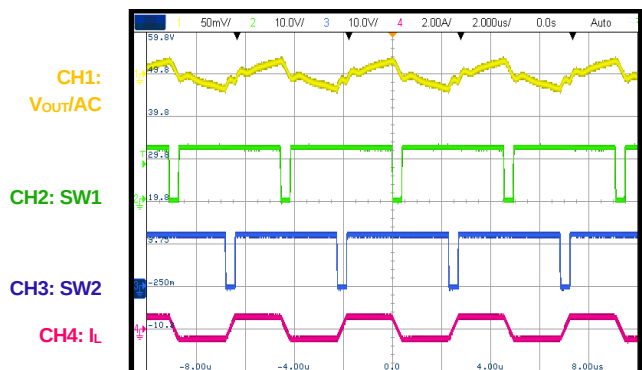
## Output Voltage Ripple

$V_{OUT} = 5V$ , load = 5A



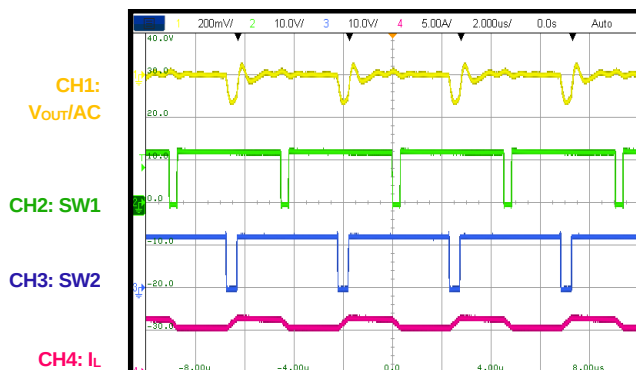
## Output Voltage Ripple

$V_{OUT} = 12V$ , load = 0A,  $f_{SW}$  reduced to half its value in buck-boost mode



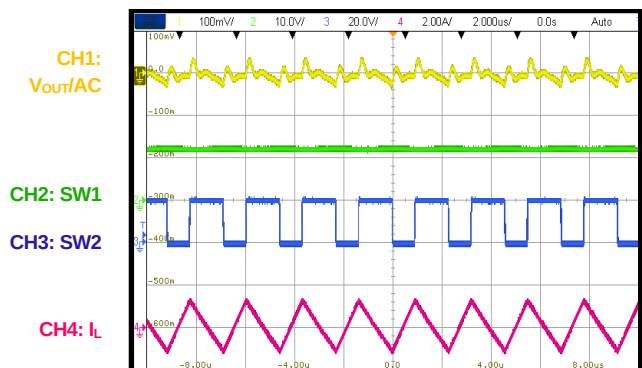
## Output Voltage Ripple

$V_{OUT} = 12V$ , load = 5A,  $f_{SW}$  reduced to half its value in buck-boost mode



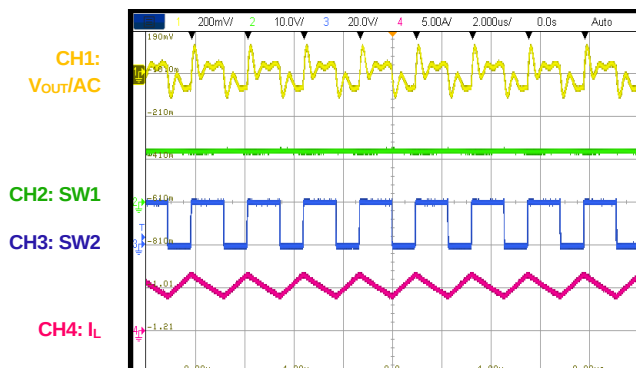
## Output Voltage Ripple

$V_{OUT} = 20V$ , load = 0A



## Output Voltage Ripple

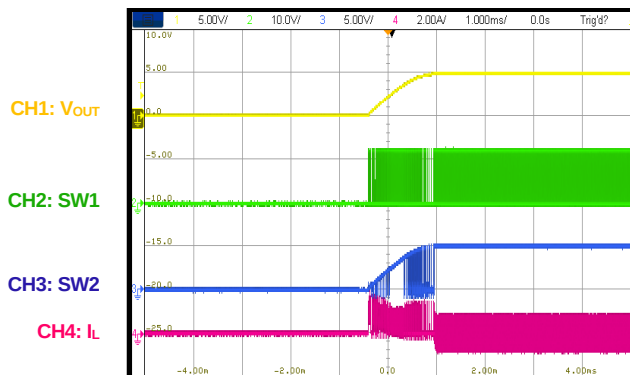
$V_{OUT} = 20V$ , load = 3A



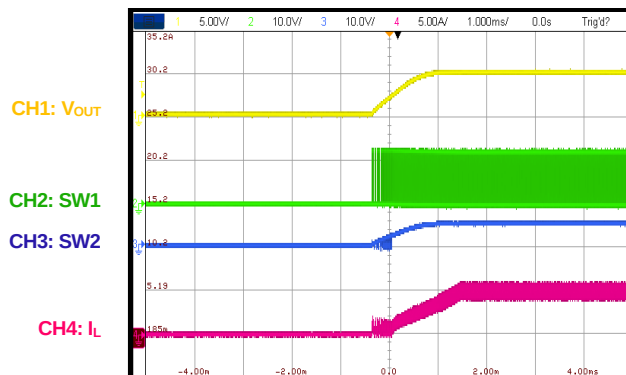
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

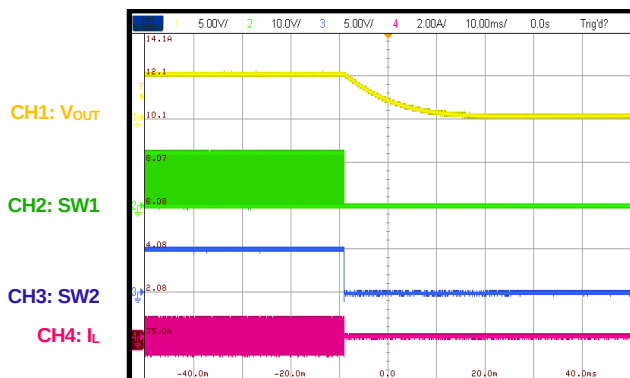
**I<sup>2</sup>C Operation On**  
Load = 0A



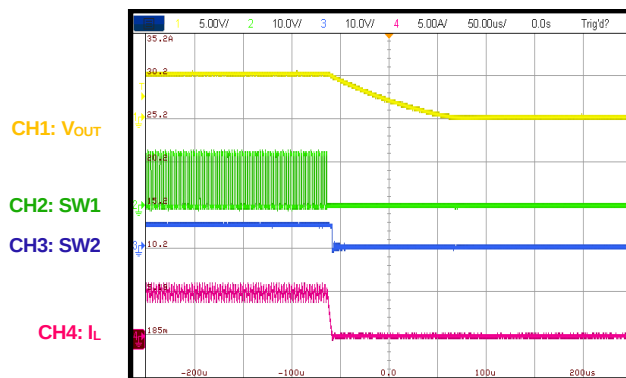
**I<sup>2</sup>C Operation On**  
Load = 5A



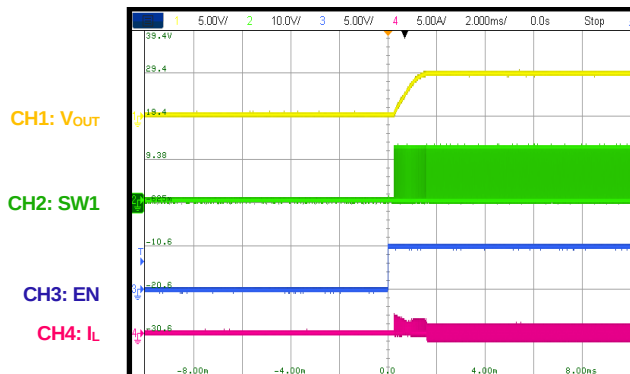
**I<sup>2</sup>C Operation Off**  
Load = 0A



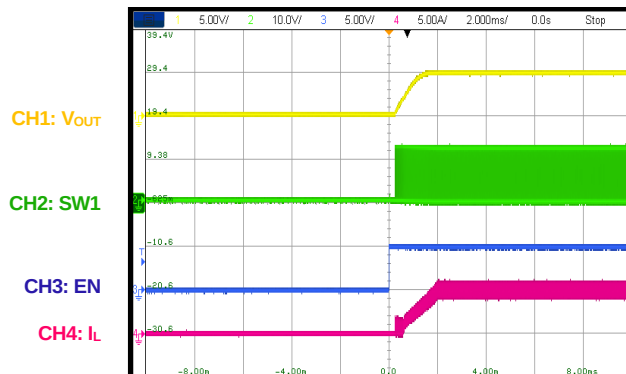
**I<sup>2</sup>C Operation Off**  
Load = 5A



**EN Pin Enabled**  
Load = 0A



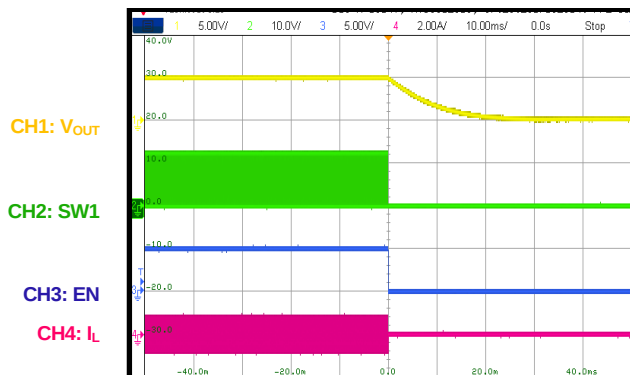
**EN Pin Enabled**  
Load = 5A



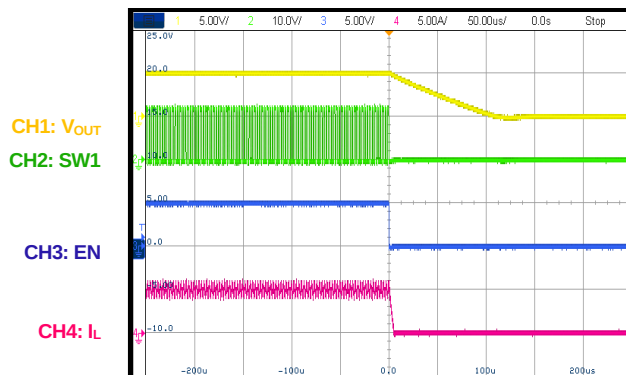
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

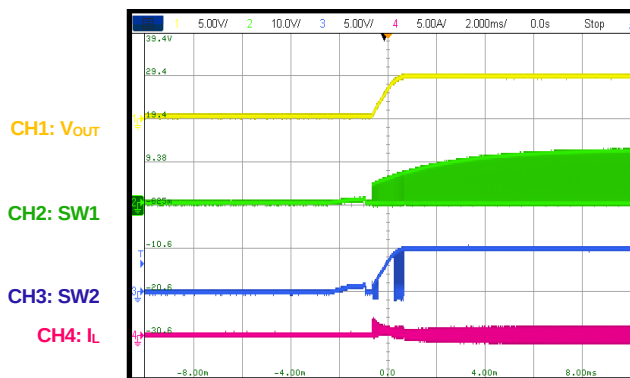
**EN Pin Disabled**  
Load = 0A



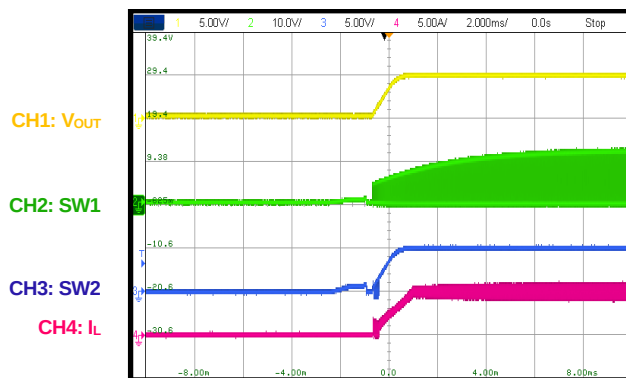
**EN Pin Disabled**  
Load = 5A



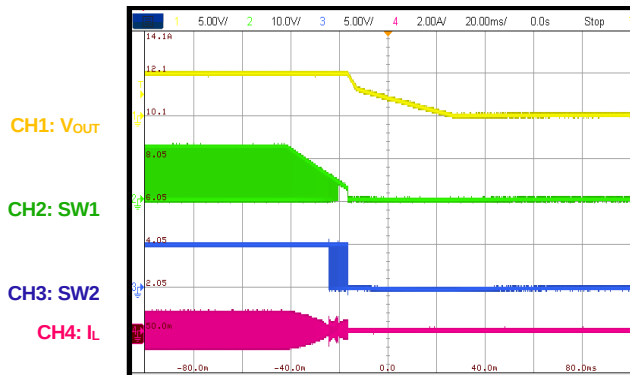
**Start-Up through VIN**  
Load = 0A



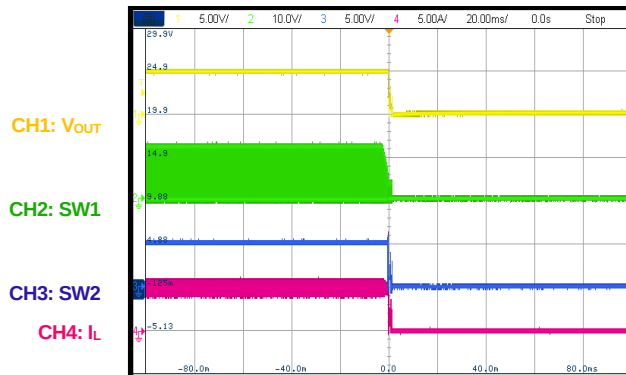
**Start-Up through VIN**  
Load = 5A



**Shutdown through VIN**  
Load = 10mA



**Shutdown through VIN**  
Load = 5A

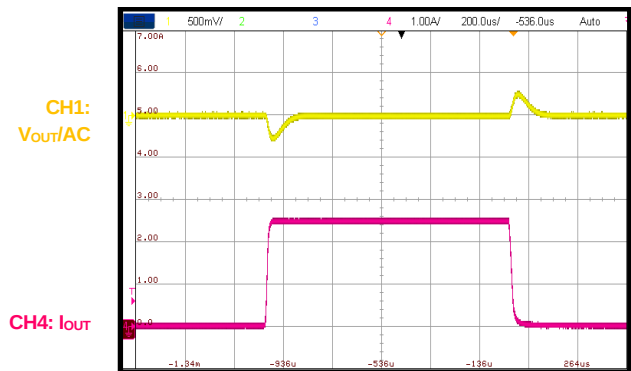


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

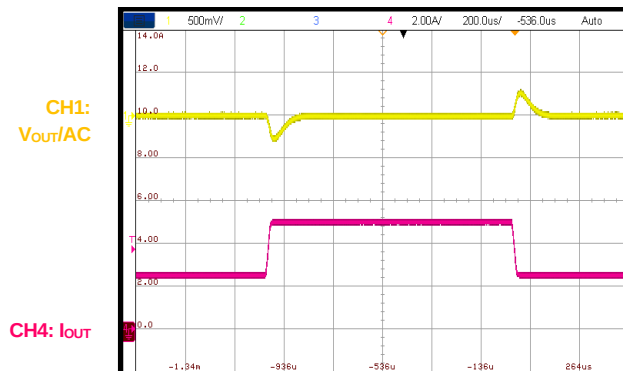
## Load Transient Response

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, I<sub>OUT</sub> = 0A to 2.5A, 150mA/μs



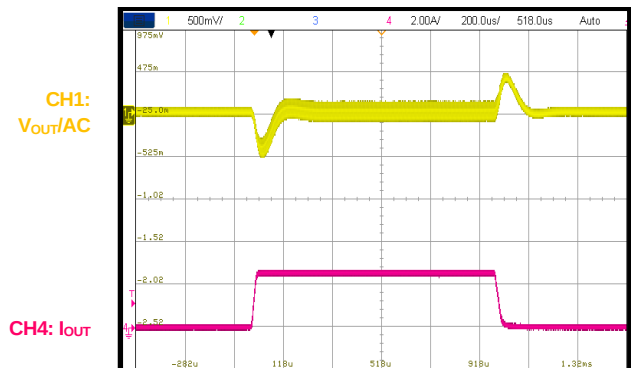
## Load Transient Response

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, I<sub>OUT</sub> = 2.5A to 5A, 150mA/μs



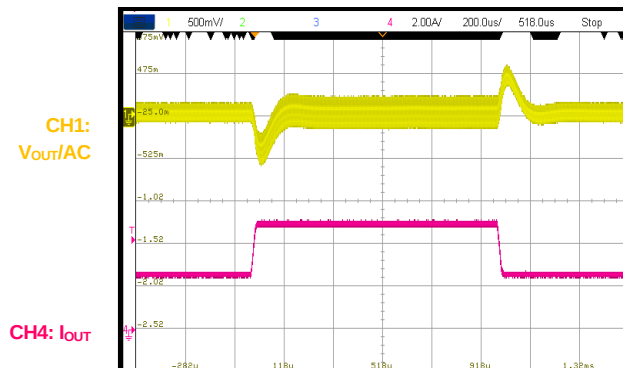
## Load Transient Response

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 20V, I<sub>OUT</sub> = 0A to 2.5A, 150mA/μs



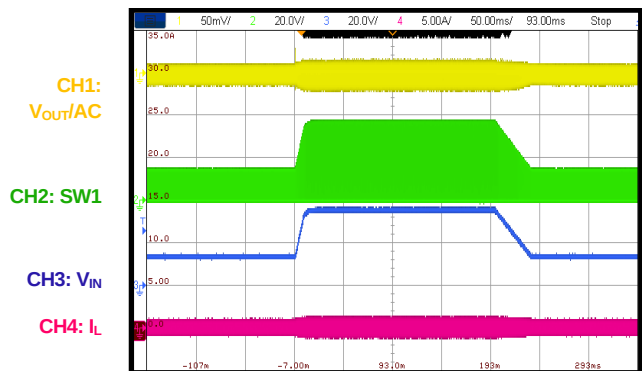
## Load Transient Response

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 20V, I<sub>OUT</sub> = 2.5A to 5A, 150mA/μs



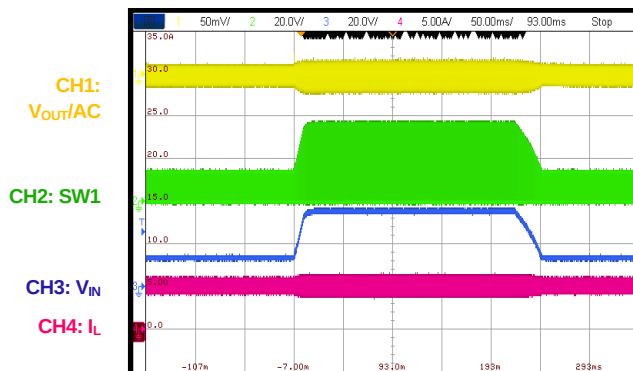
## Input Voltage Transient Response

V<sub>IN</sub> = 14V to 35V, V<sub>OUT</sub> = 5V, load = 0A



## Input Voltage Transient Response

V<sub>IN</sub> = 14V to 35V, V<sub>OUT</sub> = 5V, load = 5A

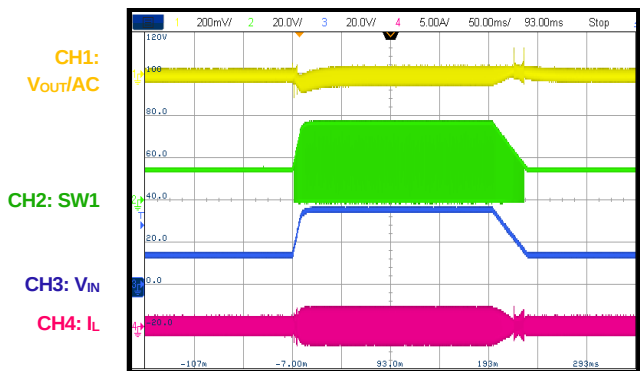


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

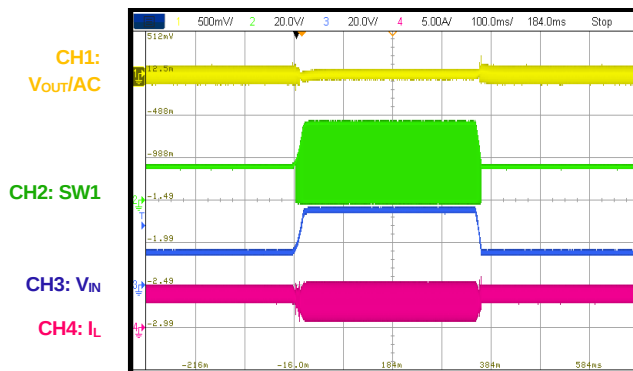
## Input Voltage Transient Response

V<sub>IN</sub> = 14V to 35V, V<sub>OUT</sub> = 20V, load = 0A



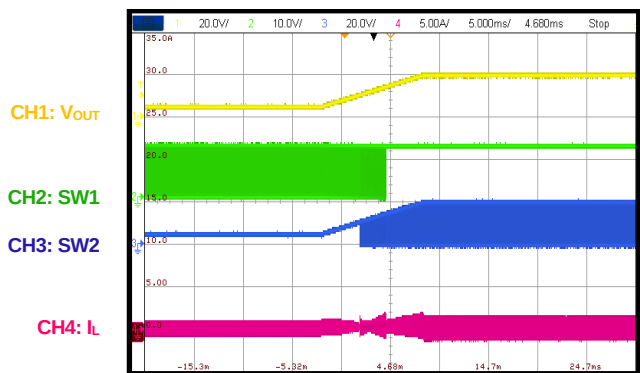
## Input Voltage Transient Response

V<sub>IN</sub> = 14V to 35V, V<sub>OUT</sub> = 20V, load = 3A



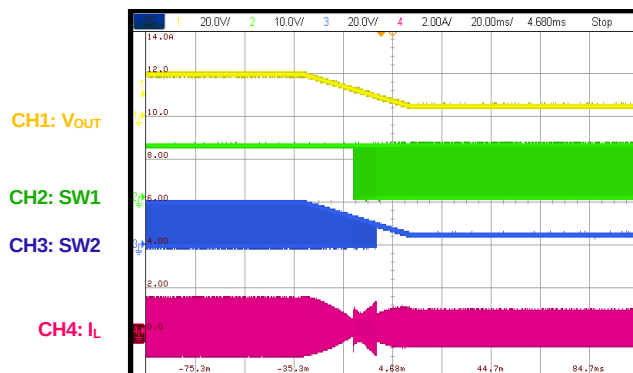
## Output Voltage Transition

V<sub>OUT</sub> = 5V to 20V, I<sub>OUT</sub> = 0A



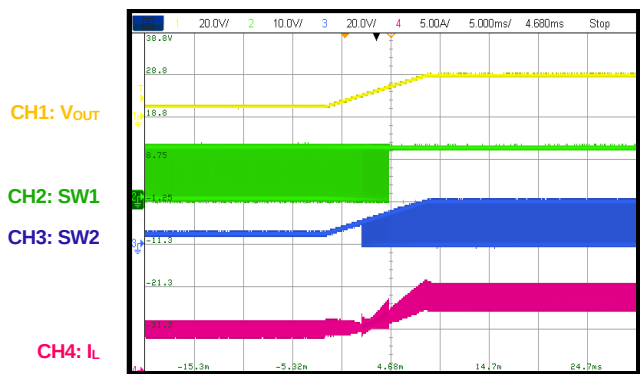
## Output Voltage Transition

V<sub>OUT</sub> = 20V to 5V, I<sub>OUT</sub> = 0A



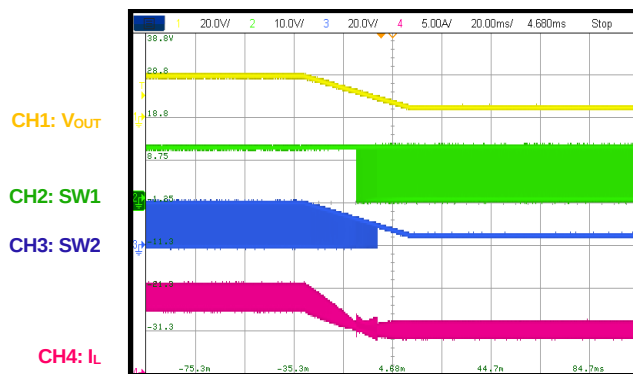
## Output Voltage Transition

V<sub>OUT</sub> = 5V to 20V, I<sub>OUT</sub> = 3A



## Output Voltage Transition

V<sub>OUT</sub> = 20V to 5V, I<sub>OUT</sub> = 3A

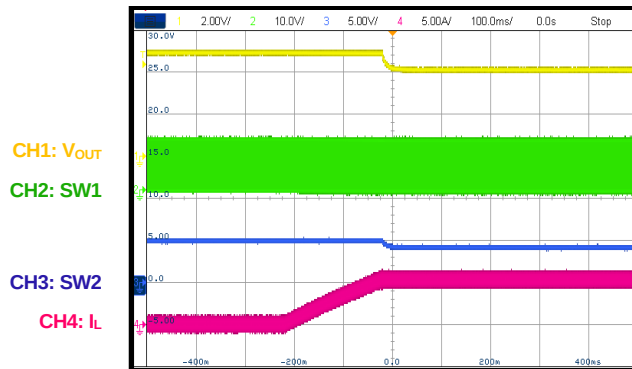


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, f<sub>SW</sub> = 420kHz, forced PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.

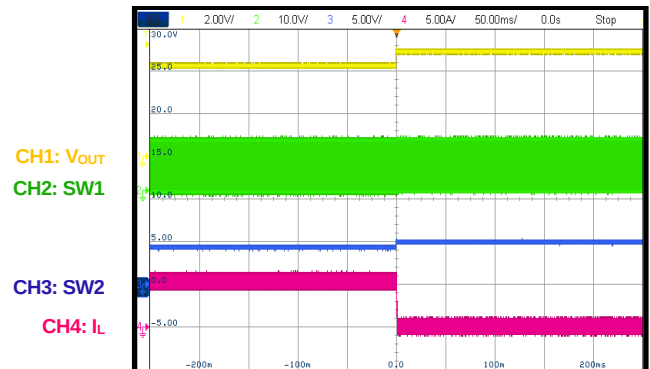
## CC Entry

CV load = 4V, CC limit = 5.4A

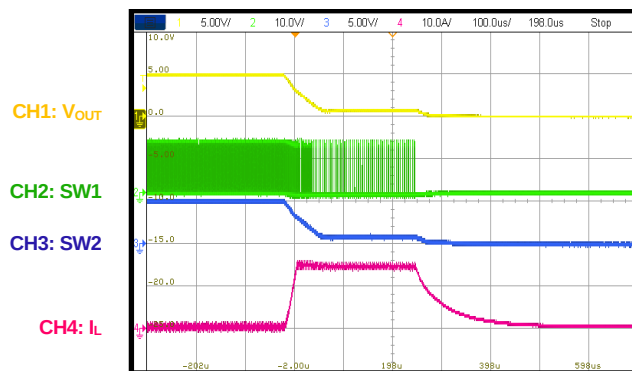


## CC Recovery

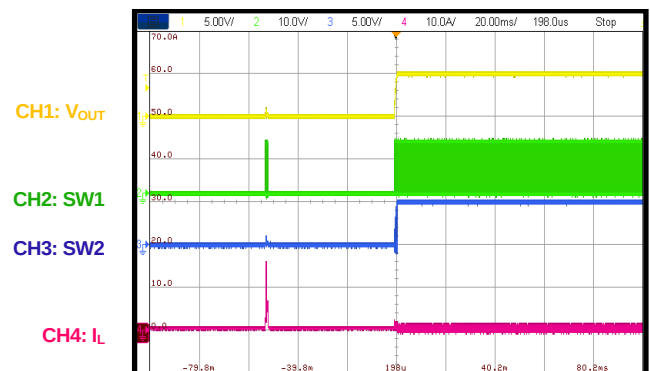
CV load = 4V, CC limit = 5.4A



## Short-Circuit Protection Entry



## Short-Circuit Protection Recovery



# FUNCTIONAL BLOCK DIAGRAM

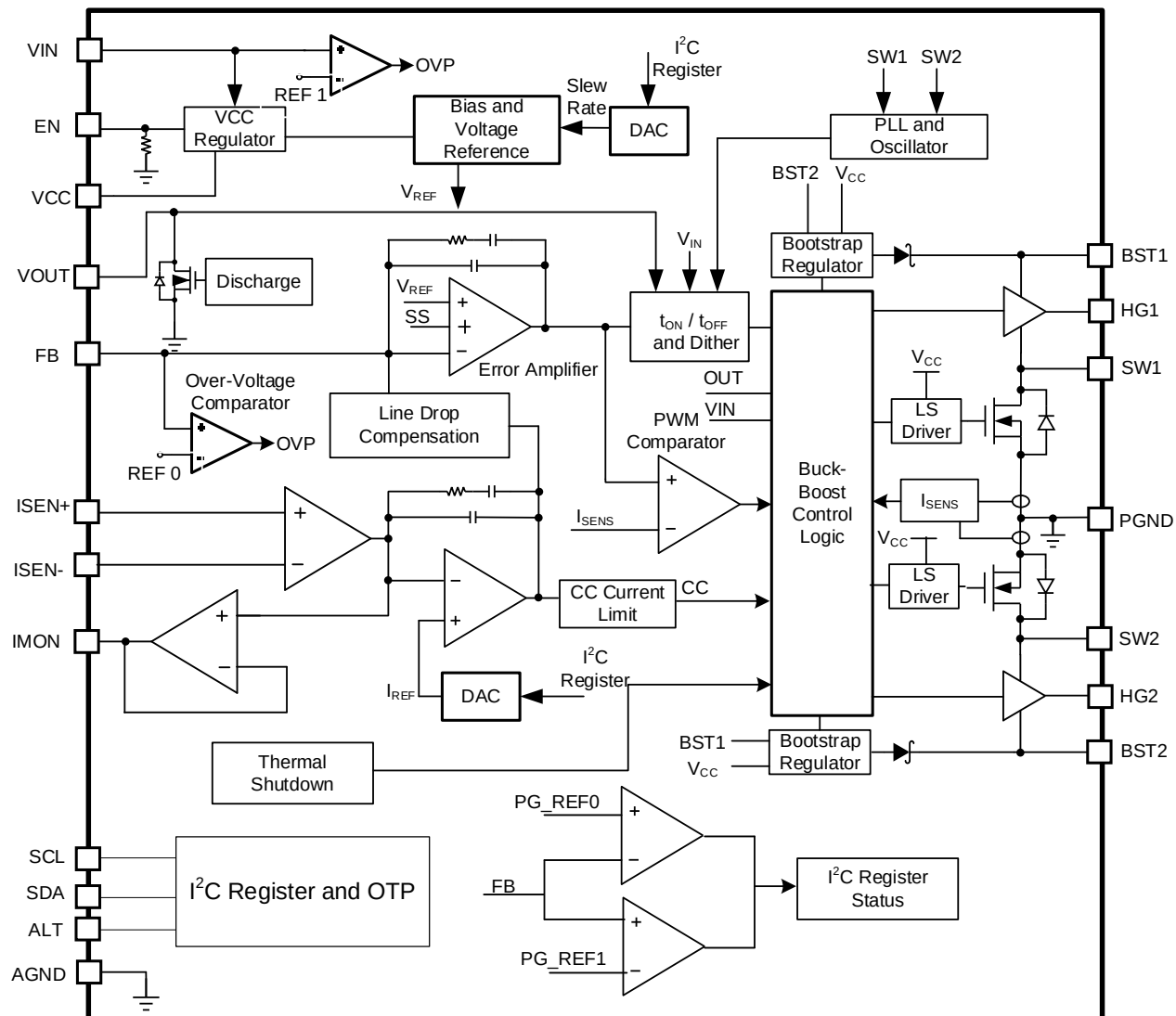


Figure 2: Functional Block Diagram

## OPERATION

The MPQ4263 is a buck-boost converter with integrated low-side MOSFETs (LS-FETs). The device works with a fixed frequency for buck, boost, and buck-boost mode. A special buck-boost control strategy provides high efficiency across the full input range and smooths the transient response between different modes. Figure 2 on page 20 shows the internal block diagram.

### Buck-Boost Operation

The MPQ4263 can regulate the output voltage ( $V_{OUT}$ ) to be above, below, or equal to the input voltage ( $V_{IN}$ ). Figure 3 shows a buck-boost power structure with one inductor and four switches (SWA, SWB, SWC, and SWD).

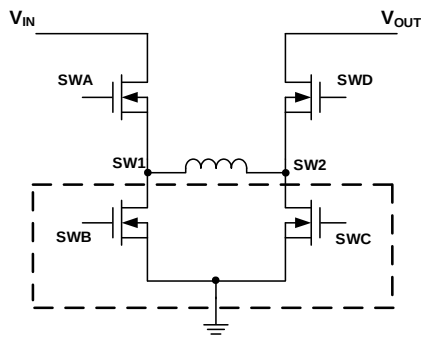


**Figure 3: Buck-Boost Topology**

Buck mode, boost mode, and buck-boost mode can have different  $V_{IN}$  inputs (see Figure 4).

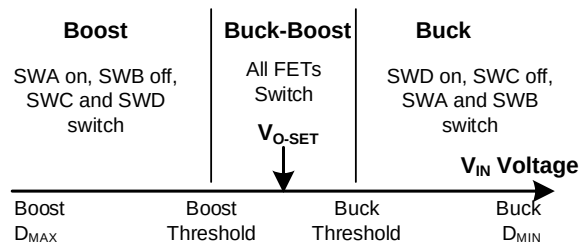


**Figure 4: Buck-Boost Operation Range**

### Buck Mode ( $V_{IN} > V_{OUT}$ )

When  $V_{IN}$  exceeds  $V_{OUT}$ , the MPQ4263 works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Meanwhile, switch C (SWC) is off, and switch D (SWD) stays on to conduct the inductor current ( $I_L$ ).

In each buck mode cycle, SWA turns on first when the FB voltage ( $V_{FB}$ ) drops below the reference voltage ( $V_{REF}$ ). After SWA turns off, SWB turns on to conduct  $I_L$  until it triggers the

COMP control signal. By repeating this operation, the converter regulates  $V_{OUT}$ .

### Boost Mode ( $V_{IN} < V_{OUT}$ )

When  $V_{IN}$  is below  $V_{OUT}$ , the MPQ4263 works in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off and SWA stays on to conduct the inductor current.

In each boost mode cycle, SWC turns on to conduct  $I_L$ . When  $I_L$  rises and triggers the control signal on the COMP pin, SWC turns off and SWD turns on for the current freewheeling period. Then SWC turns on and off repeatedly to regulate  $V_{OUT}$  in boost mode.

### Buck-Boost Mode ( $V_{IN} \approx V_{OUT}$ )

When  $V_{IN}$  is almost equal to  $V_{OUT}$ , the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MPQ4263 adopts buck-boost control to regulate the output (see Figure 5).

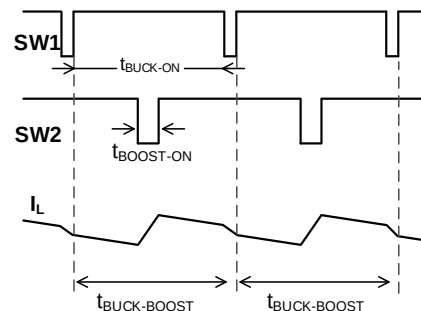


**Figure 5: Buck-Boost Waveform**

If  $V_{IN}$  is almost equal to  $V_{OUT}$ , buck-boost mode activates. One boost switching period is inserted into each buck switching period. The MOSFET turn-on sequence is as follows:

1. SWA and SWD
2. SWA and SWC
3. SWA and SWD
4. SWB and SWD

Throughout this process,  $I_L$  can reach the COMP voltage requirement, and supply enough current to the output.

## Mode Selection

The MPQ4263 works with a fixed frequency under heavy-load conditions. When the load current decreases, the MPQ4263 can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

### Forced Continuous Conduction Mode (FCCM) or Forced Pulse-Width Modulation (PWM) Mode

In forced continuous condition mode (FCCM), the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the  $V_{IN} / V_{OUT}$  ratio. When the load decreases, the average input current drops, and  $I_L$  may go negative from  $V_{OUT}$  to  $V_{IN}$  during the off time (while SWD is on). This forces the inductor current to work in continuous conduction mode (CCM) with a fixed frequency, producing a lower output voltage ripple than in PSM mode.

### Pulse-Skip Mode (PSM) and Automatic Pulse-Frequency Modulation (PFM)/PWM Mode

In power-save mode (PSM), once  $I_L$  drops to 0A, SWD turns off to prevent the current from flowing from the output to GND, forcing  $I_L$  to work in discontinuous conduction mode (DCM). Simultaneously, the internal off time clock becomes longer once the MPQ4263 enters DCM. The frequency drops when the inductor current conduction period decreases, which reduces power loss and the output voltage ripple.

If  $V_{COMP}$  drops to the PSM threshold, the MPQ4263 stops switching to reduce switching power loss. The MPQ4263 starts switching once  $V_{COMP}$  rises above the PSM threshold. The switching pulse skips are based on  $V_{COMP}$  under light-load conditions. PSM has a much higher efficiency than FCCM under light-load conditions, but the output voltage ripple may be higher due to the group switching pulse.

## Power Supply

The MPQ4263's internal circuit is powered by VCC, including the gate drivers. When  $V_{IN}$  is supplied power and EN is high, the MPQ4263 tries to regulate  $V_{CC}$  at 5V.  $V_{CC}$  and BST have separate under-voltage lockout (UVLO) thresholds that keep the gate signal off.

Both VCC and BST should have sufficient voltages to enable MPQ4263 switching.

If  $V_{IN}$  and  $V_{OUT}$  both exceed 6.8V, the MPQ4263 powers VCC from the lower voltage source between  $V_{OUT}$  or  $V_{IN}$  to reduce power loss. Otherwise, the MPQ4263 powers VCC from the higher voltage power source between  $V_{IN}$  and  $V_{OUT}$  to ensure there is sufficient VCC voltage ( $V_{CC}$ ).

## Enable (EN) Control

The MPQ4263 has an enable (EN) control pin. Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

The EN pin is a high-voltage pin that can be connected to  $V_{IN}$  directly or through a resistor. An EN resistor divider can determine  $V_{IN}$ 's on and off thresholds (see Figure 6).

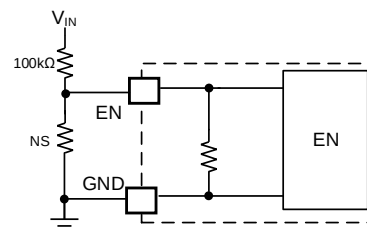


**Figure 6: EN Connection**

It is recommended to add an EN resistor divider to set the  $V_{IN}$  shutdown threshold voltage above 4V, which can prevent the input current from becoming too high during input shutdown in boost mode. If the operating  $V_{IN}$  is always below 4V, connect  $V_{IN}$  directly to EN.

## Under-Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input and  $V_{CC}$ . The MPQ4263 is enabled when  $V_{IN}$  and  $V_{CC}$  exceed their rising UVLO threshold. The MPQ4263 stops working when either  $V_{IN}$  or  $V_{CC}$  fall below their UVLO falling threshold.

The default  $V_{IN}$  UVLO rising threshold is 3.3V, and its falling threshold is 2.56V. The rising and falling thresholds can be OTP-trimmed to 5.5V and 3.3V.

## Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When

the chip starts up, the internal circuitry generates an SS voltage ( $V_{SS}$ ) that ramps up from 0V to 5V. When  $V_{SS}$  is below the reference voltage ( $V_{REF}$ ), the error amplifier uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ , the error amplifier uses  $V_{REF}$  as the reference.

If the output of the MPQ4263 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FETs and LS-FETs until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

### CC Mode Over-Current-Protection (OCP)

The MPQ4263 senses the ground current via the ISEN+ and ISEN- pins. If the output current ( $I_{OUT}$ ) exceeds the set current limit threshold, the MPQ4263 enters constant current limit mode (CC mode). In CC mode, the current amplitude is limited. After the load resistance is reduced,  $V_{OUT}$  drops, and  $V_{FB}$  falls below the under-voltage (UV) threshold (about 40% below  $V_{REF}$ ).

If a UV condition is triggered and  $V_{OUT}$  is below 2.93V, the MPQ4263 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4263 exits hiccup mode once the OC condition is removed. The average output current limit can be disabled by setting  $CC\_DISABLE = 1$ .

The MPQ4263 supports a high-side (HS) current sense in CC mode.

### Switching Current Limit

The MPQ4263 senses the LS-FET current in loop control, then provides the valley current limit in buck mode, as well as the peak current limit in boost mode for each cycle-by-cycle switch. In buck mode, the next period does not start before  $I_L$  drops to the valley current limit. This folds back the frequency when the valley current limit is triggered.

Based on the cycle-by-cycle switching current limit, the MPQ4263's maximum input current in buck mode can be calculated with Equation (1):

$$I_{INMAX}(A) = \frac{V_{OUT}}{V_{IN}} \times \eta \times (\text{ValleyCurrentLimit}(A)) + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3 \quad (1)$$

Where  $\eta$  is the efficiency. The maximum input current in boost mode can be estimated with Equation (2):

$$I_{INMAX}(A) = \text{PeakCurrentLimit}(A) - \frac{V_{IN}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3 \quad (2)$$

Typically, the buck valley current limit is 13A, while the boost peak current limit is 15A. These limits can be configured via the I<sup>2</sup>C register (0xD3, bits D[7:6]).

### Output Over-Voltage Protection (OVP)

The MPQ4263 features output over-voltage protection (OVP). If  $V_{OUT}$  exceeds 120% of  $V_{REF}$ , the switches (SWA, SWB, SWC, and SWD) turn off. There is a resistor discharge path from the OUT pin to ground that turns on. When the FB voltage drops to 110% of  $V_{REF}$ , the chip resumes operation.

The default absolute output OVP threshold is about 39V, and the discharge resistor turns on when absolute OVP is triggered.

Set  $OUTPUT\_OVP\_EN = 0$  to disable OVP and absolute OVP.

The absolute output OVP threshold can be trimmed to 26.5V via the OTP.

### Gate Driver and BST Power

The MPQ4263 provides 2 N-channel MOSFET gate drivers for the H-bridge MOSFETs. Each driver is capable of sourcing and sinking current. In buck mode, HG1 switches while HG2 stays on. In boost mode, HG2 switches while HG1 stays on. HG1 and HG2 are powered by the power from BST1 and BST2.

The capacitors placed between BST1 and SW1, then BST2 and SW2 are necessary to supply the power, which is powered by internal diode from VCC.

The BST power has its own UVLO control. Its UVLO rising threshold is about 2.7V, with a hysteresis of about 200mV.

### Switching Frequency ( $f_{SW}$ ) and Frequency Spread Spectrum (FSS) Function

The switching frequency ( $f_{SW}$ ) can be configured via the 2-bit FREQ register. The frequency can be 280kHz, 420kHz or 580kHz. Typically, a 420kHz switching frequency is recommended.

The MPQ4263 has a frequency spread spectrum (FSS) function. Set the DITHER\_ENABLE (0xD0, D[7]) = 1 to enable this function. Set the DITHER\_ENABLE = 0 to disable the function. The purpose of the spread spectrum is to minimize the peak emissions at certain frequencies.

The MPQ4263 uses a 2kHz triangle wave to modulate the internal oscillator. The frequency span for spread spectrum operation is  $\pm 8\%$ .

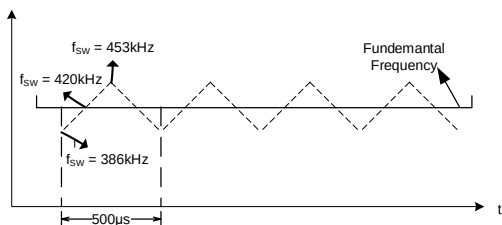


**Figure 7: Frequency Spread Spectrum**

The MPQ4263's FSS function can be enabled for a 280kHz, 420kHz, or 580kHz  $f_{SW}$ .

### Start-Up and Shutdown

If both  $V_{IN}$  and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low,  $V_{IN}$  going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

The power stage turns off after EN pulls low, but the digital circuit does not turn off immediately, according to the set-up of the discharge bit. If output discharge is enabled (OUTPUT\_DISCHARGE\_EN = 1), it is recommended to add a 300ms delay after EN pulls low to ensure that the system is fully discharged and successfully shuts down. If the output discharge is disabled (OUTPUT\_DISCHARGE\_EN = 0), a 5ms delay is recommended after EN pulls low to ensure that the chip fully shuts down. After re-enabling the chip, a 5ms delay is recommended before operating the I<sup>2</sup>C registers.

### Control and Output Discharge

The MPQ4263 sets the  $V_{OUT}$  slew rate via the SR bits (0xD3, bits D[4:3] set the rising slew rate, while bits D[2:1] set the falling slew rate). Four  $V_{REF}$  slew rates (rising and falling) can be selected under different application requirements.

If  $V_{OUT}$  has not been discharged to the target voltage when  $V_{REF}$  finishes changing due to a large output capacitance, the OVP discharge function can be used to continue discharging the output capacitor ( $C_{OUT}$ ).

The output discharge function is enabled under the following conditions:

1. The output OVP threshold (120% of  $V_{FB}$ ) or absolute OVP threshold is triggered.
2. The I<sup>2</sup>C OPERATION bit is commanded off or the EN pin turns off. Discharge works until the 200ms delay passes.
3. If  $V_{IN}$  UVLO is triggered, but  $V_{CC}$  has residual voltage, the MPQ4263 discharges for a limited time. This discharge function is disabled after  $V_{CC}$  drops below 1.8V.

### Output Line Drop Compensation

The MPQ4263 can compensate for an output voltage drop (e.g. high impedance caused by a long trace) to keep a fairly constant load-side voltage.

See the MFR\_CTRL2 (D2h) section on page 33 for a description of the line drop compensation amplitude.

### Current Monitor Output

The MPQ4263 senses average load current through one current-sense resistor, and it outputs one voltage signal on the IMON pin, which is amplified from the ISEN+ and ISEN- voltage difference. It is recommended to place one lower-value capacitor from IMON to AGND.

In PFM mode, IMON can only work normally when the part enters CCM.

## SYSTEM

### Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down.

When the temperature falls below its lower threshold (about 140°C), the chip is enabled.

## DIGITAL INTERFACE

### Digital Serial Interface Description

The digital interface is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The digital interface is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, then arranges the communication sequence. This is based on I<sup>2</sup>C operation principles.

### Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the digital interface transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge bit (ACK).

### Digital Interface Update Sequence

The MPQ4263 requires a start command, a valid digital interface address, a register address byte, and a data byte for a single data update. The device acknowledges receiving each byte by pulling the SDA line low during the high period of a single clock pulse. A valid digital interface address selects the MPQ4263. The device performs an update on the falling edge of the LSB byte.

### Digital Interface Bus Message Format

Figure 9 on page 27 shows the message format. Unshaded cells indicate that the bus host is driving the bus actively, while shaded cells indicate that the MPQ4263 is driving the bus.

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$  = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$  = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

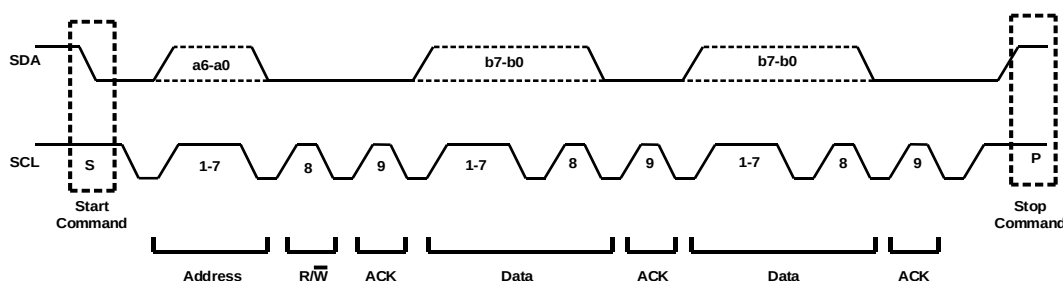


Figure 8: Data Transfer across the PMBus

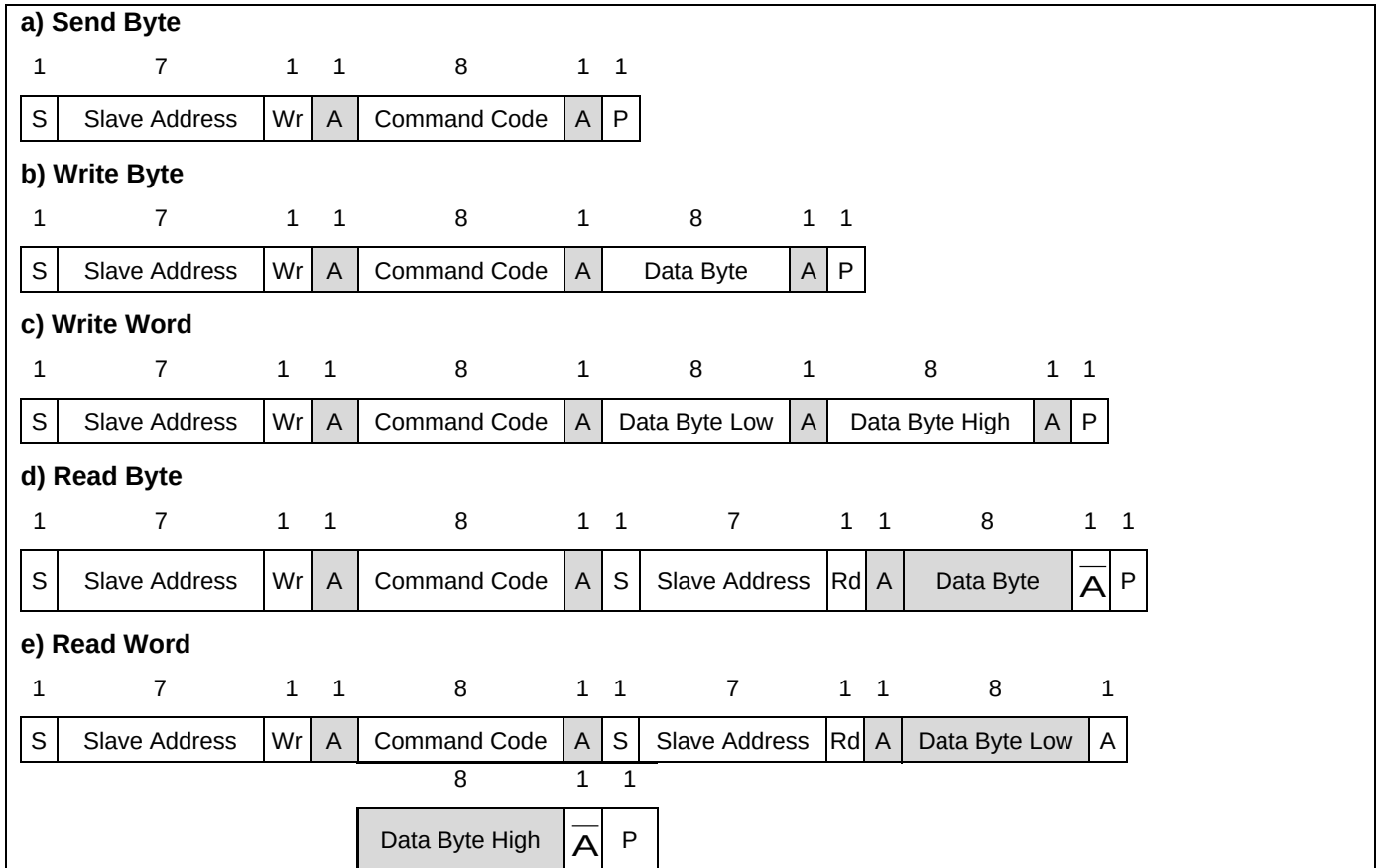


**Figure 9: PMBus Message Format**

## REGISTER DESCRIPTION

### I<sup>2</sup>C/Digital Interface Register

The I<sup>2</sup>C is active once V<sub>IN</sub> and EN exceed their under-voltage lockout (UVLO) thresholds. <sup>(8)</sup>

| Command Code | Command Name               | Type      | Bytes | Data Format | Unit | OTP | Default Value           |
|--------------|----------------------------|-----------|-------|-------------|------|-----|-------------------------|
| 0x01         | OPERATION                  | R/W       | 1     | Reg         |      | Yes | On                      |
| 0x03         | CLEAR_FAULTS               | Send Byte | 1     | Reg         |      | No  | -                       |
| 0x21         | VOUT_COMMAND               | R/W       | 2     | Linear L16  | V    | Yes | V <sub>REF</sub> = 0.5V |
| 0x79         | STATUS_WORD                | R         | 2     | Reg         |      | No  | -                       |
| 0x7D         | STATUS_TEMPERATURE         | R         | 1     | Reg         |      | No  | -                       |
| 0xD0         | MFR_CTRL1                  | R/W       | 1     | Reg         |      | Yes | -                       |
| 0xD1         | MFR_CURRENT_LIMIT          | R/W       | 1     | Reg         |      | Yes | 5.4A                    |
| 0xD2         | MFR_CTRL2                  | R/W       | 1     | Reg         |      | Yes | -                       |
| 0xD3         | MFR_CTRL3                  | R/W       | 1     | Reg         |      | Yes | -                       |
| 0xD4         | MFR_CTRL4                  | R/W       | 1     | Reg         |      | Yes | -                       |
| 0xD8         | MFR_STATUS_MASK            | R/W       | 1     | Reg         |      | Yes | -                       |
| 0xD9         | MFR_OTP_CONFIGURATION_CODE | R/W       | 1     | Reg         |      | Yes | -                       |
| 0xDA         | MFR_OTP_REVISION_NUMBER    | R/W       | 1     | Reg         |      | Yes | -                       |

Note:

8) All register values are based on the MPQ4263-0000.

### Data Format

Linear16 (L16) format is used for the V<sub>OUT</sub> command (see Figure 10).

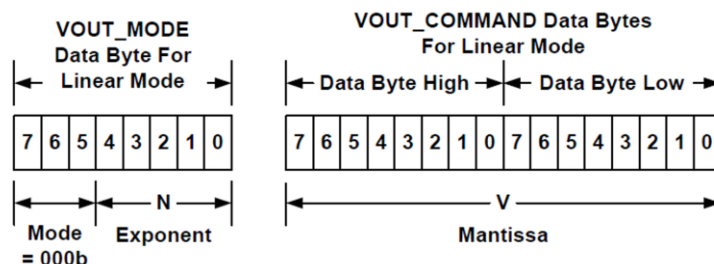


Figure 10: V<sub>OUT</sub> Command

To read V<sub>OUT</sub>, follow the description below.

The MODE bits are set to 000b. The voltage (in V) can be calculated with Equation (3):

$$\text{Voltage} = V \times 2^N \quad (3)$$

Where Voltage is the parameter of interest (in V), V is a 16-bit unsigned binary integer, and N is a 5-bit, two's complement, binary integer.

## DIGITAL INTERFACE COMMAND DESCRIPTION

### OPERATION (01h)

**Format:** Unsigned binary

The OPERATION command configures the converter's operational state.

| Bits | Access | Bit Name  | Description                                                                                                                                                                                                                            |
|------|--------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | OPERATION | Sets the output on/off. Write to 00h to disable the IC and write to 80h to enable the IC. The EN pin has a higher control priority than this bit.<br><br>8'b 0000 0000: The output is off<br>8'b 1000 0000: The output is on (default) |

### CLEAR\_FAULTS (03h)

The CLEAR\_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. If the device is asserting an ALT# signal, the device negates (clears, releases) its ALT# signal output.

The CLEAR\_FAULTS command does not restart a device that has latched off due to a fault condition. If the fault is still present when the bit is cleared, the fault bit is immediately be set again and the host notified by the usual means. This command is write-only. For more details, see the send byte format in Figure 9 on page 27.

### VOUT\_COMMAND (21h)

**Format:** Linear

The VOUT\_COMMAND command sets the output voltage. It follows the L16 linear data format.

| Command                  | VOUT_COMMAND                    |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
|--------------------------|---------------------------------|-----|-----|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|
| Format                   | Linear                          |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |
| Bit                      | 15                              | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access                   | R/W                             | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function                 | Data Byte High                  |     |     |     |     |     |     |     | Data Byte Low |     |     |     |     |     |     |     |
| Reference Voltage (0.5V) | 5120 Decimal / 1400 Hexadecimal |     |     |     |     |     |     |     |               |     |     |     |     |     |     |     |

V<sub>OUT</sub> (in V) can be estimated with (4):

$$V_{OUT} = V \times 2^{-10} \times FB\_RATIO / 10 \quad (4)$$

Where  $V$  is the decimal number corresponding to the 16-bit unsigned binary integer of VOUT\_COMMAND, bits[15:0], and FB\_RATIO is the feedback resistor ratio, calculated with Equation (5):

$$FB\_RATIO = (R_1 + R_2) / R_2 \quad (5)$$

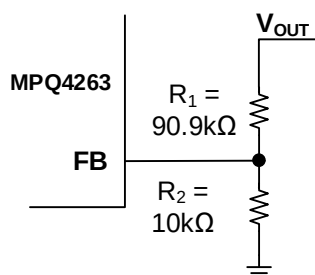


**Figure 11: Feedback Network**

The recommended feedback resistor ratio is 10 ( $V_{OUT} / V_{FB}$ ). This means the default  $V_{OUT}$  is 5V ( $0.5V \times 10$ ). Table 1 shows the  $V_{OUT}$  options when FB\_RATIO is 10.

**Table 1: VOUT\_COMMAND Setting Table (FB\_RATIO = 10)**

| $V_{OUT}$ | $V_{REF}$ | VOUT_COMMAND |
|-----------|-----------|--------------|
| 5V        | 0.5V      | 1400h        |
| 9V        | 0.9V      | 2400h        |
| 15V       | 1.5V      | 3C00h        |
| 20V       | 2V        | 5000h        |

Table 2 shows the  $V_{OUT}$  options when FB\_RATIO is 15.

**Table 2: VOUT\_COMMAND Setting Table (FB\_RATIO = 15)**

| $V_{OUT}$ | $V_{REF}$ | VOUT_COMMAND |
|-----------|-----------|--------------|
| 5V        | 0.333V    | D56h         |
| 9V        | 0.6V      | 1800h        |
| 15V       | 1V        | 2800h        |
| 20V       | 1.333V    | 3556h        |
| 28V       | 1.8667V   | 4AABh        |

Figure 12 shows the feedback network when FB\_RATIO = 15.

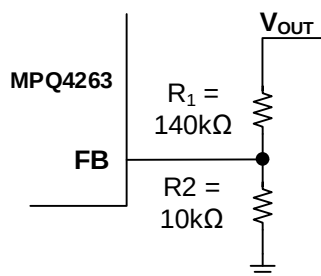


**Figure 12: Feedback Network**

The internal reference voltage ranges between 0.1V and 2.147V with 1mV steps (a total of 2047 steps). This value is set by an 11-bit digital-to-analog converter (DAC), when the DAC input for all 11 bits is 0, and the DAC output is 0.1V.

When the feedback resistor ratio ( $V_{OUT} / V_{FB}$ ) is 10, the VOUT\_COMMAND resolution is 10mV. The valid  $V_{OUT}$  range is between 1V and 21.47V.  $V_{OUT}$  is abnormal when it is beyond this range.

When the MPQ4263 is used for 28V/5A extended power range (EPR) mode, the recommended feedback resistor ratio is 15 (see Figure 12). The VOUT\_COMMAND resolution is 15mV. The valid  $V_{OUT}$  range is between 1V and 32.205V.  $V_{OUT}$  is abnormal when it is beyond this range.

If the calculated VOUT\_COMMAND is not an integer, set VOUT\_COMMAND equal to the integer part plus 1.

## STATUS\_WORD (79h)

**Format:** Unsigned binary

The STATUS\_WORD command returns 2 bytes of information with a summary of the device's fault conditions. Based on the information in these bytes, the host can get more information by reading the appropriate status registers.

| Byte | Bits | Access | Bit Name      | Description                                                                                                                                                                                                                          |
|------|------|--------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Low  | 7    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 6    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 5    | R      | VOUT_OV_FAULT | An output over-voltage (OV) fault has occurred.                                                                                                                                                                                      |
|      | 4    | R      | IOUT_OC_FAULT | An output over-current (OC) fault has occurred. This bit is set if the device enters CC current limit mode, peak current limit mode, or hiccup mode.                                                                                 |
|      | 3    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 2    | R      | TEMPERATURE   | A temperature fault has occurred.                                                                                                                                                                                                    |
|      | 1    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 0    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
| High | 7    | R      | VOUT          | An output voltage fault or warning has occurred.                                                                                                                                                                                     |
|      | 6    | R      | IOUT/POUT     | An output current fault has occurred. This bit is set if the device enters CC current limit mode, peak current limit mode, or hiccup mode.                                                                                           |
|      | 5    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 4    | R      | OC_EXIT       | Indicates whether the output current has exited the CC current limit. This bit is only set high when I <sub>OUT</sub> changes from CC (before entering hiccup mode) to non-CC mode. Recovery from hiccup mode does not set this bit. |
|      | 3    | R      | PG_STATUS#    | If the POWER_GOOD signal is present, this bit is negated. When this bit is set to 1, V <sub>OUT</sub> is not good. When this bit is clear, V <sub>OUT</sub> is power good.                                                           |
|      | 2    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 1    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |
|      | 0    | R      | RESERVED      | Reserved. The default value is 0b.                                                                                                                                                                                                   |

There is an exception; the status bit that remains set is the PG\_STATUS# bit. This bit always reflects the current state of the POWER\_GOOD signal (if present).

### STATUS\_TEMPERATURE (7Dh)

**Format:** Unsigned binary

The STATUS\_TEMPERATURE command returns 1 data byte with device information.

| Bits | Access | Description                                                                                  |
|------|--------|----------------------------------------------------------------------------------------------|
| 7    | R      | Over-temperature fault (OT_FAULT). The OTP entry threshold is 160°C.                         |
| 6    | R      | Over-temperature warning (OT_WARNING). The entry threshold is 135°C. The hysteresis is 20°C. |
| 5    | R      | Reserved.                                                                                    |
| 4    | R      | Reserved.                                                                                    |
| 3    | R      | Exiting OT_WARNING. The OT_WARNING falling edge sets this bit high.                          |
| 2    | R      | Reserved.                                                                                    |
| 1    | R      | Reserved.                                                                                    |
| 0    | R      | Reserved.                                                                                    |

## I<sup>2</sup>C REGISTER MAP

| Name                       | REG (0x) | R/W | D[7]                                                        | D[6]                                             | D[5]       | D[4]                | D[3] | D[2]           | D[1]                   | D[0]         |
|----------------------------|----------|-----|-------------------------------------------------------------|--------------------------------------------------|------------|---------------------|------|----------------|------------------------|--------------|
| MFR_CTRL1                  | D0       | R/W | DITHER_ENABLE                                               | FREQ                                             |            | SWA_FET_RON         |      | OUTPUT_OVP_EN  | OUTPUT_DISCHARGE_EN    | PFM/PWM_MODE |
| MFR_CURRENT_LIMIT          | D1       | R/W | LDC_DISSABLE                                                | CONSTANT_CURRENT_LIMIT (0.5A to 5.4A, 50mA step) |            |                     |      |                |                        |              |
| MFR_CTRL2                  | D2       | R/W | RESERVED                                                    |                                                  |            |                     |      |                | LINE_DROP_COMPENSATION |              |
| MFR_CTRL3                  | D3       | R/W | SWITCHING_CURRENT_LIMIT                                     |                                                  | RSENS      | SLEW_RATE_RISE      |      | SLEW_RATE_FALL |                        | FREQ_MODE    |
| MFR_CTRL4                  | D4       | R/W | CC_BLANK_TIMER                                              |                                                  | CC_DISABLE | I2C_ADDRESS (A5:A1) |      |                |                        |              |
| MFR_STATUS_MASK            | D8       | R/W | Masks the ALT# pin indication when a fault or event happens |                                                  |            |                     |      |                |                        |              |
| MFR_OTP_CONFIGURATION_CODE | D9       | R/W | OTP configuration code, defined by MPS                      |                                                  |            |                     |      |                |                        |              |
| MFR_OTP_REVISION_NUMBER    | DA       | R/W | OTP software revision number, defined by MPS                |                                                  |            |                     |      |                |                        |              |

### I<sup>2</sup>C Slave Address

The I<sup>2</sup>C slave address is 67h by default.

| I <sup>2</sup> C Address (A7:A1)          |                                |
|-------------------------------------------|--------------------------------|
| Binary                                    | Hex                            |
| 1100 111 (default)                        | 67h                            |
| I <sup>2</sup> C/OTP adjustable for A5:A1 | Set via MFR_CTRL4, bits D[4:0] |

### MFR\_CTRL1 (D0h)

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_CTRL1 command configures certain functions.

| Bits   | Access | Bit Name      | Default | Description                                                                                                                                                                                                                                          |
|--------|--------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[7]   | R/W    | DITHER_ENABLE | 1'b 1   | 1'b 0: No dither<br>1'b 1: Enable the frequency spread spectrum (FSS) function                                                                                                                                                                       |
| D[6:5] | R/W    | FREQ          | 2'b 01  | Sets the switching frequency.<br>2'b 00: 280kHz<br>2'b 01: 420kHz<br>2'b 10: 580kHz<br>2'b 11: Reserved                                                                                                                                              |
| D[4:3] | R/W    | SWA_FET_RON   | 2'b 01  | Sets the external SWA's on resistance under 5V <sub>GS</sub> . This value is used for zero-current detection (ZCD). The selected on resistance must match SWA's actual on resistance.<br>2'b 00: 5mΩ<br>2'b 01: 10mΩ<br>2'b 10: 15mΩ<br>2'b 11: 20mΩ |
| D[2]   | R/W    | OUTPUT_OVP_EN | 1'b 1   | Enables output over-voltage protection (OVP)<br>1'b 0: Disabled<br>1'b 1: Enabled                                                                                                                                                                    |

|      |     |                     |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-----|---------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[1] | R/W | OUTPUT_DISCHARGE_EN | 1'b 1 | <p>Enables the output discharge function, which turns on the passive discharge resistor between OUT and ground. This discharge function works until the maximum 200ms timer ends.</p> <p>1'b 0: Disable the output discharge function during EN, V<sub>IN</sub>, or I<sup>2</sup>C off</p> <p>1'b 1: The MPQ4263 turns on the output discharge function during the EN, V<sub>IN</sub> or I<sup>2</sup>C off period until V<sub>OUT</sub> is fully discharged</p> |
| D[0] | R/W | PFM/PWM_MODE        | 1'b 1 | <p>Sets the buck-boost work mode.</p> <p>1'b 0: Auto-PFM/PWM mode</p> <p>1'b 1: Forced PWM mode</p>                                                                                                                                                                                                                                                                                                                                                              |

### MFR\_CURRENT\_LIMIT (D1h)

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_CURRENT\_LIMIT command sets the constant current limit.

| Name                 | LDC_DISABLE                     | CONSTANT CURRENT LIMIT |     |     |     |     |     |     |
|----------------------|---------------------------------|------------------------|-----|-----|-----|-----|-----|-----|
| Format               | Direct, unsigned binary integer |                        |     |     |     |     |     |     |
| Bit                  | 7                               | 6                      | 5   | 4   | 3   | 2   | 1   | 0   |
| Access               | R/W                             | R/W                    | R/W | R/W | R/W | R/W | R/W | R/W |
| Default value (5.4A) | 0                               | 108 integer            |     |     |     |     |     |     |

The real-world I<sub>OUT</sub> over-current threshold (in A) can be calculated with Equation (6):

$$I_{OUT\_OC} (A) = I_{OUT\_LIM} \times 0.05 \quad (6)$$

Where I<sub>OUT\_LIM</sub> is a 7-bit unsigned binary integer of CONSTANT\_CURRENT\_LIMIT. The I<sub>OUT\_OC</sub> resolution (or minimum step) is 50mA, while the maximum value is 5.4A. If I<sub>OUT</sub> is beyond this range, it is clamped to 5.4A.

D[7] (LDC\_DISABLE) enables line drop compensation. If LDC\_DISABLE = 0, line drop compensation is controlled by MFR\_CTRL2 (D2h). If LDC\_DISABLE = 1, line drop compensation is disabled.

### MFR\_CTRL2 (D2h)

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_CTRL2 command configures certain functions.

| Bits   | Access | Bit Name               | Default | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------|------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[7:2] | -      | RESERVED               | -       | Reserved.                                                                                                                                                                                                                                                                                                                                                                                           |
| D[1:0] | R/W    | LINE_DROP_COMPENSATION | 2'b 00  | <p>Sets the V<sub>OUT</sub> compensation value at certain load currents. The compensation amplitude is fixed for any V<sub>OUT</sub>.</p> <p>2'b 00: No compensation</p> <p>2'b 01: V<sub>OUT</sub> compensates 100mV at a 3A I<sub>OUT</sub></p> <p>2'b 10: V<sub>OUT</sub> compensates 300mV at a 3A I<sub>OUT</sub></p> <p>2'b 11: V<sub>OUT</sub> compensates 600mV at a 3A I<sub>OUT</sub></p> |

### MFR\_CTRL3 (D3h)

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_CTRL3 command configures certain functions.

| Bits   | Access | Bit Name                | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|--------|-------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[7:6] | R/W    | SWITCHING_CURRENT_LIMIT | 2'b 01  | Sets the current limit for SWB and SWC.<br>2'b 00: 8A SWC peak current limit, 6A SWB valley current limit<br>2'b 01: 12A SWC peak current limit, 9A SWB valley current limit<br>2'b 10: 15A SWC peak current limit, 13A SWB valley current limit<br>2'b 11: 20A SWC peak current limit, 17A SWB valley current limit                                                                                                                                                                        |
| D[5]   | R/W    | RSNS                    | 1'b 0   | Selects the R <sub>SENS</sub> resistance.<br>1'b 0: 5mΩ<br>1'b 1: 10mΩ                                                                                                                                                                                                                                                                                                                                                                                                                      |
| D[4:3] | R/W    | SLEW_RATE_RISE          | 2'b 01  | Sets the V <sub>OUT</sub> adjusting rising slew rate. The default value is 01. The slew rate can be calculated with the following equation:<br>$V_{OUT} \text{ Slew Rate} = V_{REF} \text{ Slew Rate} \times \text{Feedback Ratio}$<br>Where Feedback Ratio = 10.<br>2'b 00: 0.08mv/μs V <sub>REF</sub> rising slew rate<br>2'b 01: 0.16mv/μs V <sub>REF</sub> rising slew rate<br>2'b 10: 0.4mv/μs V <sub>REF</sub> rising slew rate<br>2'b 11: 0.8mv/μs V <sub>REF</sub> rising slew rate |
| D[2:1] | R/W    | SLEW_RATE_FALL          | 2'b 01  | Sets the V <sub>OUT</sub> adjusting falling slew rate. The slew rate can be calculated with the following equation:<br>$V_{OUT} \text{ Slew Rate} = V_{REF} \text{ Slew Rate} \times \text{Feedback Ratio}$<br>Where Feedback Ratio = 10.<br>2'b 00: 0.02mv/μs V <sub>REF</sub> falling slew rate<br>2'b 01: 0.04mv/μs V <sub>REF</sub> falling slew rate<br>2'b 10: 0.1mv/μs V <sub>REF</sub> falling slew rate<br>2'b 11: 0.2mv/μs V <sub>REF</sub> falling slew rate                     |
| D[0]   | R/W    | FREQ_MODE               | 1'b 1   | Sets the frequency mode during buck-boost operation.<br>1'b 0: Reduce the frequency to half of that in buck and boost mode<br>1'b 1: Keep the same frequency as of that in buck and boost mode                                                                                                                                                                                                                                                                                              |

### MFR\_CTRL4 (D4h)

**Format:** Unsigned binary

**Reset value:** Set by OTP

The MFR\_CTRL4 command configures certain functions.

| Bits   | Access | Bit Name       | Default | Description                                                                                                             |
|--------|--------|----------------|---------|-------------------------------------------------------------------------------------------------------------------------|
| D[7:6] | R/W    | CC_BLANK_TIMER | 2'b 00  | Sets the blanking time before entering CC mode.<br>2'b 00: 250μs<br>2'b 01: 3ms<br>2'b 10: Reserved<br>2'b 11: Reserved |

|        |     |             |           |                                                                                                                                           |
|--------|-----|-------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------|
| D[5]   | R/W | CC_DISABLE  | 1'b 0     | Enables the CC current limit.<br>1'b 0: Enabled<br>1'b 1: Disabled                                                                        |
| D[4:0] | R/W | I2C_ADDRESS | 5'b 00111 | Sets the I <sup>2</sup> C slave address (bits A5:A1). The default value is 00111b, which means the I <sup>2</sup> C slave address is 67h. |

### MFR\_STATUS\_MASK (D8h)

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_STATUS\_MASK command can only mask off the ALT# pin's behavior; the STATUS register still indicates each event.

| Bits | Access | Bit Name        | Default | Description                                                                                                                                                                                                                          |
|------|--------|-----------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[7] | R/W    | VOUT_MSK        | 1'b 1   | 1'b 0: No mask<br>1'b 1: Mask enabled                                                                                                                                                                                                |
| D[6] | R/W    | IOUT/POUT_MSK   | 1'b 0   | 1'b 0: No mask. This bit masks IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT<br>1'b 1: Mask enabled                                                                                                                                          |
| D[5] | R/W    | RESERVED_MSK    | 1'b 1   | 1'b 0: No mask<br>1'b 1: Mask enabled                                                                                                                                                                                                |
| D[4] | R/W    | TEMP_MSK        | 1'b 1   | Masks temperature-related conditions.<br>1'b 0: No mask<br>1'b 1: Mask enabled                                                                                                                                                       |
| D[3] | R/W    | PG_STATUS#_MSK  | 1'b 1   | Masks the higher level PG control bit.<br>1'b 0: No mask<br>1'b 1: Mask enabled                                                                                                                                                      |
| D[2] | R/W    | PG_ALT_EDGE_MSK | 1'b 1   | 1'b 0: No mask. The ALT# pin indicates both the PG_STATUS# rising and falling edges<br>1'b 1: Mask enabled. The ALT pin only indicates the PG_STATUS# falling edge, which means the output voltage transitions from not good to good |
| D[1] | R/W    | RESERVED_MSK    | 1'b 1   | 1'b 0: No mask<br>1'b 1: Mask enabled                                                                                                                                                                                                |
| D[0] | R/W    | UNKNOWN_MSK     | 1'b 1   | 1'b 0: No mask<br>1'b 1: Mask enabled                                                                                                                                                                                                |

### MFR\_OTP\_CONFIGURATION\_CODE (D9h)

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_OTP\_CONFIGURATION\_CODE command sets the OTP configuration code, which is defined by MPS.

| Bits   | Access | Bit Name               | Description                                      |
|--------|--------|------------------------|--------------------------------------------------|
| D[7:0] | R/W    | OTP_CONFIGURATION_CODE | Sets the OTP configuration code, defined by MPS. |

**MFR\_OTP\_REVISION\_NUMBER (DAh)**

**Format:** Unsigned binary

**Reset value:** Set via the OTP

The MFR\_OTP\_REVISION\_NUMBER command sets the OTP software revision number, defined by MPS.

| Bits   | Access | Bit Name            | Description                                            |
|--------|--------|---------------------|--------------------------------------------------------|
| D[7:0] | R/W    | OTP_REVISION_NUMBER | Sets the OTP software revision number, defined by MPS. |

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Selecting the Inductor

Inductor selection is based on the operating mode. The inductance for buck mode can be estimated with Equation (7):

$$L_{\text{BUCK}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times \Delta I_L} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \quad (7)$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current.

For boost mode, inductor selection is based on limiting the peak-to-peak current ripple ( $\Delta I_L$ ) to be about 30% to 50% of the maximum input current. The target inductance for boost mode can be calculated with Equation (8):

$$L_{\text{BOOST}} = \frac{V_{\text{IN}} \times (V_{\text{OUT}} - V_{\text{IN}})}{V_{\text{OUT}} \times f_{\text{SW}} \times \Delta I_L} \quad (8)$$

Where  $\Delta I_L$  is the peak-to-peak ripple current.  $I_{\text{IN(MAX)}}$  can be estimated with Equation (9):

$$I_{\text{IN(MAX)}} = \frac{V_{\text{OUT}} \times I_{\text{LOAD(MAX)}}}{V_{\text{IN}} \times \eta} \quad (9)$$

Where  $I_{\text{LOAD(MAX)}}$  is the maximum load current, and  $\eta$  is the efficiency.

Choosing a larger-value inductor reduces the ripple current but increases the physical size of the inductor. A larger-value inductor also reduces the converter's achievable bandwidth by moving the right half-plane zero to lower frequencies. Select the inductor for the specific application requirements.

#### Selecting the Input Capacitor

In buck mode, the input current is discontinuous, while it is continuous in boost mode. A capacitor must supply the AC current in buck mode while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and these capacitors should be placed as close to the VIN pin as possible. Ceramic capacitors with X5R or X7R dielectrics are recommended because they are fairly stable across temperature fluctuations.

The capacitors must also have a ripple current rating greater than the converter's maximum

input ripple current. The input ripple current in buck mode can be estimated with Equation (10):

$$I_{\text{CIN}} = I_{\text{OUT}} \times \sqrt{\frac{V_{\text{OUT}}}{V_{\text{IN}}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right)} \quad (10)$$

The worst-case condition in buck mode occurs at  $V_{\text{IN}} = 2 \times V_{\text{OUT}}$ , calculated with Equation (11):

$$I_{\text{CIN}} = \frac{I_{\text{OUT}}}{2} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple in buck mode can be estimated with Equation (12):

$$\Delta V_{\text{IN}} = \frac{I_{\text{OUT}}}{f_{\text{SW}} \times C_{\text{IN}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \quad (12)$$

The worst-case condition occurs when  $V_{\text{IN}} = 2 \times V_{\text{OUT}}$ , calculated with Equation (13):

$$\Delta V_{\text{IN}} = \frac{1}{4} \frac{I_{\text{OUT}}}{f_{\text{SW}} \times C_{\text{IN}}} \quad (13)$$

The input voltage ripple in boost mode can be estimated with Equation (14):

$$\Delta V_{\text{IN}} = \frac{V_{\text{IN}}}{8 \times f_{\text{SW}}^2 \times L \times C_{\text{IN}}} \times \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \quad (14)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The input voltage ripple in boost mode can be calculated with Equation (15):

$$\Delta V_{\text{IN}} = \frac{V_{\text{IN}}}{f_{\text{SW}} \times L} \times \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \times \left(R_{\text{ESR}} + \frac{1}{8 \times f_{\text{SW}} \times C_{\text{IN}}}\right) \quad (15)$$

#### Selecting the Output Capacitor

In boost mode,  $I_{\text{OUT}}$  is discontinuous, so an output capacitor ( $C_{\text{OUT}}$ ) must be able to reduce the output voltage ripple.

A larger-value capacitor may be required to lower the output voltage ripple and transient response. Ceramic, low-ESR capacitors with X5R or X7R dielectrics are recommended. If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. The output voltage ripple in buck mode can be estimated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (16)$$

Where  $\Delta V_{OUT}$  is the output ripple voltage, and  $C_{OUT}$  is the capacitance of the output capacitor.

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output voltage ripple in buck mode can be estimated with Equation (17):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (17)$$

Where  $R_{ESR}$  is the equivalent series resistance of the output capacitors.

The output voltage ripple in boost mode can be estimated with Equation (18):

$$\Delta V_{OUT} = \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{OUT}}{C_{OUT} \times f_{SW}} \quad (18)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output voltage ripple in boost mode can be estimated with Equation (19):

$$\Delta V_{OUT} = \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{OUT}}{C_{OUT} \times f_{SW}} + \frac{I_{OUT} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (19)$$

Choose output capacitors that satisfy the design's output voltage ripple and load transient response requirements. Consider capacitance derating when designing applications with high output voltages.

### Selecting the External MOSFETs (SWA and SWD)

The MPQ4263 requires two external N-channel power MOSFETs (see Figure 13). In buck mode,

SWA and SWB switch while SWD stays on. In boost mode, SWC and SWD switch while SWA stays on.

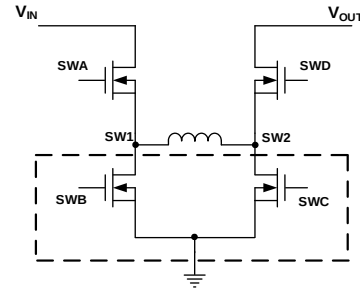


**Figure 13: Buck-Boost Topology**

The critical parameters to select a MOSFET are described below.

1. **Maximum drain-to-source voltage ( $V_{DS(MAX)}$ ):** SWA must withstand the maximum input voltage and the transient spikes at SW1 during switching. Select SWA and SWB to have a  $V_{DS(MAX)}$  that is 1.5 times the input voltage.  
SWD withstands the output voltage and additional transient spikes at SW2 during switching. Select SWD to have a  $V_{DS(MAX)}$  that is at least 1.5 times the output voltage.
2. **Maximum current ( $I_{D(MAX)}$ )**
3.  **$V_{TH}$ :** The driver voltages of the MPQ4263 are supplied by VCC. The gate plateau voltages should be below the converter's minimum VCC. Otherwise, the MOSFETs may not fully turn on during start-up or under overload conditions.
4. **On resistance ( $R_{DS(ON)}$ )**
5. **Total gate charge ( $Q_G$ ):** For the MPQ4263, the  $Q_G$  value for all switches should be below 30nC (under a 5V GATE condition). The SW1 rising time and SW2 falling time are shorter than 15ns.

### SWA

When the MPQ4263 works in boost mode, SWA is always on. SWA's conduction power loss can be calculated with Equation (20):

$$P_{C\_LOSS(SWA)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS(ON)(SWA)} \quad (20)$$

Assume that the MOSFET's thermal resistance from the junction to ambient is 50°C/W

(determined by the board's power dissipation), and that the maximum acceptable temperature rise is 50°C. The maximum power loss can be estimated with Equation (21):

$$P_{C\_LOSS(SWA)} < 1W \quad (21)$$

Use the above calculations to select a MOSFET with an appropriate on resistance.

When the MPQ4263 works in buck mode, the conduction and switching loss of SWA can be calculated with Equation (22) and Equation (23), respectively:

$$P_{C\_LOSS(SWA)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DS(ON)(SWA)} \quad (22)$$

$$P_{SW\_LOSS(SWA)} = \frac{1}{2} V_{IN} \times I_{OUT}^2 \times (t_{ON} + t_{OFF}) \times f_{SW} \quad (23)$$

Figure 14 shows the switch on/off state. The switch on time ( $t_{ON}$ ) and the switch off time ( $t_{OFF}$ ) are based on the MOSFET datasheet.

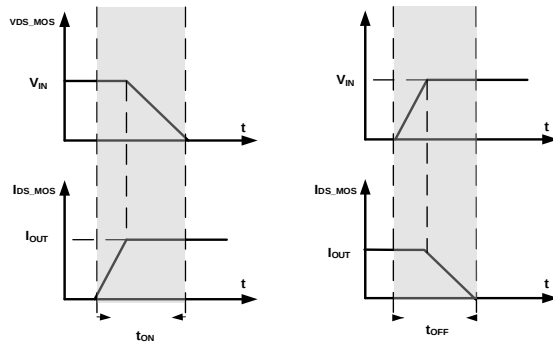


**Figure 14: Switch On/Off State**

### SWD

When the MPQ4263 works in buck mode, SWD is always on. The SWD power loss can be calculated with Equation (24):

$$P_{C\_LOSS(SWD)} = I_{OUT}^2 \times R_{DS(ON)(SWD)} \quad (24)$$

$P_{C\_LOSS(SWD)}$  should be less than the maximum power loss. When the MPQ4263 works in boost mode, the conduction loss can be estimated with Equation (25):

$$P_{C\_LOSS(SWD)} = \frac{V_{IN}}{V_{OUT}} \times \left( I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \times R_{DS(ON)(SWD)} \quad (25)$$

When determining the total power loss, the dead time and LS-FET switching loss can be ignored.

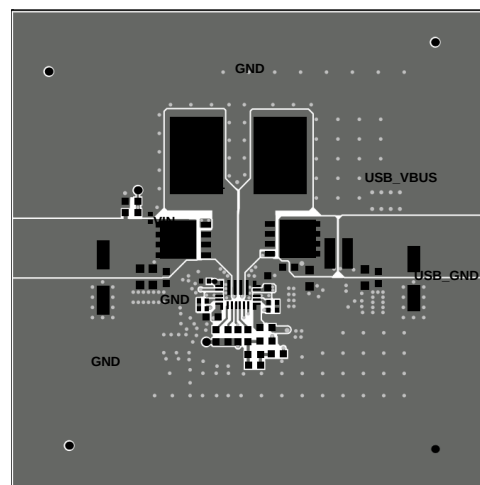
## PCB Layout Guidelines <sup>(9)</sup>

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 15 and follow the guidelines below:

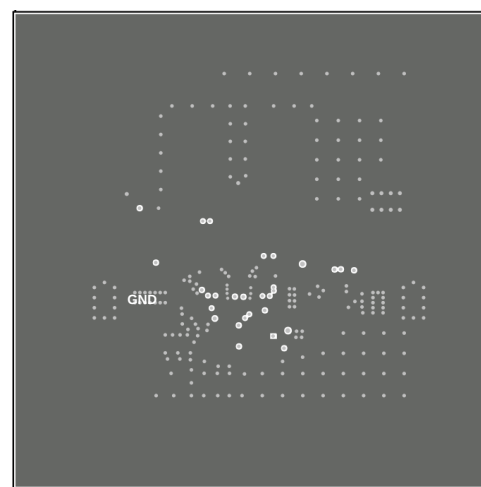
1. In buck mode, place the input power loop — including the input filter capacitor ( $C_{IN}$ ), the power MOSFET (SWA), and SW1 node — as close together as possible.
2. In boost mode, place the output power loop — including the output filter capacitor ( $C_{OUT}$ ), the power MOSFET (SWD), and SW2 node — as close together as possible.
3. Use short, direct, and wide traces to connect VOUT.
4. Add vias to GND after the output filter (if required).
5. Use a large copper plane for PGND, and add multiple vias to improve thermal dissipation.
6. Connect AGND to PGND.
7. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to the SWA and SWD drains, and PGND.
8. Place the VCC decoupling capacitor as close as possible to VCC.
9. The output current-sense traces (ISEN+ and ISEN-) must have a Kelvin connection.
10. The switching nodes of the BST1/2 capacitors must be Kelvin connected to the SW1 and SW2 pins with a wide PCB trace.
11. Kelvin connect the VIN pin to the SWA drain with a wide PCB trace.

### Note:

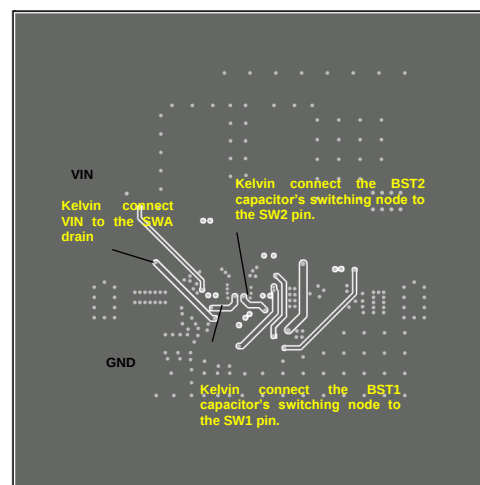
- 9) The recommended layout is based on the typical application circuit (see Figure 16 on page 42).



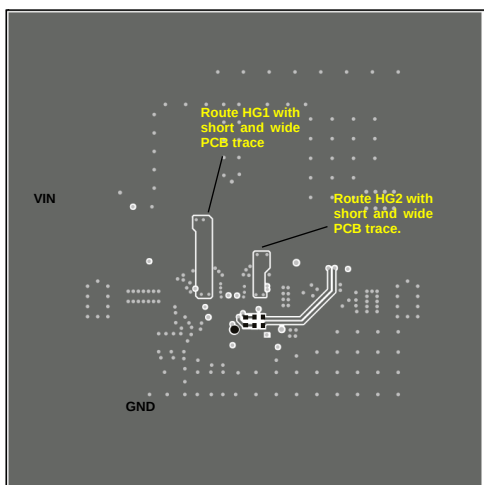
Top Layer



Mid-Layer 1



Mid-Layer 2



**Bottom Layer**

**Figure 15: Recommended PCB Layout**

# TYPICAL APPLICATION CIRCUITS

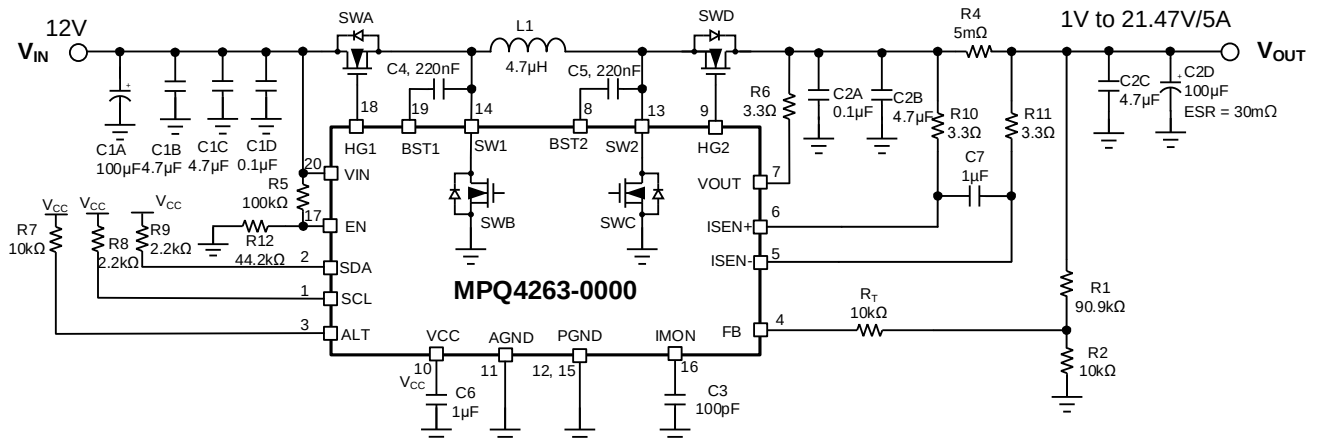


Figure 16: Typical Application Circuit ( $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$  to  $21V$ , Default On)

## MPQ4263GQVE-0000 CONFIGURATION TABLE

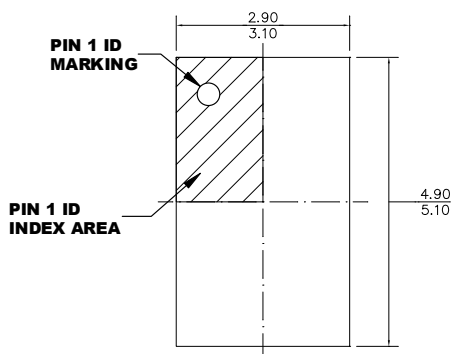
| OTP Items                      | Description                                                                                           | Value                                           |
|--------------------------------|-------------------------------------------------------------------------------------------------------|-------------------------------------------------|
| OPERATION                      | Sets the device on or off                                                                             | 1: On                                           |
| VOUT_COMMAND                   | Sets the output voltage                                                                               | V <sub>REF</sub> = 0.5V                         |
| DITHER_ENABLE                  | Enables frequency spread spectrum (FSS)                                                               | 1: Enabled                                      |
| FREQ                           | Sets the switching frequency                                                                          | 01: 420kHz                                      |
| SWA_FET RON                    | Sets SWA's on resistance                                                                              | 01: 10mΩ                                        |
| OUTPUT_OVP_EN                  | Enables output over-voltage protection (OVP)                                                          | 1: Enable (default)                             |
| OUTPUT_DISCHARGE_EN            | Enables the output discharge function during the V <sub>IN</sub> , I <sup>2</sup> C, or EN off period | 1: Enable (default)                             |
| PFM/PWM_MODE                   | Selects auto-PFM/PWM mode or forced PWM mode                                                          | 1: Forced PWM mode (default)                    |
| CONSTANT_CURRENT_LIMIT         | Sets the output current limit                                                                         | 5.4A                                            |
| LINE_DROP_COMPENSATION         | Sets the output voltage compensation value vs. load current                                           | 0: Enable line drop compensation(default)       |
| Line Drop Compensation Gain    | Sets the output voltage compensation value vs. load current                                           | 00: No compensation (default)                   |
| SWITCHING_CURRENT_LIMIT        | Sets the SWB valley current limit and SWC peak current limit                                          | 01: SWC peak 12A, SWB valley 9A (default)       |
| RSENS                          | Selects the R <sub>SENS</sub> resistance                                                              | 0: 5mΩ                                          |
| SLEW_RATE_RISE                 | Sets the V <sub>OUT</sub> rising slew rate                                                            | 01: 0.16mV/μs (default)                         |
| SLEW_RATE_FALL                 | Sets the V <sub>OUT</sub> falling slew rate                                                           | 01: 0.04mV/us                                   |
| FREQ_MODE                      | Sets the frequency for buck-boost mode                                                                | Keep the frequency unchanged in buck-boost mode |
| CC_DISABLE                     | Disables or enables the CC function                                                                   | 0: Enable CC (default)                          |
| CC_BLANK_TIMER                 | Sets the blanking time before entering CC mode                                                        | 00: 250μs (default)                             |
| V <sub>IN</sub> OV Threshold   | Selects the V <sub>IN</sub> OV threshold                                                              | 0: 38V                                          |
| V <sub>IN</sub> UVLO threshold | Selects the V <sub>IN</sub> under-voltage lockout (UVLO) threshold                                    | 0: 3.3V                                         |
| Absolute Output OVP            | Selects the absolute OVP threshold                                                                    | 1: 39V                                          |
| OT Warning Function            | Enables the over-temperature (OT) warning function                                                    | 1: Disable                                      |
| I2C_ADDRESS                    | Sets the I <sup>2</sup> C slave address                                                               | 67h                                             |
| VOUT_MSK                       | Masks ALT pin indication                                                                              | 1: Mask                                         |
| IOUT/POUT_MSK                  |                                                                                                       | 0: No mask                                      |
| RESERVED_MSK                   |                                                                                                       | 1: Mask                                         |
| TEMP_MSK                       |                                                                                                       | 1: Mask                                         |
| PG_STATUS#_MSK                 |                                                                                                       | 1: Mask                                         |
| PG_ALT_EDGE_MSK                |                                                                                                       | 1: Mask                                         |
| GND_SHORT_VBATT_MSK            |                                                                                                       | 1: Mask                                         |
| UNKNOWN_MSK                    |                                                                                                       | 1: Mask                                         |

## MPQ4263GQVE-0001 CONFIGURATION TABLE

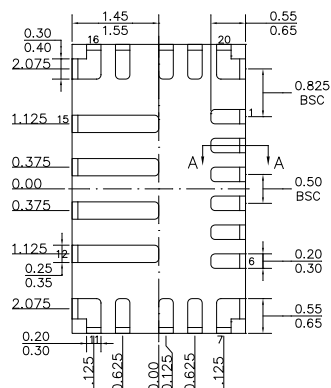
| OTP Items                      | Description                                                                                           | Value                                           |
|--------------------------------|-------------------------------------------------------------------------------------------------------|-------------------------------------------------|
| OPERATION                      | Sets the device on or off                                                                             | 0: Off                                          |
| VOUT_COMMAND                   | Sets the output voltage                                                                               | V <sub>REF</sub> = 0.5V                         |
| DITHER_ENABLE                  | Enables frequency spread spectrum (FSS)                                                               | 1: Enable                                       |
| FREQ                           | Sets the switching frequency                                                                          | 01: 420kHz                                      |
| SWA_FET RON                    | Sets SWA's on resistance                                                                              | 01: 10mΩ                                        |
| OUTPUT_OVP_EN                  | Enables output over-voltage protection (OVP)                                                          | 1: Enable (default)                             |
| OUTPUT_DISCHARGE_EN            | Enables the output discharge function during the V <sub>IN</sub> , I <sup>2</sup> C, or EN off period | 1: Enable (default)                             |
| PFM/PWM_MODE                   | Selects auto-PFM/PWM mode or forced PWM mode                                                          | 1: Forced PWM mode (default)                    |
| CONSTANT_CURRENT_LIMIT         | Sets the output current limit                                                                         | 5.4A                                            |
| LINE_DROP_COMPENSATION         | Sets the output voltage compensation value vs. load current                                           | 0: Enable line drop compensation (default)      |
| Line Drop Compensation Gain    | Sets the output voltage compensation value vs. load current                                           | 00: No compensation (default)                   |
| SWITCHING_CURRENT_LIMIT        | Sets the SWB valley current limit and SWC peak current limit                                          | 01: SWC peak 12A, SWB valley 9A (default)       |
| RSENS                          | Selects the R <sub>SENS</sub> resistance                                                              | 1: 10mΩ                                         |
| SLEW_RATE_RISE                 | Sets the V <sub>OUT</sub> rising slew rate                                                            | 01: 0.16mV/us(default)                          |
| SLEW_RATE_FALL                 | Sets the V <sub>OUT</sub> falling slew rate                                                           | 10: 0.1mV/us                                    |
| FREQ_MODE                      | Sets the frequency for buck-boost mode                                                                | Keep the frequency unchanged in buck-boost mode |
| CC_DISABLE                     | Disables or enables the CC function                                                                   | 0: Enable CC(default)                           |
| CC_BLANK_TIMER                 | Sets the blanking time before entering CC mode                                                        | 00: 250μs (default)                             |
| V <sub>IN</sub> OV Threshold   | Selects the V <sub>IN</sub> OV threshold                                                              | 0: 38V                                          |
| V <sub>IN</sub> UVLO threshold | Selects the V <sub>IN</sub> under-voltage lockout (UVLO) threshold                                    | 0: 3.3V                                         |
| Absolute Output OVP            | Selects the absolute OVP threshold                                                                    | 1: 39V                                          |
| OT Warning Function            | Enables the over-temperature (OT) warning function                                                    | 1: Disabled                                     |
| I2C_ADDRESS                    | Sets the I <sup>2</sup> C slave address                                                               | 67h                                             |
| VOUT_MSK                       | Masks ALT pin indication                                                                              | 1: Mask                                         |
| IOUT/POUT_MSK                  |                                                                                                       | 0: No Mask                                      |
| RESERVED_MSK                   |                                                                                                       | 1: Mask                                         |
| TEMP_MSK                       |                                                                                                       | 1: Mask                                         |
| PG_STATUS#_MSK                 |                                                                                                       | 1: Mask                                         |
| PG_ALT_EDGE_MSK                |                                                                                                       | 1: Mask                                         |
| GND_SHORT_VBATT_MSK            |                                                                                                       | 1: Mask                                         |
| UNKNOWN_MSK                    |                                                                                                       | 1: Mask                                         |

# PACKAGE INFORMATION

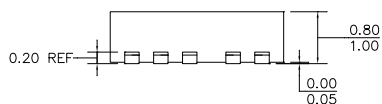
## QFN-20 (3mmx5mm)



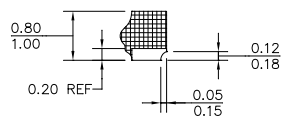
**TOP VIEW**



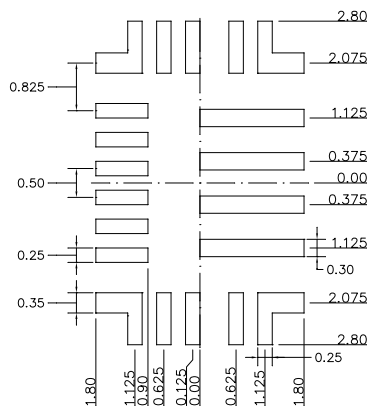
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

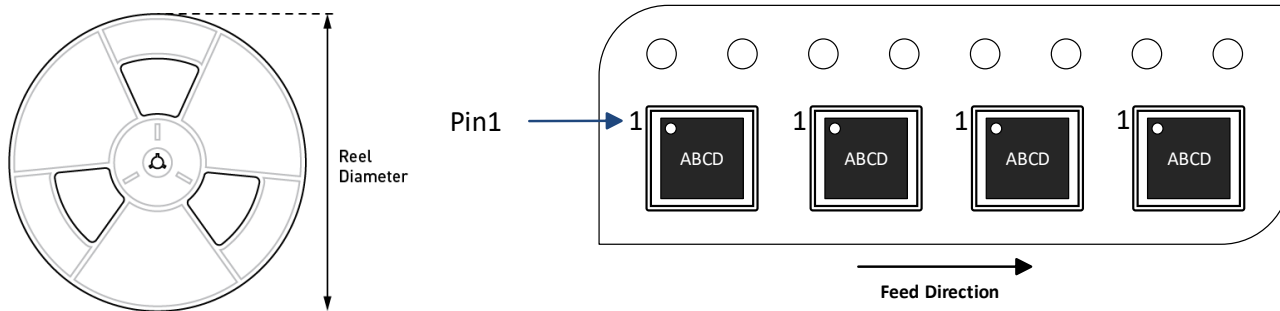


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number                     | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch | Trailer Leader/ Reel |
|---------------------------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|----------------------|
| MPQ4263GQ<br>VE-0000-<br>AEC1-Z | QFN-20<br>(3mmx5mm) | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                | 125 &<br>125         |
| MPQ4263GQ<br>VE-0001-<br>AEC1-Z |                     |                |                |                |               |                    |                    |                      |
| MPQ4263GQ<br>VE-0002-<br>AEC1-Z |                     |                |                |                |               |                    |                    |                      |
| MPQ4263GQ<br>VE-xxxx-<br>AEC1-Z |                     |                |                |                |               |                    |                    |                      |



## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 9/21/2023     | Initial Release | -             |

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