



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-AT24C01C /AT24C02C

I²C-Compatible (2-wire) Serial EEPROM

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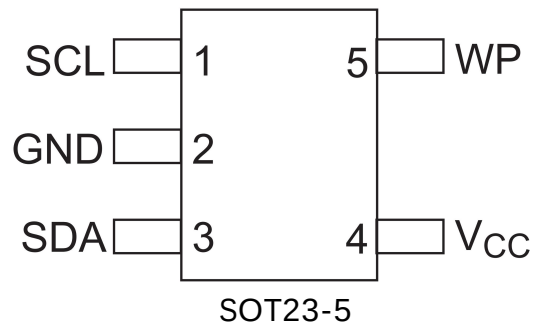
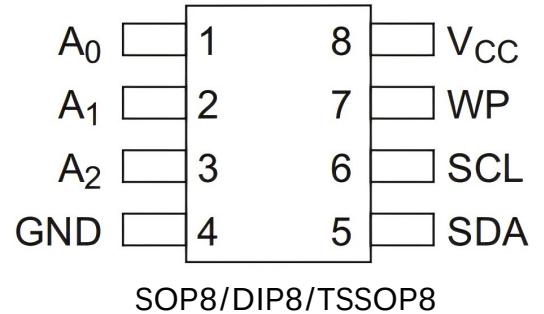
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- Low-voltage operation
- $V_{CC} = 1.7V$ to $5.5V$
- Internally organized as 128×8 (1K) or 256×8 (2K)
- I^2C compatible (2-wire) serial interface
- Schmitt Trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz (1.7V) and 1MHz (2.5V, 2.7V, 5.0V) compatibility
- Write Protect pin for hardware data protection
- 8-byte Page Write mode
- Partial page writes allowed
- Self-timed write cycle (5ms max)
- High-reliability
- Endurance: 1,000,000 write cycles
- Data retention: 100 years
- Green package options (Pb/Halide-free/RoHS-compliant)
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP and 5-lead SOT23
- Die sale options: wafer form and tape and reel available



Description

The AT24C01C/02C provides 1024/2048-bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 128/256 words of eight bits each. Both devices include a cascading feature that allows up to eight devices to share a common 2-wire bus. These devices are optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01C/02C are available in space saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP and 5-lead SOT23 packages. In addition, the entire family operates from 1.7V to 5.5V V_{CC} .



Pin Configurations and Pinouts

Pin Name	Function
A ₀ -A ₂	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V _{CC}	Power Supply

Note: 1. For use of 5-lead SOT23, the software A2, A1, and A0 bits in the device address word must be set to zero to properly communicate.

Absolute Maximum Ratings

Operating Temperature – 55°C to +125°C
Storage Temperature – 65°C to +150°C
Voltage on any pin
with respect to ground – 1.0V to +7.0V
Maximum Operating Voltage..... 6.25V
DC Output Current..... 5.0mA

Notice: Stresses beyond those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

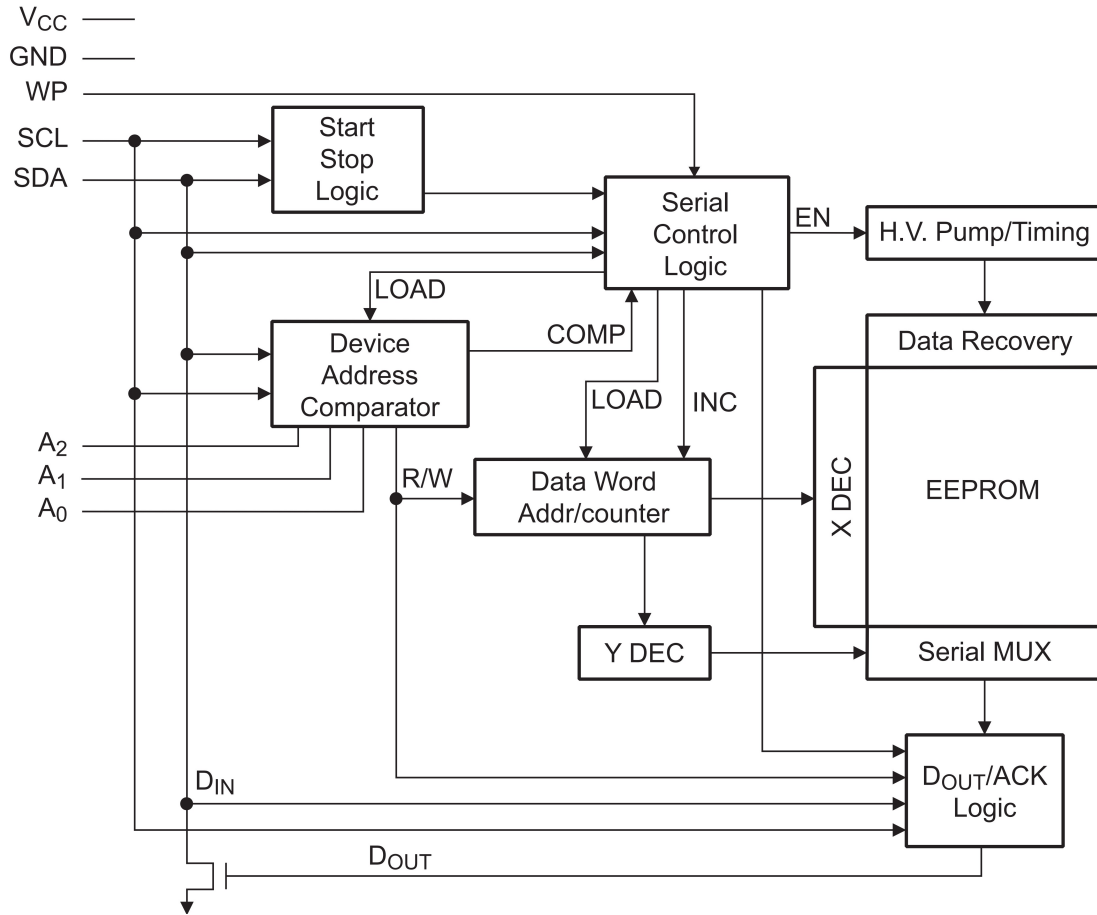
Memory Organization

AT24C01C, 1K Serial EEPROM: Internally organized with 16 pages of eight bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02C, 2K Serial EEPROM: Internally organized with 32 pages of eight bytes each, the 2K requires an 8-bit data word address for random word addressing.



Block Diagram



Pin Description

Serial Clock (SCL):The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA):The SDA pin is bidirectional for serial data transfer.This pin is open drain driven and may be wire-ORed with any number of other open drain or open collector devices.

Device/Page Addresses (A_2, A_1, A_0):The A_2, A_1 , and A_0 pins are device address inputs that are hard wired for the AT24C01C/02C.As many as eight 1-Kbit or 2-Kbit devices may be addressed on a single bus system.See “ Device Addressing ” for more details.

Write Protect (WP):The AT24C01C/02C have a Write Protect pin that provides hardware data protection.The Write Protect pin allows normal read/write operations when connected to ground (GND).When the Write Protect pin is connected to V_{CC} ,the write protection feature is enabled and operates as shown below in Table 1.



Table 1. Write Protect

WP Pin Status		Part of the Array Protected		
		AT24C01C and AT24C02C		
At V_{CC}		Full (2K) Array		
At	GND	Normal	Read/Write	Operations

Pin Capacitance(1)

Applicable over recommended operating range from $T_A = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = 1.7\text{V}$ to 5.5V

Symbol	Test Condition	Max	Units	Conditions
C_{VO}	Input/Output Capacitance (SDA)	8	pF	$V_{VO} = 0\text{V}$
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.7\text{V}$ to 5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.7		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC1}	Supply Current $V_{CC} = 5.0\text{V}$	Read at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current $V_{CC} = 5.0\text{V}$	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current $V_{CC} = 1.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			1.0	μA
I_{SB2}	Standby Current $V_{CC} = 2.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			2.0	μA
I_{SB3}	Standby Current $V_{CC} = 5.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			6.0	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾		-0.6		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL1}	Output Low Level $V_{CC} = 1.7\text{V}$	$I_{OL} = 0.15\text{mA}$			0.2	V
V_{OL2}	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{mA}$			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.



AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.7\text{V}$ to 5.5V , $C_L = 1\text{TTL Gate and } 100\text{pF}$ (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		μs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		μs
t_I	Noise Suppression Time		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	μs
t_{BUF}	Time the bus must be free before a new transmission can start.	1.2		0.5		μs
$t_{HD,STA}$	Start Hold Time	0.6		0.25		μs
$t_{SU,STA}$	Start Setup Time	0.6		0.25		μs
$t_{HD,DAT}$	Data In Hold Time	0		0		μs
$t_{SU,DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time ⁽¹⁾		0.3		0.3	μs
t_F	Inputs Fall Time ⁽¹⁾		300		100	ns
$t_{SU,STO}$	Stop Setup Time	0.6		.25		μs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance ⁽¹⁾	3.3V, +25°C, Page Mode	1,000,000				Write Cycles

Note: 1. This parameter is ensured by characterization only.

2. AC measurement conditions:

- R_L (connects to V_{CC}): 1.3 k Ω (2.5V, 5V), 10 k Ω (1.7V)
- Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
- Input rise and fall times: $\leq 50\text{ns}$
- Input and output timing reference voltages: 0.5 V_{CC}



Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4). Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command (see Figure 5).

Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode (see Figure 5).

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Standby Mode: The AT24C01C/02C features a low power standby mode which is enabled:

- Upon power-up.
- After the receipt of the stop bit and the completion of any internal operations.

2-wire Software Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a start bit condition.
2. Clock nine cycles.
3. Create another start bit followed by stop bit condition as shown in Figure 1.

The device is ready for the next communication after above steps have been completed.

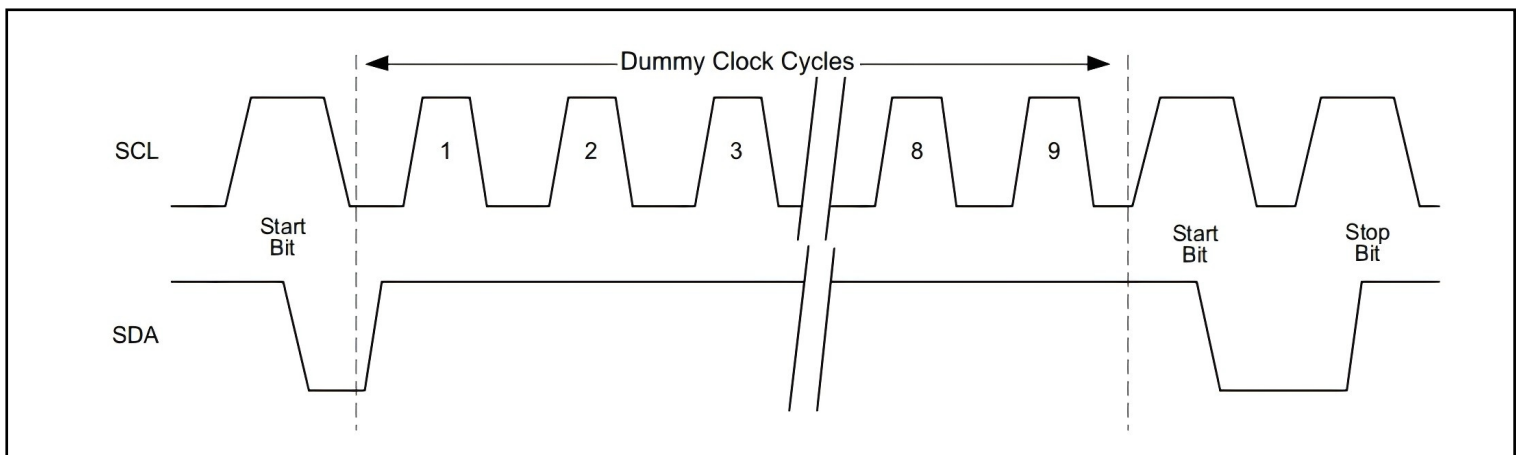


Figure 1. Software reset

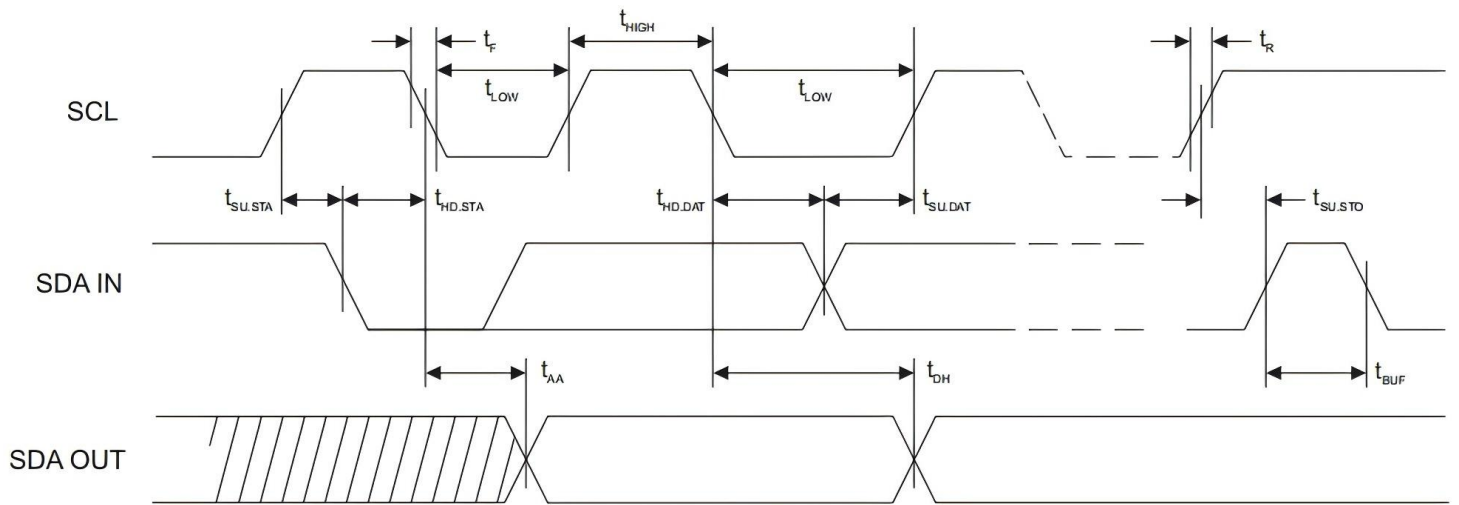


Figure 2. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

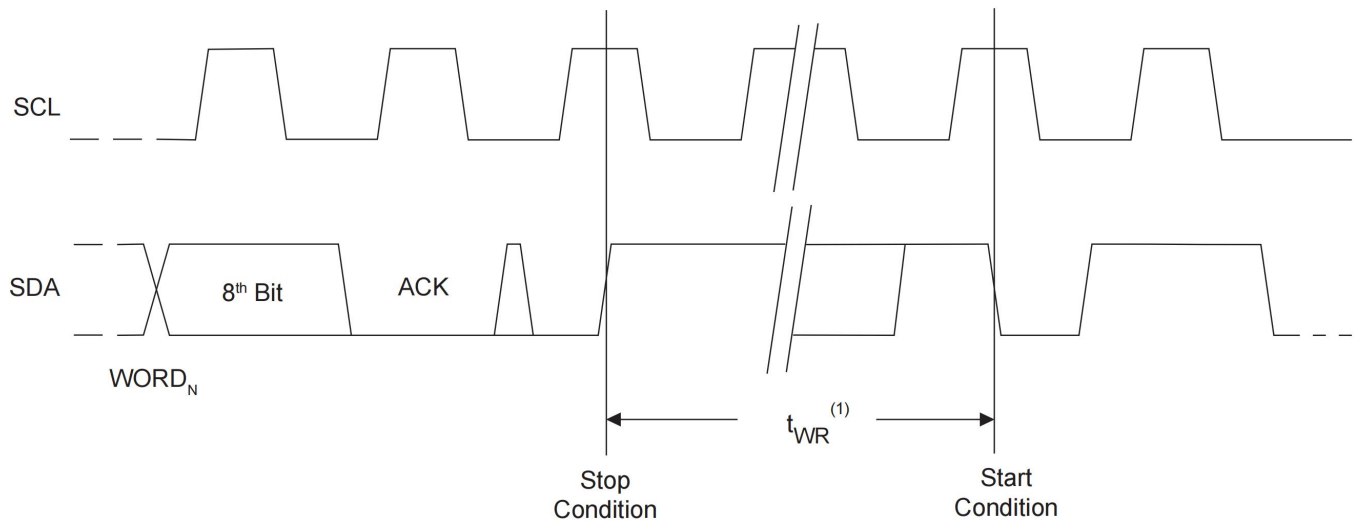


Figure 3. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O

Notes: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

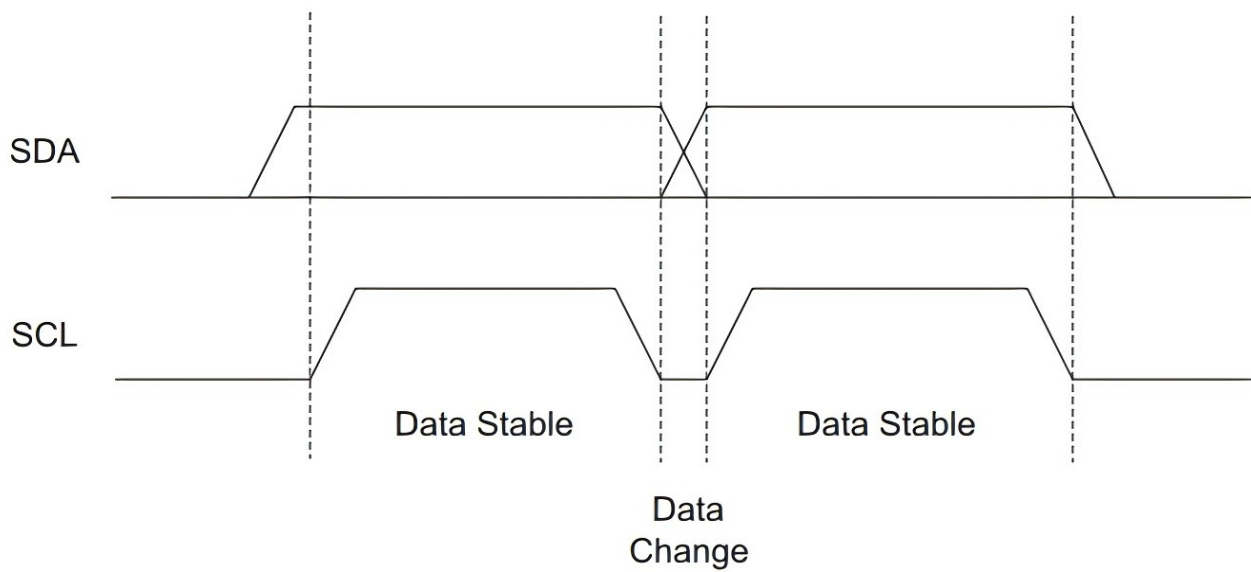


Figure 4.Data Validity

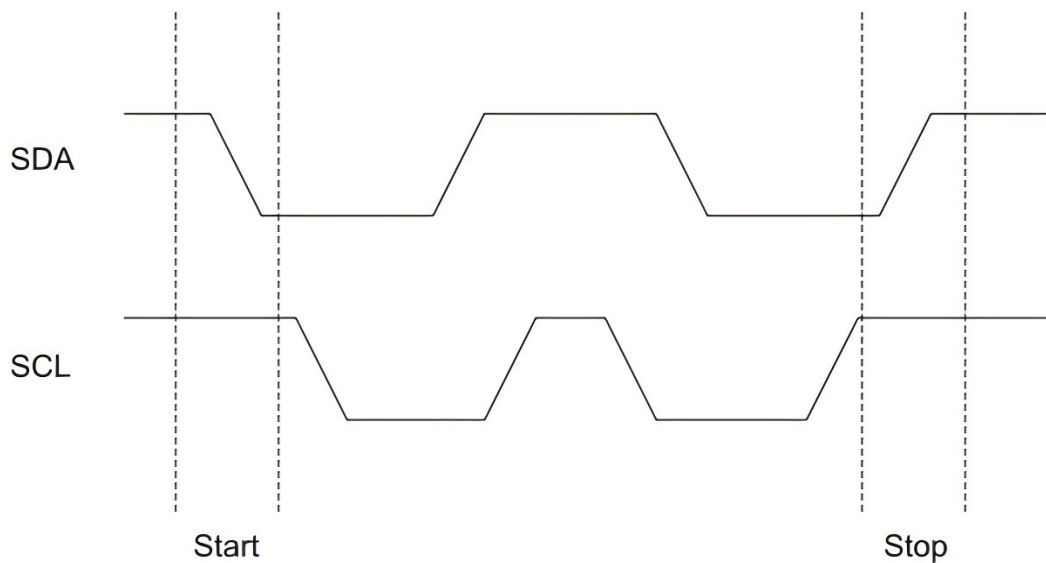


Figure 5.Start and Stop Definition

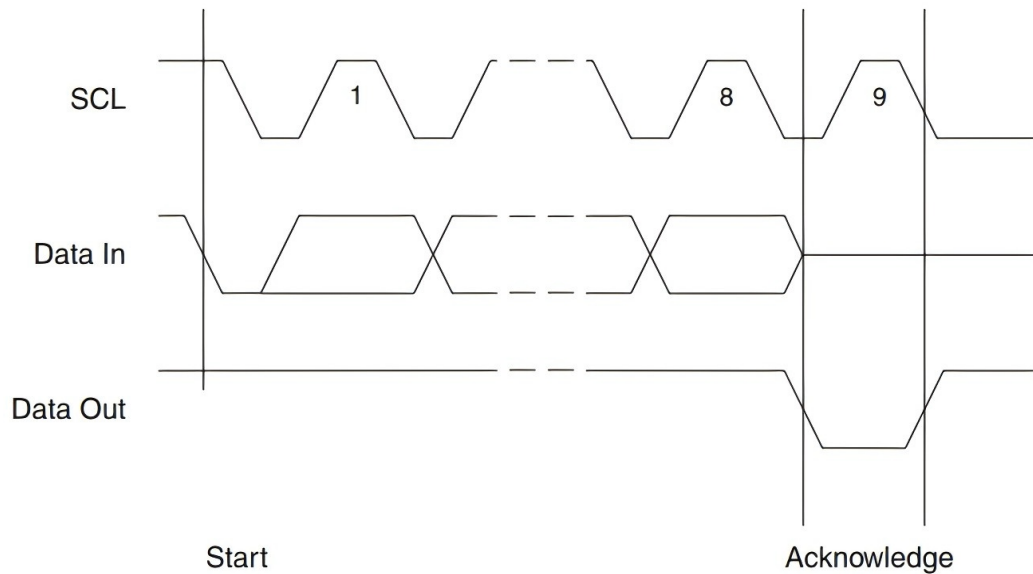


Figure 6.Output Acknowledge

Device Addressing

The 1-Kbit and 2-Kbit EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a Read or Write operation.

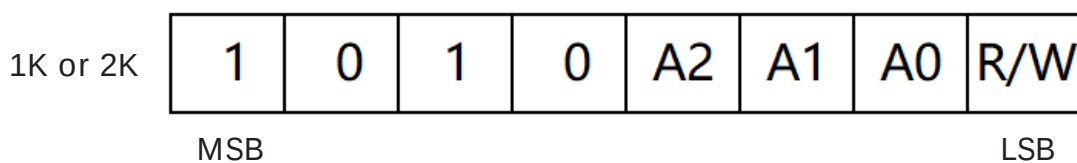
The device address word consists of a mandatory '1010' (0xA) sequence for the first four most significant bits as shown in Figure 7. This is common to all Serial EEPROM devices.

The next three bits are the A₂, A₁, and A₀ device address bits for the 1K and 2K EEPROM. These three bits must compare to their corresponding hard-wired input pins A₂, A₁, and A₀ in order for the part to acknowledge.

The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is high and a Write operation is initiated if this bit is low.

Upon a valid compare of the device address with hard-wired input pins A₂, A₁, and A₀, the EEPROM will output a zero. If a compare is not successfully made, the chip will return to a standby state.

Figure 7.Device Address





Write Operations

Byte Write: A Byte Write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8).

Page Write: The 1-Kbit and 2-Kbit EEPROM are capable of an 8-byte Page Write. A Page Write is initiated the same as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first dataword, the microcontroller can transmit up to seven data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a Stop condition (see Figure 9).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Data Security: The AT24C01C/02C has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.



Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an zero but does generate a following Stop condition (see Figure 10).

Random Read: A Random Read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 11).

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 12).

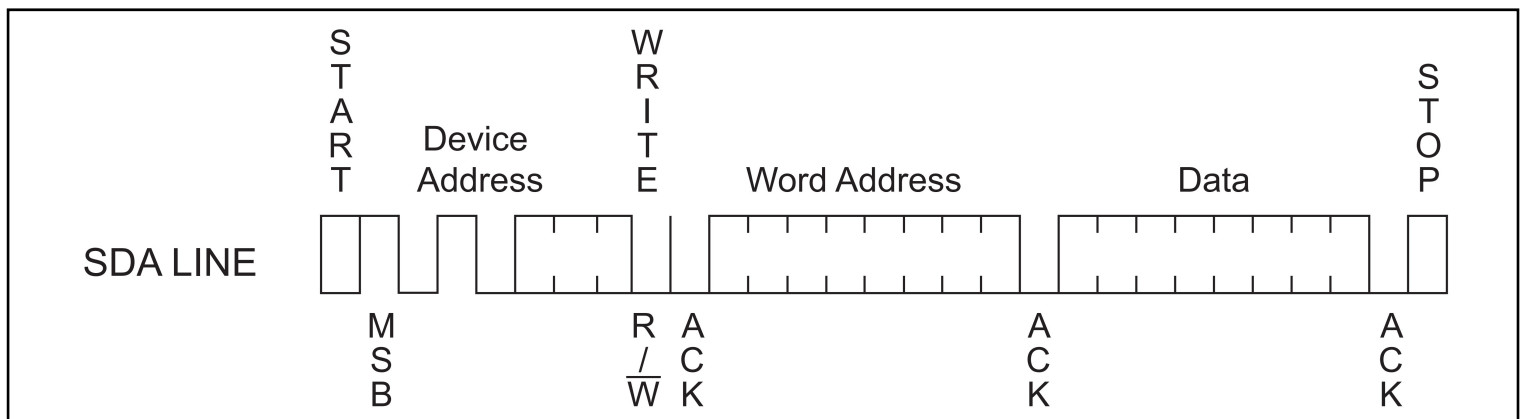


Figure 8. Byte Write

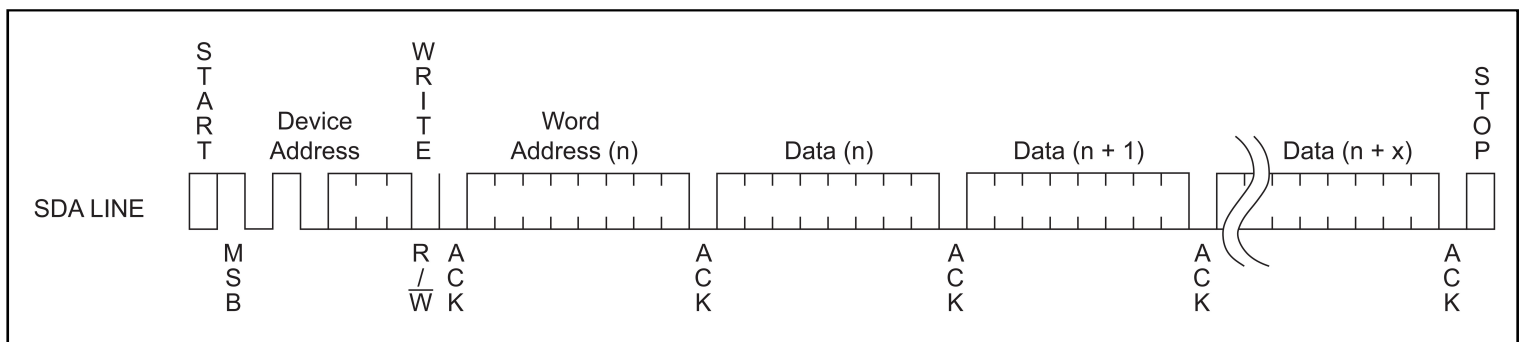


Figure 9. Page Write

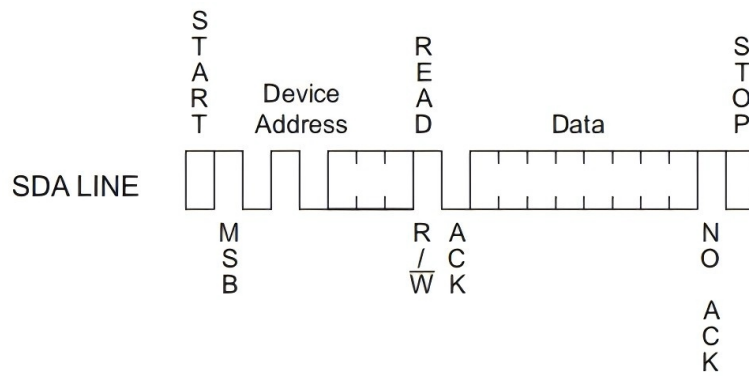


Figure 10.Current Address Read

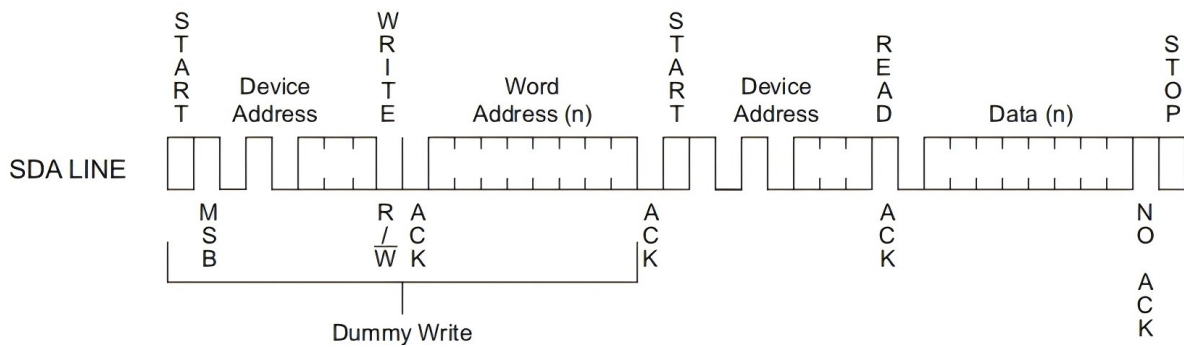


Figure 11.Random Read

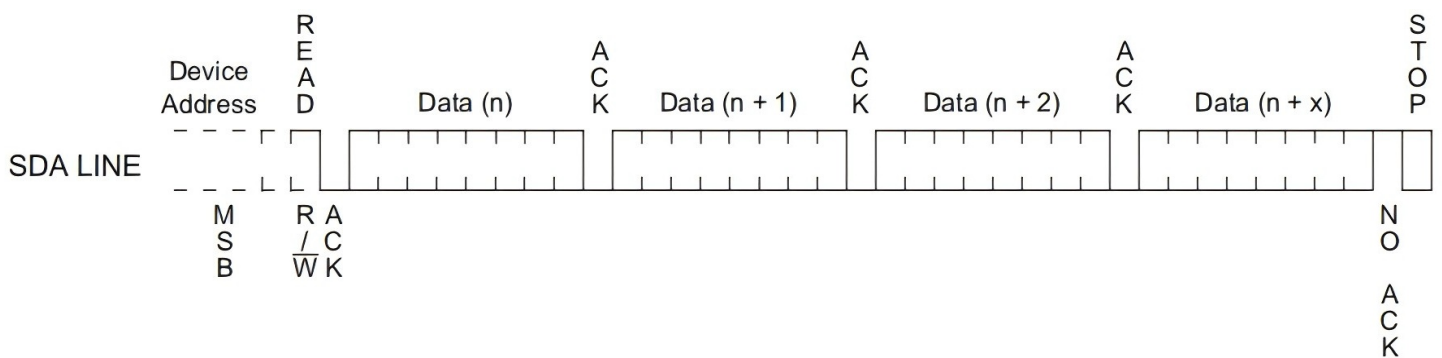


Figure 12.Sequential Read



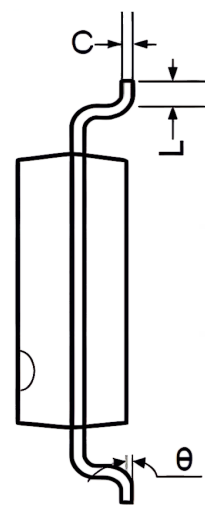
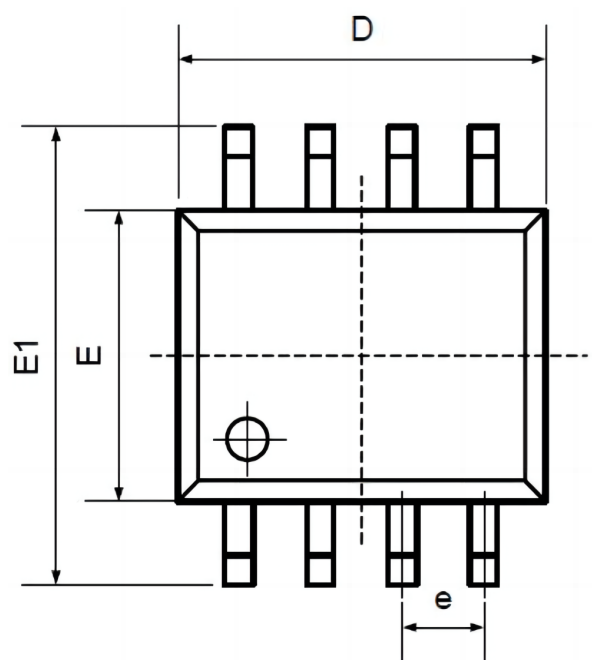
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
AT24C01C-PUM-TUDI	DIP8	Tube,50,A box of 2000	24C01C	-40°C to 85°C
			01CM	
AT24C01C-SSHM-T-TUDI	SOP8	Tape,Reel,4000	01CM	
AT24C01C-XHM-T-TUDI	TSSOP8	Tape,Reel,4000	24C01C	
			01CM	
AT24C01C-STUM-T-TUDI	SOT23	Tape,Reel,3000	24C01C	
			1CMU	
AT24C02C-PUM-TUDI	DIP8	Tube,50,A box of 2000	24C02C	
			02CM	
AT24C02C-SSHM-T-TUDI	SOP8	Tape,Reel,4000	02CM	
AT24C02C-XHM-T-TUDI	TSSOP8	Tape,Reel,4000	24C02C	
			02CM	
AT24C02C-STUM-T-TUDI	SOT23	Tape,Reel,3000	24C02C	
			2CMU	

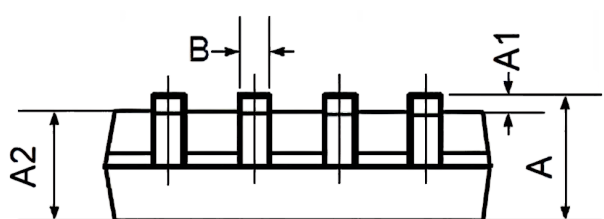
Revision history

	Date	Revision	Page
V1.0	2020/3	New	1-18
V1.1	2024/4	Update model and PDF template	1-19

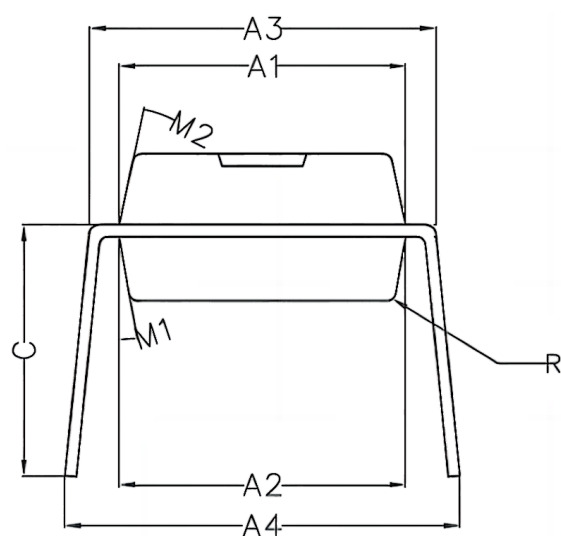
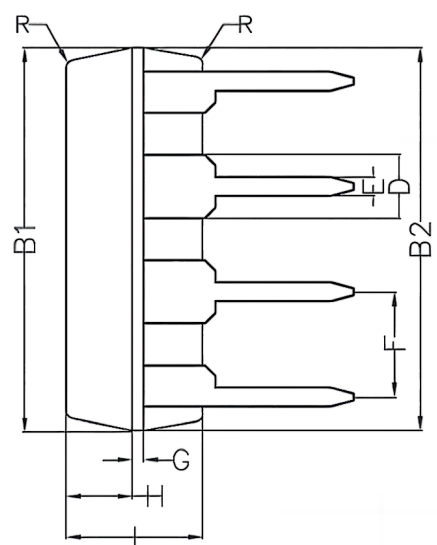
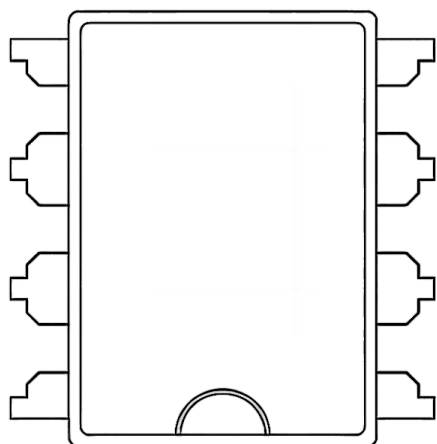
Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

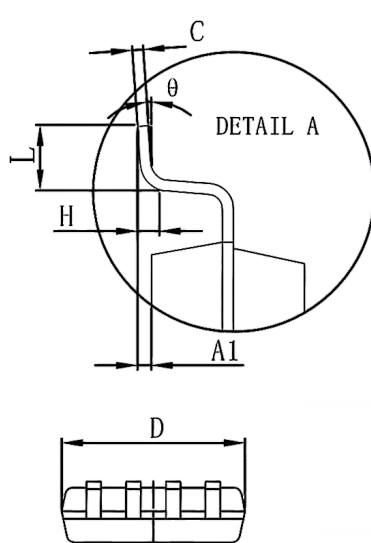
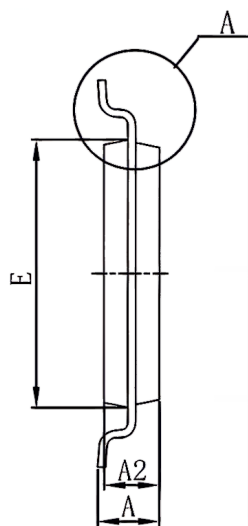
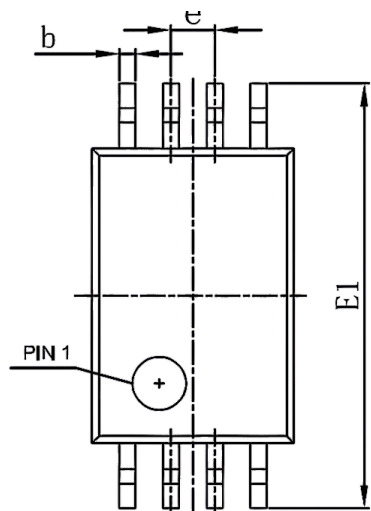


Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

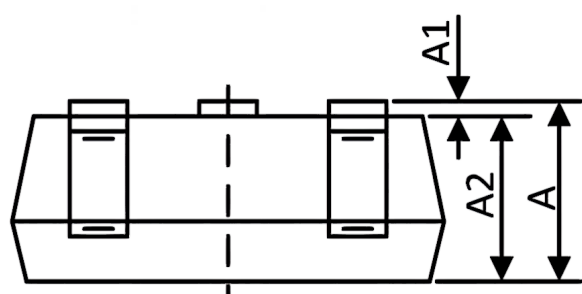
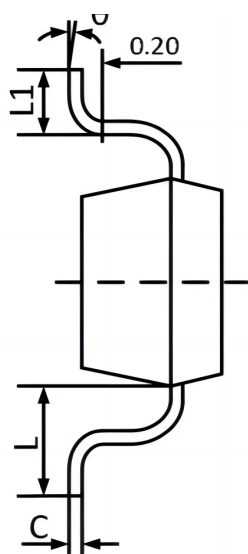
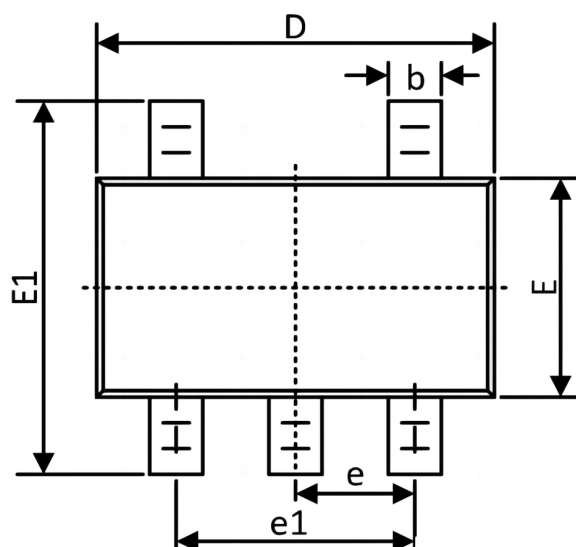
Package TSSOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	



Package SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



Important statement:

- TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.
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