# BIWIN qNAND Datasheet

## eMMC5.1

## MLC NAND

**Ver.3.0**

Mar. 2022

深圳佰维存储科技股份有限公司
BIWIN STORAGE TECHNOLOGY CO.,LTD.

*REFERENCE ONLY TO ANY INTELLECTUAL PROPERTY RIGHTS IN BIWIN PRODUCT OR TECHNOLOGY. ALL INFORMATION IN THIS DOCUMENT IS PROVIDED.*

## Revision History

| Version | Date | Description |
|---|---|---|
| 1.0 | Jun. 2021 | First Release |
| 2.0 | Sept. 2021 | Version update |
| 3.0 | Mar. 2022 | Version update |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

# Table of Contents

1. Introduction ..... 4
1.1 Overview ..... 4
1.2 Product Information ..... 4
1.3 Performance ..... 4
1.4 Features ..... 5
1.5 Functional Block Diagram ..... 6
1.6 Function Description ..... 6
1.7 Independent Technology ..... 7
1.8 Error Detect and Management ..... 7
2. Package Dimensions ..... 8
2.1 Physical Specifications ..... 8
2.1.1 11.5mm*13mm*0.9mm Package Dimension ..... 8
2.1.2 153 Ball Pin Configuration ..... 9
3. eMMC Registers ..... 10
3.1 OCR Register ..... 10
3.2 CID Register ..... 11
3.3 CSD Register ..... 11
3.4 Extended CSD Register ..... 13
3.5 RCA Register ..... 21
3.6 DSR (Drivers Stage Register) ..... 21
4. Technical Notes ..... 22
4.1 General Description ..... 22
4.2 HS400 Bus Speed Mode ..... 22
4.2.1 The HS400 mode features ..... 22
4.2.2 HS400 Device Input Timing ..... 23
4.2.3 HS400 Device Output Timing ..... 24
4.2.4 HS400 Device Output Timing (cont'd) ..... 25
4.3. Additional Timing changes in HS400 mode ..... 26
4.3.1 Write Timing ..... 26
4.3.2 Read Timing ..... 26
4.4 Production State Awareness ..... 27
4.5 Field Firmware Update (FFU) ..... 27
4.6 Sleep Notification ..... 28
4.7 Secure Removal Type ..... 30
4.8 Overshoot/Undershoot Specification ..... 31
4.9 HS400 Reference Load ..... 32
4.10 RPMB Throughput Improvement ..... 33
4.11 User Density ..... 33
4.11.1 User Data Area Capacity ..... 33
4.11.2 Capacity according to partition ..... 33
5. Electrical Characteristics ..... 34
5.1 DC Power Specification ..... 34
5.2 Power Requirement ..... 35
5.2.1 Sleep Current ..... 35
5.2.2 Active Power Consumption during operation ..... 35
6. eMMC Connection Guide ..... 36

# 1. Introduction

## 1.1 Overview

BIWIN eMMC is an embedded flash storage designed in the form of LFBGA package, using MMC protocol V5.1 interface. It combines advanced NAND flash and intelligent flash controller in single package, offering excellent performance and high reliability storage solution to embedded applications.

With industry standard eMMC 5.1 protocol, BIWIN eMMC is empowered with many new features such as Discard, Boot partitions, Secure Erase, and Trim, which are optimal for code reliability and data storage.

eMMC has an intelligent controller to manage interface protocols, data storage and retrieval, error detect and correction(ECC) algorithms, defect handling and diagnostics, and power management. The firmware inside has functions of Wear Leveling Management, Garbage Collection, and Bad Block Management.

eMMC also has features as small size, low power consumption, non-volatile, wide range of operation temperature, high reliability, which makes eMMC the ideal solution for smart phones, Tablet, digital cameras, PDAs, PMP, GPS, media player and etc.

## 1.2 Product Information

| eMMC Part ID | Capacity | Size | Package |
|---|---|---|---|
| BWCTAK611G16G | 16GB | 11.5*13*0.9mm | LFBGA153 |

## 1.3 Performance

| Capacity | Typical Sequential Read (MB/s) | Typical Sequential Write(MB/s) |
|---|---|---|
| 16GB | 235MB/s | 110MB/s |

Note:

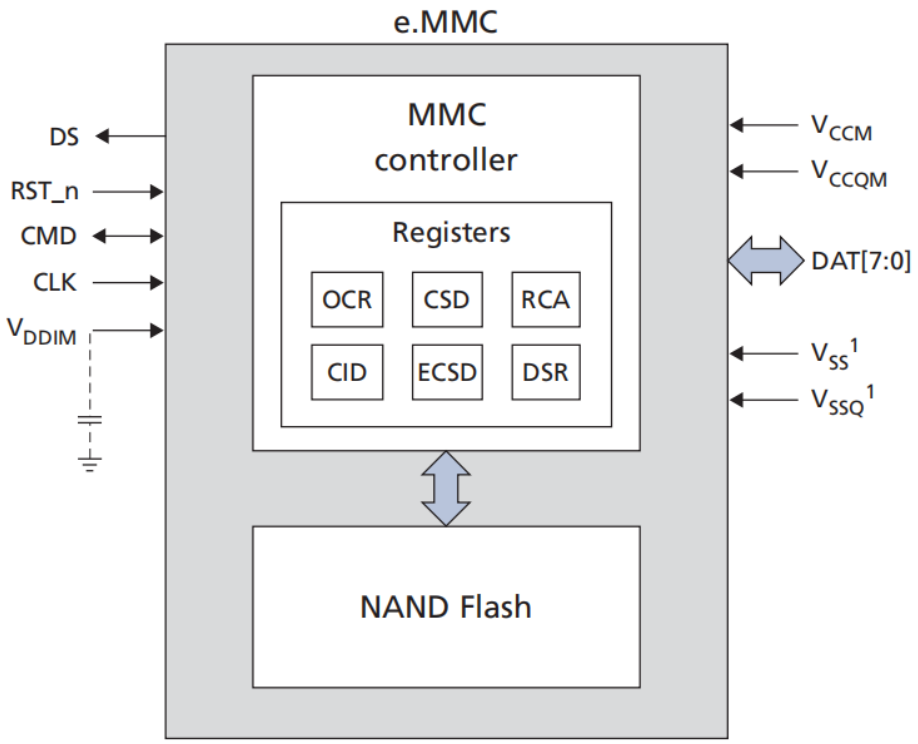
1. Test Condition : Test on MT6761 android O with user version, Bus width x8, HS400 @ Androbe nch 5.0.1 with default settings.

2. Table for reference only. Performance may vary according to platform.

## 1.4 Features

- Complies with the eMMC standard JESD84-B51
- 12 signal interface (including CMD, CLK, DS, DAT[7:0], and RST_n)
- Programmable bus width: 1-bit, 4-bit, and 8-bit
- Operating voltage range
  - Vcc(NAND): 2.7 - 3.6V
  - Vccq(Controller): 1.7 - 1.95V / 2.7 - 3.6V
- Support normal speed SDR mode and high speed DDR mode
- HS400 and HS200 mode support
- Up to 200MHz clock speed
- MMC Mode Command Class
- Class 0 (basic), Class 2 (block read), Class 4 (block write), Class 5 (erase), Class 6 (write protection), Class 7 (lock/unlock)
- High-speed, Dual Data Rate Boot support
- Supports Boot and Alternative Boot Mode
- Replay Protected Memory Block (RPMB)
- Secure Erase, Secure Trim, and Trim
- Enhanced Partition Attributes
- High Priority Interrupt (HPI)
- Background Operations
- Enhanced Reliable Write
- 32-bit RISC based architecture with advanced mapping technology
- Optimized algorithm for embedded system access
- Dynamic power management technology
- Quick standby, auto-suspend, and sleep operations
- Standby current: <100uA@25°C
- Dimensions& Package
  - 11.5mm x 13mm x 0.9mm LFBGA153ball
- Capacities: 16GB
- High data transfer speed
- Up to 104MB/s transfer rate(52MHz, DDR mode)
- Up to 400MB/s transfer rate(200MHz, HS400 mode)
- Operating temperature range
  - -25°C----- 85°C
- Storage temperature range
  - -40°C----- 85°C
- Soldering Temperature (10s) 260°C

## 1.5 Functional Block Diagram




Note: 1. VSS and VSSQ are internally connected.

**Figure.1 eMMC Functional Block Diagram**

## 1.6 Function Description

Biwin eMMC contains an intelligent eMMC Flash controller with JEDEC eMMC V5.1 interface, which achieves high data transfer rate and provides many new features. The feature was not founded in the other types of storage device:

- Support Multiple User Data Partition with Enhanced User Data Area options
- Signed access to a replay Protected Memory Block
- Support dual data rate transfer
- High speed boot
- Enhanced Write Protection with Permanent and Partial protection options
- Support hardware reset signal
- Optional high priority interrupt mechanism

## 1.7 Independent Technology

The eMMC V5.1 interface defines the communication protocol between host and eMMC device. It can not only manage wear leveling, bad block management and ECC, but also isolate host from advancing Nand flash technology. Nand flash memory, as main part of eMMC devices, is always rapidly changed to keep close tabs on generation shift. Thanks to this eMMC interface, the host can be independent of Nand flash change, which greatly accelerates product development and reduces time-to-market.

## 1.8 Error Detect and Management

Biwin eMMC incorporates advanced technology for error detect and management. If a defective block is identified, eMMC can completely replace the defective block with one of the spare blocks. This process is invisible to the host and generally does not affect data space allocated for the user.

# 2. Package Dimensions

## 2.1 Physical Specifications

### 2.1.1 11.5mm*13mm*0.9mm Package Dimension

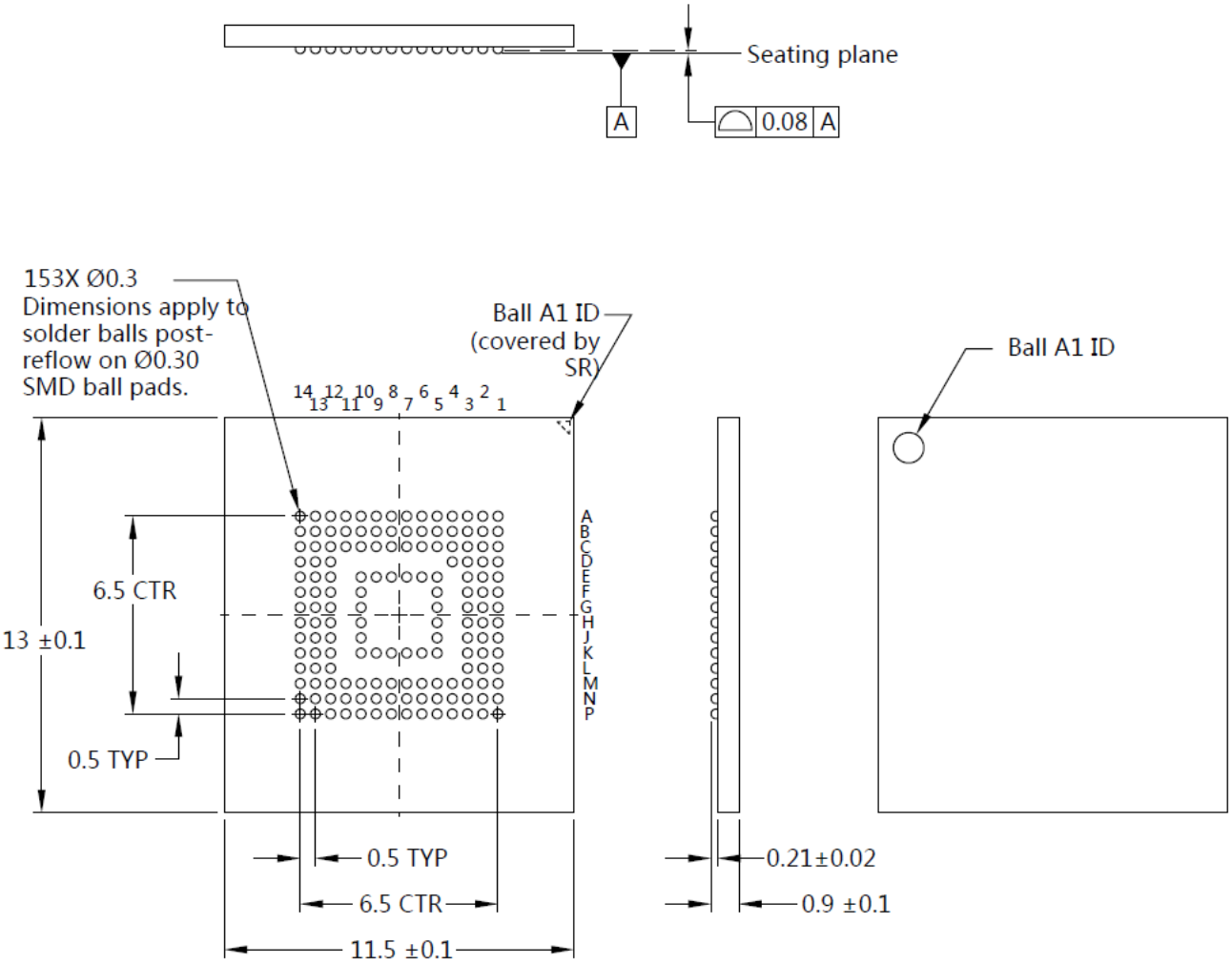



**Figure.2 11.5mm * 13mm * 0.9mm Package Dimension**

## 2.1.2 153 Ball Pin Configuration

TFBGA153 Pin Out

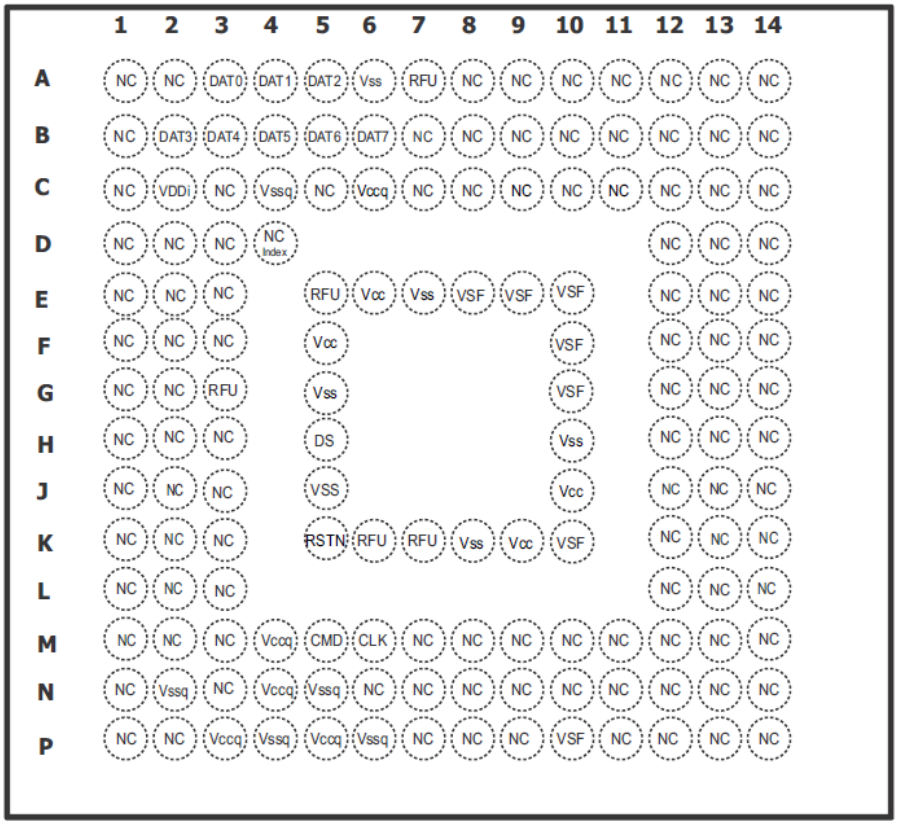



**Figure.3 BGA153 Pin Out**

| Pin Number | Name | Pin Number | Name | Pin Number | Name | Pin Number | Name |
|---|---|---|---|---|---|---|---|
| **A3** | DAT0 | **C4** | Vssq | **G10** | VSF | **M5** | CMD |
| **A4** | DAT1 | **C6** | Vccq | **H5** | DS | **M6** | CLK |
| **A5** | DAT2 | **E6** | Vcc | **H10** | Vss | **N2** | Vssq |
| **A6** | Vss | **E7** | Vss | **J5** | VSS | **N4** | Vccq |
| **B2** | DAT3 | **E8** | VSF | **J10** | Vcc | **N5** | Vssq |
| **B3** | DAT4 | **E9** | VSF | **K5** | RSTN | **P3** | Vccq |
| **B4** | DAT5 | **E10** | VSF | **K8** | Vss | **P4** | Vssq |
| **B5** | DAT6 | **F5** | Vcc | **K9** | Vcc | **P5** | Vccq |
| **B6** | DAT7 | **F10** | VSF | **K10** | VSF | **P6** | Vssq |
| **C2** | VDDi | **G5** | Vss | **M4** | Vccq | **P10** | VSF |

# 3. eMMC Registers

Within the eMMC interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR.

These registers can only be accessed by corresponding commands. The OCR, CID and CSD registers carry the eMMC specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. The EXT_CSD register carries both eMMC specific information and actual configuration parameters.

## 3.1 OCR Register

The 32-bit operation conditions register stores the VCCQ voltage profile of the eMMC. In addition, the register contains a status information bit. This status bit is set if the eMMC power up procedure has been finished. The OCR register shall be implemented by eMMC.

| OCR bit | Description | eMMC |
|---|---|---|
| [6:0] | Reserved | 000 0000b |
| [7] | 1.7-1.95 | 1b |
| [14:8] | 2.0-2.6 | 000 0000b |
| [23:15] | 2.7-3.6 | 1 1111 1111b |
| [28:24] | Reserved | 0 0000b |
| [30:29] | Access Mode | 00b (byte mode) |
| | | 10b (sector mode) |
| [31] | eMMC power up status bit(busy)[1] | |

**Table.1 OCR Register Value**

This bit is set to low if the eMMC has not finished the power up routine.

## 3.2 CID Register

| Name | Field | Width | CID-slice | CID Value | COMMENT |
|---|---|---|---|---|---|
| Manufacturer ID | MID | **8** | [127:120] | 0xF4 | BIWIN Manufacture ID |
| Reserved | | **6** | [119:114] | - | |
| Device/BGA | CBX | **2** | [113:112] | 0x01 | |
| OEM/Application ID | OID | **8** | [111:104] | 0x22 | |
| Product name | PNM | **48** | [103:56] | 0x426977696E20 | Biwin |
| Product revision | PRV | **8** | [55:48] | - | |
| Product serial number | PSN | **32** | [47:16] | random number | |
| Manufacturing date | MDT | **8** | [15:8] | Year Month | |
| CRC7 checksum | CRC | **7** | [7:1] | - | |
| not used, always '1' | - | **1** | [0:0] | - | |

**Table.2 CID Register Value**

## 3.3 CSD Register

The Device-Specific Data register provides information on how to access time, data transfer speed, and whether the DSR register can be used, etc. The programmable part of the register can be changed by CMD27. The type of the entries in Table 6 below is coded as follows:

- R: Read only.
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

- W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

| Name | Field | Width | Type | CSD Slice | CSD Value | Note |
|---|---|---|---|---|---|---|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 3h | |
| System specification version | SPEC_VERS | 4 | R | [125:122] | 4h | |
| Reserved | - | 2 | R | [121:120] | - | |
| Data read access-time-1 | TAAC | 8 | R | [119:112] | Fh | |
| Data read access-time-2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] | 1h | |
| Max. bus clock frequency | TRAN_SPEED | 8 | R | [103:96] | 32h | |
| Device Command classes | CCC | 12 | R | [95:84] | F5h | |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] | 9h | |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 0h | |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0h | |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0h | |
| DSR implemented | DSR_IMP | 1 | R | [76:76] | 0h | |
| Reserved | - | 2 | R | [75:74] | - | |
| Device size | C_SIZE | 12 | R | [73:62] | FFFh | |
| Max.read current @VDD min | VDD_R_CURR_MIN | 3 | R | [61:59] | 7h | |
| Max.read current @VDD max | VDD_R_CURR_MAX | 3 | R | [58:56] | 7h | |
| Max.write current @VDD min | VDD_W_CURR_MIN | 3 | R | [55:53] | 7h | |
| Max.write current @VDD max | VDD_W_CURR_MAX | 3 | R | [52:50] | 7h | |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 7h | |
| Erase group size | ERASE_GRP_EN | 5 | R | [46:42] | 1Fh | |
| Erase group size multiplier | ERASE _GRP_MULT | 5 | R | [41:37] | 1Fh | |
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] | Fh | |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31:31] | 1h | |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | 0h | |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] | 2h | |
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 9h | |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0h | |
| Reserved | - | 1 | - | [20:17] | - | |

| Name | Field | Width | Type | CSD Slice | CSD Value | Note |
|---|---|---|---|---|---|---|
| Content protection application | CONTENT_PROT_APP | 1 | R | [16:16] | 0h | |
| File format group | FILE_FORMAT_GRP | 1 | R/W | [15:15] | 0h | |
| Copy flag(OTP) | COPY | 1 | R/W | [14:14] | 1h | |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | [13:13] | 0h | |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] | 0h | |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | 0h | |
| ECC code | ECC | 2 | R/W/E | [9:8] | 0h | |
| CRC | CRC | 7 | R/W/E | [7:1] | TBD | |
| Not used, always' 1' | - | 1 | - | [0:0] | TBD | |

**Table.3 CSD Register Value**

## 3.4 Extended CSD Register

The Extended CSD register defines the eMMC properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment, which defines the configuration the eMMC is working in. These modes can be changed by the host by means of the SWITCH command.

- R: Read only.
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C_P: Writable after value cleared by power failure and H/W rest assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Reserved | - | 6 | - | [511:506] | - | |
| Extended Security Commands Error | EXT_SECURITY_ ERR | 1 | R | [505] | 0h | |
| Supported command sets | S_CMD_SET | 1 | R | [504] | 1h | |
| HPI features | HPI_FEATURES | 1 | R | [503] | 1h | |
| Background operations support | BKOPS_SUPPORT | 1 | R | [502] | 1h | BKOPS supported |
| Max packed read commands | MAX_PACKED_READS | 1 | R | [501] | 3Fh | Max. 63 commands in a packed command |
| Max packed write commands | MAX_PACKED_WRITES | 1 | R | [500] | 3Fh | Max. 63 commands in a packed command |
| Data Tag Support | DATA_TAG_SUPPORT | 1 | R | [499] | 0h | |
| Tag Unit Size | TAG_UNIT_SIZE | 1 | R | [498] | 0h | |
| Tag Resources Size | TAG_RES_SIZE | 1 | R | [497] | 0h | |
| Context management capabilities | CONTEXT_CAPABILITIES | 1 | R | [496] | 78h | Max Tag Size = 8*2 = 16MB; Max_ Context ID = 8 |
| Large Unit size | LARGE_UNIT_SIZE_M1 | 1 | R | [495] | 1h | 1MB*2=2MB |
| Extended partitions attribute support | EXT_SUPPORT | 1 | R | [494] | 3h | Support "System code"; Support "Non-persistent" |
| Support modes | SUPPORT_MODES | 1 | R | [493] | 1h | FFU is Supported |
| FFU features | FFU_FEATURES | 1 | R | [492] | 0h | |
| Operation code time out | OPERATION_CODE_TIMEOUT | 1 | R | [491] | 17h | |
| FFU Argument | FFU_ARG | 4 | R | [490:487] | 6600h | |
| Barrier support | BARRIER_SUPPORT | 1 | R | [486] | 1h | |
| Reserved | - | 177 | - | [485:309] | - | |
| CMD Queuing Support | CMDQ_SUPPORT | 1 | R | [308] | 1h | Support CMDQ |
| CMD Queuing Depth | CMDQ_DEPTH | 1 | R | [307] | 1Fh | 32 CMDQ_DEPTH |
| Reserved | - | 1 | - | [306] | - | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4 | R | [305:302] | 0h | |
| Vendor proprietary health report | VENDOR_PROPRIETARY_HEALTH_REPORT | 32 | R | [301:270] | 0h | |
| Device life time estimation type B | DEVICE_LIFE_TIME_EST_TYPE_B | 1 | R | [269] | 1h | |
| Device life time estimation type A | DEVICE_LIFE_TIME_EST_TYPE_A | 1 | R | [268] | 1h | |
| Pre EOL information | PRO_EOL_INFO | 1 | R | [267] | 0h | |
| Optimal read size | OPTIMAL_READ_SIZE | 1 | R | [266] | 0h | |
| Optimal write size | OPTIMAL_WRITE_SIZE | 1 | R | [265] | 0h | |
| Optimal trim unit size | OPTIMAL_TRIM_UNIT_SIZE | 1 | R | [264] | 0h | |
| Device version | DEVICE_VERSION | 2 | R | [263:262] | TBD | |
| Firmware version | FIREWARE_ VERSION | 8 | R | [261:254] | TBD | Not same to PRV |
| Power class for 200MHz,DDR at VCC=3.6V | PWR_CL_DDR_200_360 | 1 | R | [253] | 0h | |
| Cache size | CACHE_SIZE | 4 | R | [252:249] | 0h | |
| Generic CMD6 timeout | GENERIC_CMD6_TIME | 1 | R | [248] | 64h | |
| Power off notification (long) timeout | POWER_OFF_LONG_TIME | 1 | R | [247] | 64h | |
| Background operations status | BKOPS_STATUS | 1 | R | [246] | 0h | |
| Number of Correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | 4 | R | [245:242] | 0h | |
| First initialization time after partitioning | INI_TIMEOUT_AP | 1 | R | [241] | Ah | |
| Cache flushing policy | CACHE_FLUSH_POLICY | 1 | R | [240] | 0h | |
| Power class for 52MHz,DDR at Vcc=3.6V | PWR_CL_DDR_52_360 | 1 | R | [239] | 0h | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Power class for 52MHz, DDR at 1.95V | PWR_CL_DDR_52_195 | 1 | R | [238] | 0h | |
| Power class for 200MHz At Vccq=1.95V, Vcc=3.6V | PWR_CL_200_195 | 1 | R | [237] | 0h | |
| Power class for 200MHz at Vccq=1.3V, Vcc=3.6V | PWR_CL_200_130 | 1 | R | [236] | 0h | |
| Minimum write performance for 8 bit at 52MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | R | [235] | 0h | |
| Minimum read performance for 8 bit at 52MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | R | [234] | 0h | |
| Reserved | - | 1 | - | [233] | - | |
| TRIM multiplier | TRIM_MULT | 1 | R | [232] | 3h | |
| Secure feature support | SEC_FEATURE_SUPPORT | 1 | R | [231] | 55h | |
| Secure erase multiple | SEC_ERASE_MULT | 1 | R | [230] | Ah | |
| Secure trim multiple | SEC_ERASE_MULT | 1 | R | [229] | Ah | |
| Boot information | BOOT_INFO | 1 | R | [228] | 7h | |
| Reserved | - | 1 | - | [227] | - | |
| Boot partition size | BOOT_SIZE_MULTI | 1 | R | [226] | 20h | |
| Access size | ACC_SIZE | 1 | R | [225] | 6h | |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | 1 | R | [224] | 1h | |
| High-capacity erase timeout | ERASE_TIMEOUT_MULT | 1 | R | [223] | 3h | |
| Reliable write sector count | REL_WR_SEC_C | 1 | R | [222] | 1h | |
| High-capacity write protect group size | HC_WP_GRP_SIZE | 1 | R | [221] | 10h | |
| Sleep current (VCC) | S_C_VCC | 1 | R | [220] | 7h | |
| Sleep current (VCCQ) | S_C_VCCQ | 1 | R | [219] | 7h | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Production state awareness timeout | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | R | [218] | 11h | |
| Sleep/awake timeout | S_A_TIMEOUT | 1 | R | [217] | 10h | |
| Sleep Notification timeout | SLEEP_NOTIFICATION_TIME | 1 | R | [216] | Ch | |
| Sector count | SEC_COUNT | 4 | R | [215:212] | 16GB: 1D20000h | |
| Secure write protect information | SECURE_WP_INFC | 1 | R | [211] | 1h | |
| Minimum write performance for 8bit at 52MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 0h | |
| Minimum read performance for 8bit at 52MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 0h | |
| Minimum write performance for 8bit at 26MHz,for 4bit at 52MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 0h | |
| Minimum read performance for 8bit at 26MHz,for 4bit at 52MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 0h | |
| Minimum write performance for 8bit at 26MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 0h | |
| Minimum read performance for 8bit at 26MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 0h | |
| Reserved | - | 1 | - | [204] | - | |
| Power class for 26MHz at 3.6V 1R | PWR_CL_26_360 | 1 | R | [203] | 0h | |
| Power class for 52MHz at 3.6V | PWR_CL_52_360 | 1 | R | [202] | 0h | |
| Power class for 26MHz at 1.95V | PWR_CL_26_195 | 1 | R | [201] | 0h | |
| Power class for 52MHz at 1.95V | PWR_CL_52_195 | 1 | R | [200] | 0h | |
| Partition switching | PARTITION_SWITCH_TIME | 1 | R | [199] | 1h | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | 1 | R | [198] | Ah | |
| I/O Driver Strength | DRIVER_STRENGTH | 1 | - | [197] | 1Fh | |
| Device type | DEVICE_TYPE | 1 | R | [196] | 57h | |
| Reserved | - | 1 | - | [195] | - | |
| CSD structure | CSD_STRUCTURE | 1 | R | [194] | 2h | |
| Reserved | - | 1 | - | [193] | - | |
| Extended CSD revision | EXT_CSD_REV | 1 | R | [192] | 8h | |
| Command set | CMD_SET | 1 | R/W/E_P | [191] | 0h | |
| Reserved | - | 1 | - | [190] | - | |
| Command set revision | CMD_SET_REV | 1 | R | [189] | 0h | |
| Reserved | - | 1 | R | [188] | - | |
| Power class | POWER_SUPPORT | 1 | R | [187] | 0h | |
| Reserved | - | 1 | - | [186] | - | |
| High-speed interface timing | HS_TIMING | 1 | W/E_P | [185] | 1h | |
| Strobe support | STROBE_SUPPORT | 1 | R | [184] | 1h | |
| Bus width mode | BUS_WIDTH | 1 | W/E_P | [183] | 6h | |
| Reserved | - | 1 | - | [182] | - | |
| Erased memory content | ERASED_MEM_CONT | 1 | R | [181] | 0h | |
| Reserved | - | 1 | - | [180] | - | |
| Partition configuration | PARTITION_CONFIRATION | 1 | R/W/E<br>R/W/E_P | [179] | 0h | |
| Boot configuration protection | BOOT_COMFIG_PROT | 1 | R/W<br>R/W/C_P | [178] | 0h | |
| Boot bus condition | BOOT_BUS_CONDITION | 1 | R/W/E | [177] | 0h | |
| Reserved | - | 1 | - | [176] | - | |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W/E | [175] | 0h | |
| Boot write protection status register | BOOT_WP_STATUS | 1 | R | [174] | 0h | |
| Boot area protection status register | BOOT_WP | 1 | R/W<br>R/W/C_P | [173] | 0h | |
| Reserved | - | 1 | - | [172] | - | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| User area write protection register | USER_WP | 1 | R/W<br>R/W/C_P<br>R/W/E_P | [171] | 0h | |
| Reserved | - | 1 | - | [170] | - | |
| FW configuration | FW_CONFIG | 1 | R/W | [169] | 0h | |
| RPMB size | RPMB_SIZE_MULT | 1 | R | [168] | 20h | |
| Write reliability setting register | WR_REL_PARAM | 1 | R/W | [167] | 1Fh | |
| Write parameter setting register | WR_REL_PARAM | 1 | R | [166] | 5h | |
| Start sanitize operation | SANITIZE_START | 1 | W/E_P | [165] | 0h | |
| Manually start background operations | BKOPS_START | 1 | W/E_P | [164] | 0h | |
| Enable background operations handshake | BKOPS_EN | 1 | R/W<br>R/W/E | [163] | 0h | |
| H/W reset function | RST_ R_FUCTION | 1 | R/W | [162] | 1h | |
| HPI management | HPI_MGMT | 1 | R/W/E_P | [161] | 0h | |
| Partitioning Support | PARTITIONING_SUPPORT | 1 | R | [160] | 7h | |
| Max enhanced area size | MAX_ENH_SIZE_MULT | 3 | R | [159:157] | TBD | |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | [156] | 0h | |
| Partitioning setting | PARTITION_SETTING_ | 1 | R/W | [155] | 0h | |
| General purpose partition size | GP_SIZE_MULT | 12 | R/w | [154:143] | 0h | |
| Enhanced user data area size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 0h | |
| Enhanced user data start | ENH_START_ADDR | 4 | R | [139:136] | 0h | |
| Reserved | - | 1 | - | [135] | - | |
| Secure bad block | SEC_BAD_BLK_MGMNT | 1 | R | [134] | 0h | |
| Production state awareness | PRODUCTION_STATE_AWARENESS | 1 | R/W/E | [133] | 0h | |
| Package Case temperature is control | TCASE_SUPPORT | 1 | W/E_P | [132] | 0h | |
| Periodic Wake-up | PERIODIC_WAKEUP | 1 | R | [131] | 0h | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | R | [130] | 1h | |
| Reserved | - | 2 | - | [129:128] | - | |
| Vendor Specific Fields | VENDOR_SPECIFIC_FIELD | 64 | <vendor specific> | [127:64] | TBD | |
| Native sector size | NATIVE_SECTOR_SIZE | 1 | R | [63] | 0h | |
| Sector size emulation | USE_NATIVE_SECTOR | 1 | R/W | [62] | 0h | |
| Sector size | DATA_SECTOR_SIZE | 1 | R | [61] | 0h | |
| 1st initialization after | INI_TIMEOUT_EMU | 1 | R | [60] | Ah | |
| Class 6 commands | CLASS_6_CTRL | 1 | R | [59] | 0h | |
| Number of addressed | DYNCAP_NEEDED | 1 | R | [58] | 0h | |
| Exception events control | EXCEPTION_EVENTS_CTRL | 2 | R/W/E_P | [57:56] | 0h | |
| Exception events status | EXCEPTION_EVENTS_ST | 2 | R | [55:54] | 0h | |
| Extended Partitions attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | R/W | [53:52] | 0h | |
| Context configuration | CONTEXT_CONF | 15 | R/W/E_P | [51:37] | 0h | |
| Packed command status | PACKED_COMMAND_ST | 1 | R | [36] | 0h | |
| Packed command failure index | PACKED_FAILURE_INDEX | 1 | R | [35] | 0h | |
| Power Off Notification | POWER_OFF_NOTIFICAT | 1 | R | [34] | 0h | |
| Control to turn the Cache ON/OFF | CACHE_CTRL | 1 | R/W/E_P | [33] | 0h | |
| Flushing of the cache | FLUSH_CACHE | 1 | W/E_P | [32] | 0h | |
| Control to turn the barrier ON/OFF | BARRIER_CTRL | 1 | R/W | [31] | 1h | |
| Mode config | MODE_CONFIG | 1 | R/W/E_P | [30] | 0h | |
| Mode operation codes | MODE_OPERATION_CODES | 1 | W/E_P | [29] | 0h | |
| Reserved | - | 1 | TBD | [28:27] | - | |
| FFU status | FFU_STATUS | 1 | R | [26] | 0h | |

| Name | Field | Byte | Type | Slice | Value | Note |
|---|---|---|---|---|---|---|
| Pre loading data size | PRE_LOADING_DATA_SIZE | 4 | R/W/E_P | [25:22] | 0h | |
| Max pre loading data size | MAX_PRE_LOADING_DATA_E | 4 | R | [21:18] | TBD | |
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1 | R/W/E&R | [17] | 3h | |
| Secure removal type | SETURE_REMOVAL_TYPE | 1 | R/E&R | [16] | 3Bh | |
| Command queue mode enable | CMDQ_MODE_EN | 1 | R/W/E_P | [15] | 0h | |
| Reserved | - | 15 | - | [14:0] | - | |

NOTE: Reversed bits should read as ‘0’ .

**Table.4 Extended CSD Register Table**

## 3.5 RCA Register

The writable 16-bit relative device address register carries the device address assigned by the host during the device identification. This address is used for the addressing host device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x000 is reserved to set all devices into the stand-by status with CMD7.

## 3.6 DSR (Drivers Stage Register)

The 16-bit driver stage register (DSR) is described in detail in 0. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of device). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

# 4. Technical Notes

## 4.1 General Description

All communication between host and device is controlled by the host (master). The host sends commands, which result in a device response.

From eMMC4.51 to eMMC5.1, some new powerful functions are introduced, such as:

- HS400 ultra speed mode (Data Strobe Line)
- Production State Awareness function
- FFU function (Field Firmware Update)
- Sleep Notification in Power Off Notification
- Secure Removal Type
- Overshoot and undershoot
- Reference load for HS400
- RPMB address failure on Read operation

## 4.2 HS400 Bus Speed Mode

### 4.2.1 The HS400 mode features

| Driver Type Values | Support | Nominal Impedance | Approximated driving capability compared to Type0 | Remark |
|---|---|---|---|---|
| 0 | Mandatory | 50Ω | x1 | Default Driver Type, support up to 200MHz operation. |
| 1 | Optional | 33Ω | ×1.5 | Support up to 200MHz operation. |
| 2 | | 66Ω | ×0.75 | The weakest drive that supports up to 200MHz Operation. |
| 3 | | 100Ω | ×0.5 | For low noise and low EMI systems.<br>Maximal operating frequency is decided by Host design. |
| 4 | | 40Ω | ×1.2 | |

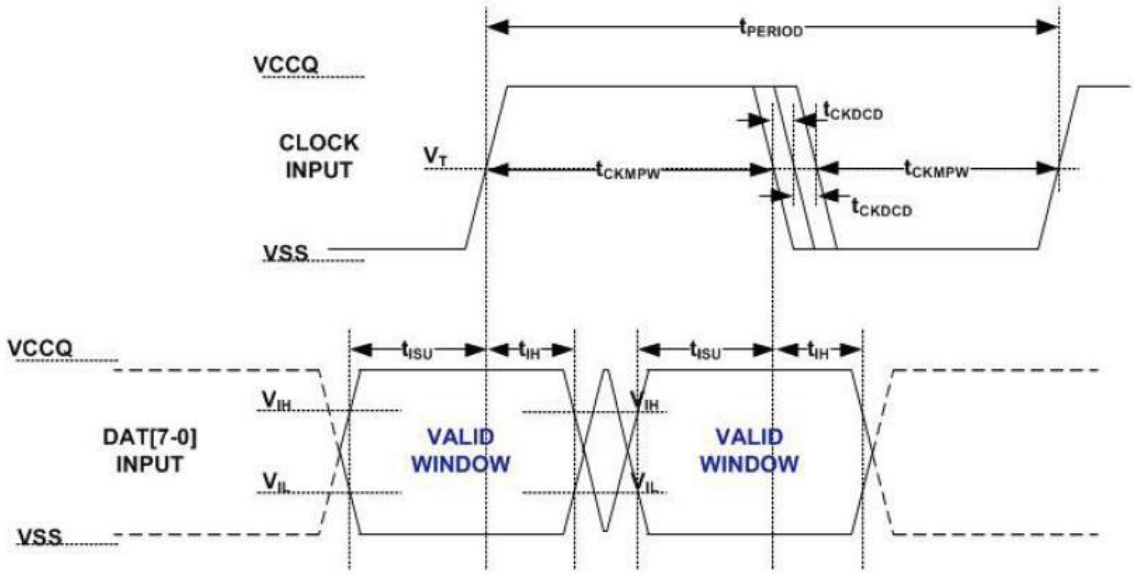
Note: Support of Driver Type-0 is mandatory for HS200 and HS400 device.

**Table.5 I/0 Driver Strength Types**

### 4.2.2 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.

The device input timing is shown in figure below.




Note: $V_T$ = 50% of $V_{CCQ}$, indicates clock reference point for timing measurements.

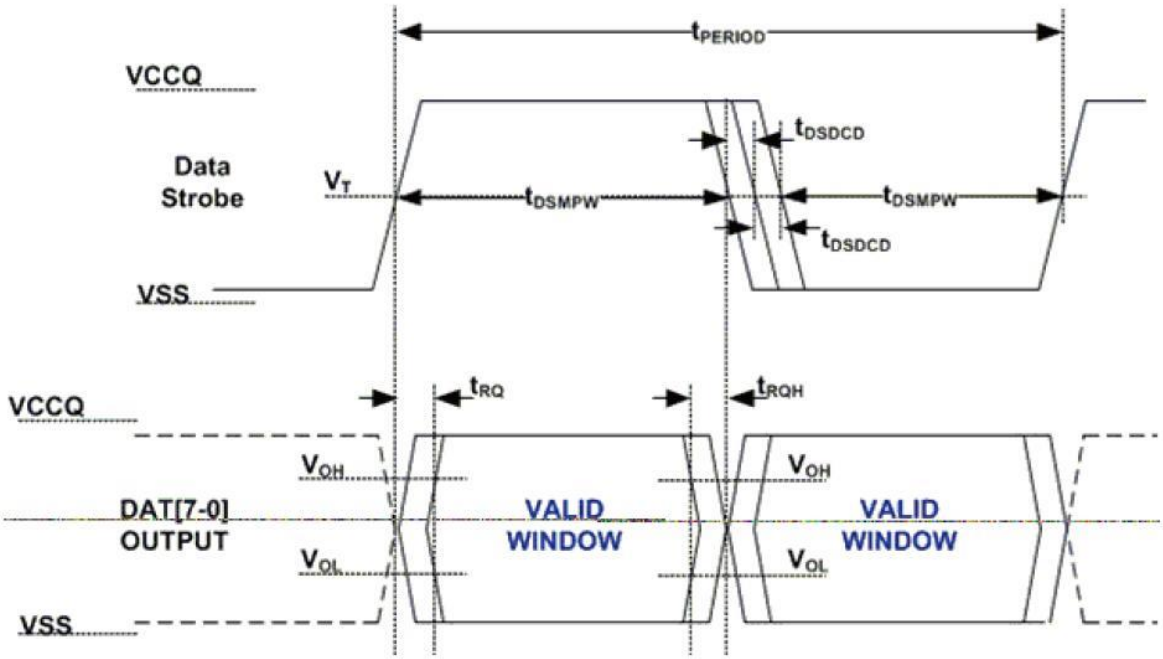
**Figure.4 HS400 eMMC input timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Input CLK | | | | | |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5 | | | 200MHz(Max), between rising edges With respect to $V_T$. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{IH}/V_{IL}$. |
| Duty cycle distortion | $t_{CKDCD}$ | 0.0 | 0.3 | ns | Allowable deviation from an ideal 50% duty cycle. With respect to $V_T$. includes jitter, phase noise |
| Minimum pulse width | $t_{CKMPW}$ | 2.2 | | ns | With respect to $V_T$. |
| Input DAT (referenced to CLK) | | | | | |

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Input set-up time | $t_{ISUddr}$ | 0.4 | | ns | $C_{Device} \leq 6pF$ With respect to $V_{IH}/V_{IL}$. |
| Input hold time | $t_{IHddr}$ | 0.4 | | ns | $C_{Device} \leq 6pF$ With respect to $V_{IH}/V_{IL}$. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{IH}/V_{IL}$. |

**Table.6 HS400 eMMC input timing**

## 4.2.3 HS400 Device Output Timing




Note: $V_T$ = 50% of $V_{CCQ}$, indicates clock reference point for timing measurements.

**Figure.5 HS400 eMMC mode output timing**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Data Strobe | | | | | |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5 | | | 200MHz(Max),between rising edges, with respect to $V_T$ |
| Slew rate | SR | 1.125 | ------ | V/ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Duty cycle distortion | $t_{DSDCD}$ | 0.0 | 0.2 | ns | Allowable deviation from the input CLK duty cycle distortion ($t_{CKDCD}$)<br>With respect to $V_T$<br>Includes jitter, phase noise |
| Minimum pulse width | $t_{DSMPW}$ | 2.0 | | ns | With respect to $V_T$ |
| Read pre-amble | $t_{RPRE}$ | 0.4 | - | $t_{PERIOD}$ | Max value is specified by manufacturer.<br>Value up to infinite is valid |
| Read post-amble | $t_{RPST}$ | 0.4 | - | $t_{PERIOD}$ | Max value is specified by manufacturer.<br>Value up to infinite is valid |
| Output DAT (referenced to Data Strobe) | | | | | |
| Output skew | $t_{RQ}$ | | 0.4 | ns | With respect to $V_{OH}/V_{OL}$ and HS400reference load |
| Output hold skew | $t_{RQH}$ | | 0.4 | ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load. |
| Slew rate | SR | 1.125 | | V/ns | With respect to $V_{OH}/V_{OL}$ and HS400 reference load |

**Table.7 HS400 eMMC output timing**

## 4.2.4 HS400 Device Output Timing (cont' d)

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Pull-up resistance for CMD | $R_{CMD}$ | 4.7 | 100(1) | kΩ | |
| Pull-up resistance for DAT0-7 | $R_{DAT}$ | 10 | 100(1) | kΩ | |
| Pull-down resistance for Data Strobe | $R_{DS}$ | 10 | 100(1) | kΩ | |
| Internal pull up resistance DAT1-DAT7 | $R_{int}$ | 10 | 150 | kΩ | |
| Single Device capacitance | $C_{Device}$ | | 6 | pF | |

Note 1: Recommended maximum value is 30 kΩ for 1.2 V and 50 kΩ for 1.8 V interface supply voltages.

**Table.8 HS400 Capacitance**

## 4.3. Additional Timing changes in HS400 mode

### 4.3.1 Write Timing

In HS400 mode, default Start Bit position is valid at rising edge. In addition, the host may stop CLK between data blocks or within a data block. The Data Strobe is used only in read operation. The Data Strobe is always High-Z (not driven by the device and pulled down by RDS) or Driven Low in write operation, except during CRC status response.

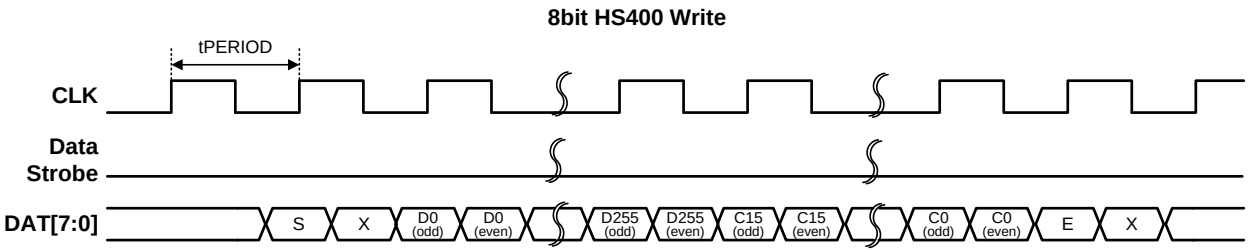



**Figure.6 HS400 Write Timing with data block size of 512 bytes**

### 4.3.2 Read Timing

The Data Strobe is toggled only during data valid period (Start bit, Data, CRC16, End bit, CRC status token). In HS400 mode, Start Bit position is valid at both rising and falling edge. In addition, the host may stop CLK between data blocks and not within a data block.

Data Strobe shall be driven tRPRE prior to the first Data Strobe rising edge and tRPST after the last falling edge.

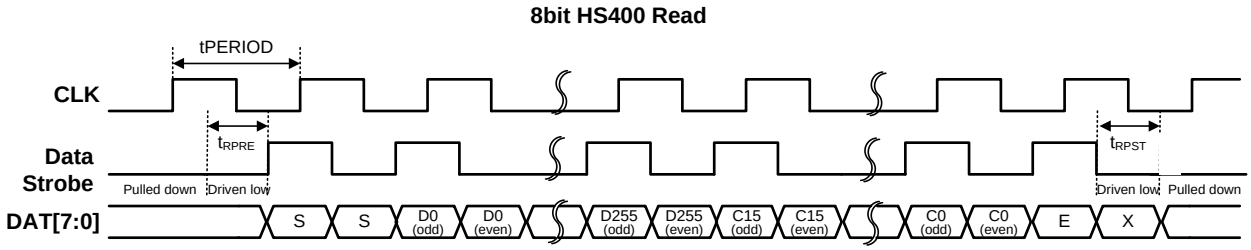



**Figure.7 HS400 Read Timing**

## 4.4 Production State Awareness

eMMC device could utilize the information of whether it is in production environment and operate differently than it operates in the field.

For example, content that was loaded into the storage device prior to soldering might get corrupted, at higher probability, during device soldering. The eMMC device could use "special" internal operations for loading content prior to device soldering that would reduce production failures and use "regular" operations postsoldering.

PRODUCTION_STATE_AWARENESS [133] field in extended CSD is used as a mechanism through which the host should report to the device whether it is pre or post soldering state.

This standard defines two methods, Manual Mode and Auto Mode, to manage the device production state.

The trigger for starting or re-starting the process is setting correctly PRE_LOADING_DATA_SIZE field. Before setting this field the host is expected to make sure that the device is clean and any data that was written before to the device is expected to be erased using CMD35, CMD36 and CMD38.

In case the host erased data, overrode existing data or performed re-partition during production state awareness it should restart the production state awareness process by re-setting PRE_LOADING_DATA_SIZE.

## 4.5 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the eMMC device and, following a successful download, instructs the eMMC device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the eMMC device supports FFU capabilities by reading SUPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the eMMC device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands (CMD17/CMD18/CMD24/CMD25) for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail.

The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required).

Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionally of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When switched back-in to FFU Mode, the host should check the FFU Status to get indication about the number of sectors that were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors that were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors that were downloaded successfully is positive the host should continue the download from the next sector, that would resume the firmware download operation.

## 4.6 Sleep Notification

Host may use to a power off notification when it intends to turn-off VCC after moving the device to sleep state. Some features are added to clarify the spec for entering sleep mode when power off notification enabled.

- **Add the SLEEP_NOTIFICATION on the interruptible Command List**

| CMD | Description | Is interruptible |
|---|---|---|
| CMD6 | SWITCH, Byte POWER_OFF_NOTIFICATION, Value POWER_OFF_LONG or SLEEP_NOTIFICATION | Yes |

■ **SLEEP_NOTIFICATION_TIME[216](Read Only)**

Maximum timeout for the SWITCH command when notifying the device that it is about to move to sleep state by writing SLEEP_NOTIFICATION to POWER_OFF_NOTIFICATION [34] byte. (Unit: 10us)

| Value | Description | Timeout value |
|---|---|---|
| 0x01 ~ 0x17 | Sleep Notification Timeout = 10us x 2 SLEEP_NOTIFICATION_TIME | 0xC (40.96ms) |
| 0x18 ~ 0xFF | Reserved | |

■ **Power_ Off_ NOTIFICATION[34] (R/W/E_P)**

This field allows host to notify the device before the device is powered off. Values not in Table are invalid and setting them will result in SWITCH_ERROR.

| Value | Field | Description |
|---|---|---|
| 0x00 | NO_POWER_NOTIFICATION | Power off notification is not supported by host, device shall not assume any notification |
| 0x01 | POWERED_ON | Host shall notify before powering off the device, and keep power supplies alive and active until then |
| 0x02 | POWER_OFF_SHORT | Host is going to power off the device, The device shall respond within GENERIC_CMD6_TIME. |
| 0x03 | POWER_OFF_LONG | Host is going to power off the device, the device shall respond within POWER_OFF_LONG_TIME |
| 0x04 | SLEEP_NOTIFICATION | Host is going to put device in sleep mode, the device shall respond within SLEEP_NOTIFICATION_TIME |

Note: eMMC device should be able to guard against sudden power loss even when POWER_OFF_NOTIFICATION is set to 0x01 (POWER_ON) since unintentional power loss event may still occur.

## 4.7 Secure Removal Type

This field indicates that how information is removed from the physical memory during a Purge operation.

The first 4bits (Bit0~Bit3) indicate the capability of the eMMC device. The next two bit indicates configurable option. It can be set once during system integration by host.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | Configure Secure Removal Type | | Supported Secure Removal Type | | | |
| | | R/W | | R | | | |

**Table.9 Secure Removal Type**

Supported Secure Removal Type

**Bit [7:6]: Reserved**

**Bit [5:4]: Configure Secure Removal Type**

0x0: information removed by an erase of the physical memory

0x1: information removed by an overwriting the addressed locations with a character followed by an erase

0x2: information removed by an overwriting the addressed locations with a character, its complement, then a random character

0x3: information removed using a vendor defined

**Bit [3:0]: Supported Secure Removal Type**

Bit 0: information removed by an erase of the physical memory

Bit 1: information removed by an overwriting the addressed locations with a character followed by an erase

Bit 2: information removed by an overwriting the addressed locations with a character, its complement, then a random character

Bit 3: Information removed using a vendor defined.

## 4.8 Overshoot/Undershoot Specification

| | | VCCQ | Unit |
|---|---|---|---|
| | | 1.70V – 1.95V | |
| Maximum peak amplitude allowed for overshoot area. | Max | 0.9 | V |
| Maximum peak amplitude allowed for undershoot area. | Max | 0.9 | V |
| Maximum area above $V_{CCQ}$ | Max | 1.5 | V-ns |
| Maximum area below $V_{SSQ}$ | Max | 1.5 | V-ns |

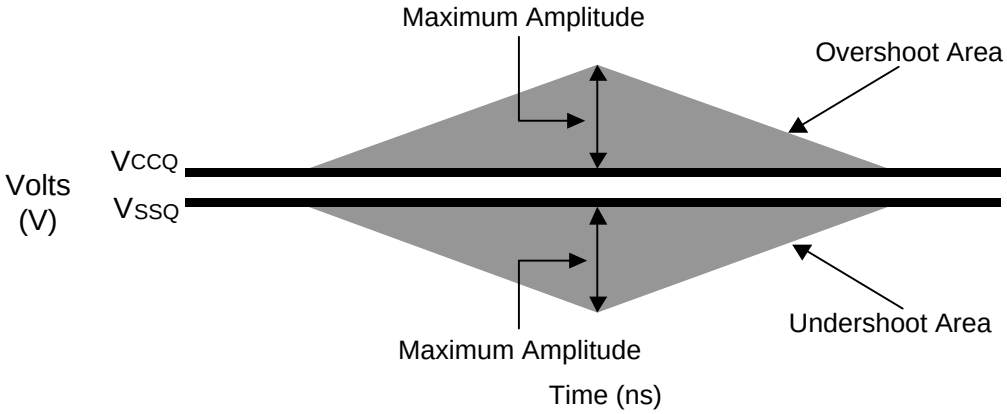



**Figure.8 Overshoot/undershoot definition**

## 4.9 HS400 Reference Load

The circuit in Figure 9 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.

The reference load is made up by the transmission line and the CREFERENCE capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.

Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

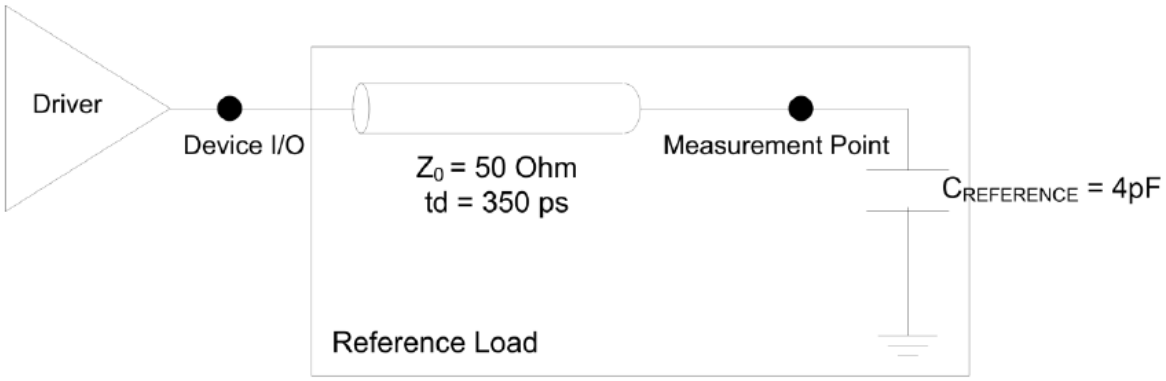



**Figure.9 HS400 reference load**

## 4.10 RPMB Throughput Improvement

Related parameter register in EXT_CSD : WR_REL_PARAM [166]

| Name | Max. data size | Bit | Type |
|---|---|---|---|
| Enhanced RPMB Reliable Write EN_RPMB_REL_WR | EN_RPMB_REL_WR | 4 | R |

Bit[4]: EN_RPMB_REL_WR(R)

0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).

0x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame), or 8KB(Thirthy two 512B frames).

## 4.11 User Density

### 4.11.1 User Data Area Capacity

| Capacity | LBA[Hex] | LBA[Dec] | Capacity[Bytes] |
|---|---|---|---|
| 16GB | 1D20000h | 30,539,776 | 15,636,365,312 |

**Table.10 User Data Area Capacity**

### 4.11.2 Capacity according to partition

| | Boot partition 1 | Boot partition 2 | RPMB |
|---|---|---|---|
| Default | 4096KB | 4096KB | 4096KB |

**Table.11 Capacity according to partition**

# 5. Electrical Characteristics

## 5.1 DC Power Specification

| Parameter | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage (Controller and I/O) | 2.7(1.7) | 3.3(1.8) | 3.6(1.95) | V | VCCQ |
| Supply voltage (NAND Flash and NAND Flash interface) | 2.7 | 3.3 | 3.6 | V | VCC |
| Supply voltage for core | -0.5 | 0 | 0.5 | V | VSS |
| I/O input leakage current | -100 | | 100 | uA | |
| I/O output leakage current | -100 | | 100 | uA | |
| Programmable pull-up resistor | 50 | 75 | 100 | KΩ | VCCQ = 3.3V |
| Programmable pull-down resistor | 50 | 75 | 100 | KΩ | VCCQ = 3.3V |
| Pre-initial standby current | | | | uA | |
| Sleep current | | | | uA | |
| Operating temperature | -25 | +25 | +85 | °C | |

**Table.12 General DC Characteristics for eMMC**

## 5.2 Power Requirement

### 5.2.1 Sleep Current

| Density | $I_{CC}$ ( 3.3V ) | $I_{CCQ(1.8V)}$ | Unit |
|---|---|---|---|
| 16GB | 100 | 100 | μA |

**Table.13 Sleep Current**

### 5.2.2 Active Power Consumption during operation

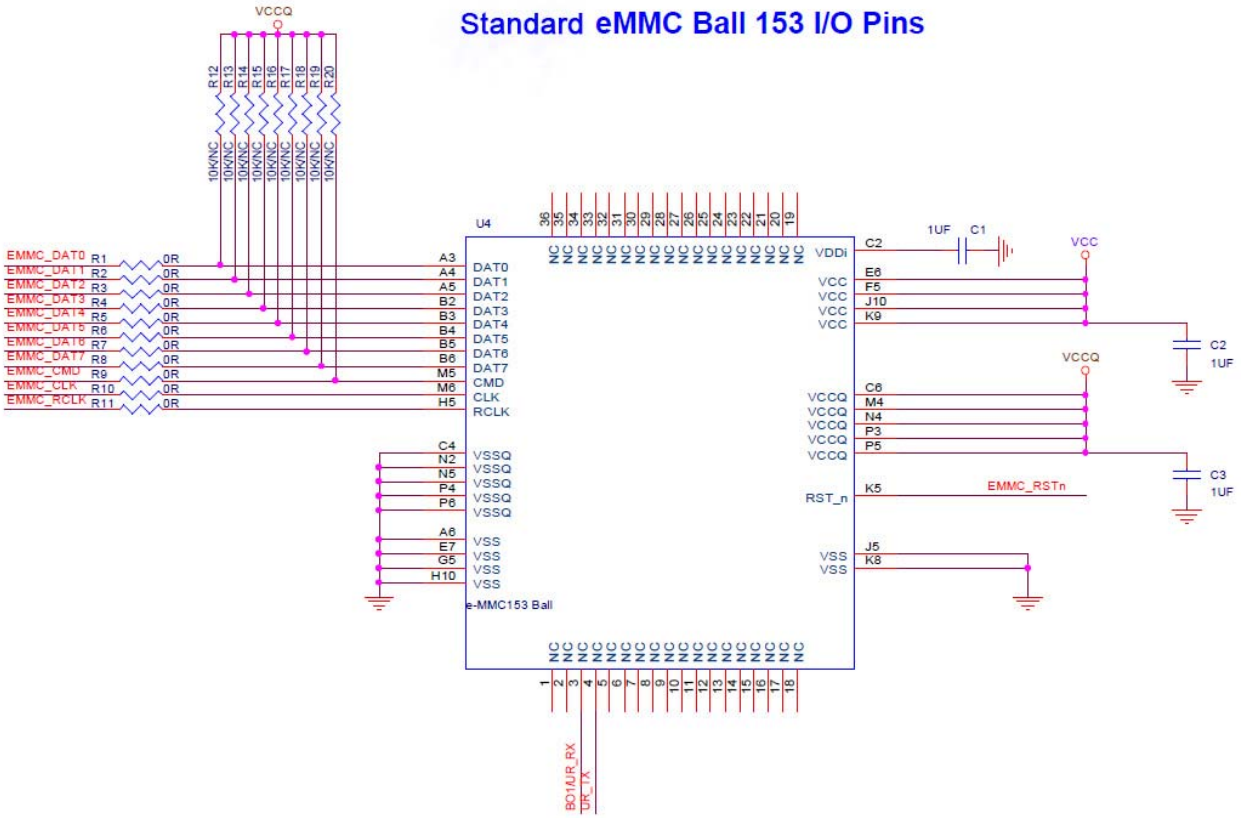
| Density | $I_{CC(3.3V)}$ | $I_{CCQ(1.8V)}$ | Unit |
|---|---|---|---|
| 16GB | 60 | 70 | mA |

**Table.14 Active Power Consumption during operation**

# 6. eMMC Connection Guide

This appendix is just guideline for eMMC connection. The values in the below Schematic can be changed depending on the system environment.

Coupling capacitor should be connected with VDD and VSS as closely as possible. VDDI capacitor is min 1uF.

If host does not use H/W reset, it is not needed to put 10K pull-up resistance on H/W rest line. It is recommended to separate VCCQ and VCC power.

The below connection guide is an example for customers to adopt eMMC more easily.