



# MP8880A

## 60V, 4.5A, High-Efficiency, Digital, Configurable, Synchronous Step-Down Converter with PMBus Interface

### DESCRIPTION

The MP8880A is a high-frequency, synchronous, rectified step-down converter with a PMBus control interface. It can achieve up to 4.5A of continuous output current ( $I_{OUT}$ ), with excellent load and line regulation across the wide input voltage ( $V_{IN}$ ) supply range.

The output voltage ( $V_{OUT}$ ) can be controlled on the fly via the PMBus serial interface.  $V_{OUT}$  can be set between 0.6V and 24V in internal feedback divider mode, with a 48V maximum in external feedback divider mode. The voltage slew rate, switching frequency ( $f_{SW}$ ), and power-save mode can also be selected via the PMBus interface.

Current mode operation provides fast transient response and facilitates loop stabilization. Full protection features include under-voltage lockout (UVLO), over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8880A supports multiple-time programmable (MTP) memory to provide flexible configurations. The device can be paralleled with up to 4 phases for applications with a higher  $I_{OUT}$ . The integrated, internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively) provide high efficiency without the use of an external Schottky diode.

The internal feedback divider and compensation make the MP8880A a very compact solution with a minimal number of readily available, standard external components. It is available in a QFN-20 (4mmx5mm) package.

### FEATURES

- Wide 4V to 60V Input Voltage ( $V_{IN}$ ) Range
- Wide 0.6V to 48V Output Voltage ( $V_{OUT}$ ) Range
- 4.5A Output Current ( $I_{OUT}$ )
- Can be Paralleled with Up to 4 Phases
- Supports PD EPR 240W and AVS
- Configurable Constant 150kHz to 2.2MHz Switching Frequency ( $f_{SW}$ ) with External Clock Synchronization
- Internal 60m $\Omega$ /43m $\Omega$  Low On Resistance ( $R_{DS(ON)}$ ) MOSFETs
- 97.5% Peak Efficiency
- Frequency Spread Spectrum (FSS) for Low EMI
- Power Good (PG) and Fault Indication
- Output Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), and Over-Temperature Protection (OTP)
- Low-Dropout Mode
- Telemetry Readback Includes  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{OUT}$ , and Faults
- Configurable MTP Parameters:
  - $V_{OUT}$
  - $f_{SW}$
  - Compensation Network
  - Output OCP, OVP, and UVP Thresholds
  - Input OVP and UVP Thresholds
  - PWM/AAM Mode
- Cyclic Redundancy Check (CRC) Protection for MTP Integrity
- Available in a QFN-20 (4mmx5mm) Package



Optimized Performance with MPS  
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### APPLICATIONS

- DC/DC Power Systems
- USB Power Delivery (PD)
- High-Input Power Systems

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# TYPICAL APPLICATION

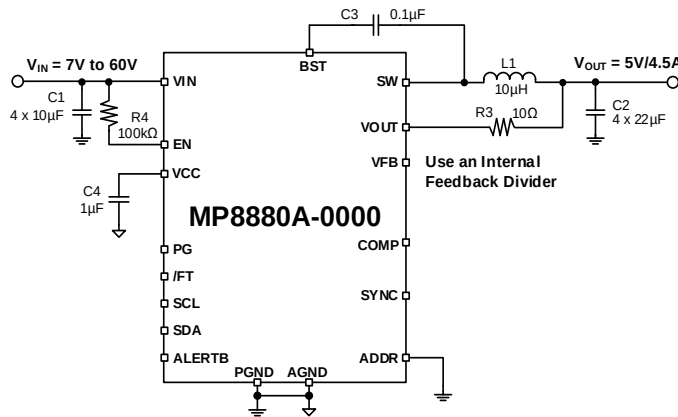
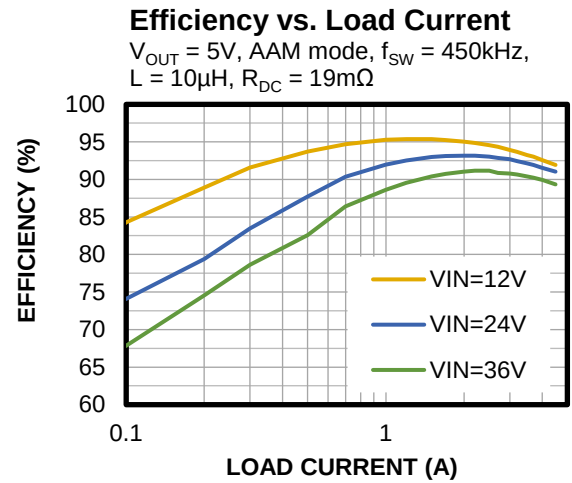


Figure 1: Single-Phase Application



## ORDERING INFORMATION

| Part Number*      | Package          | Top Marking | MSL |
|-------------------|------------------|-------------|-----|
| MP8880AGVE-0000   | QFN-20 (4mmx5mm) | See Below   | 1   |
| MP8880AGVE-0001   | QFN-20 (4mmx5mm) | See Below   |     |
| MP8880AGVE-0002   | QFN-20 (4mmx5mm) | See Below   |     |
| MP8880AGVE-xxxx** | QFN-20 (4mmx5mm) | See Below   |     |
| EVKT-MP8880A      | Evaluation kit   | -           |     |

\*For Tape & Reel, add suffix -Z (e.g. MP8880AGVE-0000-Z, MP8880AGVE-0001-Z, MP8880AGVE-0002-Z, and MP8880AGVE-xxxx-Z).

\*\* “xxxx” is the configuration code identifier for the register settings stored in the MTP memory. Each “x” can be a hexadecimal value between 0 and F. The MP8880AGVE-0000 is the default code for internal feedback divider mode with a 5V output. The MP8880AGVE-0002 is the default code for internal feedback divider mode with a 12V output. The MP8880AGVE-0001 is the default code for external feedback divider mode. For customized configurations, contact an MPS FAE to create a unique code.

## TOP MARKING

**MPSYWW**

**M8880A**

**LLLLLL**

**E**

MPS: MPS prefix  
Y: Year code  
WW: Week code  
M8880A: Part number  
LLLLLL: Lot number  
E: Wettable flank

## EVALUATION KIT (EVKT-MP8880A)

EVKT-MP8880A kit contents (items below can be ordered separately): <sup>(1)</sup>

| # | Part Number      | Item                                                                                                     | Quantity |
|---|------------------|----------------------------------------------------------------------------------------------------------|----------|
| 1 | EVL8880A-V-00A   | MP8880A evaluation board for single-phase operation                                                      | 1        |
| 2 | EVKT-USB2C-02    | Includes one USB-to-I <sup>2</sup> C communication interface device, one USB cable, and one ribbon cable | 1        |
| 3 | MP8880AGVE-0000  | The MP8880A, which can be configured via the MTP                                                         | 2        |
| 4 | Online resources | MPS's Virtual Bench Pro 4.0, supplemental files including GUI                                            | 1        |

**Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.**

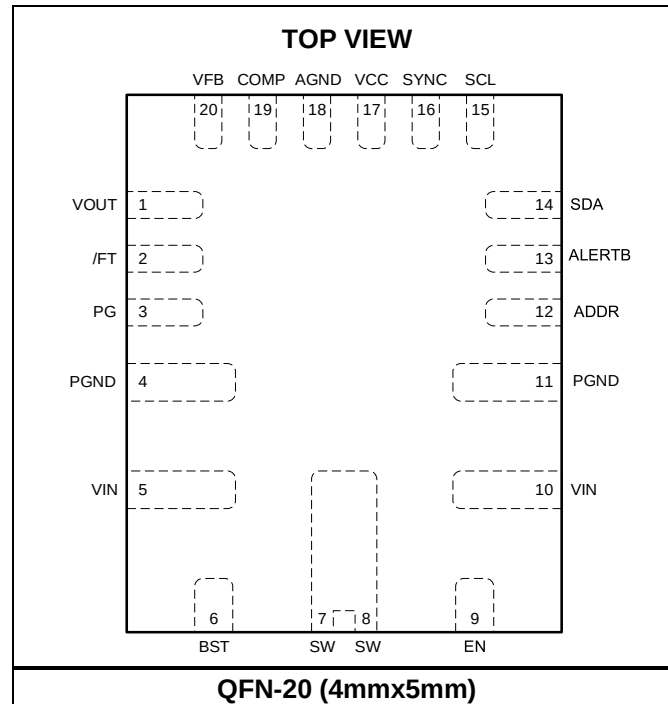


**Figure 2: EVKT-MP8880A Evaluation Kit Set-Up**

**Note:**

- 1) Ensure that  $V_{IN}$  exceeds 10V when using the MTP. To use the evaluation kit, download the graphical user interface (GUI) from the MPS website or contact an MPS FAE.

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | VOUT   | <b>Sense input for the output voltage (V<sub>OUT</sub>).</b> The VOUT pin is also used for the V <sub>OUT</sub> bias input. When V <sub>OUT</sub> > 4.8V, VCC can be supplied power through this pin. The V <sub>OUT</sub> biased function can be selected via the registers.                                                                                                                                                                                                                                                                                                  |
| 2     | /FT    | <b>Fault indicator.</b> The /FT pin is pulled down if V <sub>IN</sub> over-voltage protection (OVP), V <sub>OUT</sub> OVP, V <sub>OUT</sub> under-voltage protection (UVP), or over-current protection (OCP) occurs. The MFR_FAULT_CTRL (DBh) register can determine which events control /FT. /FT is an open-drain output that requires an external pull-up resistor. Pull /FT up to VCC or float this pin if it is not used. /FT is a multi-function pin that can be used for multi-phase configurations. See the Multi-Phase Operation section on page 19 for more details. |
| 3     | PG     | <b>Power good (PG) indicator.</b> The PG pin is pulled down if V <sub>OUT</sub> OVP or UVP occurs. PG is an open-drain output that requires an external pull-up resistor. Connect PG to GND or float this pin if it is not used.                                                                                                                                                                                                                                                                                                                                               |
| 4, 11 | PGND   | <b>Power ground.</b> The PGND pin is the reference ground for the regulated output voltage. Connect these pins to larger copper areas at the negative terminals of the input and output capacitors.                                                                                                                                                                                                                                                                                                                                                                            |
| 5, 10 | VIN    | <b>Supply voltage.</b> The VIN pin supplies all power to the converter. Place a decoupling capacitor from VIN to ground, and as close as possible to the IC to reduce switching spikes. Make the VIN connection using a wide PCB trace.                                                                                                                                                                                                                                                                                                                                        |
| 6     | BST    | <b>Bootstrap.</b> Connect a capacitor between the SW and BST pins to form a floating supply across the high-side switch driver.                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7, 8  | SW     | <b>Switch output.</b> Use a wide PCB trace to make the connection between the SW pins and the inductor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | EN     | <b>Enable.</b> Drive the EN pin high to turn on the device; drive EN low to turn off the device. Do not float the EN pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 12    | ADDR   | <b>Address setting for the PMBus.</b> The ADDR pin sets the lower 3 bits of the PMBus address with a resistor connected to GND (see Table 2 on page 21).                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 13    | ALERTB | <b>Alert.</b> The ALERTB pin is pulled down if any fault or warning is indicated by STATUS_WORD (79h). This pin is an open-drain output that requires an external pull-up resistor. Connect ALERTB to GND or float this pin if it is not used.                                                                                                                                                                                                                                                                                                                                 |
| 14    | SDA    | <b>PMBus serial data.</b> Pull the SDA pin up to VCC if SDA is not used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15    | SCL    | <b>PMBus serial clock.</b> Pull the SCL pin up to VCC if SCL is not used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 16    | SYNC   | <b>Synchronized to external clock signal.</b> The SYNC pin can be configured as the sync input or sync output via the PMBus.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 17    | VCC    | <b>Internal 4.9V LDO regulator output.</b> Decouple the VCC pin with a 1μF capacitor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 18    | AGND   | <b>Signal ground.</b> The AGND pin is the ground for the internal logic and signal circuit. AGND is not internally connected to PGND, but ensure that AGND is connected to PGND in the PCB layout.                                                                                                                                                                                                                                                                                                                                                                             |
| 19    | COMP   | <b>Compensation for parallel operation.</b> For multi-phase applications, connect all COMP pins together. Float COMP for single-phase applications.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 20    | VFB    | <b>Feedback voltage input for external feedback divider mode.</b> Connect the VFB pin to a voltage divider to set the initial output voltage in external feedback divider mode. VFB should be floating or connected to GND in internal feedback divider mode.                                                                                                                                                                                                                                                                                                                  |

## ABSOLUTE MAXIMUM RATINGS <sup>(2)</sup>

|                                                                    |                 |
|--------------------------------------------------------------------|-----------------|
| $V_{IN}$ .....                                                     | -0.3V to +61V   |
| $V_{SW}$ .....                                                     | ...             |
| ...-0.3V (-5V for <5ns) to +60.5V (+61V for <5ns)                  |                 |
| $V_{EN}$ .....                                                     | -0.3V to +60V   |
| $V_{BST}$ .....                                                    | $V_{SW} + 5.5V$ |
| $V_{OUT}$ .....                                                    | -0.3V to +35V   |
| $V_{CC}$ .....                                                     | -0.3V to +5.5V  |
| All other pins .....                                               | -0.3V to +5.3V  |
| Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(3)</sup> | 6.1W            |
| Junction temperature ( $T_J$ ) .....                               | 125°C           |
| Lead temperature .....                                             | 260°C           |
| Storage temperature .....                                          | -65°C to +125°C |

## Recommended Operating Conditions <sup>(5)</sup>

|                                        |                 |
|----------------------------------------|-----------------|
| Supply voltage ( $V_{IN}$ ) .....      | 4V to 60V       |
| Output voltage ( $V_{OUT}$ ) .....     | 0.6V to 48V     |
| Operating junction temp ( $T_J$ ) .... | -40°C to +125°C |

## Thermal Resistance

 $\theta_{JA}$      $\theta_{JC}$ 

|                                     |           |            |
|-------------------------------------|-----------|------------|
| EVL8880A-V-00A <sup>(6)</sup> ..... | 20.4..... | 5.4...°C/W |
| JESD51-7 <sup>(7)</sup> .....       | 48.....   | 11...°C/W  |

### Notes:

- 2) Exceeding these ratings may damage the device.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) = ( $T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
- 5) The device is not guaranteed to function outside of its operating conditions. For outputs exceeding 30V, the  $V_{OUT}$  pin should be floated and the  $VO\_BIAS$  function is not supported. See Figure 16 on page 48 for the reference circuit.
- 6) Measured on the EVL8880A-V-00A, a 4-layer PCB.
- 7) Measured on a JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values refer to  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                                                | Symbol          | Conditions                                                                                | Min    | Typ    | Max    | Units      |
|--------------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------|--------|--------|--------|------------|
| Input voltage ( $V_{IN}$ ) under-voltage lockout (UVLO) rising threshold | $V_{INUV-R}$    | 35h = 0x46                                                                                | 9      | 9.3    | 9.6    | V          |
|                                                                          |                 | 35h = 0xE6                                                                                | 29     | 30.6   | 32     | V          |
| $V_{IN}$ UVLO falling threshold                                          | $V_{INUV-F}$    | 36h = 0x46                                                                                | 8.9    | 9.2    | 9.5    | V          |
|                                                                          |                 | 36h = 0xD2                                                                                | 26     | 28     | 30     | V          |
| VIN quiescent current                                                    | $I_Q$           | $V_{FB} > V_{REF}$ , disable the VO_BIAS bit, no load                                     |        | 93     | 200    | $\mu A$    |
|                                                                          |                 | Force $V_{OUT} = 5V$ , enable the VO_BIAS bit, no load                                    |        | 8      | 50     | $\mu A$    |
| VIN shutdown current                                                     | $I_{IN-STD}$    | $V_{EN} = 0V$                                                                             |        |        | 3.5    | $\mu A$    |
| Output voltage accuracy                                                  | $V_{OUT}$       | 21h = 0x190, D2h, bits[2:0] = 0b000                                                       | 0.575  | 0.6    | 0.625  | V          |
|                                                                          |                 | 21h = 0x226, D2h, bits[2:0] = 0b010                                                       | 3.23   | 3.3    | 3.37   | V          |
|                                                                          |                 | 21h = 0x341, D2h, bits[2:0] = 0b010                                                       | 4.93   | 5      | 5.07   | V          |
|                                                                          |                 | 21h = 0x3E8, D2h, bits[2:0] = 0b011                                                       | 11.7   | 12     | 12.3   | V          |
|                                                                          |                 | 21h = 0x3E8, D2h, bits[2:0] = 0b100                                                       | 23.2   | 23.8   | 24.4   | V          |
| FB voltage accuracy                                                      | $V_{FB}$        | External feedback divider mode, $T_J = 25^{\circ}C$ , 21h = 0x64, D2h, bits[2:0] = 0b100  | 147.75 | 150    | 152.25 | mV         |
|                                                                          |                 | External feedback divider mode, $T_J = 25^{\circ}C$ , 21h = 0x190, D2h, bits[2:0] = 0b100 | 595    | 600    | 605    | mV         |
|                                                                          |                 | External feedback divider mode, $T_J = 25^{\circ}C$ , 21h = 0x29A, D2h, bits[2:0] = 0b100 | 991    | 999    | 1007   | mV         |
|                                                                          |                 | External feedback divider mode, $T_J = 25^{\circ}C$ , 21h = 0x3E8, D2h, bits[2:0] = 0b100 | 1491   | 1500   | 1509   | mV         |
| Default switching frequency                                              | $f_{SW}$        | D4h, bits[2:0] = 0b010                                                                    | 350    | 450    | 550    | kHz        |
| Sync frequency range <sup>(8) (9)</sup>                                  | $f_{SYNC}$      | Sync clock set range                                                                      | 200    |        | 2500   | kHz        |
| Sync voltage high level                                                  | $V_{SYNC-HIGH}$ |                                                                                           | 1.6    |        |        | V          |
| Sync voltage low level                                                   | $V_{SYNC-LOW}$  |                                                                                           |        |        | 0.4    | V          |
| Minimum on time <sup>(9)</sup>                                           | $t_{ON-MIN}$    |                                                                                           |        | 130    |        | ns         |
| Minimum off time <sup>(9)</sup>                                          | $t_{OFF-MIN}$   |                                                                                           |        | 190    |        | ns         |
| High-side MOSFET (HS-FET) on resistance                                  | $R_{DS(on)-H}$  | $V_{BST} - V_{SW} = 5V$                                                                   |        | 60     | 120    | m $\Omega$ |
| Low-side MOSFET (LS-FET) on resistance                                   | $R_{DS(on)-L}$  |                                                                                           |        | 43     | 80     | m $\Omega$ |
| Switch leakage current                                                   | $I_{SW-LKG}$    | $V_{SW} = 60V$                                                                            |        |        | 9      | $\mu A$    |
| Default soft-start time                                                  | $t_{SS}$        | 61h = 0x01                                                                                | 0.8    | 1.3    | 1.8    | ms         |
| EN voltage rising threshold                                              | $V_{EN}$        |                                                                                           | 0.95   | 1.15   | 1.35   | V          |
| EN voltage hysteresis                                                    | $V_{EN-HYS}$    | D9h, bit[2] = 0b0                                                                         |        | 130    |        | mV         |
|                                                                          |                 | D9h, bit[2] = 0b1                                                                         |        | 330    |        | mV         |
| Default PG upper rising threshold                                        | $V_{PG-U}$      | E3h, bit[0] = 0b0                                                                         | 112%   | 115.5% | 119%   | $V_{OUT}$  |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values refer to  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                  | Symbol                    | Conditions                                | Min  | Typ   | Max  | Units            |
|--------------------------------------------|---------------------------|-------------------------------------------|------|-------|------|------------------|
| PG upper rising threshold hysteresis       | V <sub>PG-U-HYS</sub>     | D9h, bit[1] = 0b1                         |      | 10%   |      | V <sub>OUT</sub> |
|                                            |                           | D9h, bit[1] = 0b0                         |      | 5%    |      | V <sub>OUT</sub> |
| Default PG lower rising threshold          | V <sub>PG-L</sub>         | E5h, bit[0] = 0b1                         | 87%  | 90.5% | 94%  | V <sub>OUT</sub> |
| PG lower rising threshold hysteresis       | V <sub>PG-L-HYS</sub>     | D9h, bit[0] = 0b1                         |      | 10%   |      | V <sub>OUT</sub> |
|                                            |                           | D9h, bit[0] = 0b0                         |      | 5%    |      | V <sub>OUT</sub> |
| PG output voltage low                      | V <sub>PG-LOW</sub>       | I <sub>SINK</sub> = 1mA                   |      |       | 0.3  | V                |
| PG deglitch timer <sup>(9)</sup>           | t <sub>PG-DELAY</sub>     |                                           |      | 20    |      | μs               |
| VCC regulator                              | V <sub>CC</sub>           | I <sub>VCC</sub> = 0mA                    | 4.7  | 4.9   | 5.1  | V                |
| VCC regulation                             |                           | I <sub>VCC</sub> = 20mA                   |      | 2.2   | 5.5  | %                |
| Peak current limit                         | I <sub>PEAK-LIMIT</sub>   | E0h, bits[6:4] = 0b110                    | 2.62 | 3.5   | 4.38 | A                |
|                                            |                           | E0h, bits[6:4] = 0b001                    | 5.3  | 6.8   | 8.3  | A                |
|                                            |                           | E0h, bits[6:4] = 0b011                    | 6.9  | 9     | 11.1 | A                |
| Valley current limit                       | I <sub>VALLEY-LIMIT</sub> | E0h, bits[2:0] = 0b001                    | 2.25 | 3     | 3.75 | A                |
|                                            |                           | E0h, bits[2:0] = 0b101                    | 4.2  | 5.5   | 6.8  | A                |
|                                            |                           | E0h, bits[2:0] = 0b111                    | 5    | 6.5   | 8    | A                |
| Input OVP threshold                        | V <sub>IN-OV</sub>        | 55h = 0x10E                               | 33.2 | 35.6  | 38   | V                |
| Input OVP hysteresis                       | V <sub>IN-OV-HYS</sub>    | D9h, bit[3] = 0b0                         |      | 1.32  |      | V                |
|                                            |                           | D9h, bit[3] = 0b1                         |      | 2.64  |      | V                |
| Thermal shutdown <sup>(9)</sup>            | T <sub>TSD</sub>          |                                           |      | 165   |      | °C               |
| Thermal shutdown hysteresis <sup>(9)</sup> | T <sub>TSD-HYS</sub>      |                                           |      | 25    |      | °C               |
| ALERTB sink capability                     | V <sub>ALERTB_SINK</sub>  | I <sub>SINK</sub> = 1mA                   |      |       | 20   | mV               |
| ALERTB leakage                             | I <sub>LKG_ALERTB</sub>   | Pull up with 5V, T <sub>J</sub> = 25°C    |      |       | 300  | nA               |
| /FT sink capability                        | V <sub>/FT_SINK</sub>     | I <sub>SINK</sub> = 1mA                   |      |       | 20   | mV               |
| /FT leakage                                | I <sub>LKG_FT</sub>       | Pull up with 5V, T <sub>J</sub> = 25°C    |      |       | 300  | nA               |
| ADDR pin source current                    | I <sub>ADDR</sub>         | Only works during start-up                | 7    | 10    | 13   | μA               |
| ADDR address 1                             | ADDR1                     | R <sub>ADDR</sub> = GND, D0h = 0x00       |      | 00h   |      |                  |
| ADDR address 2                             | ADDR2                     | R <sub>ADDR</sub> = 30kΩ/1%, D0h = 0x00   |      | 01h   |      |                  |
| ADDR address 3                             | ADDR3                     | R <sub>ADDR</sub> = 49.9kΩ/1%, D0h = 0x00 |      | 02h   |      |                  |
| ADDR address 4                             | ADDR4                     | R <sub>ADDR</sub> = 68kΩ/1%, D0h = 0x00   |      | 03h   |      |                  |
| ADDR address 5                             | ADDR5                     | R <sub>ADDR</sub> = 88.7kΩ/1%, D0h = 0x00 |      | 04h   |      |                  |
| ADDR address 6                             | ADDR6                     | R <sub>ADDR</sub> = 105kΩ/1%, D0h = 0x00  |      | 05h   |      |                  |
| ADDR address 7                             | ADDR7                     | R <sub>ADDR</sub> = 127kΩ/1%, D0h = 0x00  |      | 06h   |      |                  |
| ADDR address 8                             | ADDR8                     | ADDR = VCC, D0h = 0x00                    |      | 07h   |      |                  |
| PMBus DC Characteristics (SDA, SCL)        |                           |                                           |      |       |      |                  |
| Input high voltage                         | V <sub>IH</sub>           |                                           | 1.4  |       |      | V                |
| Input low voltage                          | V <sub>IL</sub>           |                                           |      |       | 0.5  | V                |
| Output low voltage                         | V <sub>OL</sub>           | I <sub>OL</sub> = 1mA                     |      |       | 0.4  | V                |
| Input leakage current                      | I <sub>LKG</sub>          | SDA, SCL pulled up with 5V                |      |       | 10   | μA               |
| Pin capacitance on SDA, SCL <sup>(9)</sup> | C <sub>PIN</sub>          |                                           |      |       | 400  | pF               |

# ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values refer to  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                                       | Symbol        | Conditions | Min | Typ | Max  | Units   |
|-----------------------------------------------------------------|---------------|------------|-----|-----|------|---------|
| <b>PMBus Timing Characteristics</b>                             |               |            |     |     |      |         |
| Operating frequency                                             | $f_{SCL}$     |            |     | 400 | 1000 | kHz     |
| Bus free time between a start and a stop command <sup>(9)</sup> | $t_{BUF}$     |            | 160 |     |      | ns      |
| Holding time for start command <sup>(9)</sup>                   | $t_{HD\_STA}$ |            | 160 |     |      | ns      |
| Set-up time for repeated start command <sup>(9)</sup>           | $t_{SU\_STA}$ |            | 160 |     |      | $\mu s$ |
| Set-up time for stop command <sup>(9)</sup>                     | $t_{SU\_STO}$ |            | 160 |     |      | $\mu s$ |
| Data hold time <sup>(9)</sup>                                   | $t_{HD\_DAT}$ |            |     | 60  |      | ns      |
| Data set-up time <sup>(9)</sup>                                 | $t_{SU\_DAT}$ |            | 10  |     |      | ns      |
| Clock low timeout <sup>(9)</sup>                                | $t_{LOW\_TO}$ |            | 25  |     | 35   | ms      |
| Clock low period <sup>(9)</sup>                                 | $t_{LOW}$     |            | 160 |     |      | ns      |
| Clock high period <sup>(9)</sup>                                | $t_{HIGH}$    |            | 60  |     |      | ns      |
| Clock/data falling time <sup>(9)</sup>                          | $t_F$         |            | 10  |     | 300  | ns      |
| Clock/data rising time <sup>(9)</sup>                           | $t_R$         |            | 10  |     | 300  | ns      |

## Notes:

8) For thermal consideration, do not use frequencies exceeding 1MHz when the input voltage exceeds 30V.

9) Not tested in production. Guaranteed by design and characterization.

# PMBUS-COMPATIBLE INTERFACE TIMING DIAGRAM

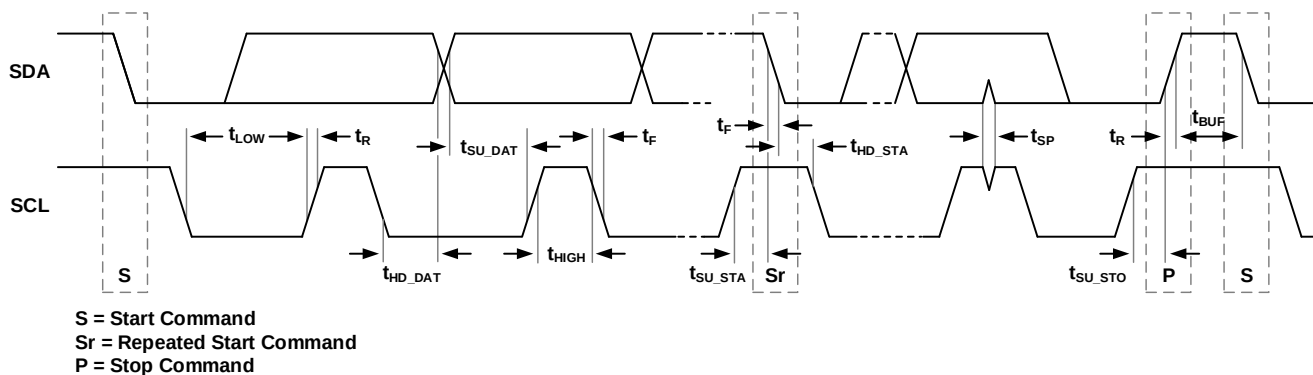
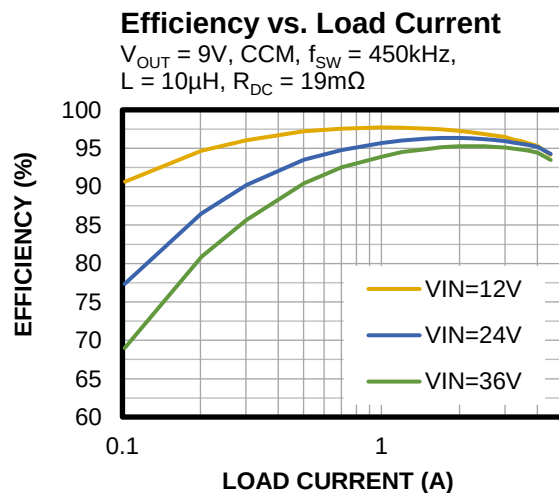
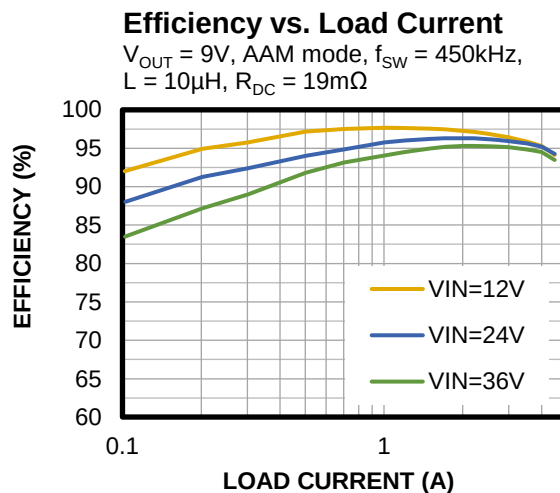
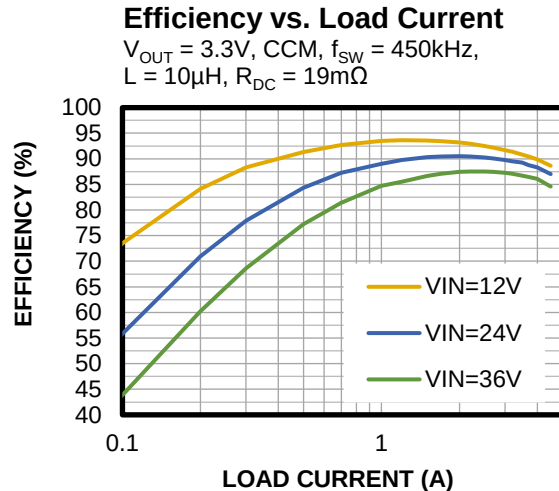
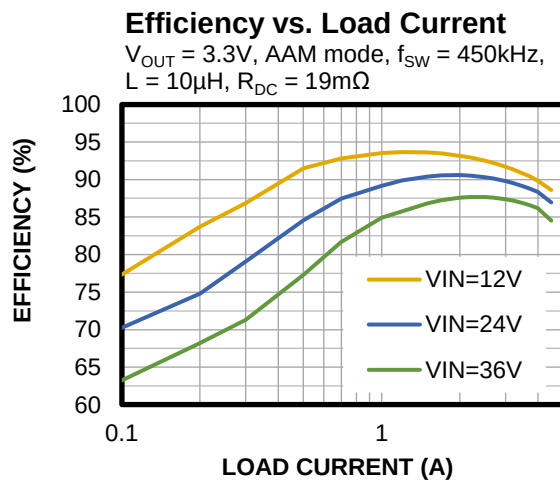
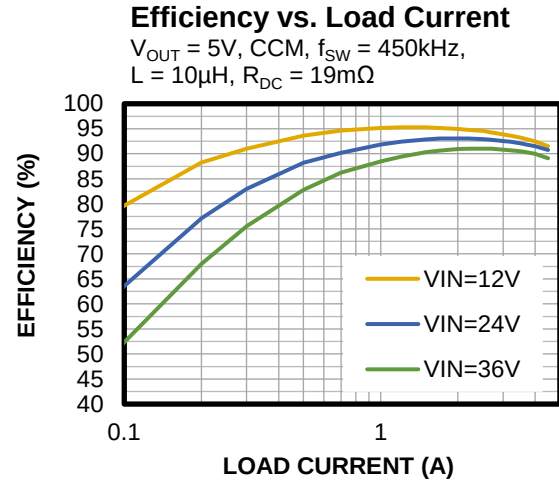
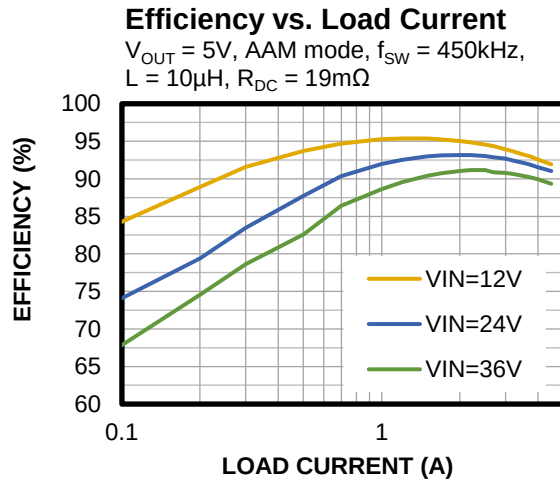


Figure 3: PMBus Timing Diagram

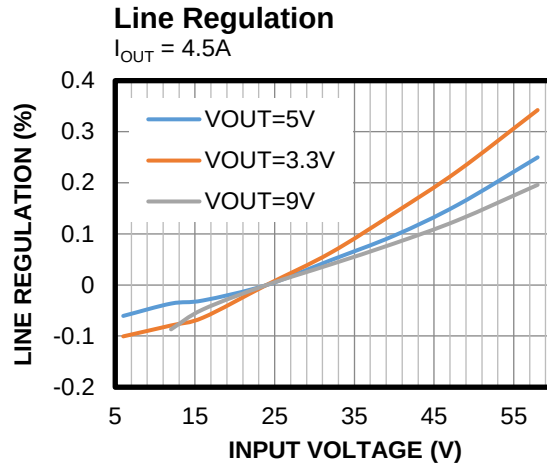
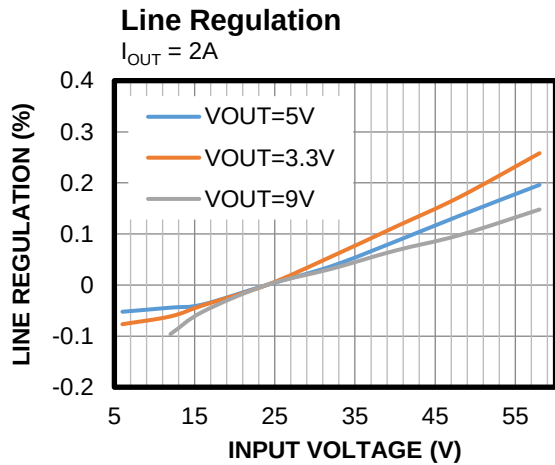
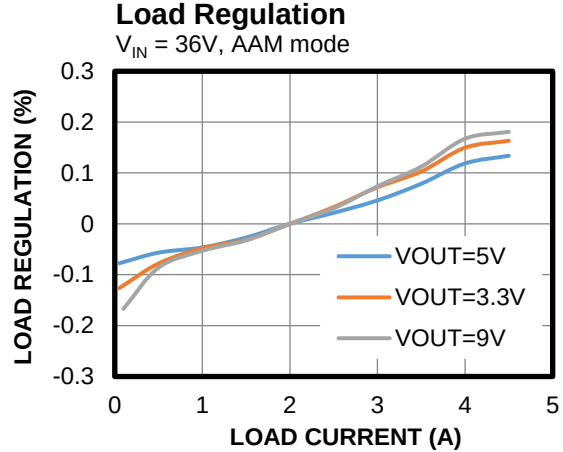
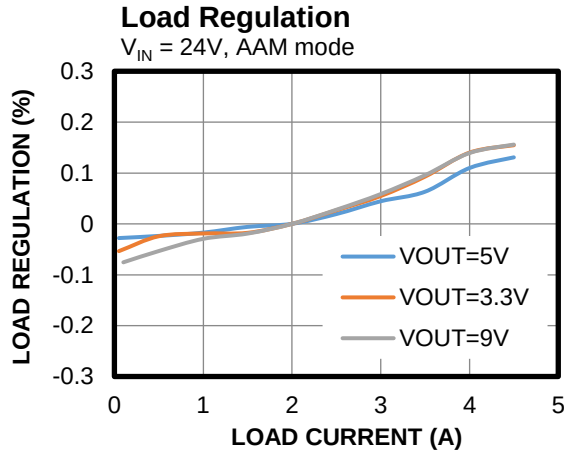
# TYPICAL CHARACTERISTICS

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , tested with the MP8880AGVE-0000, unless otherwise noted.



## TYPICAL CHARACTERISTICS *(continued)*

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , tested with the MP8880AGVE-0000, unless otherwise noted.

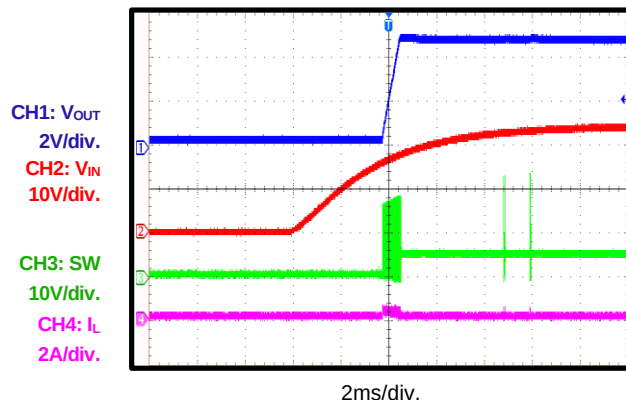


# TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , tested with the MP8880AGVE-0000, unless otherwise noted.

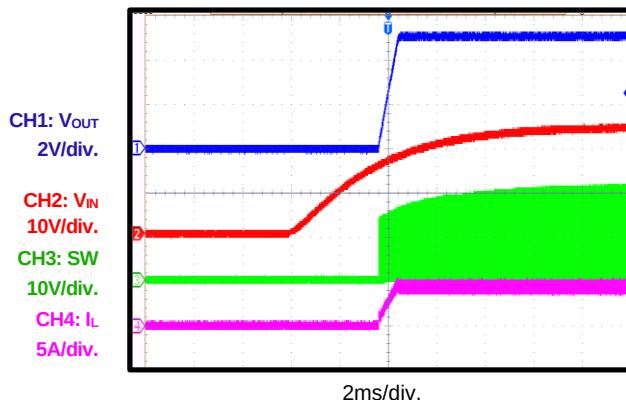
## Start-Up through VIN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$



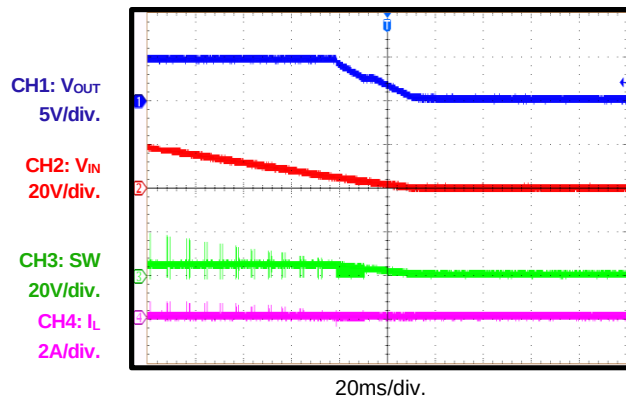
## Start-Up through VIN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$



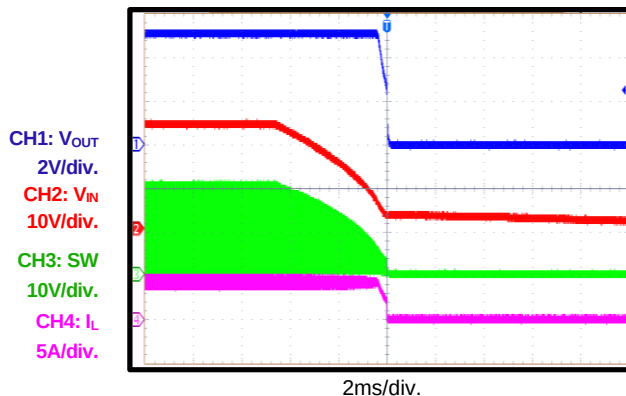
## Shutdown through VIN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$



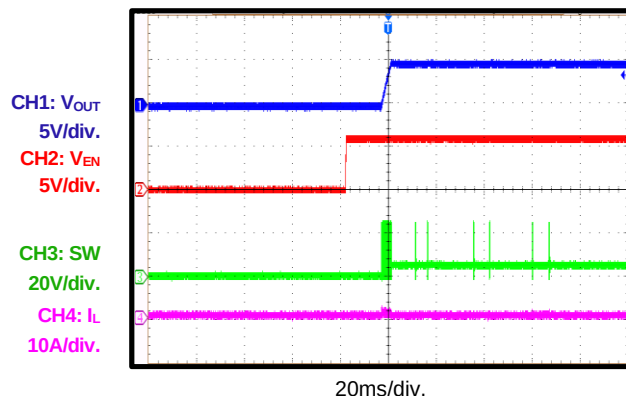
## Shutdown through VIN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$



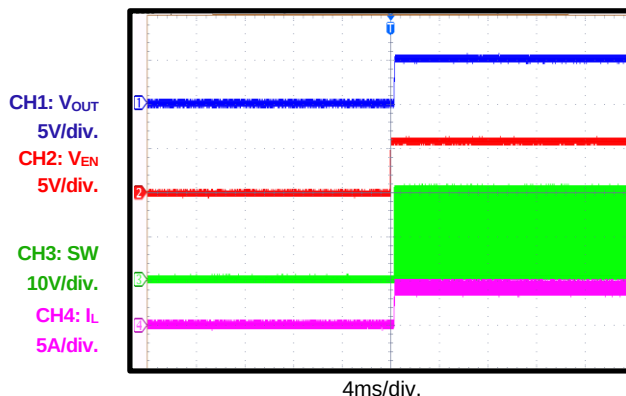
## Start-Up through EN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$



## Start-Up through EN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$

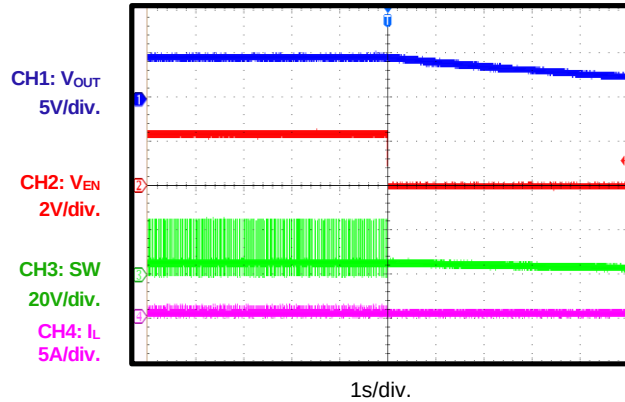


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , tested with the MP8880AGVE-0000, unless otherwise noted.

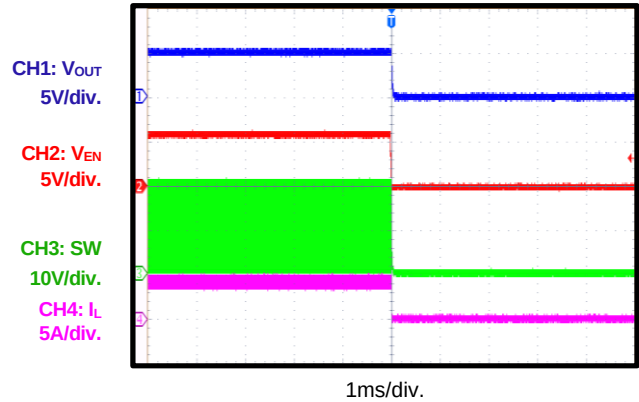
## Shutdown through EN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$



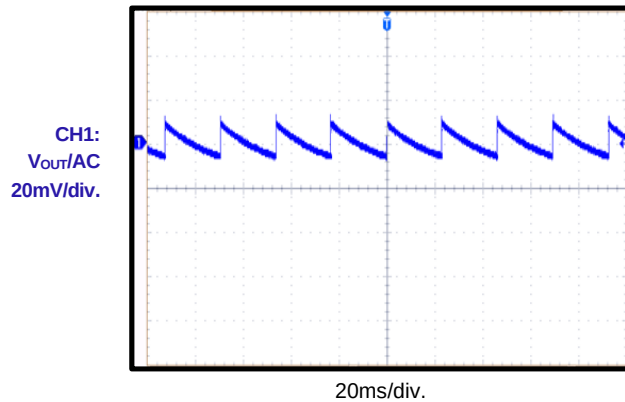
## Shutdown through EN

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$



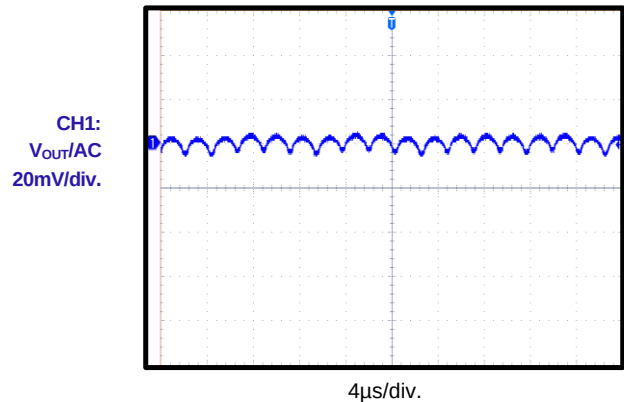
## Output Voltage Ripple

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$ ,  
 $C_{OUT} = 5 \times 22\mu F$



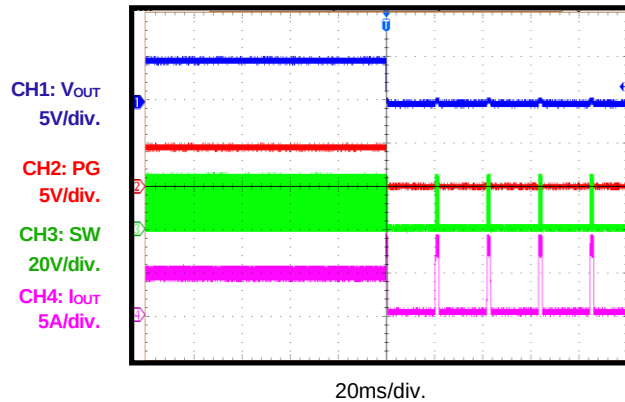
## Output Voltage Ripple

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$ ,  
 $C_{OUT} = 5 \times 22\mu F$



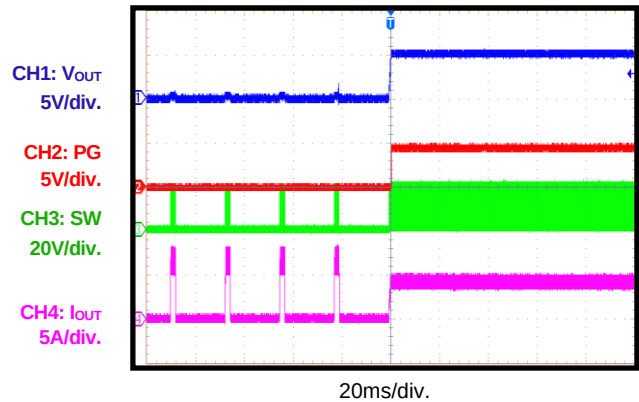
## SCP Entry

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$



## SCP Recovery

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$

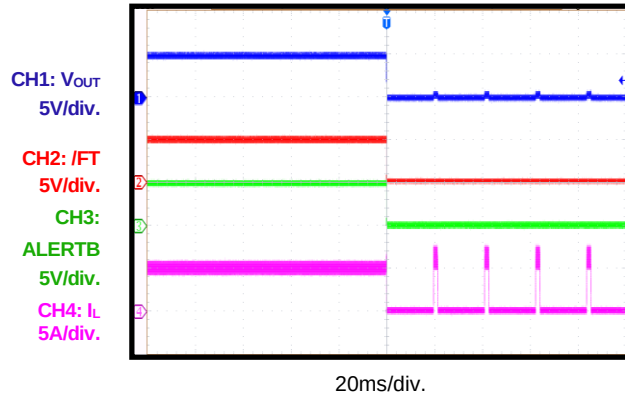


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , tested with the MP8880AGVE-0000, unless otherwise noted.

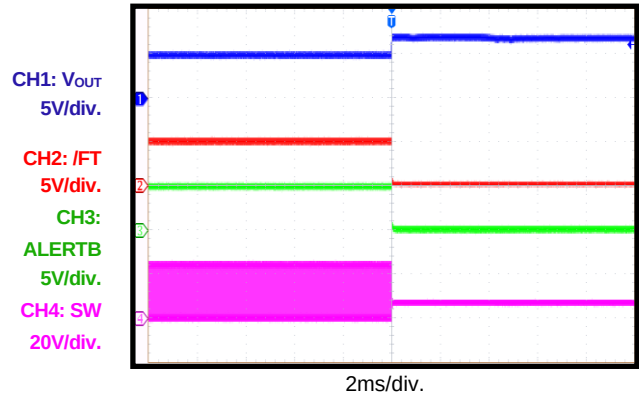
### OCP Entry

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$



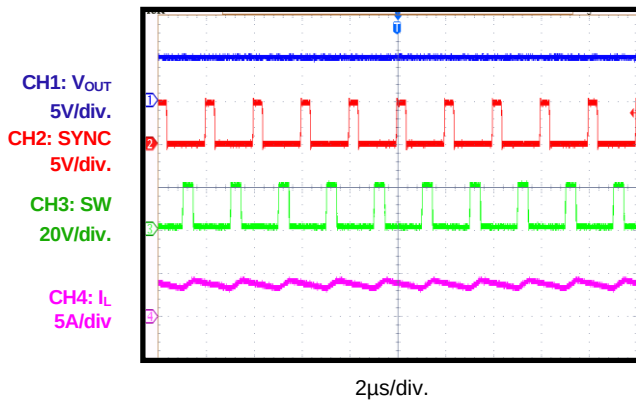
### OVP Entry

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$ , add 7V on  $V_{OUT}$



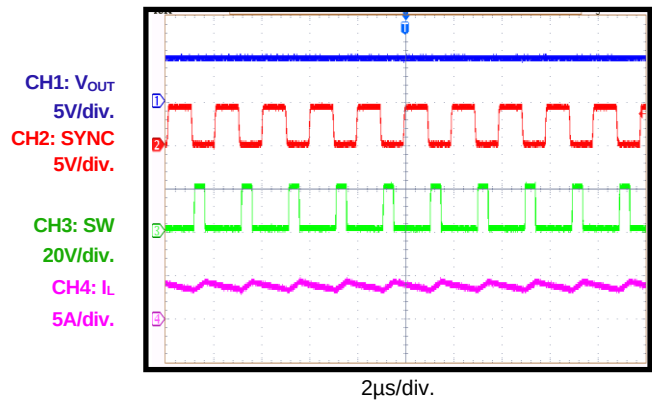
### SYNC In

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$ , SYNC input 500kHz with  $180^\circ$  phase shift



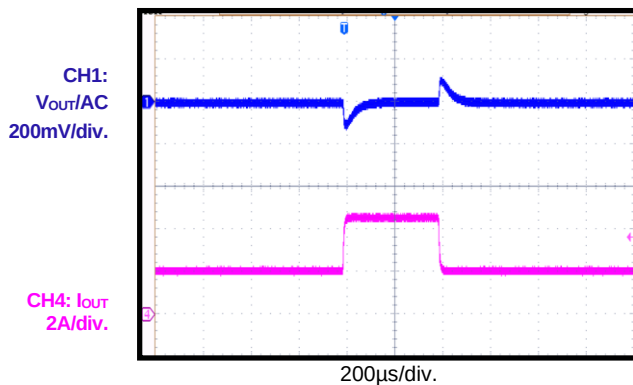
### SYNC Out

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 4.5A$ , SYNC output



### Load Transient Response

$V_{OUT} = 5V$ ,  $I_{OUT} = 2A$  to  $4.5A$ ,  $0.8A/\mu s$ ,  $C_{OUT} = 4 \times 22\mu F$



## FUNCTIONAL BLOCK DIAGRAM

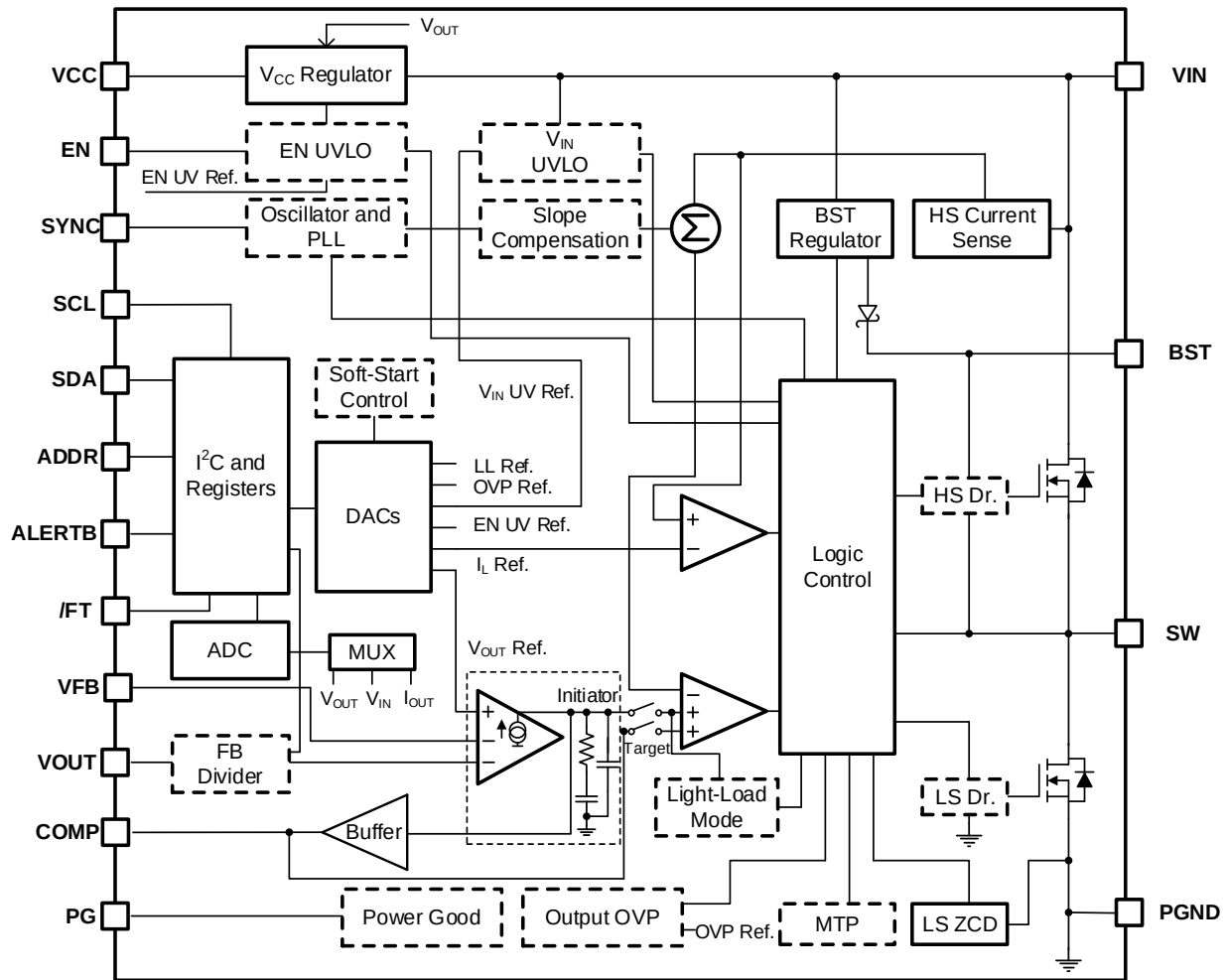


Figure 4: Functional Block Diagram

## OPERATION

The MP8880A is a high-frequency, synchronous, rectified, step-down switch-mode converter with built-in power MOSFETs. Figure 4 on page 15 shows the device's block diagram. The MP8880A is available with a wide input supply range and can achieve up to 4.5A of continuous output current ( $I_{OUT}$ ), with excellent load and line regulation across the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ambient temperature ( $T_A$ ) range.

### Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP8880A operates in fixed frequency, peak current control mode to regulate the output voltage ( $V_{OUT}$ ). An internal clock initiates the pulse-width modulation (PWM) cycle. At the clock's rising edge, the high-side MOSFET (HS-FET) turns on, and the inductor current ( $I_L$ ) rises linearly to provide energy to the load.

The HS-FET remains on until its current reaches the COMP voltage ( $V_{COMP}$ ), which is the output of the internal error amplifier.  $V_{COMP}$  depends on the difference between the output feedback voltage and the internal, high precision reference voltage.  $V_{COMP}$  determines how much energy should be transferred to the load.  $V_{COMP}$  is greater at higher load currents. Both the feedback divider ratio and the internal voltage reference can be adjusted by the PMBus, which allows  $V_{OUT}$  to be adjusted.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately and stays on until the next clock starts. During this period, the inductor current flows through the LS-FET. To avoid shoot-through, a dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time.

If the current in the HS-FET does not reach the COMP value in one switching period, the HS-FET remains on, avoiding a turn-off operation, until it reaches the peak current limit (see the Over-Current Protection (OCP) section on page 18 for more details).

### Light-Load Mode Selection (AAM Mode and FCCM)

At light loads, the MP8880A features configurable advanced asynchronous modulation (AAM) mode and forced continuous conduction mode (FCCM). The mode can be

selected via the PMBus. AAM mode optimizes light-load efficiency, while FCCM provides a constant switching frequency ( $f_{SW}$ ) and smaller output voltage ripples with lower efficiency at light loads.

When AAM mode is enabled, the MP8880A first enters discontinuous conduction mode (DCM) as  $I_L$  approaches zero. As the load further decreases to a no-load condition, the inductor peak current drops below the AAM mode peak current threshold set by the PMBus. The MP8880A enters AAM mode while consuming a very low quiescent current to further improve light-load efficiency (see Figure 5).

In AAM mode, the internal clock is blocked, and the MP8880A skips some pulses. If the feedback voltage ( $V_{FB}$ ) is below the reference voltage ( $V_{REF}$ ),  $V_{COMP}$  ramps up until the inductor peak current exceeds the AAM mode threshold. Then the internal clock is reset and the crossover time is used as the benchmark of the next clock. This control scheme helps the MP8880A achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As  $I_{OUT}$  increases from a light-load condition,  $V_{COMP}$  rises, and  $f_{SW}$  increases. If  $I_{OUT}$  exceeds the critical level set by the  $V_{COMP}$  threshold, the MP8880A resumes fixed-frequency PWM control in DCM or CCM.

When FCCM is enabled, the MP8880A operates in a fixed-frequency, peak current control mode to regulate  $V_{OUT}$ , regardless of  $I_{OUT}$ .

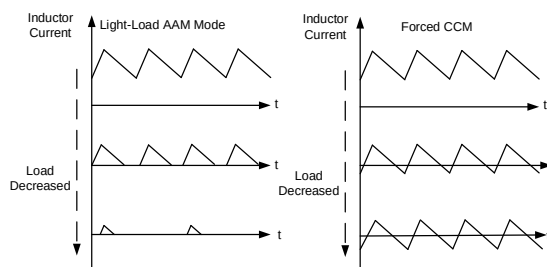


Figure 5: AAM Mode and Forced CCM

### Internal Regulator

An internal regulator powers most of the internal circuitries. This regulator takes  $V_{IN}$  and operates across the full  $V_{IN}$  range.

When  $V_{IN}$  exceeds 4.9V, the output of the regulator is in full regulation. Lower  $V_{IN}$  values result in lower output voltages. The regulator is enabled when  $V_{IN}$  exceeds its under-voltage lockout (UVLO) threshold and EN is high. After shutdown through EN, the internal VCC regulator is disabled to reduce power dissipation.

To improve thermal performance, a biased function can be enabled via the PMBus. When  $V_{OUT}$  exceeds 4.8V, VCC and the internal circuit are powered by  $V_{OUT}$ .

### Enable (EN) Control

EN is a digital control pin that controls the regulator, including when the PMBus block is on or off. Drive EN high to turn on the regulator; drive EN low to turn it off. The EN pin tolerates high voltages, and it can be pulled up to  $V_{IN}$ .

### Switching Frequency ( $f_{SW}$ )

The MP8880A's default  $f_{SW}$  is 450kHz, though this value can be set between 150kHz and 2.2MHz via the PMBus. The frequency can be set by a logic level synchronizing signal. For thermal considerations, do not use frequencies exceeding 1MHz when  $V_{IN}$  exceeds 30V.

### SYNC In and SYNC Out

The SYNC pin can be configured via the PMBus as SYNC in or SYNC out. When the device is configured as SYNC in, the internal oscillator frequency can be synchronized by an external clock via this pin. During start-up, the MP8880A first operates at frequencies set by the internal oscillator and quickly synchronizes to the external clock once soft start is finished. To drive the SYNC in function, ensure that the SYNC high-level voltage exceeds 1.6V, and the SYNC low-level voltage is below 0.4V. The recommended external SYNC frequency is between 200kHz and 2.5MHz.

The MP8880A operates in FCCM with a fixed frequency when there is a SYNC clock. It is recommended for clock pulses to be longer than 200ns.

When the SYNC pin is set as SYNC out, the device outputs a 180° phase-shift clock based on the internal oscillator. The SYNC pin does not need to be externally pulled up when the device is configured as SYNC out. This function allows two devices to operate at the same frequency with a 180° phase shift, which reduces the total

input current ripple and the input bypass capacitance.

The MP8880A supports up to 4 paralleled phases when the devices operate with a phase shift. All SYNC pins should be connected together during parallel operation. The initiator or target roles should be set to the correct phase shift via MFR\_POWER\_STAGE (EAh).

### Under-Voltage Lockout (UVLO)

The MP8880A has input UVLO protection to ensure there is reliable output power. This function prevents the device from operating at an insufficient  $V_{IN}$ . Assuming EN is active, the MP8880A turns on when  $V_{IN}$  exceeds the UVLO rising threshold. The device turns off when  $V_{IN}$  drops below the UVLO falling threshold. This is a non-latch protection. The UVLO threshold can be configured via the PMBus.

### Soft Start (SS)

To avoid overshoot during start-up, the MP8880A has built-in soft start (SS) to ramp up  $V_{OUT}$  with a controlled slew rate. When the device starts up, the internal circuitry generates a SS voltage ( $V_{SS}$ ) that ramps up slowly. When  $V_{SS}$  is below the internal reference voltage ( $V_{REF}$ ),  $V_{SS}$  overrides  $V_{REF}$  as the error amplifier reference. When  $V_{SS}$  exceeds  $V_{REF}$ ,  $V_{REF}$  acts as the reference. Then soft start finishes and the MP8880A enters steady state.

The SS time ( $t_{SS}$ ) can be configured via the PMBus. When the output is shorted to GND,  $V_{FB}$  is pulled low, and  $V_{SS}$  is discharged. The device initiates a normal soft start when it returns to a normal state.

### Pre-Biased Start-Up

If the output feedback voltage exceeds  $V_{SS}$  during start-up, this means that the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turn on until  $V_{SS}$  exceeds the feedback voltage.

### Power Good (PG) Indicator

The MP8880A has power good (PG) indication. The PG pin is an open-drain output that should be pulled up to a voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to GND before soft start is ready.

When  $V_{OUT}$  moves outside its rated voltage range, PG is pulled low to indicate an output failure status. When  $V_{OUT}$  recovers to be within the rated voltage range with a hysteresis, PG is pulled high after a delay (about 20 $\mu$ s). Both the PG threshold and hysteresis can be configured via the PMBus.

In multi-phase applications, only the initiator device's PG pin indicates the power good status.

### FAULT Indicator (/FT)

The /FT pin is an open-drain output that should be pulled up to a voltage source through a resistor (e.g. 100k $\Omega$ ). The /FT pin is pulled high during normal operation. Fault or warning statuses pull down the /FT pin, including input OVP, output OVP, OCP, and SCP. These statuses can be configured via the MFR\_FAULT\_CTRL (DBh) register.

The CLEAR\_FAULTS (03h) command clears any fault bits that have been set. If the fault is still present when the bit is cleared, the fault bit immediately sets again.

The /FT pin can be set to different power roles during multi-phase applications (see the Multiple-Phase Operation section on page 19).

### Over-Current Protection (OCP)

The MP8880A has cycle-by-cycle over-current limit control. The inductor current ( $I_L$ ) is monitored while the HS-FET is on. Once the inductor peak current exceeds the peak current limit, the HS-FET immediately turns off. Then the LS-FET turns on to discharge the energy, and  $I_L$  decreases. The HS-FET does not turn on again until  $I_L$  drops below the valley current limit. This prevents the inductor current from rising and damaging the components. Both the peak current and valley current limit can be configured via the PMBus.

When  $I_L$  exceeds the valley current limit, the OCP timer starts immediately. When the OCP timer reaches 32 continuous cycles, OCP is triggered. As  $I_L$  reaches the peak current limit during each cycle with this OCP timer, short-circuit protection (SCP, which triggers hiccup mode by default) may be triggered.

### Short-Circuit Protection (SCP)

If a short circuit occurs, the MP8880A immediately reaches its current limit.

Meanwhile,  $V_{OUT}$  drops to its under-voltage threshold, which is 90% of  $V_{OUT}$  by default. The device considers this an output dead short event and directly triggers SCP. There are three SCP modes that can be selected via the PMBus: hiccup mode (the default), current limit only mode, and latch-off mode.

In hiccup mode, the MP8880A first disables its output and resets the soft-start voltage, then initiates soft start. The hiccup time can be configured via the PMBus. If the short-circuit condition remains after soft start ends, the device repeats this operation until the short-circuit condition disappears, then the output returns to its regulation level. This protection greatly reduces the average short-circuit current by periodically restarting the part to alleviate thermal concerns and protect the regulator.

In current limit only mode, the MP8880A continues to operate while maintaining  $I_{OUT}$  at the value set via MFR\_OC\_FAULT\_LIMIT (E0h). In latch-off mode, the MP8880A turns off until its power is cycled or it is enabled again.

### Over-Voltage Protection (OVP)

The MP8880A monitors the feedback voltage to detect output over-voltage (OV) conditions. When  $V_{OUT}$  exceeds the OVP threshold, OVP is triggered. There are three OVP modes that can be selected via the PMBus: discharge mode (the default), ignore, and latch-off mode. In discharge mode, the LS-FET turns on to discharge the output until the current reaches the negative current limit. In ignore mode, the MP8880A takes no action and continues to operate without interruption. In latch-off mode, the MP8880A turns off until power is cycled or until it is enabled again.

The MP8880A also has optional input OVP. The threshold can be set via the PMBus. If  $V_{IN}$  exceeds its OVP threshold, the MP8880A stops switching. This is a non-latch protection, and the device returns to normal operation when the input OVP condition is removed.

### Thermal Shutdown

The MP8880A provides thermal protection by monitoring the IC temperature internally. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature ( $T_J$ ) exceeds the threshold, the

entire chip shuts down. This is a non-latch protection, meaning that once  $T_J$  drops below the hysteresis threshold, the device resumes operation by initiating a soft start.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating HS-FET driver. The floating driver has its own UVLO protection, with a rising threshold of 2.6V and a hysteresis of 200mV. When the LS-FET is on, the bootstrap capacitor voltage is charged to about 4.9V from VCC through a P-channel MOSFET pass transistor (see Figure 6).

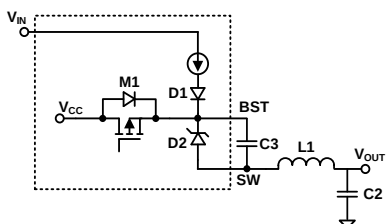


Figure 6: Internal Bootstrap Charging Circuit

When the voltage from BST to SW drops below the UVLO threshold, the HS-FET turns off. Then the LS-FET turns on with an HS minimum off time to conduct and refresh the charge on the BST capacitor.

At higher duty cycles, the internal charging circuit may not have sufficient voltage and time to charge the bootstrap capacitor. Add external circuitry to ensure that the bootstrap voltage is within the normal operation region.

### Low-Dropout Operation

To improve dropout, the MP8880A is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage exceeds the UVLO threshold.

If  $V_{IN}$  falls, the HS-FET remains on and close to 100% duty cycle to maintain output regulation, until the BST-to-SW voltage falls below the UVLO threshold. Since the supply current sourced from the BST capacitor is low, the BST charge refreshes infrequently, and the HS-FET can remain on for more switching cycles. This keeps the switching regulator's effective duty cycle high. The effective maximum duty cycle is 98%.

The effective duty cycle during regulator dropout is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, and PCB resistance.

### Multi-Phase Operation

The MP8880A supports up to 4-phase parallel operation, with phase shifts for high current capability. The MP8880A can use the /FT pin or multiple-time programmable (MTP) memory register to set the different power roles in parallel mode.

When MFR\_PWR\_STAGE\_SET (EAh), bit[4] is set to 0, multi-phase operation is set by the /FT pin during start-up. Table 1 shows the /FT configurations. /FT must be pulled up to VCC or pulled down to GND via a resistor (see Table 1).

Table 1: /FT Configuration in Multi-Phase Operation

| /FT Configuration             | 4-Phase Power Role | 2-Phase Power Role | Phase Delay |
|-------------------------------|--------------------|--------------------|-------------|
| Pull up to VCC                | Initiator          | Initiator          | 0°          |
| Pull down to GND via 20kΩ/1%  | Target 1           | N/A                | 90°         |
| Pull down to GND via 59kΩ/1%  | Target 2           | Target             | 180°        |
| Pull down to GND via 100kΩ/1% | Target 3           | N/A                | 270°        |

When MFR\_PWR\_STAGE\_SET (EAh), bit[4] is set to 1, multi-phase operation is set via the MTP. See the MFR\_PWR\_STAGE\_SET (EAh) section on page 40 for more details.

In multi-phase applications, connect the COMP pins of different chips together, then connect the SYNC pins together. If using the internal feedback divider, the VFB pin can be floating or connected to GND. If using the external feedback divider, only the VFB pin in the initiator chip must be configured with a feedback divider; meanwhile, the VFB pins in the target devices should be connected to the initiator's VFB. All devices should be set to same frequency via MFR\_FREQUENCY\_SWITCH (D4h). Figure 7 on page 20 shows the multi-phase connection with an internal FB divider.

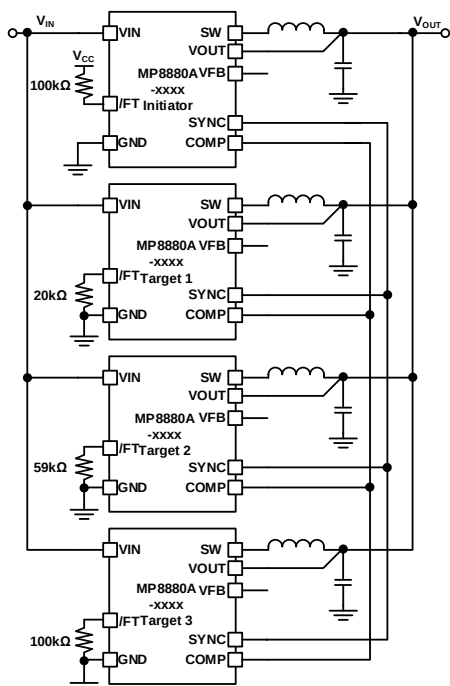


Figure 7: 4-Phase Connection with /FT (Internal FB Divider)

Figure 8 shows the multi-phase connection with an external FB divider.

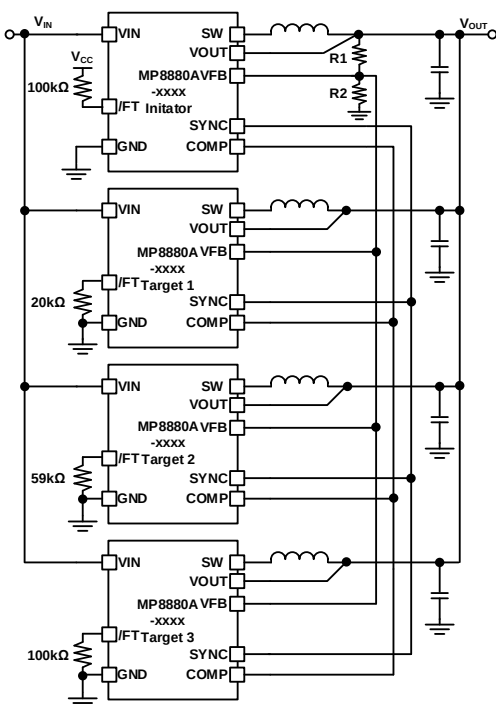


Figure 8: 4-Phase Connection with /FT (External FB Divider,  $V_{OUT} < 30V$ )<sup>(10)</sup>

**Note:**

- 10) When  $V_{OUT}$  exceeds 30V, the VOUT pin should be floating and not connected to the output.

## PMBus Control and Default Output Voltage

When the MP8880A is enabled,  $V_{IN}$  exceeds its UVLO threshold, EN is high, and OPERATION (01h), bit[7] is set to 1, the chip starts up at the default output voltage ( $V_{OUT}$ ).  $V_{OUT}$  is determined via PMBus control once the PMBus receives a valid  $V_{OUT}$ .

$V_{OUT}$  is set by adjusting the internal reference voltage and output feedback divider ratio. See the VOUT\_COMMAND (21h) section on page 26 and the MFR\_VOUT\_CTRL (D2h) section on page 33 for more details.

## Cyclic Redundancy Check (CRC) Protection

The integrity of the MTP is checked after the power cycle is reset. Each time the MTP contents are read, the MP8880A initiates a cyclic redundancy check (CRC). If a CRC error occurs, the registers attempt to read the contents again. If the error still occurs, the CML bit is set in the STATUS\_BYTE (78h) and STATUS\_WORD (79h) commands, and the ALERTB pin is pulled low.

## PMBUS INTERFACE

### PMBus Serial Interface Description

The power management bus (PMBus) is an open, standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled up to a bus voltage when they are idle. When connecting to the lines, an initiator device generates the SCL signal and device address, then arranges the communication sequence. The MP8880A is a PMBus target device that supports two fast modes: 400kHz and 1000kHz. The PMBus interface adds flexibility to the power supply solution.

### Target Address

Set a unique address for each target device that is connected to the same PMBus. The ADDR pin configures the lower 3 bits of the PMBus address. Table 2 shows the different resistor values from the ADDR pin to GND for the lower 3 bits. If the ADDR pin is floating, the address for the lower 3 bits is 111.

The higher 4 bits of the PMBus address are set via the MFR\_ADDRESS (D0h) register. These bits range between 0000 and 1111.

Table 2: PMBus Lower 3 Bits Address

| R <sub>ADDR</sub> (k $\Omega$ ) 1%      | Lower 3 Bits of Target Address |
|-----------------------------------------|--------------------------------|
| 0                                       | 000                            |
| 30                                      | 001                            |
| 49.9                                    | 010                            |
| 68                                      | 011                            |
| 88.7                                    | 100                            |
| 105                                     | 101                            |
| 127                                     | 110                            |
| Float the ADDR pin or pull it up to VCC | 111                            |

In addition, MFR\_RAIL\_ADDRESS (E8h) can be used to set the PMBus address digitally.

### Start and Stop Commands

The start and stop commands are signaled by the initiator device, and they signify the beginning and the end of the PMBus transfer, respectively. The start command is defined as the SDA signal transitioning from high to low while SCL is high. The stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 9).

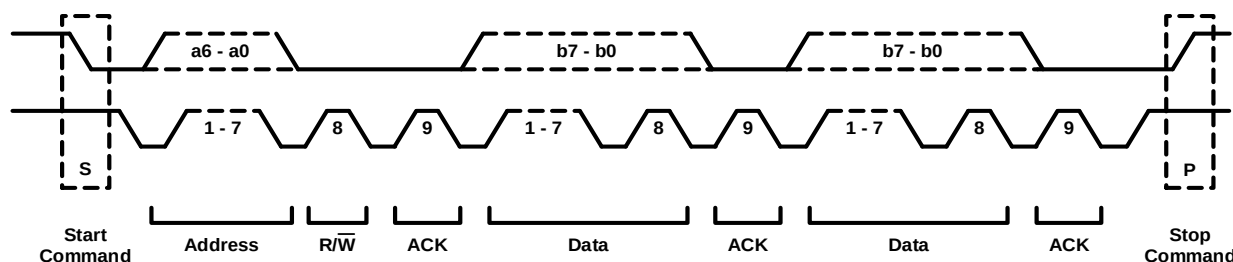


Figure 9: Data Transfer over the PMBus

The initiator then generates the SCL clocks, and transmits the device address and the read/write direction bit (R/W) on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge (ACK) bit.

### PMBus Update Sequence

The MP8880A requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8880A acknowledges by

pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP8880A. The MP8880A performs an update on the falling edge of the least significant bit (LSB) byte.

### PMBus Message Format

Figure 10 on page 22 shows the PMBus message format. Unshaded cells indicate when the bus host is driving the bus actively, while shaded cells indicate that the MP8880A is driving the bus. The symbols are listed below.

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$  = Write bit
- A = Acknowledge bit (0)

- $\overline{A}$  = Acknowledge bit (1)

Where A represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus initiator, the acknowledge bit for the last byte read is logic 1, indicated by  $\overline{A}$ .

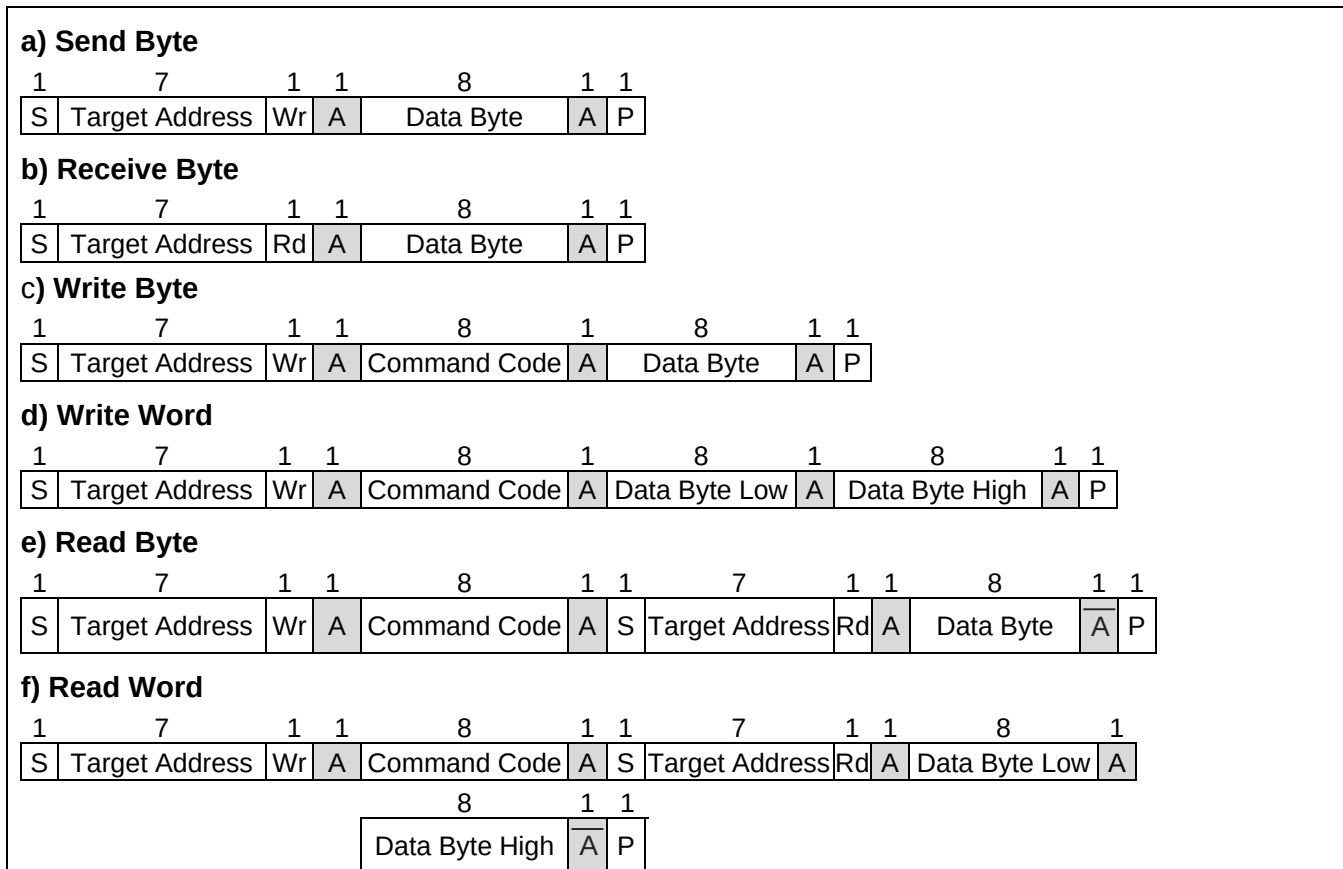


Figure 10: PMBus Message Format

## REGISTER DESCRIPTION <sup>(11)</sup>

| Command Name       | Command Code | Description                                                                                                                                          | Type      | Data Format | Units | MTP | Default Value |
|--------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------|-------|-----|---------------|
| OPERATION          | 0x01         | Turns the device on, off, or initiates a soft shutdown. Also determines if $V_{OUT}$ is margin high or margin low                                    | R/W Byte  | Reg         | -     | Yes | 80h           |
| CLEAR_FAULTS       | 0x03         | -                                                                                                                                                    | Send Byte | Reg         | -     | No  | -             |
| WRITE_PROTECT      | 0x10         | -                                                                                                                                                    | R/W Byte  | Reg         | -     | No  | 0h            |
| STORE_USER_ALL     | 0x15         | -                                                                                                                                                    | Send Byte | Reg         | -     | No  | -             |
| RESTORE_USER_ALL   | 0x16         | -                                                                                                                                                    | Send Byte | Reg         | -     | No  | -             |
| VOUT_COMMAND       | 0x21         | Sets the reference voltage. 1.5mV per LSB. $V_{OUT}$ can be calculated with the following equation:<br>$V_{OUT} = V_{REF} / \text{FB divider ratio}$ | R/W Word  | Direct      | V     | Yes | 1F4h          |
| VOUT_MAX           | 0x24         | -                                                                                                                                                    | R/W Word  | Direct      | V     | Yes | 395h          |
| VOUT_MARGIN_HIGH   | 0x25         | Default: 110% of $V_{OUT}$                                                                                                                           | R/W Word  | Direct      | V     | Yes | 226h          |
| VOUT_MARGIN_LOW    | 0x26         | Default: 90% of $V_{OUT}$                                                                                                                            | R/W Word  | Direct      | V     | Yes | 1C2h          |
| VIN_ON             | 0x35         | 132mV/LSB                                                                                                                                            | R/W Word  | Direct      | V     | Yes | 0h            |
| VIN_OFF            | 0x36         | 132mV/LSB                                                                                                                                            | R/W Word  | Direct      | V     | Yes | 0h            |
| VIN_OV_FAULT_LIMIT | 0x55         | 132mV/LSB                                                                                                                                            | R/W Word  | Direct      | V     | Yes | 1FCh          |
| TON_DELAY          | 0x60         | -                                                                                                                                                    | R/W Word  | Direct      | ms    | Yes | 0h            |
| TON_RISE           | 0x61         | -                                                                                                                                                    | R/W Word  | Direct      | ms    | Yes | 1h            |
| TOFF_DELAY         | 0x64         | -                                                                                                                                                    | R/W Word  | Direct      | ms    | Yes | 0h            |
| TOFF_FALL          | 0x65         | -                                                                                                                                                    | R/W Word  | Direct      | ms    | Yes | 1h            |
| STATUS_BYTE        | 0x78         | -                                                                                                                                                    | R Byte    | Reg         | -     | No  | -             |
| STATUS_WORD        | 0x79         | -                                                                                                                                                    | R Word    | Reg         | -     | No  | -             |
| STATUS_VOUT        | 0x7A         | -                                                                                                                                                    | R Byte    | Reg         | -     | No  | -             |
| STATUS_INPUT       | 0x7C         | -                                                                                                                                                    | R Byte    | Reg         | -     | No  | -             |
| STATUS_CML         | 0x7E         | -                                                                                                                                                    | R Byte    | Reg         | -     | No  | -             |
| READ_VIN           | 0x88         | 132mV/LSB                                                                                                                                            | R Word    | Direct      | V     | No  | -             |
| READ_VOUT          | 0x8B         | Reads the FB voltage. 3mV per LSB. $V_{OUT}$ can be calculated with the following equation:<br>$V_{OUT} = V_{REF} / \text{FB divider ratio}$         | R Word    | Direct      | V     | No  | -             |
| READ_IOUT          | 0x8C         | 19mA/LSB (23mA/LSB in low-dropout operation)                                                                                                         | R Word    | Direct      | V     | No  | -             |

## MFR COMMAND DESCRIPTION <sup>(11)</sup>

| Command Name               | Command Code | Description                                                                 | Type     | Data Format | Units | MTP | Default Value |
|----------------------------|--------------|-----------------------------------------------------------------------------|----------|-------------|-------|-----|---------------|
| MFR_ADDRESS                | 0xD0         | Sets the higher 4 bits of the 7-bit PMBus address                           | R/W Byte | Reg         | -     | Yes | 0h            |
| MFR_DITHER_CTRL            | 0xD1         | Configures dithering                                                        | R/W Byte | Reg         | -     | Yes | FDh           |
| MFR_VOUT_CTRL              | 0xD2         | Sets the V <sub>OUT</sub> mode, V <sub>OUT</sub> bias, and FB divider ratio | R/W Byte | Reg         | -     | Yes | 1Ch           |
| MFR_VOUT_TRANSITION_RATE   | 0xD3         | -                                                                           | R/W Byte | Reg         | V/ms  | Yes | 1h            |
| MFR_FREQ_SWITCH            | 0xD4         | The default f <sub>SW</sub> = 300kHz                                        | R/W Byte | Reg         | kHz   | Yes | 1h            |
| MFR_COMP1_CTRL             | 0xD6         | CTH, CTHP                                                                   | R/W Byte | Reg         | -     | Yes | 0h            |
| MFR_COMP2_CTRL             | 0xD7         | RTH, GM                                                                     | R/W Byte | Reg         | -     | Yes | Bh            |
| MFR_SLOPE_CTRL             | 0xD8         | Slope compensation                                                          | R/W Byte | Reg         | A/T   | Yes | Fh            |
| MFR_HYS_CTRL               | 0xD9         | Hysteresis control                                                          | R/W Byte | Reg         | -     | Yes | 3h            |
| MFR_PWM_CTRL               | 0xDA         |                                                                             | R/W Byte | Reg         | V/ns  | Yes | 3h            |
| MFR_FAULT_CTRL             | 0xDB         | Sets the indication for /FT                                                 | R/W Byte | Reg         | -     | Yes | 1Bh           |
| MFR_PRODUCT_ID             | 0xDD         | -                                                                           | R/W Byte | Reg         | -     | Yes | Ch            |
| MFR_PRODUCT_VERSION        | 0xDE         | -                                                                           | R/W Byte | Byte        | -     | Yes | 2h            |
| MFR_USER_VERSION           | 0xDF         | -                                                                           | R/W Byte | Reg         | -     | Yes | 0h            |
| MFR_OC_FAULT_LIMIT         | 0xE0         | -                                                                           | R/W Byte | Reg         | A     | Yes | 37h           |
| MFR_OC_RESPONSE            | 0xE1         | -                                                                           | R/W Byte | Reg         | -     | Yes | 60h           |
| MFR_VIN_OV_FAULT_RESPONSE  | 0xE2         | -                                                                           | R/W Byte | Reg         | -     | Yes | A0h           |
| MFR_VOUT_OV_FAULT_LIMIT    | 0xE3         | -                                                                           | R/W Byte | Reg         | -     | Yes | 0h            |
| MFR_VOUT_OV_FAULT_RESPONSE | 0xE4         | -                                                                           | R/W Byte | Reg         | -     | Yes | C0h           |
| MFR_VOUT_UV_FAULT_LIMIT    | 0xE5         | -                                                                           | R/W Byte | Reg         | -     | Yes | 1h            |
| MFR_VOUT_UV_FAULT_RESPONSE | 0xE6         | -                                                                           | R/W Byte | Reg         | -     | Yes | 20h           |
| MFR_RAIL_ADDRESS           | 0xE8         | -                                                                           | R/W Byte | Reg         | -     | Yes | 0h            |
| MFR_LIGHT_CTRL             | 0xE9         | -                                                                           | R/W Byte | Reg         | -     | Yes | 24h           |
| MFR_PWR_STAGE_SET          | 0xEA         | -                                                                           | R/W Byte | Reg         | -     | Yes | 10h           |

### Note:

11) All default values are based on the MP8880AGVE-0002.

## OPERATION (01h)

**Format:** Unsigned binary

The OPERATION command controls some behaviors for the MP8880A. Bit[7] controls when the DC/DC converter switches on or off. This means the MP8880A output can be turned on/off under host control via the PMBus. Bit[6] controls the shutdown behavior. If the PMBus device output is on (bit[7] = 1), then bits[5:4] control the basic source of the V<sub>OUT</sub> command.

| Bits | Access | Bit Name  | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|--------|-----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4  | R/W    | OPERATION | 4'b1000 | Selects the operation mode.<br>4'b00xx: The converter immediately turns off without the configurable delay and falling time<br>4'b01xx: The converter initiates a shot shutdown with a configurable delay and falling time set via TOFF_DELAY and TOFF_FALL, respectively<br>4'b1000: The converter is on with a normal output set via VOUT_COMMAND<br>4'b1001: The converter is on with a lower output set via VOUT_MARGIN_LOW<br>4'b1010: The converter is on with a higher output set via VOUT_MARGIN_HIGH |
| 3:0  | R      | RESERVED  | 4'b0000 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

## CLEAR\_FAULTS (03h)

**Format:** Unsigned binary

The CLEAR\_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. If the fault is still present when the bit is cleared, the fault bit immediately sets again. This command is write-only. There is no data byte for this command.

## WRITE\_PROTECT (10h)

**Format:** Unsigned binary

The WRITE\_PROTECT command controls writing to the MP8880A. The intent of this command is to provide protection against accidental changes. Write commands to all registers are enabled by default.

| Bits | Access | Bit Name      | Default   | Description                                                                                                                                                                                                                                                                                                                         |
|------|--------|---------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2  | R/W    | WRITE_PROTECT | 6'b000000 | Selects the operation mode.<br>6'b100000: Disable all writes except to the WRITE_PROTECT command<br>6'b010000: Disable all writes except to the WRITE_PROTECT and OPERATION commands<br>6'b001000: Disable all writes except to the WRITE_PROTECT, OPERATION, and VOUT_COMMAND commands<br>6'b000000: Enable writes to all commands |
| 1:0  | R      | RESERVED      | 2'b00     | Reserved.                                                                                                                                                                                                                                                                                                                           |

## STORE\_USER\_ALL (15h)

**Format:** Unsigned binary

The STORE\_USER\_ALL command instructs the PMBus device to copy the entire contents of the operating memory to the matching locations in the MTP (the non-volatile user store memory). Any items in the operating memory that do not have matching locations in the user store are ignored.

The MP8880A automatically turns off EN then writes all the data from the converter memory map to the internal MTP. After the device finishes writing to the MTP block, the device restarts again with the new configuration data from the MTP. This process starts when the MP8880A receives a STORE\_USER\_ALL command from the PMBus interface.

The MTP can be configured an unlimited number of times. To configure the MTP successfully,  $V_{IN}$  must exceed 10V.

This command has no data bytes. This command is write-only.

### RESTORE\_USER\_ALL (16h)

**Format:** Unsigned binary

The RESTORE\_USER\_ALL command instructs the PMBus device to copy the entire contents of the non-volatile user store memory (MTP) to the matching locations in the operating memory (PMBus register). The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored.

It is permitted to use the RESTORE\_USER\_ALL even when the device is not configured for the MTP. While restoring MTP data to the user memory, the device executes a CRC calculation and compares the calculation with the stored CRC result in the MTP cell. The MTP value is restored to the operating memory only when these values match.

First the output turns off during this operation. After MTP configuration is complete, the output turns on again with the new configuration data from the MTP.

There is no data byte for this command. This command is write-only.

### VOUT\_COMMAND (21h)

**Format:** Direct

The VOUT\_COMMAND command sets the feedback reference voltage, which can be used to calculate  $V_{OUT}$ .

| Bits  | Access | Bit Name     | Default            | Description                 |
|-------|--------|--------------|--------------------|-----------------------------|
| 15:10 | R/W    | RESERVED     | 6'b000000          | Reserved.                   |
| 9:0   | R/W    | VOUT_COMMAND | 10'b011111<br>0100 | Sets $V_{REF}$ . 1.5mV/LSB. |

The output voltage is determined by the reference voltage and FB divider ratio. The output voltage ( $V_{OUT}$ , in V) can be estimated with Equation (1):

$$V_{OUT} (V) = 0.0015 \times (X / \text{FB Divider Ratio}) \quad (1)$$

Where  $X$  is the 10-bit, unsigned binary integer of VOUT\_COMMAND, bits[9:0] (1.5mV per LSB). The internal FB divider ratio is selected via MFR\_VOUT\_CTRL (D2h), while the external divider ratio is defined by  $R2 / (R1 + R2)$  (see Figure 12 on page 45).

In external feedback divider mode, the external resistor divider sets  $V_{OUT}$ . In addition, the internal feedback divider ratio should be set to 1:16 when using an external divider. In internal feedback divider mode, the internal FB divider ratio should be selected via MFR\_VOUT\_CTRL (D2h) (see Table 3).

**Table 3: Internal FB Divider Ratio**

| MFR_VOUT_CTRL (D2h), Bits[2:0] | Internal FB Divider Ratio | Output Range             |
|--------------------------------|---------------------------|--------------------------|
| 000                            | 1:1                       | Range 1: 0.6V to 1.5345V |
| 001                            | 1:2                       | Range 2: 0.6V to 3.069V  |
| 010                            | 1:4                       | Range 3: 0.6V to 6.138V  |
| 011                            | 1:8                       | Range 4: 1.2V to 12.276V |
| 100                            | 1:16                      | Range 5: 2.4V to 24.552V |

## VOUT\_MAX (24h)

**Format:** Direct

The VOUT\_MAX command sets an upper limit on the reference voltage ( $V_{REF}$ ), which limits  $V_{OUT}$ . This command provides a safeguard against accidentally setting  $V_{OUT}$  to a possibly destructive level, rather than keeping it below the primary output over-voltage protection (OVP) threshold.

| Bits  | Access | Bit Name | Default        | Description                             |
|-------|--------|----------|----------------|-----------------------------------------|
| 15:10 | R/W    | RESERVED | 6'b000000      | Reserved.                               |
| 9:0   | R/W    | VOUT_MAX | 10'b1110010101 | Sets the maximum $V_{REF}$ . 1.5mV/LSB. |

The maximum  $V_{OUT}$  limit is determined by the maximum reference voltage and FB divider ratio. The maximum  $V_{OUT}$  limit ( $V_{OUT\_MAX}$ , in V) can be estimated with Equation (2):

$$V_{OUT\_MAX} (V) = 0.0015 \times (X / \text{FB Divider Ratio}) \quad (2)$$

Where  $X$  is the 10-bit, unsigned binary integer of VOUT\_MAX, bits[9:0] (1.5mV per LSB). The internal FB divider ratio is set via MFR\_VOUT\_CTRL (D2h), while the external divider ratio is defined by  $R2 / (R1 + R2)$  (see Figure 12 on page 45).

## VOUT\_MARGIN\_HIGH (25h)

**Format:** Direct

The VOUT\_MARGIN\_HIGH command stores the reference voltage in response to the margin high action in OPERATION (01h).

| Bits  | Access | Bit Name         | Default        | Description                                 |
|-------|--------|------------------|----------------|---------------------------------------------|
| 15:10 | R/W    | RESERVED         | 6'b000000      | Reserved.                                   |
| 9:0   | R/W    | VOUT_MARGIN_HIGH | 10'b1000100110 | Sets the margin high $V_{REF}$ . 1.5mV/LSB. |

The margin high  $V_{OUT}$  is determined by the margin high reference voltage and the FB divider ratio. The margin high  $V_{OUT}$  ( $V_{OUT\_MARGIN\_HIGH}$ , in V) can be calculated with Equation (3):

$$V_{OUT\_MARGIN\_HIGH} (V) = 0.0015 \times (X / \text{FB Divider Ratio}) \quad (3)$$

Where  $X$  is the 10-bit, unsigned binary integer of VOUT\_MARGIN\_HIGH, bits[9:0] (1.5mV per LSB). The internal FB divider ratio is set via MFR\_VOUT\_CTRL (D2h), while the external divider ratio is defined by  $R2 / (R1 + R2)$  (see Figure 12 on page 45).

## VOUT\_MARGIN\_LOW (26h)

**Format:** Direct

The VOUT\_MARGIN\_LOW command stores the reference voltage in response to the margin low action in OPERATION (01h).

| Bits  | Access | Bit Name        | Default        | Description                                |
|-------|--------|-----------------|----------------|--------------------------------------------|
| 15:10 | R/W    | RESERVED        | 6'b000000      | Reserved.                                  |
| 9:0   | R/W    | VOUT_MARGIN_LOW | 10'b0111000010 | Sets the margin low $V_{REF}$ . 1.5mV/LSB. |

The margin low  $V_{OUT}$  is determined by the margin low reference voltage and FB divider ratio. The margin low  $V_{OUT}$  ( $V_{OUT\_MARGIN\_LOW}$ , in V) can be estimated with Equation (4):

$$V_{OUT\_MARGIN\_LOW} (V) = 0.0015 \times (X / \text{FB Divider Ratio}) \quad (4)$$

Where  $X$  is the 10-bit, unsigned binary integer of VOUT\_MARGIN\_LOW, bits[9:0] (1.5mV per LSB). The internal FB divider ratio is set by MFR\_VOUT\_CTRL (D2h), while the external divider ratio is defined by  $R2 / (R1 + R2)$  (see Figure 12 on page 45).

### VIN\_ON (35h)

**Format:** Direct

The VIN\_ON command sets the V<sub>IN</sub> under-voltage lockout (UVLO) rising threshold via the PMBus.

| Bits | Access | Bit Name | Default           | Description                                                |
|------|--------|----------|-------------------|------------------------------------------------------------|
| 15:9 | R/W    | RESERVED | 7'b00000000       | Reserved.                                                  |
| 8:0  | R/W    | VIN_ON   | 9'b00000000<br>00 | Sets the V <sub>IN</sub> UVLO rising threshold. 132mV/LSB. |

When the VIN\_ON register value is set to be below 1Bh, the V<sub>IN</sub> UVLO rising threshold is 3.5V. When the VIN\_ON register value exceeds 1Bh, the V<sub>IN</sub> UVLO rising threshold is set via the VIN\_ON register.

### VIN\_OFF (36h)

**Format:** Direct

The VIN\_OFF command sets the V<sub>IN</sub> under-voltage lockout (UVLO) falling threshold via the PMBus.

| Bits | Access | Bit Name | Default           | Description                                                 |
|------|--------|----------|-------------------|-------------------------------------------------------------|
| 15:9 | R/W    | RESERVED | 7'b00000000       | Reserved.                                                   |
| 8:0  | R/W    | VIN_OFF  | 9'b00000000<br>00 | Sets the V <sub>IN</sub> UVLO falling threshold. 132mV/LSB. |

When the VIN\_OFF register value is set to be below 18h, the V<sub>IN</sub> UVLO falling threshold is 3V. When the VIN\_OFF register value exceeds 18h, the V<sub>IN</sub> UVLO falling threshold is set by the VIN\_OFF register.

### VIN\_OV\_FAULT\_LIMIT (55h)

**Format:** Direct

The VIN\_OV\_FAULT\_LIMIT command sets the input over-voltage (OV) fault threshold.

| Bits | Access | Bit Name           | Default           | Description                                   |
|------|--------|--------------------|-------------------|-----------------------------------------------|
| 15:9 | R/W    | RESERVED           | 7'b00000000       | Reserved.                                     |
| 8:0  | R/W    | VIN_OV_FAULT_LIMIT | 9'b11111111<br>00 | Sets the input OV fault threshold. 132mV/LSB. |

### TON\_DELAY (60h)

**Format:** Direct

The TON\_DELAY command sets the delay time from when EN turns on to when the output starts rising. TON\_DELAY is valid when the EN pin is on and PMBus commands the device on.

| Bits | Access | Bit Name  | Default           | Description                                                                          |
|------|--------|-----------|-------------------|--------------------------------------------------------------------------------------|
| 15:7 | R/W    | RESERVED  | 9'b00000000<br>00 | Reserved.                                                                            |
| 6:0  | R/W    | TON_DELAY | 7'b00000000       | Sets the delay time from when EN turns on to when the output starts rising. 1ms/LSB. |

### TON\_RISE (61h)

**Format:** Direct

The TON\_RISE command sets the period when V<sub>OUT</sub> rises from 10% to 90% of its target voltage.

| Bits | Access | Bit Name | Default               | Description                                                                                 |
|------|--------|----------|-----------------------|---------------------------------------------------------------------------------------------|
| 15:5 | R/W    | RESERVED | 11'b00000000<br>00000 | Reserved.                                                                                   |
| 4:0  | R/W    | TON_RISE | 5'b000001             | Sets the period when V <sub>OUT</sub> rises from 10% to 90% of its target voltage. 1ms/LSB. |

## TOFF\_DELAY (64h)

**Format:** Direct

The TOFF\_DELAY command sets the delay time from when EN turns off to when the output starts falling. TOFF\_DELAY is valid when the PMBus receives an off command. When the EN pin turns off, the output falls immediately.

| Bits | Access | Bit Name   | Default     | Description                                                                            |
|------|--------|------------|-------------|----------------------------------------------------------------------------------------|
| 15:7 | R/W    | RESERVED   | 9'b00000000 | Reserved.                                                                              |
| 6:0  | R/W    | TOFF_DELAY | 7'b00000000 | Sets the delay time from when EN turns off to when the output starts falling. 1ms/LSB. |

## TOFF\_FALL (65h)

**Format:** Direct

The TOFF\_FALL command sets the period when V<sub>OUT</sub> falls from 90% to 10% of its target voltage.

| Bits | Access | Bit Name  | Default          | Description                                                                                 |
|------|--------|-----------|------------------|---------------------------------------------------------------------------------------------|
| 15:5 | R/W    | RESERVED  | 11'b000000000000 | Reserved.                                                                                   |
| 4:0  | R/W    | TOFF_FALL | 5'b00001         | Sets the period when V <sub>OUT</sub> falls from 90% to 10% of its target voltage. 1ms/LSB. |

## STATUS\_BYTE (78h)

**Format:** Unsigned binary

The STATUS\_BYTE command returns the flags indicating the state of the MP8880A. Once a live fault is removed, the bit is cleared automatically. To clear the latched fault bits, remove the underlying fault and issue a CLEAR\_FAULTS (03h) command.

| Bits | Access | Bit Name      | Behavior | Default | Description                                                                                                                    |
|------|--------|---------------|----------|---------|--------------------------------------------------------------------------------------------------------------------------------|
| 7    | R      | BUSY          | Live     | 1'b0    | Declares a fault when the device is busy and unable to respond.                                                                |
| 6    | R      | OFF           | Live     | 1'b0    | Asserts whether the device is not providing power to the output, regardless of the reason (even if the device is not enabled). |
| 5    | R      | VOUT_OV_FAULT | Latch    | 1'b0    | Indicates whether an output over-voltage fault has occurred.                                                                   |
| 4    | R      | IOUT_OC_FAULT | Latch    | 1'b0    | Indicates whether an output over-current fault has occurred.                                                                   |
| 3:2  | R      | RESERVED      | N/A      | 2'b00   | Reserved.                                                                                                                      |
| 1    | R      | CML           | Latch    | 1'b0    | Indicates whether a communications, memory, or logic fault has occurred.                                                       |
| 0    | R      | RESERVED      | N/A      | 1'b0    | Reserved.                                                                                                                      |

## STATUS\_WORD (79h)

**Format:** Unsigned binary

The STATUS\_WORD returns the flags indicating the state of the MP8880A. Once a live fault is removed, the bit is cleared automatically. To clear the latched fault bits, remove the underlying fault and issue a CLEAR\_FAULTS (03h) command.

| Bits | Access | Bit Name | Behavior | Default | Description                                                        |
|------|--------|----------|----------|---------|--------------------------------------------------------------------|
| 15   | R      | VOUT     | Latch    | 1'b0    | Indicates whether an output voltage fault or warning has occurred. |

|      |   |               |       |        |                                                                                                                                |
|------|---|---------------|-------|--------|--------------------------------------------------------------------------------------------------------------------------------|
| 14   | R | IOUT/POUT     | Latch | 1'b0   | Indicates whether an output current or output power fault or warning has occurred.                                             |
| 13   | R | INPUT         | Latch | 1'b0   | An input voltage, input current, or input power fault or warning has occurred.                                                 |
| 12   | R | RESERVED      | N/A   | 1'b0   | Reserved.                                                                                                                      |
| 11   | R | PG_STATUS     | Live  | 1'b0   | Returns the POWER_GOOD signal. If this bit is set to 0, an output is present.                                                  |
| 10:8 | R | RESERVED      | N/A   | 3'b000 | Reserved.                                                                                                                      |
| 7    | R | BUSY          | Live  | 1'b0   | Indicates whether a fault was declared because the device was busy and unable to respond.                                      |
| 6    | R | OFF           | Live  | 1'b0   | Asserts whether the device is not providing power to the output, regardless of the reason (even if the device is not enabled). |
| 5    | R | VOUT_OV_FAULT | Latch | 1'b0   | Indicates whether an output over-voltage fault has occurred.                                                                   |
| 4    | R | IOUT_OC_FAULT | Latch | 1'b0   | Indicates whether an output over-current fault has occurred.                                                                   |
| 3    | R | VIN_UV_FAULT  | Latch | 1'b0   | Indicates whether an input under-voltage fault has occurred.                                                                   |
| 2    | R | RESERVED      | N/A   | 1'b0   | Reserved.                                                                                                                      |
| 1:0  | R | RESERVED      | N/A   | 1'b0   | Reserved.                                                                                                                      |

### STATUS\_VOUT (7Ah)

**Format:** Unsigned binary

The STATUS\_VOUT command returns the flags indicating the device's output voltage status. To clear bits in this register, remove the underlying fault and issue a CLEAR\_FAULTS (03h) command.

| Bits | Access | Bit Name      | Behavior | Default | Description                                                   |
|------|--------|---------------|----------|---------|---------------------------------------------------------------|
| 7    | R      | VOUT_OV_FAULT | Latch    | 1'b0    | Indicates whether an output over-voltage fault has occurred.  |
| 6:5  | R      | RESERVED      | N/A      | 2'b00   | Reserved.                                                     |
| 4    | R      | VOUT_UV_FAULT | Latch    | 1'b0    | Indicates whether an output under-voltage fault has occurred. |
| 3:0  | R      | RESERVED      | N/A      | 4'b0000 | Reserved.                                                     |

### STATUS\_INPUT (7Ch)

**Format:** Unsigned binary

The STATUS\_INPUT command returns the flags indicating the device's input voltage status. To clear bits in this register, remove the underlying fault and issue a CLEAR\_FAULTS (03h) command.

| Bits | Access | Bit Name     | Behavior | Default | Description                                                  |
|------|--------|--------------|----------|---------|--------------------------------------------------------------|
| 7    | R      | VIN_OV_FAULT | Latch    | 1'b0    | Indicates whether an input over-voltage fault has occurred.  |
| 6:5  | R      | RESERVED     | N/A      | 2'b00   | Reserved.                                                    |
| 4    | R      | VIN_UV_FAULT | Latch    | 1'b0    | Indicates whether an input under-voltage fault has occurred. |
| 3:0  | R      | RESERVED     | N/A      | 4'b0000 | Reserved.                                                    |

## STATUS\_CML (7Eh)

**Format:** Unsigned binary

The STATUS\_CML command returns the flags indicating the device's PMBus command status. To clear bits in this register, remove the underlying fault and issue a CLEAR\_FAULTS (03h) command.

| Bits | Access | Bit Name            | Behavior | Default | Description                                                                                                           |
|------|--------|---------------------|----------|---------|-----------------------------------------------------------------------------------------------------------------------|
| 7    | R      | INVALID_COMMAND     | Latch    | 1'b0    | Indicates whether an invalid command has been received by the PMBus.                                                  |
| 6    | R      | INVALID_DATA        | Latch    | 1'b0    | Indicates whether invalid data has been received by the PMBus.                                                        |
| 5    | R      | PEC_FAIL            | Latch    | 1'b0    | Indicates whether a PMBus package error check (PEC) fails.                                                            |
| 4    | R      | MEMORY_FAULT        | Latch    | 1'b0    | Indicates whether a memory fault has been detected (e.g. the CRC of the memory does not match the initial CRC value). |
| 3:2  | R      | RESERVED            | N/A      | 2'b00   | Reserved.                                                                                                             |
| 1    | R      | COMMUNICATION_FAULT | Latch    | 1'b0    | Indicates whether a communication fault other than the ones listed in this table has occurred                         |
| 0    | R      | RESERVED            | N/A      | 1'b0    | Reserved.                                                                                                             |

## READ\_VIN (88h)

**Format:** Direct

The READ\_VIN command returns the measured input voltage.

| Bits | Access | Bit Name | Default      | Description                                    |
|------|--------|----------|--------------|------------------------------------------------|
| 15:9 | R      | RESERVED | 7'b0000000   | Reserved.                                      |
| 8:0  | R      | READ_VIN | 9'b000000000 | Returns the measured input voltage. 132mV/LSB. |

The input voltage ( $V_{IN}$ , in V) can be calculated with Equation (5):

$$V_{IN} (V) = 0.132 \times (X) \quad (5)$$

Where  $X$  is the 9-bit, unsigned binary integer of READ\_VIN, bits[8:0] (132mV per LSB). It is recommended to read this result more than 5 times and take the average value to improve accuracy.

## READ\_VOUT (8Bh)

**Format:** Direct

The READ\_VOUT command returns the feedback voltage.

| Bits | Access | Bit Name  | Default      | Description                            |
|------|--------|-----------|--------------|----------------------------------------|
| 15:9 | R      | RESERVED  | 7'b0000000   | Reserved.                              |
| 8:0  | R      | READ_VOUT | 9'b000000000 | Returns the feedback voltage. 3mV/LSB. |

The output voltage is determined by the feedback voltage and FB divider ratio.  $V_{OUT}$  can be estimated with Equation (6):

$$V_{OUT} (V) = 0.003 \times (X / \text{FB Divider Ratio}) \quad (6)$$

Where  $X$  is the 9-bit, unsigned binary integer of READ\_VOUT, bits[8:0] (3mV per LSB). The internal FB divider ratio is selected by MFR\_VOUT\_CTRL (D2h), while the external divider ratio is defined by  $R2 / (R1 + R2)$  (see Figure 12 on page 45). It is recommended to read this result more than 5 times and take the average value to improve accuracy.

## READ\_IOUT (8Ch)

**Format:** Direct

The READ\_IOUT command returns the measured  $I_{OUT}$ .

| Bits | Access | Bit Name  | Default           | Description                                                                    |
|------|--------|-----------|-------------------|--------------------------------------------------------------------------------|
| 15:9 | R      | RESERVED  | 7'b0000000        | Reserved.                                                                      |
| 8:0  | R      | READ_IOUT | 9'b0000000<br>000 | Returns the measured $I_{OUT}$ . 19mA/LSB (23mA/LSB in low-dropout operation). |

READ\_IOUT returns the output current with 19mA per LSB when the device is not operating in low-dropout mode. When the device operates in low-dropout mode and the duty cycle is close to 100%, the LSB is 23mA.

## MFR\_ADDRESS (D0h)

**Format:** Unsigned binary

The MFR\_ADDRESS command sets the 4 higher bits of the 7-bit PMBus address.

| Bits | Access | Bit Name      | Default | Description                                                                                                           |
|------|--------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------|
| 7:4  | R/W    | RESERVED      | 4'b0000 | Reserved.                                                                                                             |
| 3:0  | R/W    | PMBUS_ADDRESS | 4'b0000 | Sets the higher 4 bits of the 7-bit PMBus address. The lower 3 bits are set by the ADDR pin (see Table 2 on page 21). |

## MFR\_DITHER\_CTRL (D1h)

**Format:** Unsigned binary

The MFR\_DITHER\_CTRL command controls the frequency dithering function. Frequency dithering reduces peak emissions at a specific frequency.

| Bits | Access                          | Bit Name              | Default                           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
|------|---------------------------------|-----------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------|------|--------------|------|---------------------------------|------|-----------------------------------|------|--------------------------------|------|---------------------------------|------|--------------------------------|------|-----------------------------------|------|--------------------------------|------|-----------|------|------|------|-------|------|------|------|-------|------|------|------|-------|------|------|------|-------|
| 7    | R/W                             | DITHER_ENABLE/DISABLE | 1'b1                              | 0: Disable frequency dithering<br>1: Enable frequency dithering                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 6:3  | R/W                             | DITHER_CYCLE          | 4'b1111                           | Sets the dither cycle. <table><tr><th>Bits</th><th>Dither Cycle</th><th>Bits</th><th>Dither Cycle</th></tr><tr><td>0000</td><td>No dither</td><td>1000</td><td>108μs</td></tr><tr><td>0001</td><td>14μs</td><td>1001</td><td>120μs</td></tr><tr><td>0010</td><td>28μs</td><td>1010</td><td>132μs</td></tr><tr><td>0011</td><td>42μs</td><td>1011</td><td>146μs</td></tr><tr><td>0100</td><td>54μs</td><td>1100</td><td>160μs</td></tr><tr><td>0101</td><td>68μs</td><td>1101</td><td>175μs</td></tr><tr><td>0110</td><td>81μs</td><td>1110</td><td>190μs</td></tr><tr><td>0111</td><td>94μs</td><td>1111</td><td>204μs</td></tr></table> | Bits | Dither Cycle | Bits | Dither Cycle | 0000 | No dither                       | 1000 | 108μs                             | 0001 | 14μs                           | 1001 | 120μs                           | 0010 | 28μs                           | 1010 | 132μs                             | 0011 | 42μs                           | 1011 | 146μs     | 0100 | 54μs | 1100 | 160μs | 0101 | 68μs | 1101 | 175μs | 0110 | 81μs | 1110 | 190μs | 0111 | 94μs | 1111 | 204μs |
| Bits | Dither Cycle                    | Bits                  | Dither Cycle                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0000 | No dither                       | 1000                  | 108μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0001 | 14μs                            | 1001                  | 120μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0010 | 28μs                            | 1010                  | 132μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0011 | 42μs                            | 1011                  | 146μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0100 | 54μs                            | 1100                  | 160μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0101 | 68μs                            | 1101                  | 175μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0110 | 81μs                            | 1110                  | 190μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 0111 | 94μs                            | 1111                  | 204μs                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 2:0  | R/W                             | DITHER_RANGE          | 3'b101                            | Sets the dither range, where f <sub>sw</sub> is switching frequency. <table><tr><th>Bits</th><th>Dither Range</th><th>Bits</th><th>Dither Range</th></tr><tr><td>000</td><td>108% to 126% of f<sub>sw</sub></td><td>100</td><td>102.5% to 110% of f<sub>sw</sub></td></tr><tr><td>001</td><td>104% to 121% x f<sub>sw</sub></td><td>101</td><td>102% to 107% of f<sub>sw</sub></td></tr><tr><td>010</td><td>104% to 117% x f<sub>sw</sub></td><td>110</td><td>102% to 103.5% of f<sub>sw</sub></td></tr><tr><td>011</td><td>103% to 113% x f<sub>sw</sub></td><td>111</td><td>No dither</td></tr></table>                                | Bits | Dither Range | Bits | Dither Range | 000  | 108% to 126% of f <sub>sw</sub> | 100  | 102.5% to 110% of f <sub>sw</sub> | 001  | 104% to 121% x f <sub>sw</sub> | 101  | 102% to 107% of f <sub>sw</sub> | 010  | 104% to 117% x f <sub>sw</sub> | 110  | 102% to 103.5% of f <sub>sw</sub> | 011  | 103% to 113% x f <sub>sw</sub> | 111  | No dither |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| Bits | Dither Range                    | Bits                  | Dither Range                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 000  | 108% to 126% of f <sub>sw</sub> | 100                   | 102.5% to 110% of f <sub>sw</sub> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 001  | 104% to 121% x f <sub>sw</sub>  | 101                   | 102% to 107% of f <sub>sw</sub>   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 010  | 104% to 117% x f <sub>sw</sub>  | 110                   | 102% to 103.5% of f <sub>sw</sub> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |
| 011  | 103% to 113% x f <sub>sw</sub>  | 111                   | No dither                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |              |      |              |      |                                 |      |                                   |      |                                |      |                                 |      |                                |      |                                   |      |                                |      |           |      |      |      |       |      |      |      |       |      |      |      |       |      |      |      |       |

## MFR\_VOUT\_CTRL (D2h)

**Format:** Unsigned binary

The MFR\_VOUT\_CTRL command sets the V<sub>OUT</sub> feedback behavior and selects feedback divider mode, the feedback divider ratio, and the VCC bias supply function.

| Bits | Access        | Bit Name               | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
|------|---------------|------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------------|------------------------|-----|--------------|-----------------|-----|--------------|----------------|-----|--------------|----------------|-----|--------------|-----------------|-----|---------------|-----------------|
| 7:5  | R/W           | RESERVED               | 3'b000  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 4    | R/W           | VOUT_SET_MODE          | 1'b1    | 0: Selects external feedback divider mode. When using the external feedback divider, bits[2:0] of this command should be set to 100<br>1: Selects internal feedback divider mode                                                                                                                                                                                                                                                                                                                                                                     |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 3    | R/W           | VOBIAS_EN              | 1'b1    | Enables the V <sub>OUT</sub> bias. If enabled, VCC can be supplied power through the VOUT pin when V <sub>OUT</sub> > 4.8V.<br>0: Disabled<br>1: Enabled                                                                                                                                                                                                                                                                                                                                                                                             |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 2:0  | R/W           | FEEDBACK_DIVIDER_RATIO | 3'b100  | Sets the feedback divider ratio. Before changing these bits, disable the DC/DC converter via the OPERATION (01h). <table><tr><th>Bits</th><th>Divider Ratio</th><th>V<sub>OUT</sub> Range</th></tr><tr><td>000</td><td>1:1, range 1</td><td>0.6V to 1.5345V</td></tr><tr><td>001</td><td>1:2, range 2</td><td>0.6V to 3.069V</td></tr><tr><td>010</td><td>1:4, range 3</td><td>0.6V to 6.138V</td></tr><tr><td>011</td><td>1:8, range 4</td><td>1.2V to 12.276V</td></tr><tr><td>100</td><td>1:16, range 5</td><td>2.4V to 24.552V</td></tr></table> | Bits | Divider Ratio | V <sub>OUT</sub> Range | 000 | 1:1, range 1 | 0.6V to 1.5345V | 001 | 1:2, range 2 | 0.6V to 3.069V | 010 | 1:4, range 3 | 0.6V to 6.138V | 011 | 1:8, range 4 | 1.2V to 12.276V | 100 | 1:16, range 5 | 2.4V to 24.552V |
| Bits | Divider Ratio | V <sub>OUT</sub> Range |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 000  | 1:1, range 1  | 0.6V to 1.5345V        |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 001  | 1:2, range 2  | 0.6V to 3.069V         |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 010  | 1:4, range 3  | 0.6V to 6.138V         |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 011  | 1:8, range 4  | 1.2V to 12.276V        |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |
| 100  | 1:16, range 5 | 2.4V to 24.552V        |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |      |               |                        |     |              |                 |     |              |                |     |              |                |     |              |                 |     |               |                 |

## MFR\_VOUT\_TRANSITION\_RATE (D3h)

**Format:** Unsigned binary

The MFR\_VOUT\_TRANSITION\_RATE command sets the V<sub>OUT</sub> transition rate while adjusting V<sub>OUT</sub> via the PMBus.

| Bits | Access                         | Bit Name                       | Default  | Description                                                                                                                                                                                                                                                                                                                                                                                                             |      |                                |     |         |     |          |     |         |     |       |     |       |
|------|--------------------------------|--------------------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------------------------|-----|---------|-----|----------|-----|---------|-----|-------|-----|-------|
| 7:3  | R/W                            | RESERVED                       | 5'b00000 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                               |      |                                |     |         |     |          |     |         |     |       |     |       |
| 2:0  | R/W                            | OUTPUT_VOLTAGE_TRANSITION_RATE | 3'b001   | Controls the V <sub>OUT</sub> changing slew rate. This control only works after soft start finishes. The rising and falling slew rates are the same. <table><tr><th>Bits</th><th>Output Voltage Transition Rate</th></tr><tr><td>000</td><td>0.1V/ms</td></tr><tr><td>001</td><td>0.25V/ms</td></tr><tr><td>010</td><td>0.5V/ms</td></tr><tr><td>011</td><td>1V/ms</td></tr><tr><td>100</td><td>2V/ms</td></tr></table> | Bits | Output Voltage Transition Rate | 000 | 0.1V/ms | 001 | 0.25V/ms | 010 | 0.5V/ms | 011 | 1V/ms | 100 | 2V/ms |
| Bits | Output Voltage Transition Rate |                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |                                |     |         |     |          |     |         |     |       |     |       |
| 000  | 0.1V/ms                        |                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |                                |     |         |     |          |     |         |     |       |     |       |
| 001  | 0.25V/ms                       |                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |                                |     |         |     |          |     |         |     |       |     |       |
| 010  | 0.5V/ms                        |                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |                                |     |         |     |          |     |         |     |       |     |       |
| 011  | 1V/ms                          |                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |                                |     |         |     |          |     |         |     |       |     |       |
| 100  | 2V/ms                          |                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |                                |     |         |     |          |     |         |     |       |     |       |

When using the internal feedback divider, the V<sub>OUT</sub> slew rate is the set by the value in bits[2:0] of this command, regardless of the feedback ratio. When using the external feedback divider (MFR\_VOUT\_CTRL (D2h), bits[2:0] is always 100), the transition rate can be estimated with Equation (7):

$$V_{\text{OUT\_TRANSITION\_RATE}} (V) = X / 16 / (\text{FB Divider Ratio}) \quad (7)$$

Where X is the value set by bits[2:0] of this command, and the external divider ratio is defined by R2 / (R1 + R2) (see Figure 12 on page 45).

### MFR\_FREQUENCY\_SWITCH (D4h)

**Format:** Unsigned binary

The MFR\_FREQUENCY\_SWITCH command sets the switching frequency ( $f_{sw}$ ).

| Bits | Access          | Bit Name                | Default         | Description                                                                                                                                                                                                                                                                                                                                                                            |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |
|------|-----------------|-------------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------|------|-----------------|-----|--------|-----|--------|-----|--------|-----|---------|-----|--------|-----|---------|-----|--------|-----|---------|
| 7:3  | R/W             | RESERVED                | 5'b00000        | Reserved.                                                                                                                                                                                                                                                                                                                                                                              |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |
| 2:0  | R/W             | SWITCHING_FREQUENCY_SET | 3'b001          | Sets f <sub>sw</sub> . <table><tr><th>Bits</th><th>f<sub>sw</sub></th><th>Bits</th><th>f<sub>sw</sub></th></tr><tr><td>000</td><td>150kHz</td><td>100</td><td>750kHz</td></tr><tr><td>001</td><td>300kHz</td><td>101</td><td>1000kHz</td></tr><tr><td>010</td><td>450kHz</td><td>110</td><td>1500kHz</td></tr><tr><td>011</td><td>600kHz</td><td>111</td><td>2200kHz</td></tr></table> | Bits | f <sub>sw</sub> | Bits | f <sub>sw</sub> | 000 | 150kHz | 100 | 750kHz | 001 | 300kHz | 101 | 1000kHz | 010 | 450kHz | 110 | 1500kHz | 011 | 600kHz | 111 | 2200kHz |
| Bits | f <sub>sw</sub> | Bits                    | f <sub>sw</sub> |                                                                                                                                                                                                                                                                                                                                                                                        |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |
| 000  | 150kHz          | 100                     | 750kHz          |                                                                                                                                                                                                                                                                                                                                                                                        |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |
| 001  | 300kHz          | 101                     | 1000kHz         |                                                                                                                                                                                                                                                                                                                                                                                        |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |
| 010  | 450kHz          | 110                     | 1500kHz         |                                                                                                                                                                                                                                                                                                                                                                                        |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |
| 011  | 600kHz          | 111                     | 2200kHz         |                                                                                                                                                                                                                                                                                                                                                                                        |      |                 |      |                 |     |        |     |        |     |        |     |         |     |        |     |         |     |        |     |         |

### MFR\_COMP1\_CTRL (D6h)

**Format:** Unsigned binary

The MFR\_COMP1\_CTRL command sets some slope functions (see Figure 11 on page 35 for more details on the slope compensation network).

| Bits  | Access | Bit Name | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                  |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
|-------|--------|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|-------|-----|-------|-------|-------|-------|-------|-----|------|-----|------|-----|------|-----|------|-----|------|
| 7     | R/W    | RESERVED | 1'b0    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                    |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 6:4   | R/W    | CTH      | 3'b000  | Sets the configurable CTH to adjust the compensation capacitor. 10pF per LSB. The offset is 20pF. <table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>000</td><td>20pF</td><td>100</td><td>60pF</td></tr><tr><td>001</td><td>30pF</td><td>101</td><td>70pF</td></tr><tr><td>010</td><td>40pF</td><td>110</td><td>80pF</td></tr><tr><td>011</td><td>50pF</td><td>111</td><td>90pF</td></tr></table> | Bits | Value | Bits | Value | 000 | 20pF  | 100   | 60pF  | 001   | 30pF  | 101 | 70pF | 010 | 40pF | 110 | 80pF | 011 | 50pF | 111 | 90pF |
| Bits  | Value  | Bits     | Value   |                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 000   | 20pF   | 100      | 60pF    |                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 001   | 30pF   | 101      | 70pF    |                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 010   | 40pF   | 110      | 80pF    |                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 011   | 50pF   | 111      | 90pF    |                                                                                                                                                                                                                                                                                                                                                                                                                              |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 3:2   | R/W    | RESERVED | 2'b00   | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                    |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| 1:0   | R/W    | CTHP     | 2'b00   | Sets the configurable CTHP to adjust the high-frequency compensation capacitor. <table><tr><th>Bits</th><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><th>Value</th><td>0.1pF</td><td>0.2pF</td><td>0.3pF</td><td>0.4pF</td></tr></table>                                                                                                                                                                             | Bits | 00    | 01   | 10    | 11  | Value | 0.1pF | 0.2pF | 0.3pF | 0.4pF |     |      |     |      |     |      |     |      |     |      |
| Bits  | 00     | 01       | 10      | 11                                                                                                                                                                                                                                                                                                                                                                                                                           |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |
| Value | 0.1pF  | 0.2pF    | 0.3pF   | 0.4pF                                                                                                                                                                                                                                                                                                                                                                                                                        |      |       |      |       |     |       |       |       |       |       |     |      |     |      |     |      |     |      |     |      |

### MFR\_COMP2\_CTRL (D7h)

**Format:** Unsigned binary

The MFR\_COMP2\_CTRL command sets some slope functions. See Figure 11 on page 35 for more details on the slope compensation network.

| Bits | Access  | Bit Name | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |          |       |         |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|------|---------|----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------|---------|-------|------|----------|------|---------|------|----------|------|---------|------|----------|------|---------|------|----------|------|---------|------|---------|------|---------|------|---------|------|---------|------|---------|------|---------|------|---------|------|---------|
| 7:4  | R/W     | GM       | 4'b0000 | Sets the configurable error amplifier gain.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |          |       |         |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | <table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>0000</td><td>25.0μA/V</td><td>1000</td><td>5.0μA/V</td></tr><tr><td>0001</td><td>16.7μA/V</td><td>1001</td><td>4.5μA/V</td></tr><tr><td>0010</td><td>12.5μA/V</td><td>1010</td><td>4.2μA/V</td></tr><tr><td>0011</td><td>10.0μA/V</td><td>1011</td><td>3.8μA/V</td></tr><tr><td>0100</td><td>8.3μA/V</td><td>1100</td><td>3.6μA/V</td></tr><tr><td>0101</td><td>7.1μA/V</td><td>1101</td><td>3.3μA/V</td></tr><tr><td>0110</td><td>6.3μA/V</td><td>1110</td><td>3.1μA/V</td></tr><tr><td>0111</td><td>5.6μA/V</td><td>1111</td><td>2.9μA/V</td></tr></table> | Bits     | Value | Bits    | Value | 0000 | 25.0μA/V | 1000 | 5.0μA/V | 0001 | 16.7μA/V | 1001 | 4.5μA/V | 0010 | 12.5μA/V | 1010 | 4.2μA/V | 0011 | 10.0μA/V | 1011 | 3.8μA/V | 0100 | 8.3μA/V | 1100 | 3.6μA/V | 0101 | 7.1μA/V | 1101 | 3.3μA/V | 0110 | 6.3μA/V | 1110 | 3.1μA/V | 0111 | 5.6μA/V | 1111 | 2.9μA/V |
|      |         |          |         | Bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Value    | Bits  | Value   |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 25.0μA/V | 1000  | 5.0μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0001                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 16.7μA/V | 1001  | 4.5μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0010                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 12.5μA/V | 1010  | 4.2μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0011                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 10.0μA/V | 1011  | 3.8μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 8.3μA/V  | 1100  | 3.6μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 7.1μA/V  | 1101  | 3.3μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
|      |         |          |         | 0110                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 6.3μA/V  | 1110  | 3.1μA/V |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |
| 0111 | 5.6μA/V | 1111     | 2.9μA/V |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |          |       |         |       |      |          |      |         |      |          |      |         |      |          |      |         |      |          |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |      |         |

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|-----|-----|-----|---------|------------------------------------------------------------------------------------------------------|--|--|--|--|
| 3:0 | R/W | RTH | 4'b1011 | Sets the configurable <b>RTH</b> to adjust the compensation resistor. 80kΩ/LSB. The offset is 200kΩ. |  |  |  |  |
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### MFR\_SLOPE\_CTRL (D8h)

**Format:** Unsigned binary

The MFR\_COMP\_CTRL command sets some slope functions. Figure 11 shows more details on the slope compensation network.

| Bits | Access     | Bit Name  | Default    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
|------|------------|-----------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|-------|------|----------|------|----------|------|-----------|------|------------|------|------------|------|------------|------|------------|------|-----------|------|------------|------|----------|------|------------|------|------------|------|----------|------|----------|------|------------|------|-----------|
| 7:4  | R/W        | RESERVED  | 4'b0000    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 3:0  | R/W        | SLOP_COMP | 4'b1111    | Sets the configurable slop compensation rate, where $T$ is the switching period ( $T = 1 / f_{sw}$ ). <table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>0000</td><td>0.5A / T</td><td>1000</td><td>0.5A / T</td></tr><tr><td>0001</td><td>0.45A / T</td><td>1001</td><td>0.563A / T</td></tr><tr><td>0010</td><td>0.409A / T</td><td>1010</td><td>0.643A / T</td></tr><tr><td>0011</td><td>0.375A / T</td><td>1011</td><td>0.75A / T</td></tr><tr><td>0100</td><td>0.346A / T</td><td>1100</td><td>0.9A / T</td></tr><tr><td>0101</td><td>0.321A / T</td><td>1101</td><td>1.125A / T</td></tr><tr><td>0110</td><td>0.3A / T</td><td>1110</td><td>1.5A / T</td></tr><tr><td>0111</td><td>0.281A / T</td><td>1111</td><td>2.25A / T</td></tr></table> | Bits | Value | Bits | Value | 0000 | 0.5A / T | 1000 | 0.5A / T | 0001 | 0.45A / T | 1001 | 0.563A / T | 0010 | 0.409A / T | 1010 | 0.643A / T | 0011 | 0.375A / T | 1011 | 0.75A / T | 0100 | 0.346A / T | 1100 | 0.9A / T | 0101 | 0.321A / T | 1101 | 1.125A / T | 0110 | 0.3A / T | 1110 | 1.5A / T | 0111 | 0.281A / T | 1111 | 2.25A / T |
| Bits | Value      | Bits      | Value      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0000 | 0.5A / T   | 1000      | 0.5A / T   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0001 | 0.45A / T  | 1001      | 0.563A / T |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0010 | 0.409A / T | 1010      | 0.643A / T |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0011 | 0.375A / T | 1011      | 0.75A / T  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0100 | 0.346A / T | 1100      | 0.9A / T   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0101 | 0.321A / T | 1101      | 1.125A / T |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0110 | 0.3A / T   | 1110      | 1.5A / T   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |
| 0111 | 0.281A / T | 1111      | 2.25A / T  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |       |      |       |      |          |      |          |      |           |      |            |      |            |      |            |      |            |      |           |      |            |      |          |      |            |      |            |      |          |      |          |      |            |      |           |

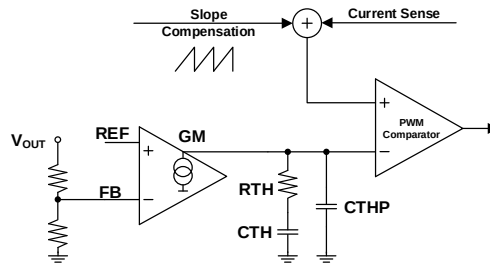


**Figure 11: Compensation Network**

### MFR\_HYS\_CTRL (D9h)

**Format:** Unsigned binary

The MFR\_HYS\_CTRL command sets hysteresis values.

| Bits | Access | Bit Name                    | Default | Description                               |
|------|--------|-----------------------------|---------|-------------------------------------------|
| 7:4  | R/W    | RESERVED                    | 4'b0000 | Reserved.                                 |
| 3    | R/W    | VIN_OVER_VOLTAGE_HYSTERESIS | 1'b0    | 0: 1.32V<br>1: 2.64V                      |
| 2    | R/W    | EN_HYSTERESIS               | 1'b0    | 0: 130mV<br>1: 330mV                      |
| 1    | R/W    | VOUT_OV_HYSTERESIS          | 1'b1    | 0: 5% of $V_{OUT}$<br>1: 10% of $V_{OUT}$ |

|   |     |                   |      |                                                         |
|---|-----|-------------------|------|---------------------------------------------------------|
| 0 | R/W | VOUT_UV_HYSTERSIS | 1'b1 | 0: 5% of V <sub>OUT</sub><br>1: 10% of V <sub>OUT</sub> |
|---|-----|-------------------|------|---------------------------------------------------------|

### MFR\_PWM\_CTRL (DAh)

**Format:** Unsigned binary

The MFR\_PWM\_CTRL command sets the switching rising and falling slew rates.

| Bits      | Access | Bit Name                    | Default | Description                                                                                                                                                                                                                   |      |    |    |    |    |           |       |       |       |       |
|-----------|--------|-----------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----|----|----|----|-----------|-------|-------|-------|-------|
| 7:6       | R/W    | RESERVED                    | 2'b00   | Reserved.                                                                                                                                                                                                                     |      |    |    |    |    |           |       |       |       |       |
| 5:4       | R/W    | SWITCHING_RISING_SLEW_RATE  | 2'b00   | Sets the switching rising slew rate.<br><table border="1"> <tr> <th>Bits</th><th>00</th><th>01</th><th>10</th><th>11</th></tr> <tr> <th>Slew Rate</th><td>4V/ns</td><td>2V/ns</td><td>8V/ns</td><td>6V/ns</td></tr> </table>  | Bits | 00 | 01 | 10 | 11 | Slew Rate | 4V/ns | 2V/ns | 8V/ns | 6V/ns |
| Bits      | 00     | 01                          | 10      | 11                                                                                                                                                                                                                            |      |    |    |    |    |           |       |       |       |       |
| Slew Rate | 4V/ns  | 2V/ns                       | 8V/ns   | 6V/ns                                                                                                                                                                                                                         |      |    |    |    |    |           |       |       |       |       |
| 3:2       | R/W    | RESERVED                    | 2'b00   | Reserved.                                                                                                                                                                                                                     |      |    |    |    |    |           |       |       |       |       |
| 1:0       | R/W    | SWITCHING_FALLING_SLEW_RATE | 2'b11   | Sets the switching falling slew rate.<br><table border="1"> <tr> <th>Bits</th><th>00</th><th>01</th><th>10</th><th>11</th></tr> <tr> <th>Slew Rate</th><td>1V/ns</td><td>2V/ns</td><td>3V/ns</td><td>4V/ns</td></tr> </table> | Bits | 00 | 01 | 10 | 11 | Slew Rate | 1V/ns | 2V/ns | 3V/ns | 4V/ns |
| Bits      | 00     | 01                          | 10      | 11                                                                                                                                                                                                                            |      |    |    |    |    |           |       |       |       |       |
| Slew Rate | 1V/ns  | 2V/ns                       | 3V/ns   | 4V/ns                                                                                                                                                                                                                         |      |    |    |    |    |           |       |       |       |       |

### MFR\_FAULT\_CTRL (DBh)

**Format:** Unsigned binary

The MFR\_FAULT\_CTRL command determines the behavior of the /FT pin. The /FT pin is pulled down to indicate faults that are enabled via MFR\_FAULT\_CTRL.

| Bits | Access | Bit Name                    | Default | Description               |
|------|--------|-----------------------------|---------|---------------------------|
| 7:5  | R/W    | RESERVED                    | 3'b000  | Reserved.                 |
| 4    | R/W    | VIN_OVER_VOLTAGE_INDICATE   | 1'b1    | 0: Disabled<br>1: Enabled |
| 3    | R/W    | RESERVED                    | 1'b1    | Reserved.                 |
| 2    | R/W    | VOUT_UNDER_VOLTAGE_INDICATE | 1'b0    | 0: Disabled<br>1: Enabled |
| 1    | R/W    | VOUT_OVER_VOLTAGE_INDICATE  | 1'b1    | 0: Disabled<br>1: Enabled |
| 0    | R/W    | OVER_CURRENT_INDICATE       | 1'b1    | 0: Disabled<br>1: Enabled |

### MFR\_PRODUCT\_ID (DDh)

**Format:** Unsigned binary

The MFR\_PRODUCT\_ID command is for manufacturer use only.

| Bits | Access | Bit Name | Default | Description            |
|------|--------|----------|---------|------------------------|
| 7:4  | R/W    | RESERVED | 4'b0000 | Reserved.              |
| 3:0  | R/W    | ID       | 4'b1100 | Manufacturer use only. |

### MFR\_PRODUCT\_VERSION (DEh)

**Format:** Unsigned binary

The MFR\_PRODUCT\_VERSION command is for manufacturer use only.

| Bits | Access | Bit Name        | Default | Description            |
|------|--------|-----------------|---------|------------------------|
| 7:4  | R/W    | RESERVED        | 4'b0000 | Reserved.              |
| 3:0  | R/W    | PRODUCT_VERSION | 4'b0010 | Manufacturer use only. |

## MFR\_USER\_VERSION (DFh)

**Format:** Unsigned binary

The MFR\_USER\_VERSION command is for manufacturer use only.

| Bits | Access | Bit Name     | Default | Description            |
|------|--------|--------------|---------|------------------------|
| 7:4  | R/W    | RESERVED     | 4'b0000 | Reserved.              |
| 3:0  | R/W    | USER_VERSION | 4'b0000 | Manufacturer use only. |

## MFR\_OC\_FAULT\_LIMIT (E0h)

**Format:** Unsigned binary

The MFR\_OC\_FAULT\_LIMIT command sets the peak and valley current limits.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                                           |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
|------|--------|----------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|-------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|----|-----|------|
| 7    | R/W    | RESERVED             | 1'b0    | Reserved.                                                                                                                                                                                                                                                                                                                                             |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 6:4  | R/W    | PEAK_CURRENT_LIMIT   | 3'b011  | Sets the peak current limit. <table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>000</td><td>5.5A</td><td>100</td><td>1.5A</td></tr><tr><td>001</td><td>6.8A</td><td>101</td><td>2.5A</td></tr><tr><td>010</td><td>7.5A</td><td>110</td><td>3.5A</td></tr><tr><td>011</td><td>9A</td><td>111</td><td>4.5A</td></tr></table> | Bits | Value | Bits | Value | 000 | 5.5A | 100 | 1.5A | 001 | 6.8A | 101 | 2.5A | 010 | 7.5A | 110 | 3.5A | 011 | 9A | 111 | 4.5A |
| Bits | Value  | Bits                 | Value   |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 000  | 5.5A   | 100                  | 1.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 001  | 6.8A   | 101                  | 2.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 010  | 7.5A   | 110                  | 3.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 011  | 9A     | 111                  | 4.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 3    | R/W    | RESERVED             | 1'b0    | Reserved.                                                                                                                                                                                                                                                                                                                                             |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 2:0  | R/W    | VALLEY_CURRENT_LIMIT | 3'b111  | Sets the valley current limit. <table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>000</td><td>2.5A</td><td>100</td><td>4.5A</td></tr><tr><td>001</td><td>3A</td><td>101</td><td>5.5A</td></tr><tr><td>010</td><td>3.5A</td><td>110</td><td>6A</td></tr><tr><td>011</td><td>4A</td><td>111</td><td>6.5A</td></tr></table>   | Bits | Value | Bits | Value | 000 | 2.5A | 100 | 4.5A | 001 | 3A   | 101 | 5.5A | 010 | 3.5A | 110 | 6A   | 011 | 4A | 111 | 6.5A |
| Bits | Value  | Bits                 | Value   |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 000  | 2.5A   | 100                  | 4.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 001  | 3A     | 101                  | 5.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 010  | 3.5A   | 110                  | 6A      |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |
| 011  | 4A     | 111                  | 6.5A    |                                                                                                                                                                                                                                                                                                                                                       |      |       |      |       |     |      |     |      |     |      |     |      |     |      |     |      |     |    |     |      |

## MFR\_OC\_RESPONSE (E1h)

**Format:** Unsigned binary

The MFR\_OC\_RESPONSE command sets basic functions if an over-current (OC) condition is triggered.

| Bits           | Access | Bit Name         | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |      |    |    |    |    |                |      |      |       |       |
|----------------|--------|------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----|----|----|----|----------------|------|------|-------|-------|
| 7:6            | R/W    | OC_RESPONSE_MODE | 2'b01   | 00: Current limit only. The device continues to operate while maintaining the output current at the value set via MFR_OC_FAULT_LIMIT (E0h)<br>01: Deglitch off. The device continues to maintain the current set via MFR_OC_FAULT_LIMIT (E0h) for the delay time specified in bits[2:0] of this command. If the fault condition is still present at the end of the delay time, the device responds following bit[5] of this command<br>10: The device shuts down immediately and responds according to bit[5] of this command |      |    |    |    |    |                |      |      |       |       |
| 5              | R/W    | RETRY_SETTING    | 1'b1    | 0: Latch-off. The device does not retry until power is cycled or the device is re-enabled<br>1: Hiccup. The device attempts to restart continuously. The retry interval is defined by bits[4:3] of this command                                                                                                                                                                                                                                                                                                               |      |    |    |    |    |                |      |      |       |       |
| 4:3            | R/W    | RETRY_INTERVAL   | 2'b00   | Sets the retry interval. <table border="1"> <thead> <tr> <th>Bits</th><th>00</th><th>01</th><th>10</th><th>11</th></tr> </thead> <tbody> <tr> <td>Retry Interval</td><td>20ms</td><td>50ms</td><td>100ms</td><td>150ms</td></tr> </tbody> </table>                                                                                                                                                                                                                                                                            | Bits | 00 | 01 | 10 | 11 | Retry Interval | 20ms | 50ms | 100ms | 150ms |
| Bits           | 00     | 01               | 10      | 11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |      |    |    |    |    |                |      |      |       |       |
| Retry Interval | 20ms   | 50ms             | 100ms   | 150ms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |      |    |    |    |    |                |      |      |       |       |

|     |     |            |        |                                                         |       |      |       |
|-----|-----|------------|--------|---------------------------------------------------------|-------|------|-------|
| 2:0 | R/W | DELAY_TIME | 3'b000 | Sets the delay time after an OC condition is triggered. |       |      |       |
|     |     |            |        | Bits                                                    | Value | Bits | Value |
|     |     |            |        | 000                                                     | 15µs  | 100  | 75µs  |
|     |     |            |        | 001                                                     | 30µs  | 101  | 90µs  |
|     |     |            |        | 010                                                     | 45µs  | 110  | 105µs |
|     |     |            |        | 011                                                     | 60µs  | 111  | 120µs |

### MFR\_VIN\_OV\_FAULT\_RESPONSE (E2h)

**Format:** Unsigned binary

The MFR\_VIN\_OV\_FAULT\_RESPONSE command sets basic functions if an input over-voltage (OV) condition is triggered.

| Bits           | Access | Bit Name                   | Default | Description                                                                                                                                                                                                         |      |    |    |    |    |                |      |      |       |       |
|----------------|--------|----------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----|----|----|----|----------------|------|------|-------|-------|
| 7:6            | R/W    | VIN_OV_FAULT_RESPONSE_MODE | 2'b10   | 00: Ignore. The device takes no action and continues to operate without interruption<br>01: Not supported<br>10: The device shuts down immediately and responds according to bit[5] of this command                 |      |    |    |    |    |                |      |      |       |       |
| 5              | R/W    | RETRY_SETTING              | 1'b1    | 0: The device does not attempt to restart<br>1: The device attempts to restart continuously. The retry interval is defined by bits[4:3] of this command                                                             |      |    |    |    |    |                |      |      |       |       |
| 4:3            | R/W    | RETRY_INTERVAL             | 2'b00   | Sets the retry interval.<br><table border="1"> <tr> <th>Bits</th><th>00</th><th>01</th><th>10</th><th>11</th></tr> <tr> <th>Retry Interval</th><td>20ms</td><td>50ms</td><td>100ms</td><td>150ms</td></tr> </table> | Bits | 00 | 01 | 10 | 11 | Retry Interval | 20ms | 50ms | 100ms | 150ms |
| Bits           | 00     | 01                         | 10      | 11                                                                                                                                                                                                                  |      |    |    |    |    |                |      |      |       |       |
| Retry Interval | 20ms   | 50ms                       | 100ms   | 150ms                                                                                                                                                                                                               |      |    |    |    |    |                |      |      |       |       |
| 2:0            | R/W    | RESERVED                   | 3'b000  | Reserved.                                                                                                                                                                                                           |      |    |    |    |    |                |      |      |       |       |

### MFR\_VOUT\_OV\_FAULT\_LIMIT (E3h)

**Format:** Unsigned binary

The MFR\_VOUT\_OV\_FAULT\_LIMIT command sets the output over-voltage (OV) fault threshold.

| Bits | Access | Bit Name            | Default     | Description                                                |
|------|--------|---------------------|-------------|------------------------------------------------------------|
| 7:1  | R/W    | RESERVED            | 7'b00000000 | Reserved.                                                  |
| 0    | R/W    | VOUT_OV_FAULT_LIMIT | 1'b0        | 0: +15% of V <sub>OUT</sub><br>1: +20% of V <sub>OUT</sub> |

### MFR\_VOUT\_OV\_FAULT\_RESPONSE (E4h)

**Format:** Unsigned binary

The MFR\_VOUT\_OV\_FAULT\_RESPONSE command sets basic functions if an output over-voltage (OV) condition is triggered.

| Bits | Access | Bit Name                    | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|--------|-----------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W    | VOUT_OV_FAULT_RESPONSE_MODE | 2'b11   | 00: Ignore. The device takes no action and continues to operate without interruption<br>01: Deglitch off. The device continues to operate for the delay time specified in bits[2:0] of this command. If the fault condition is still present at the end of the delay time, the device responds following bit[5] of this command<br>10: The device shuts down immediately and responds according to bit[5] of this command<br>11: Discharge mode. The LS-FET turns on to discharge the output until the current reaches the negative current limit |

|     |     |                |        |                                                                                                                                                                                                                 |  |       |      |       |       |       |  |
|-----|-----|----------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-------|------|-------|-------|-------|--|
| 5   | R/W | RETRY_SETTING  | 1'b0   | 0: Latch-off. The device does not retry until power is cycled or the device is re-enabled<br>1: Hiccup. The device attempts to restart continuously. The retry interval is defined by bits[4:3] of this command |  |       |      |       |       |       |  |
| 4:3 | R/W | RETRY_INTERVAL | 2'b00  | Sets the retry interval.                                                                                                                                                                                        |  |       |      |       |       |       |  |
|     |     |                |        | Bits                                                                                                                                                                                                            |  | 00    | 01   | 10    | 11    |       |  |
|     |     |                |        | Retry Interval                                                                                                                                                                                                  |  | 20ms  | 50ms | 100ms | 150ms |       |  |
| 2:0 | R/W | DELAY_TIME     | 3'b000 | Sets the delay time after an OV condition is triggered.                                                                                                                                                         |  |       |      |       |       |       |  |
|     |     |                |        | Bits                                                                                                                                                                                                            |  | Value |      | Bits  |       | Value |  |
|     |     |                |        | 000                                                                                                                                                                                                             |  | 15μs  |      | 100   |       | 75μs  |  |
|     |     |                |        | 001                                                                                                                                                                                                             |  | 30μs  |      | 101   |       | 90μs  |  |
|     |     |                |        | 010                                                                                                                                                                                                             |  | 45μs  |      | 110   |       | 105μs |  |
|     |     |                |        | 011                                                                                                                                                                                                             |  | 60μs  |      | 111   |       | 120μs |  |

### MFR\_VOUT\_UV\_FAULT\_LIMIT (E5h)

**Format:** Unsigned binary

The MFR\_VOUT\_UV\_FAULT\_LIMIT command sets the output under-voltage (UV) fault threshold.

| Bits | Access | Bit Name            | Default    | Description                                                |
|------|--------|---------------------|------------|------------------------------------------------------------|
| 7:1  | R/W    | RESERVED            | 7'b0000000 | Reserved.                                                  |
| 0    | R/W    | VOUT_UV_FAULT_LIMIT | 1'b1       | 0: -15% of V <sub>OUT</sub><br>1: -20% of V <sub>OUT</sub> |

### MFR\_VOUT\_UV\_FAULT\_RESPONSE (E6h)

**Format:** Unsigned binary

The MFR\_VOUT\_OV\_FAULT\_RESPONSE command sets basic functions if an output under-voltage (UV) condition is triggered.

| Bits           | Access | Bit Name                    | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                             |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
|----------------|--------|-----------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|-------|-----|----------------|------|------|-------|-------|-----|------|-----|------|-----|-------|-----|------|-----|-------|
| 7:6            | R/W    | VOUT_UV_FAULT_RESPONSE_MODE | 2'b00   | 00: Ignore. The device has no action and continues to operate without interruption<br>01: Deglitch off. The device continues to operate for the delay time specified in bits[2:0] of this command. If the fault condition is still present at the end of the delay time, the device responds following bit[5] of this command<br>10: The device shuts down immediately and responds according to bit[5] of this command |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 5              | R/W    | RETRY_SETTING               | 1'b1    | 0: Latch-off. The device does not retry until power is cycled or the device is re-enabled<br>1: Hiccup. The device attempts to restart continuously. The retry interval is defined by bits[4:3] of this command                                                                                                                                                                                                         |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 4:3            | R/W    | RETRY_INTERVAL              | 2'b00   | Sets the retry interval. <table><tr><th>Bits</th><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><th>Retry Interval</th><td>20ms</td><td>50ms</td><td>100ms</td><td>150ms</td></tr></table>                                                                                                                                                                                                                        | Bits | 00    | 01   | 10    | 11  | Retry Interval | 20ms | 50ms | 100ms | 150ms |     |      |     |      |     |       |     |      |     |       |
| Bits           | 00     | 01                          | 10      | 11                                                                                                                                                                                                                                                                                                                                                                                                                      |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| Retry Interval | 20ms   | 50ms                        | 100ms   | 150ms                                                                                                                                                                                                                                                                                                                                                                                                                   |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 2:0            | R/W    | DELAY_TIME                  | 3'b000  | Sets the delay time after a UV condition is triggered. <table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>000</td><td>15μs</td><td>100</td><td>75μs</td></tr><tr><td>001</td><td>30μs</td><td>101</td><td>90μs</td></tr><tr><td>010</td><td>45μs</td><td>110</td><td>105μs</td></tr><tr><td>011</td><td>60μs</td><td>111</td><td>120μs</td></tr></table>                                     | Bits | Value | Bits | Value | 000 | 15μs           | 100  | 75μs | 001   | 30μs  | 101 | 90μs | 010 | 45μs | 110 | 105μs | 011 | 60μs | 111 | 120μs |
| Bits           | Value  | Bits                        | Value   |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 000            | 15μs   | 100                         | 75μs    |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 001            | 30μs   | 101                         | 90μs    |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 010            | 45μs   | 110                         | 105μs   |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |
| 011            | 60μs   | 111                         | 120μs   |                                                                                                                                                                                                                                                                                                                                                                                                                         |      |       |      |       |     |                |      |      |       |       |     |      |     |      |     |       |     |      |     |       |

### MFR\_RAIL\_ADDRESS (E8h)

**Format:** Unsigned binary

The MFR\_RAIL\_ADDRESS command determines the rail address.

| Bits | Access | Bit Name | Default    | Description                                               |
|------|--------|----------|------------|-----------------------------------------------------------|
| 7    | R/W    | ENABLE   | 1'b0       | 0: Disable the rail address<br>1: Enable the rail address |
| 6:0  | R/W    | ADDRESS  | 7'b0000000 | Sets the 7-bit PMBus address.                             |

### MFR\_LIGHT\_CTRL (E9h)

**Format:** Unsigned binary

The MFR\_LIGHT\_CTRL command determines the PWM mode at light loads.

| Bits | Access | Bit Name                     | Default | Description                                                                                                                        |
|------|--------|------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W    | PWM_MODE                     | 1'b0    | 0: Advanced asynchronous modulation (AAM) mode<br>1: Forced continuous conduction mode (FCCM)                                      |
| 6:4  | R/W    | DECREASE_FREQUENCY_THRESHOLD | 3'b010  | 000: No threshold<br>001: 0.4A<br>010: 0.6A<br>011: 0.8A<br>100: 1A                                                                |
| 3:0  | R/W    | AAM_THRESHOLD                | 4'b0100 | 0000: No threshold<br>0001: 0.1A<br>0010: 0.2A<br>0011: 0.3A<br>0100: 0.4A<br>0101: 0.5A<br>0110: 0.6A<br>0111: 0.7A<br>1000: 0.8A |

### MFR\_PWR\_STAGE\_SET (EAh)

**Format:** Unsigned binary

The MFR\_POWER\_STAGE command determines the device's power role. In multi-phase applications, power stage control can be set by the /FT pin or selected via the MTP (see the Multi-Phase Operation section on page 19 for more details). In addition, the power stage mode should be selected depending on the total paralleled phases, and the initiator or target roles.

| Bits | Access | Bit Name            | Default | Description                                                                                                        |
|------|--------|---------------------|---------|--------------------------------------------------------------------------------------------------------------------|
| 7:5  | R/W    | RESERVED            | 3'b000  | Reserved.                                                                                                          |
| 4    | R/W    | POWER_STAGE_CONTROL | 1'b1    | 0: The /FT pin sets the power stage<br>1: The MTP sets the power stage mode according to bits[3:0] of this command |

|     |     |                  |         |                                                        |                                                                                                                                                               |
|-----|-----|------------------|---------|--------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | R/W | POWER_STAGE_MODE | 4'b0000 | Sets the power stage mode for up to 4-phase operation. |                                                                                                                                                               |
|     |     |                  |         | <b>Single-Phase Operation</b>                          | IN_CLK:<br>0100: SYNC in (no shift)<br>0110: SYNC in (180° shift)<br>EX_CLK:<br>0000: SYNC out                                                                |
|     |     |                  |         | <b>2-Phase Operation</b>                               | 1000: Initiator for 2-phase operation<br>1100: Target for 2-phase operation                                                                                   |
|     |     |                  |         | <b>3-Phase Operation</b>                               | 1010: Initiator for 3-phase operation<br>1100: Target 1 for 3-phase operation<br>1110: Target 2 for 3-phase operation                                         |
|     |     |                  |         | <b>4-Phase Operation</b>                               | 1001: Initiator for 4-phase operation<br>1100: Target 1 for 4-phase operation<br>1110: Target 2 for 4-phase operation<br>1101: Target 3 for 4-phase operation |

## DEFAULT MTP CONFIGURATIONS

Table 4 and Table 5 show the default MTP configurations for the MP8880AGVE-0000.

**Table 4: 0000 Suffix Code Configuration**

| MTP Items                   | Parameter Settings               |
|-----------------------------|----------------------------------|
| VOUT_SET_MODE               | Internal feedback divider mode   |
| MFR_VOUT_CTRL               | Range 3, 1:4, 0.6V to 6.138V     |
| OUTPUT_VOLTAGE              | 5V                               |
| VOBIAS_EN                   | Enabled                          |
| OUTPUT_INITIAL_STATE        | On                               |
| PWM_MODE                    | AAM mode                         |
| TON_RISE                    | 1ms                              |
| TOFF_FALL                   | 1ms                              |
| PEAK_CURRENT_LIMIT          | 9A                               |
| VALLEY_CURRENT_LIMIT        | 6.5A                             |
| SWITCHING_FREQUENCY_SET     | 450kHz                           |
| OCP_RESPONSE_MODE           | Hiccup mode                      |
| SWITCHING_RISING_SLEW_RATE  | 2V/ns                            |
| SWITCHING_FALLING_SLEW_RATE | 2V/ns                            |
| PMBUS_ADDRESS               | 0x00 with R <sub>ADDR</sub> = 0Ω |
| MTP_CONFIGURE_CODE          | 0x0000                           |

**Table 5: 0000 Suffix Code Register Value**

| Suffix Code | Register | Hex Value | Suffix Code | Register | Hex Value |
|-------------|----------|-----------|-------------|----------|-----------|
| 0000        | 0x01     | 80h       | 0000        | 0xD4     | 2h        |
| 0000        | 0x21     | 341h      | 0000        | 0xD6     | 20h       |
| 0000        | 0x24     | 3FFh      | 0000        | 0xD7     | 78h       |
| 0000        | 0x25     | 382h      | 0000        | 0xD8     | 0h        |
| 0000        | 0x26     | 2FEh      | 0000        | 0xD9     | 3h        |
| 0000        | 0x35     | 0h        | 0000        | 0xDA     | 11h       |
| 0000        | 0x36     | 0h        | 0000        | 0xDB     | 1Bh       |
| 0000        | 0x55     | 1FCh      | 0000        | 0xE0     | 37h       |
| 0000        | 0x60     | 0h        | 0000        | 0xE1     | 60h       |
| 0000        | 0x61     | 1h        | 0000        | 0xE2     | A0h       |
| 0000        | 0x64     | 0h        | 0000        | 0xE3     | 0h        |
| 0000        | 0x65     | 1h        | 0000        | 0xE4     | C0h       |
| 0000        | 0xD0     | 0h        | 0000        | 0xE5     | 1h        |
| 0000        | 0xD1     | 0h        | 0000        | 0xE6     | 20h       |
| 0000        | 0xD2     | 1Ah       | 0000        | 0xE9     | 24h       |
| 0000        | 0xD3     | 1h        | 0000        | 0xEA     | 0h        |

## DEFAULT MTP CONFIGURATIONS *(continued)*

Table 6 and Table 7 show the default MTP configurations for the MP8880AGVE-0001.

**Table 6: 0001 Suffix Code Configuration**

| MTP Items                   | Parameter Settings               |
|-----------------------------|----------------------------------|
| VOUT_SET_MODE               | External feedback divider mode   |
| MFR_VOUT_CTRL               | Range 5, 1:16, 0.6V to 24.552V   |
| REFERENCE_VOLTAGE           | 1V                               |
| VOBIAS_EN                   | Enabled                          |
| OUTPUT_INITIAL_STATE        | On                               |
| PWM_MODE                    | AAM mode                         |
| TON_RISE                    | 1ms                              |
| TOFF_FALL                   | 1ms                              |
| PEAK_CURRENT_LIMIT          | 9A                               |
| VALLEY_CURRENT_LIMIT        | 6.5A                             |
| SWITCHING_FREQUENCY_SET     | 450kHz                           |
| OCP_RESPONSE_MODE           | Hiccup mode                      |
| SWITCHING_RISING_SLEW_RATE  | 2V/ns                            |
| SWITCHING_FALLING_SLEW_RATE | 2V/ns                            |
| PMBUS_ADDRESS               | 0x00 with R <sub>ADDR</sub> = 0Ω |
| MTP_CONFIGURE_CODE          | 0x0001                           |

In external feedback divider mode, V<sub>OUT</sub> is equal to the reference voltage multiplied by the external divider ratio. The reference voltage is set via VOUT\_COMMAND (21h), with 1.5mV/LSB. The internal divider ratio should always be set to 1:16 via MFR\_VOUT\_CTRL (D2h).

**Table 7: 0001 Suffix Code Register Value**

| Suffix Code | Register | Hex Value | Suffix Code | Register | Hex Value |
|-------------|----------|-----------|-------------|----------|-----------|
| 0001        | 0x01     | 80h       | 0001        | 0xD4     | 2h        |
| 0001        | 0x21     | 29Bh      | 0001        | 0xD6     | 20h       |
| 0001        | 0x24     | 3FFh      | 0001        | 0xD7     | 78h       |
| 0001        | 0x25     | 2D0h      | 0001        | 0xD8     | 0h        |
| 0001        | 0x26     | 265h      | 0001        | 0xD9     | 3h        |
| 0001        | 0x35     | 0h        | 0001        | 0xDA     | 11h       |
| 0001        | 0x36     | 0h        | 0001        | 0xDB     | 1Bh       |
| 0001        | 0x55     | 1FCh      | 0001        | 0xE0     | 37h       |
| 0001        | 0x60     | 0h        | 0001        | 0xE1     | 60h       |
| 0001        | 0x61     | 1h        | 0001        | 0xE2     | A0h       |
| 0001        | 0x64     | 0h        | 0001        | 0xE3     | 0h        |
| 0001        | 0x65     | 1h        | 0001        | 0xE4     | C0h       |
| 0001        | 0xD0     | 0h        | 0001        | 0xE5     | 1h        |
| 0001        | 0xD1     | 0h        | 0001        | 0xE6     | 20h       |
| 0001        | 0xD2     | Ch        | 0001        | 0xE9     | 24h       |
| 0001        | 0xD3     | 1h        | 0001        | 0xEA     | 0h        |

## DEFAULT MTP CONFIGURATIONS *(continued)*

Table 8 and Table 9 show the default MTP configurations for the MP8880AGVE-0002.

**Table 8: 0002 Suffix Code Configuration**

| MTP Items                   | Parameter Settings               |
|-----------------------------|----------------------------------|
| VOUT_SET_MODE               | Internal feedback divider mode   |
| MFR_VOUT_CTRL               | Range 5, 1:16, 2.4V to 24.552V   |
| OUTPUT_VOLTAGE              | 12V                              |
| VOBIAS_EN                   | Enabled                          |
| OUTPUT_INITIAL_STATE        | On                               |
| PWM_MODE                    | AAM mode                         |
| TON_RISE                    | 1ms                              |
| TOFF_FALL                   | 1ms                              |
| DITHER_ENABLE/DISABLE       | Enables frequency dither         |
| DITHER_CYCLE                | 204μs                            |
| DITHER_RANGE                | 102% to 107% of f <sub>sw</sub>  |
| PEAK_CURRENT_LIMIT          | 9A                               |
| VALLEY_CURRENT_LIMIT        | 6.5A                             |
| SWITCHING_FREQUENCY_SET     | 300kHz                           |
| OCP_RESPONSE_MODE           | Hiccup mode                      |
| SWITCHING_RISING_SLEW_RATE  | 4V/ns                            |
| SWITCHING_FALLING_SLEW_RATE | 4V/ns                            |
| PMBUS_ADDRESS               | 0x00 with R <sub>ADDR</sub> = 0Ω |
| MTP_CONFIGURE_CODE          | 0x0002                           |

**Table 9: 0002 Suffix Code Register Value**

| Suffix Code | Register | Hex Value | Suffix Code | Register | Hex Value |
|-------------|----------|-----------|-------------|----------|-----------|
| 0002        | 0x01     | 80h       | 0002        | 0xD4     | 1h        |
| 0002        | 0x21     | 1F4h      | 0002        | 0xD6     | 0h        |
| 0002        | 0x24     | 395h      | 0002        | 0xD7     | Bh        |
| 0002        | 0x25     | 226h      | 0002        | 0xD8     | Fh        |
| 0002        | 0x26     | 1C2h      | 0002        | 0xD9     | 3h        |
| 0002        | 0x35     | 0h        | 0002        | 0xDA     | 3h        |
| 0002        | 0x36     | 0h        | 0002        | 0xDB     | 1Bh       |
| 0002        | 0x55     | 1FCh      | 0002        | 0xE0     | 37h       |
| 0002        | 0x60     | 0h        | 0002        | 0xE1     | 60h       |
| 0002        | 0x61     | 1h        | 0002        | 0xE2     | A0h       |
| 0002        | 0x64     | 0h        | 0002        | 0xE3     | 0h        |
| 0002        | 0x65     | 1h        | 0002        | 0xE4     | C0h       |
| 0002        | 0xD0     | 0h        | 0002        | 0xE5     | 1h        |
| 0002        | 0xD1     | FDh       | 0002        | 0xE6     | 20h       |
| 0002        | 0xD2     | 1Ch       | 0002        | 0xE9     | 24h       |
| 0002        | 0xD3     | 1h        | 0002        | 0xEA     | 10h       |

## APPLICATION INFORMATION

### Setting the Output Voltage ( $V_{OUT}$ )

The MP8880A has two modes to set the output voltage: internal feedback divider mode and external feedback divider mode.

VOUT\_COMMAND sets the feedback reference voltage with 1.5mV/LSB and a maximum value of 1.5345V.  $V_{OUT}$  is determined by the reference voltage and FB divider ratio. In internal feedback divider mode, the internal FB divider ratio is set via MFR\_VOUT\_CTRL (D2h) (see Table 10)

**Table 10: Internal Feedback Divider Mode**

| MFR_VOUT_CTRL (D2h), Bits[2:0] | Internal FB Divider Ratio <sup>(12)</sup> | Output Range    |
|--------------------------------|-------------------------------------------|-----------------|
| 000                            | 1:1, range 1                              | 0.6V to 1.5345V |
| 001                            | 1:2, range 2                              | 0.6V to 3.069V  |
| 010                            | 1:4, range 3                              | 0.6V to 6.138V  |
| 011                            | 1:8, range 4                              | 1.2V to 12.276V |
| 100                            | 1:16, range 5                             | 2.4V to 24.552V |

**Note:**

12) The internal divider ratio is defined as R2: (R1 + R2).

In external feedback divider mode, the external resistor divider sets the output voltage. In addition, the internal FB divider ratio should be set to 1:16 when using the external divider. It is recommended to choose a resistor between 10kΩ and 100kΩ for R2. R1 can be estimated with Equation (8):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (8)$$

Figure 12 shows the external feedback circuit.

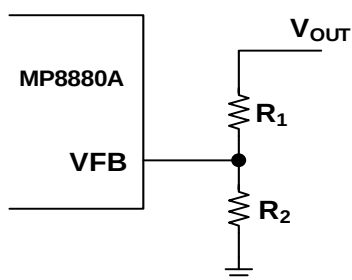


**Figure 12: Feedback Network**

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Place the input capacitor as close to the VIN pin as possible.

Since  $C_{IN}$  absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , estimated with Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor determines the input voltage ripple. Select an input capacitor that meets the system's input voltage ripple requirement. The input voltage ripple can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , estimated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

### Selecting the Output Capacitor

The output capacitor must maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be calculated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (13)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

When using capacitors with a higher ESR (e.g. an electrolytic capacitor), the ESR dominates the impedance at the switching frequency. The output voltage ripple can be determined by the ESR values. For simplification, the output voltage ripple can be calculated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (15)$$

Larger-value output capacitors reduce the output voltage ripple and improve load transient response. However, the maximum output capacitance limit should also be considered in design application. If the output capacitance is too large, the output voltage cannot reach the target value during soft start, and then it fails to regulate. The maximum output capacitance ( $C_{O\_MAX}$ ) can be calculated with Equation (16):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (16)$$

Where  $I_{LIM\_AVG}$  is the average start-up current during soft start, and  $t_{SS}$  is the soft-start time.

### Selecting the Inductor



**Optimized Performance with MPS Inductor MPL-AY1050 Series**

The inductor supplies constant current to the output load while being driven by the high-frequency SW node voltage.

A larger-value inductor results in less ripple current and lower output voltage ripple, but also has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductance is to allow the peak-to-peak ripple current in the inductor to be 30% to 60% of the maximum output load current. The inductance can be calculated with Equation (17):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (17)$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (18):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (18)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 11 lists our power inductor recommendations. Select a part number based on your design requirements.

**Table 11: Power Inductor Selection**

| Part Number    | Inductor Value | Manufacturer |
|----------------|----------------|--------------|
| MPL-AY1050-100 | 10μH           | MPS          |

Visit [MonolithicPower.com](http://MonolithicPower.com) under Products > Inductors for more information.

## PCB Layout Guidelines

An optimized PCB layout is critical for reliable operation. For the best results, refer to Figure 13 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
3. Ensure that the high-current paths (PGND, IN, and OUT) have short and wide traces.
4. Place as many PGND vias as possible close to the pin to minimize parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the VCC and AGND pins.
6. Connect AGND and PGND at the point of the VCC capacitor's ground.
7. Place the BST capacitor as close to BST and SW as possible.
8. Place the external feedback resistors close to the VFB pin.
9. Avoid routing sensitive traces close to the input plane and SW node.

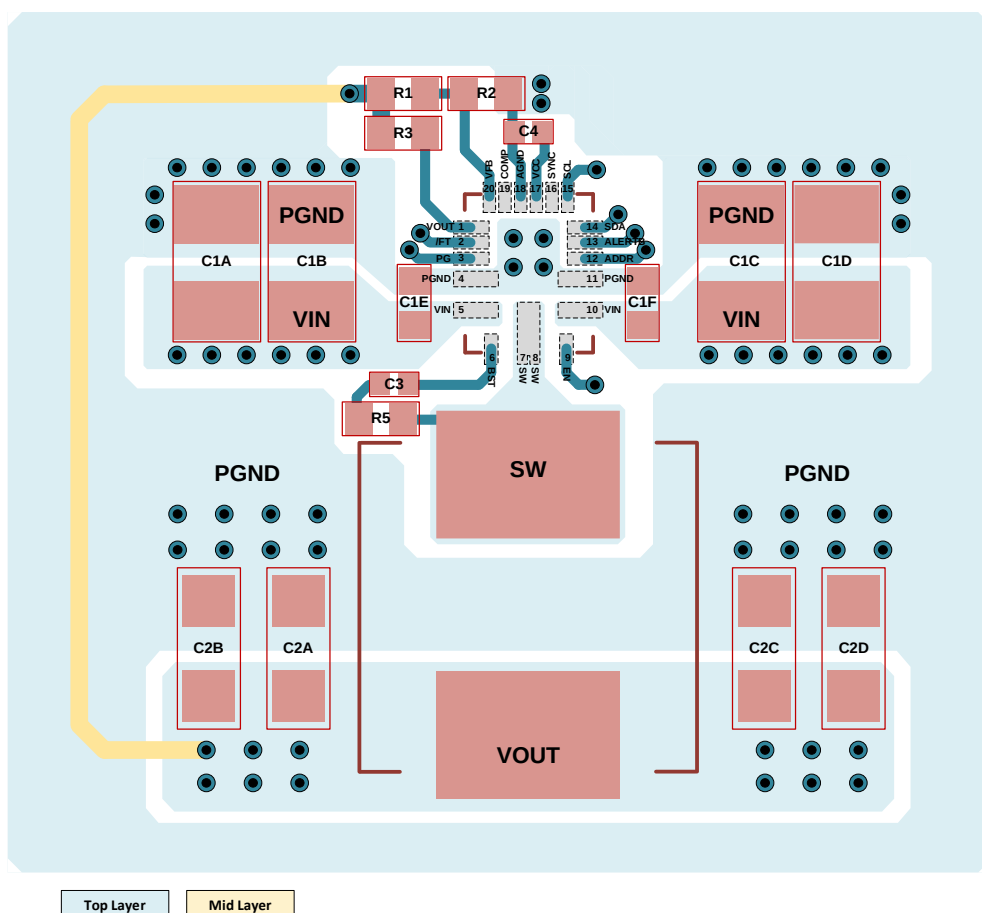


Figure 13: Recommended PCB Layout (Placement and Top Layer PCB)

# TYPICAL APPLICATION CIRCUITS

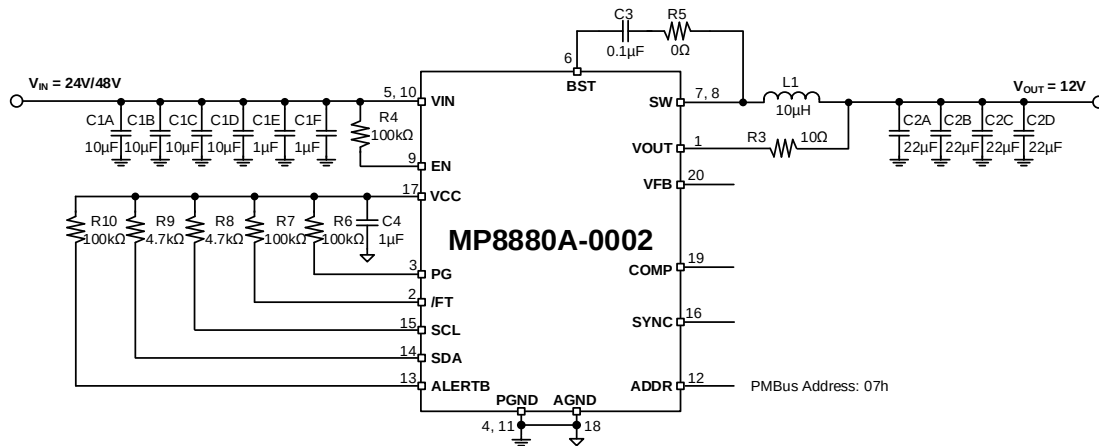


Figure 14: Typical Application Circuit (Single-Phase Operation with Internal Feedback Divider,  $V_{IN} = 24V/48V$ ,  $V_{OUT} = 12V$ ) (13)

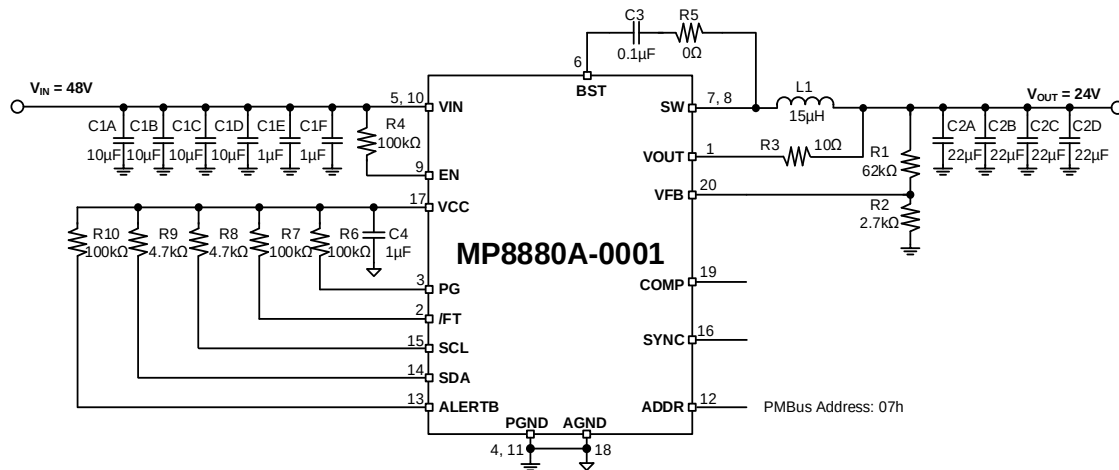


Figure 15: Typical Application Circuit (Single-Phase Operation with External Feedback Divider,  $V_{IN} = 48V$ ,  $V_{OUT} = 24V$ ) (13)

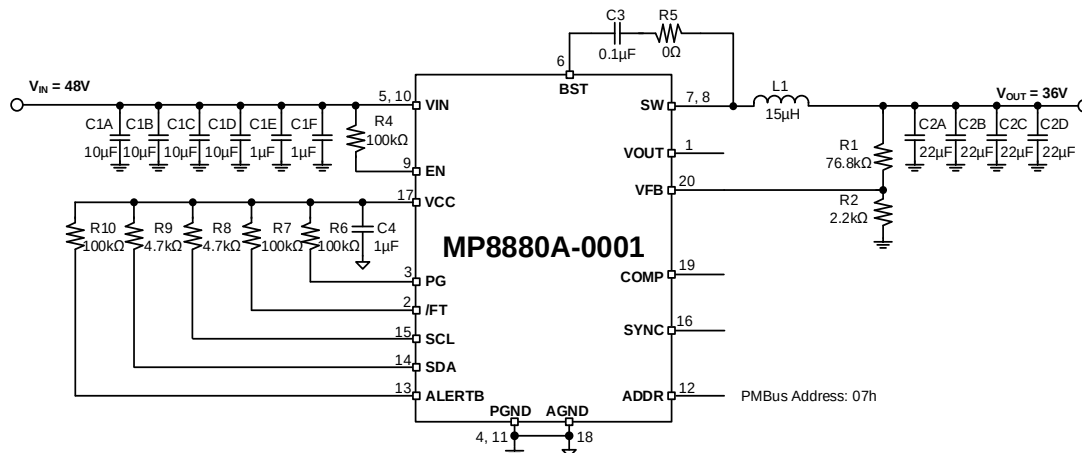


Figure 16: Typical Application Circuit (Single-Phase Operation with External Feedback Divider,  $V_{IN} = 48V$ ,  $V_{OUT} = 36V$ ) (13) (14)

## TYPICAL APPLICATION CIRCUITS *(continued)*

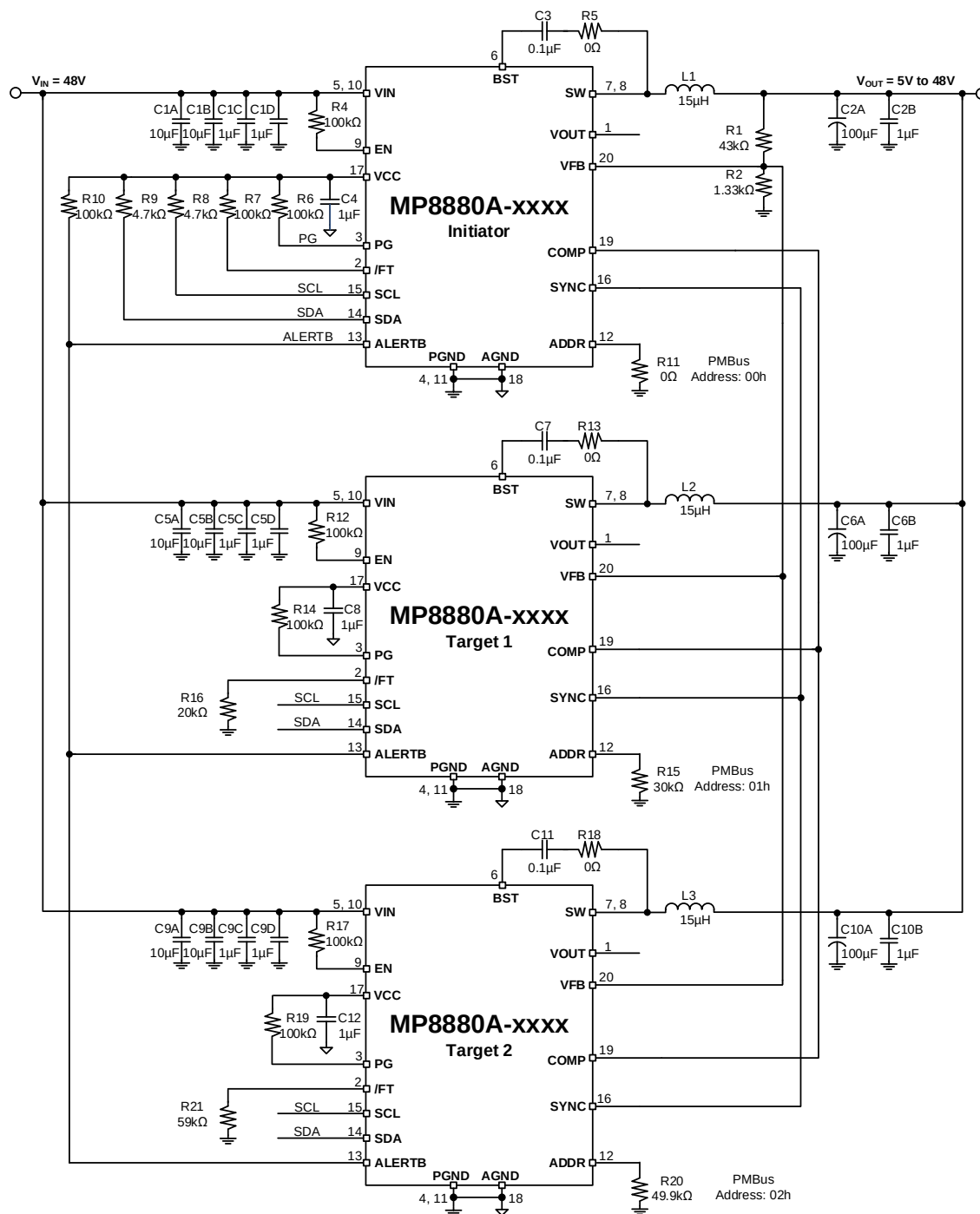


**Figure 17: Typical Application Circuit (3-Phase Parallel Operation for PD EPR 240W Application,  $V_{IN} = 48V$ ,  $V_{OUT} = 5V$  to  $48V$ )<sup>(13)</sup> <sup>(15)</sup>**

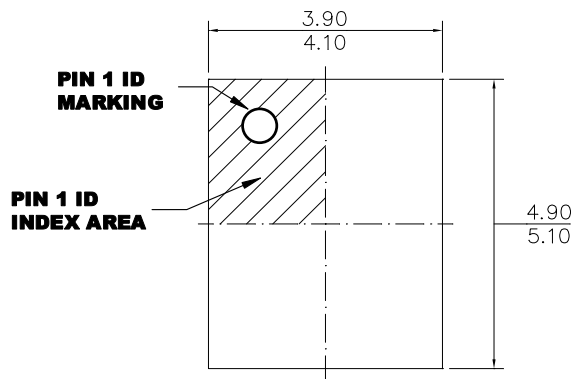
**Notes:**

- 13) Do not use frequencies exceeding 1MHz when  $V_{IN}$  exceeds 30V due to thermal considerations.
- 14) If  $V_{OUT}$  exceeds 30V, the VOUT pin should be floating and the VO\_BIAS function is not supported.
- 15) For EPR 140W applications, 2-phase paralleled operation is recommended. If better thermal performance is required, 4-phase paralleled operation can be implemented. In EPR applications, the external  $V_{OUT}$  bias circuit can be added to improve efficiency when  $V_{OUT}$  is below 20V. Contact an MPS FAE for more information.

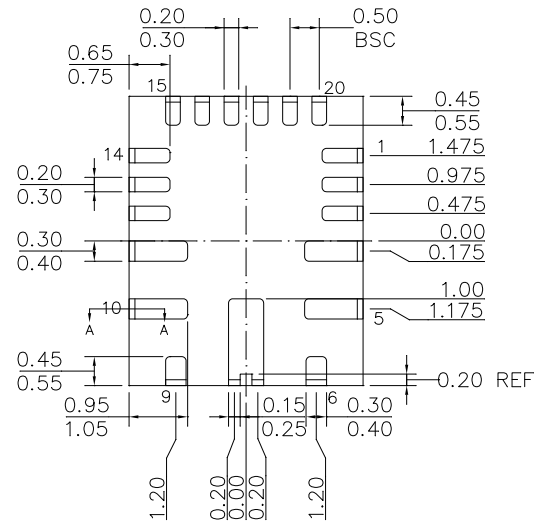
## PACKAGE INFORMATION

### QFN-20 (4mmx5mm)

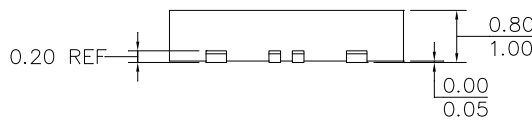
## Wettable Flank



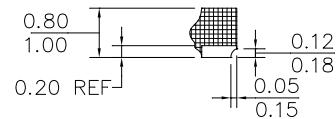
**TOP VIEW**



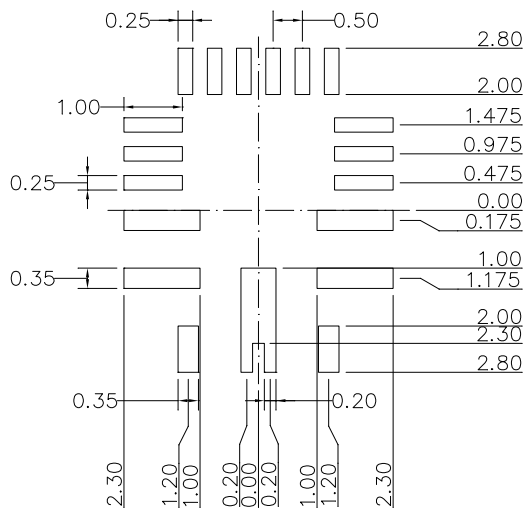
### BOTTOM VIEW



### SIDE VIEW



**SECTION A-A**

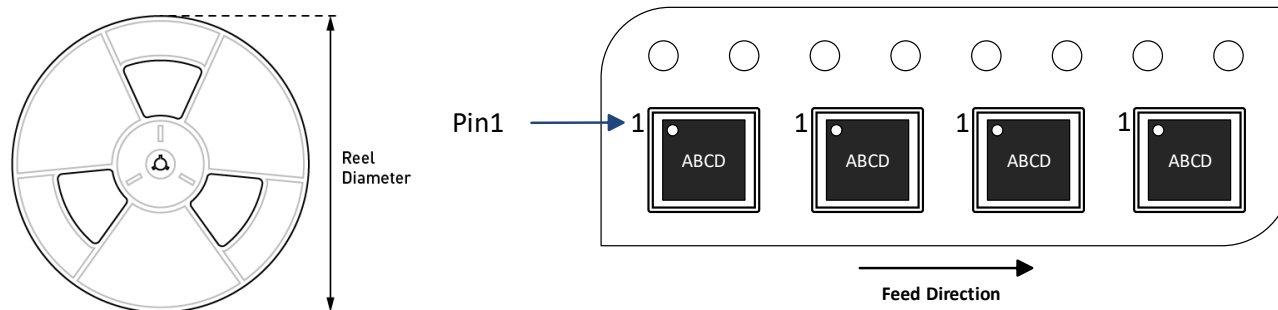


## **RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) LAND PATTERNS OF PIN 4, PIN 5, PIN 10, AND PIN 11 HAVE THE SAME LENGTH AND WIDTH.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



| Part Number       | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MP8880AGVE-0000-Z | QFN-20<br>(4mmx5mm) | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |
| MP8880AGVE-0001-Z |                     |                |                |                |               |                    |                    |
| MP8880AGVE-0002-Z |                     |                |                |                |               |                    |                    |
| MP8880AGVE-xxxx-Z |                     |                |                |                |               |                    |                    |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 9/12/2025     | Initial Release | -             |

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