钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD485E

Half-duplex RS-485 transceiver

网址 www.sztdbdt.com

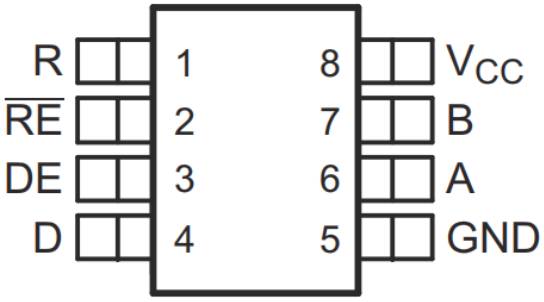
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Up to 15kV bus pin ESD protection
- 1/2 unit load: up to 64 nodes on a single bus
- Bus fail-safe receiver
- Non-intrusive power-up and power-down bus inputs and outputs
- Small VSSOP-8 package
- Meets or TIA/EIA-485A standard requirements
- Industry-standard SN75176 compatible package



SOIC/ MSOP/PDIP

Description

The SN65HVD485E device is a half-duplex transceiver specifically designed for RS-485 bus networks. This device is powered by a 5V supply and is fully compliant with the TIA/EIA-485A standard. It is suitable for transmitting data rates up to 10Mbps over long twisted-pair cables and is designed to operate at extremely low supply currents (typically less than 2mA, excluding load). When the is in the inactive shutdown mode, the supply current drops to less than 1mA.
The wide common-mode range and high ESD protection level of this device make it suitable for applications, such as electrical inverters, status/command signals on telecom racks, wired chassis interconnects, and industrial automation networks where noise immunity is critical. The SN65H485E device is industry-standard pin-compatible with the SN75176 device. The power-on reset circuitry keeps the outputs in a high-imped state until the supply voltage stabilizes. The thermal shutdown feature protects the device from damage caused by system fault conditions. The SN65HVD485E device can operate in temperatures ranging from －40°C to 85°C.

Applications

- Motor control
- Power inverters
- Industrial automation
- Building automation networks
- Industrial process control
- Battery-powered applications
- communications equipment

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable,active high
GND	5	Reference potential	Local device ground
R	1	Digital input	Receive data output
RE	2	Digital input	Receiver enable,active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

	MIN	MAX	UNIT
V_{CC} Supply voltage	-0.5	7	V
Voltage range at A or B	-9	14	V
Voltage range at any logic pin	-0.3	V_{CC}+0.3	V
Receiver output current	-24	24	mA
Voltage input range,transient pulse,A and B,through 100Ω(seeFigure13)	-50	50	V
Junction temperature	170	170	℃
Continuous total power dissipation			
Tstg Storage temperature	-65	130	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM),per ANSI/ ESDAJEDECJS-001(1)	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model(CDM),per JEDEC specification JESD22-C101(2)		± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{cc}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		-7		12	V
V_{IH}	High-level input voltage(D,DE,or RE inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage(D,DE,or RE inputs)		0		0.8	V
V_{ID}	Differential input voltage		-12		12	V
I_o	Output current	Driver	-60		60	mA
		Receiver	-8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0		10	Mbps
T_A	Operating free-air temperature		-40		85	℃
T_J	Junction temperature		-40		130	℃

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

Thermal Information

THERMAL METRIC		SN65HVD485E			UNIT
		D(SOIC)	DGK (VSSOP)	P(PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	137.8	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top)thermal resistance	56.3	31.2	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	71.7	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.6	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	70.5	60.4	°C/W

Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\lvert V_{OD}\rvert$	Differential output voltage	I_O=0,No load	3	4.3		V
		R_L=54 W(see Figure 1)	1.5	2.3		
		V_{TEST}=-7V to12V (see Figure2)	1.5			
$\triangle\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	-0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1	2.6	3	V
$\triangle V_{OC(SS)}$	Change in steady-state common-mode output voltage		-0.1	0	0.1	V
$V_{OC(PP)}$	Common-mode output voltage	See Figure 3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				μA
I_I	Input current	D,DE	-100		100	μA
I_{OS}	Short-circuit output current	-7V≤V_O≤12V(see Figure 7)	-250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_o=-8mA		-85	-10	mV
V_{IT-}	Negative-going input threshold voltage	I_o=8 mA	-200	-115		mV
V_{hys}	Hysteresis voltage(V_{IT+}-V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID}=200 mV,I_{OH}=-8 mA(see Figure 8)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID}=-200 mV,I_{OH} =8 mA(see Figure 8)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_o=0 to V_{cc},RE=V_{cc}	-1		1	μA
I_I	Bus input current	V_{IH}=12V,V_{cc}=5V			0.5	mA
		V_{IH}=12V,V_{cc}=0			0.5	
		V_{IH}=-7V,V_{cc}=5V	-0.4			
		V_{IH}=-7V,V_{cc}=0	-0.4			
I_{IH}	High-level input current(RE)	V_{IH}=2V	-60	-30		μA
I_{IL}	Low-level input current(RE)	V_{IL}=0.8 V	-60	-30		μA
C_{diff}	Diferential input capacitance	V_I=0.4 sin(4E6 π t)+0.5 V,DE at 0V		7		pF

(1) All typical values are at 25°C and with a 5-V supply

Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(AVG)}$	Average power dissipation	R_L=54Ω,Input to D is a 10 Mbps 50%duty cycle square wave V_{cc} at 5.5V,T_j=130℃			219	mW
T_{SD}	Thermal shut-down junction temperature			165		℃

Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{cc}	Driver and receiver enabled	D at V_{cc} or open or 0V,DE at V_{cc},RE at 0V,No load			2	mA
	Driver and receiver disabled	D at V_{cc} or open, DE at 0V,RE at V_{cc}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time,low-to-high-level output	R_L=54Ω,C_L=50 pF (see Figure 4)			30	ns
t_{PHL} Propagation delay time,high-to-low-level output				30	ns
t_r Differential output signal rise time				25	ns
t_f Differential output signal fall time				25	ns
$t_{sk(p)}$ Pulse skew(It_{PHL}-t_{PLH}I)				5	ns
t_{PZH} Propagation delay time, high-impedance-to-high-level output	R_L=110Ω,RE at 0V (see Figure 5)			150	ns
t_{PHZ} Propagation delay time, high-level-to-high-impedance output				100	ns
P_{ZL} Propagation delay time, high-impedance-to-low-level output	R_L=110Ω,RE at 0V (see Figure 6)			150	ns
P_{LZ} Propagation delay time, low-level-to-high-impedance output				100	ns
$t_{PZH(SHN)}$ Propagation delay time, shutdown-to-high-level output	R_L=110Ω,RE at V_{CC} (see Figure 5)			2600	ns
$t_{PZL(SHDN)}$ Propagation delay time, shutdown-to-low-level output	R_L=110 Ω,RE at V_{CC} (see Figure 6)			2600	ns

Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time,low-to-high-level output	V_{ID}=-1.5V to 1.5V,C_L=15 pF (see Figure 9)			200	ns
t_{PHL}	Propagation delay time,high-to-low-level output				200	ns
$t_{sk(p)}$	Pulse skew($\|t_{PHL}-t_{PLH}\|$)			6		ns
t_r	Output signal rise time				3	ns
t_f	Output signal fall time				3	ns
t_{pzH}	Output enable time to high level	C_L=15 pF,DE at 3 V, (see Figure 10 and Figure11)			50	ns
t_{pzL}	Output enable time to low level				50	ns
t_{PHz}	Output enable time from high level				50	ns
t_{pLZ}	Output enable time from low level				50	ns
$t_{PZH(SHDN)}$	Propagation delay time,shutdown-to-high-level output	C_L=15 pF,DE at 0V, (see Figure 12)			3500	ns
$t_{PZL(SHDN)}$	Propagation delay time,shutdown-to-low-level output				3500	ns

Parameter Measurement Information

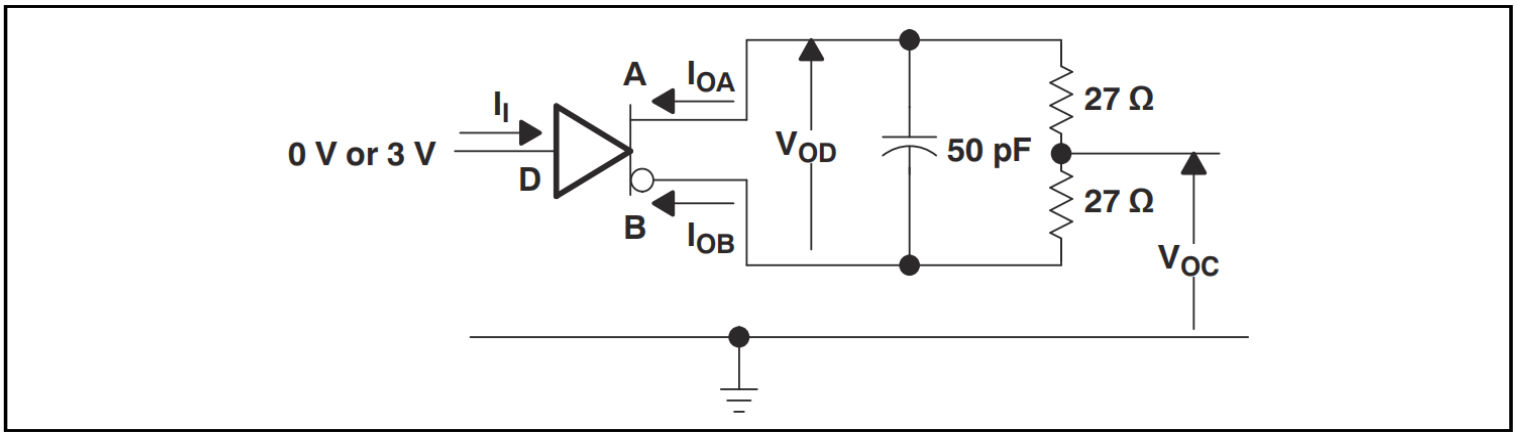


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

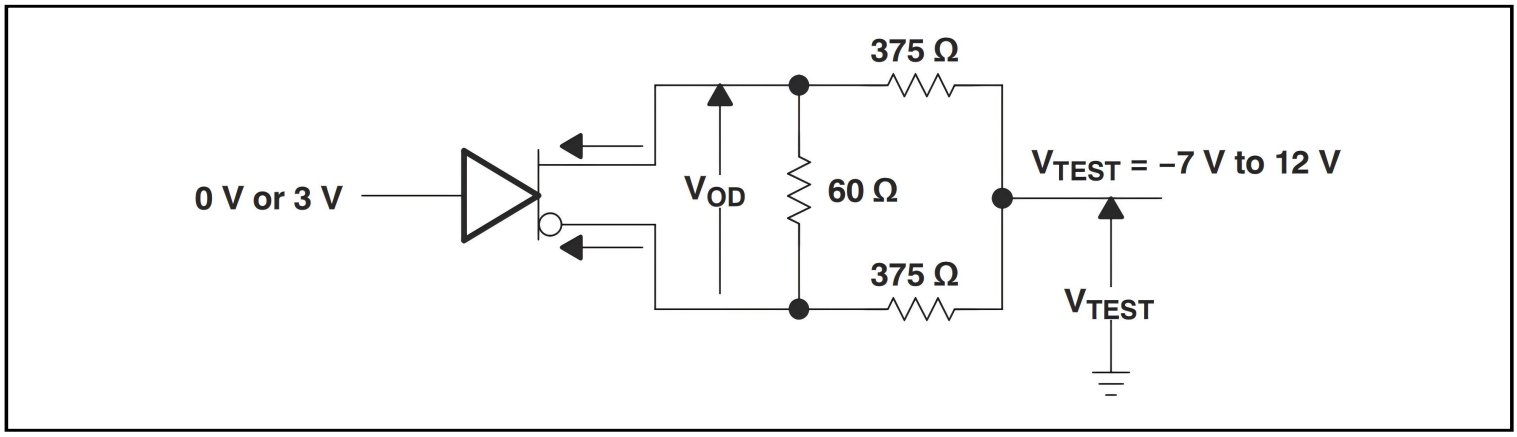


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

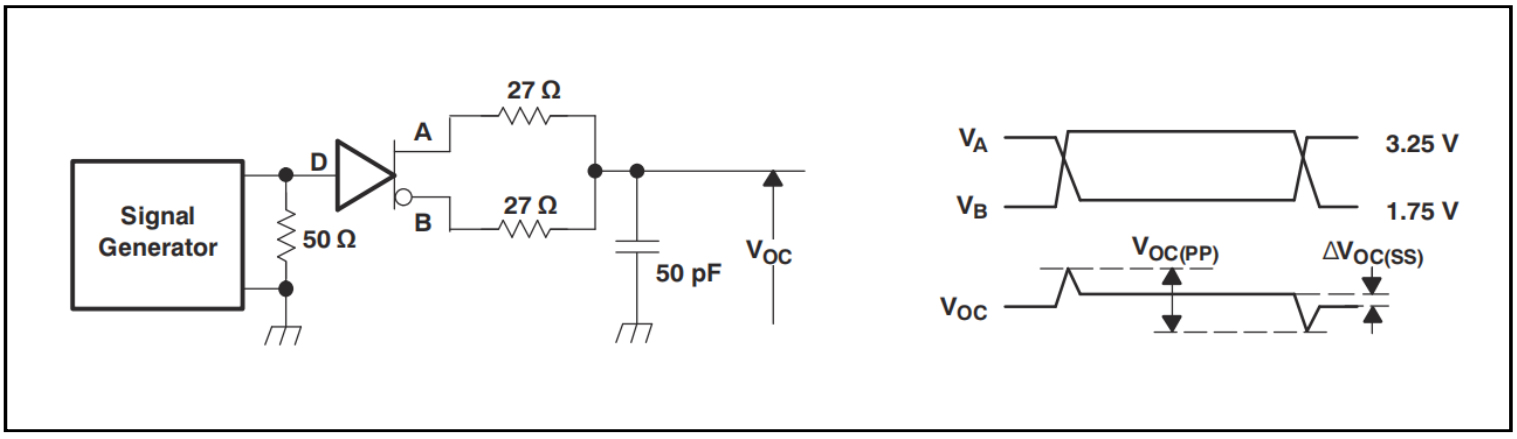


Figure 3. Driver V_{OC} Test Circuit and Waveforms

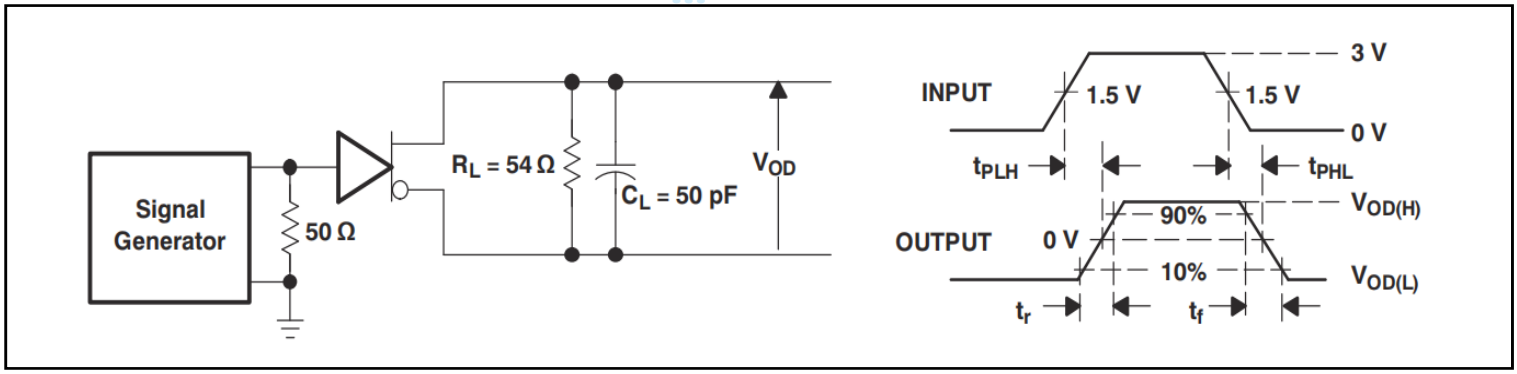


Figure 4. Driver Switching Test Circuit and Waveforms

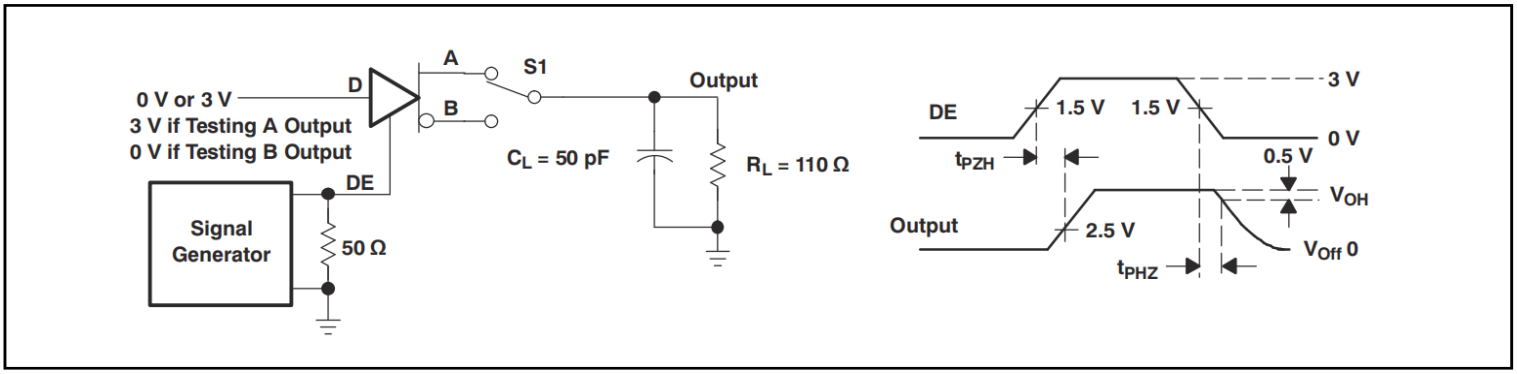


Figure 5. Driver Enable/Disable Test Circuit and Waveforms, High Output

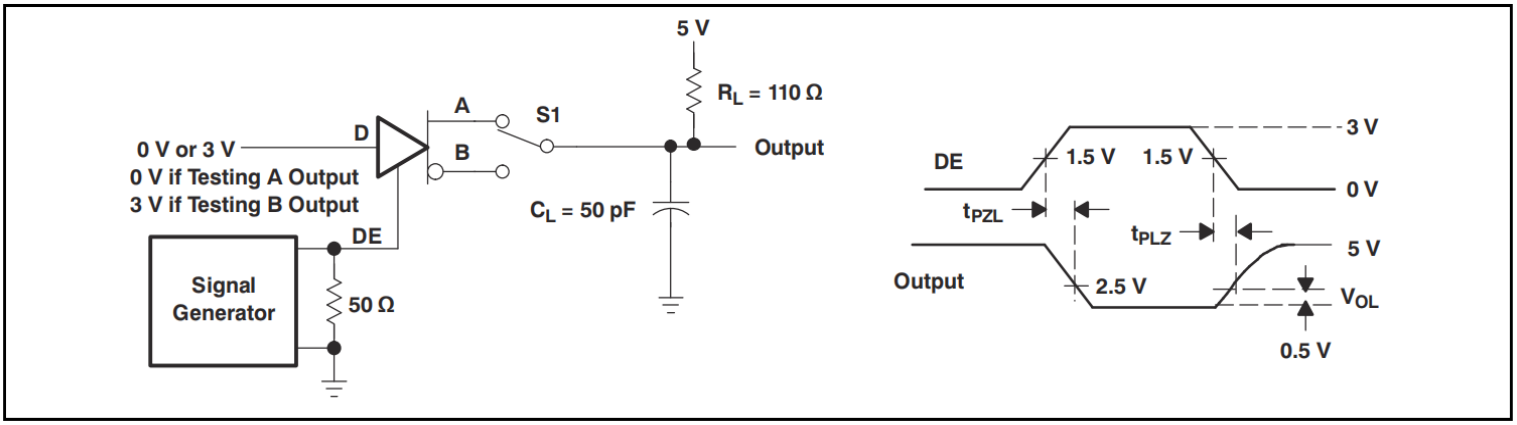


Figure 6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

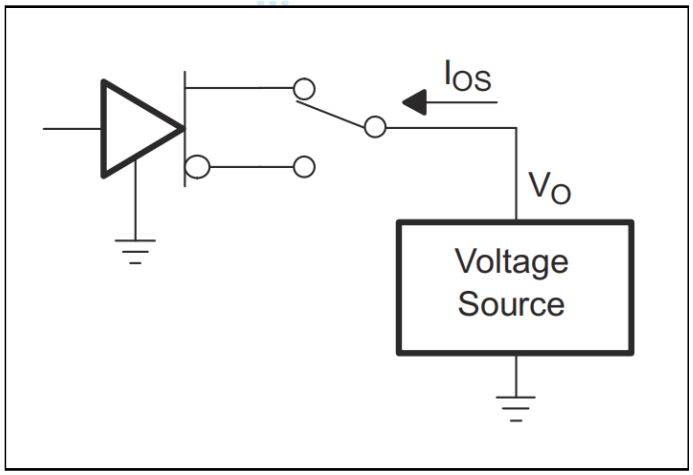


Figure 7. Driver Short-Circuit Test

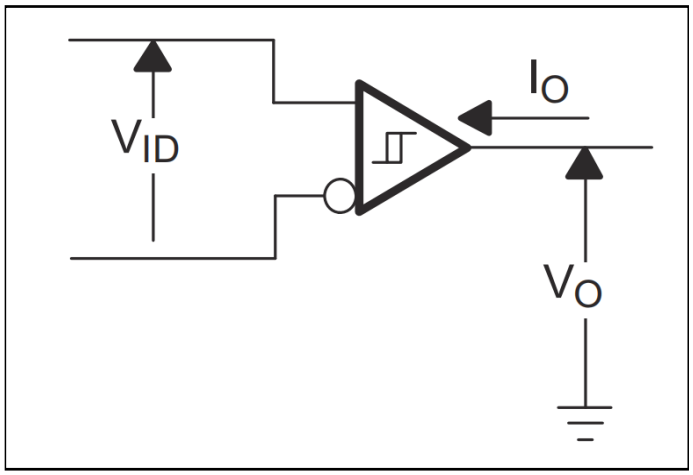


Figure 8. Receiver Parameter Definitions

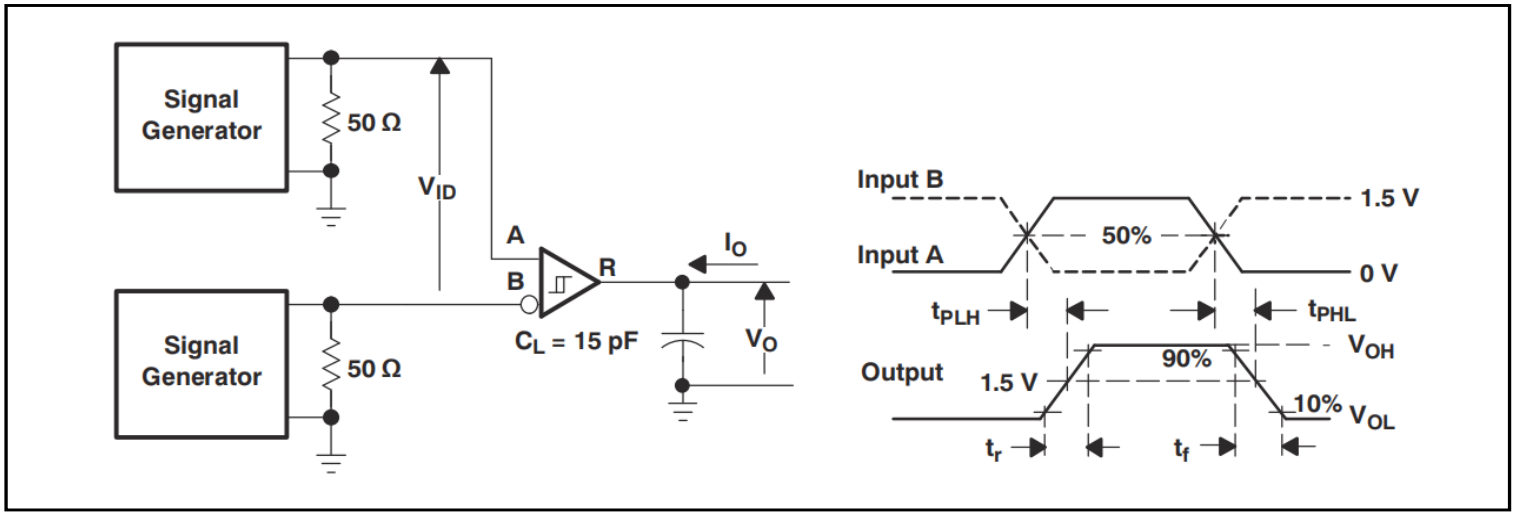


Figure 9. Receiver Switching Test Circuit and Waveforms

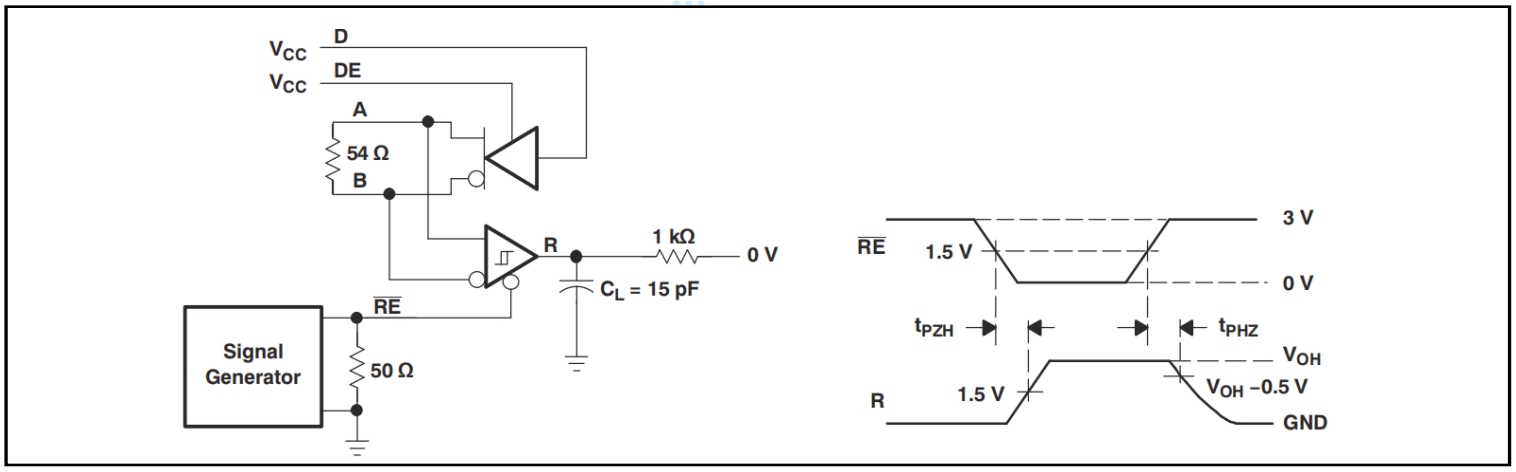


Figure 10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

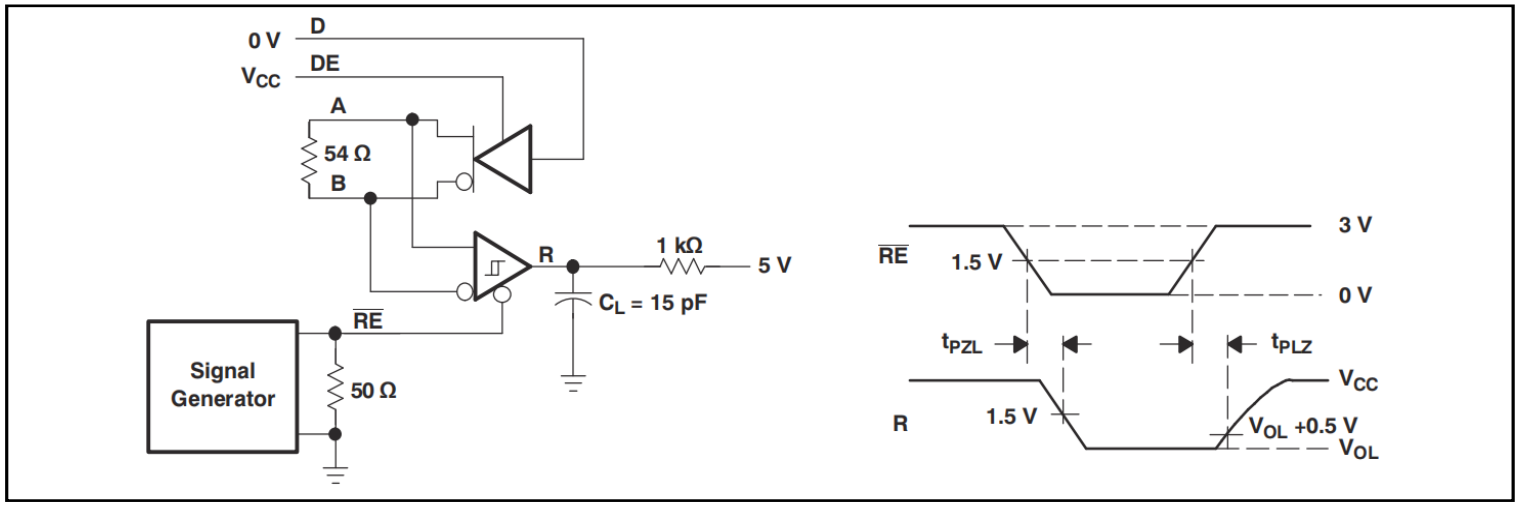


Figure 11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

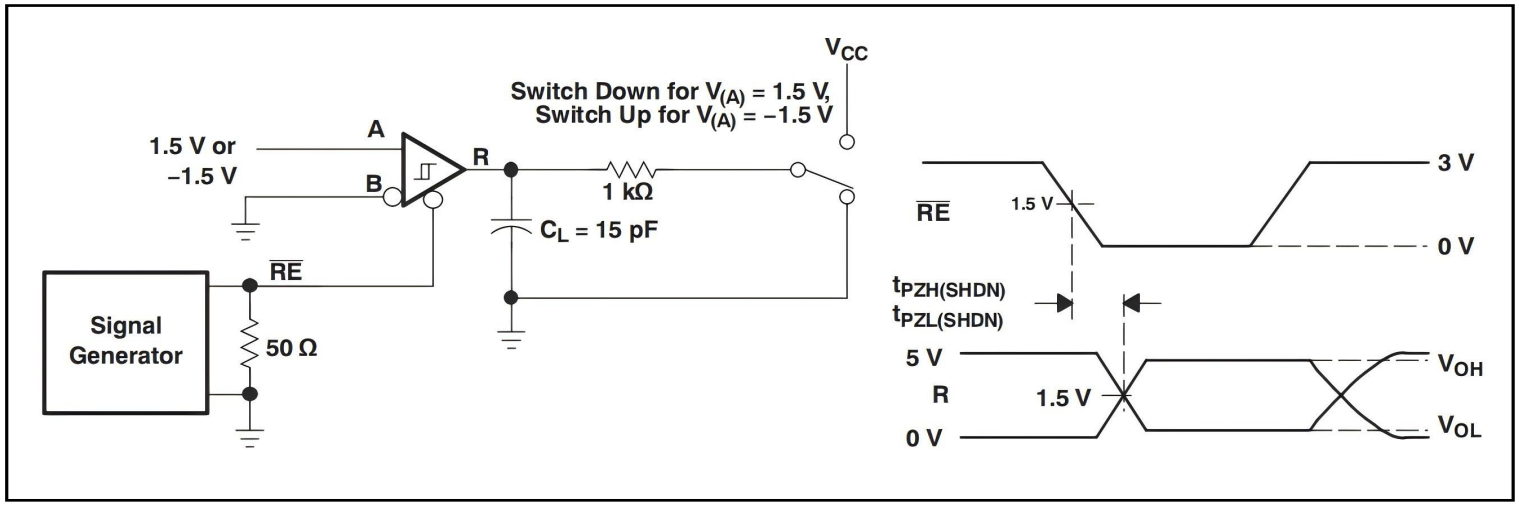


Figure 12. Receiver Enable From Shutdown Test Circuit and Waveforms

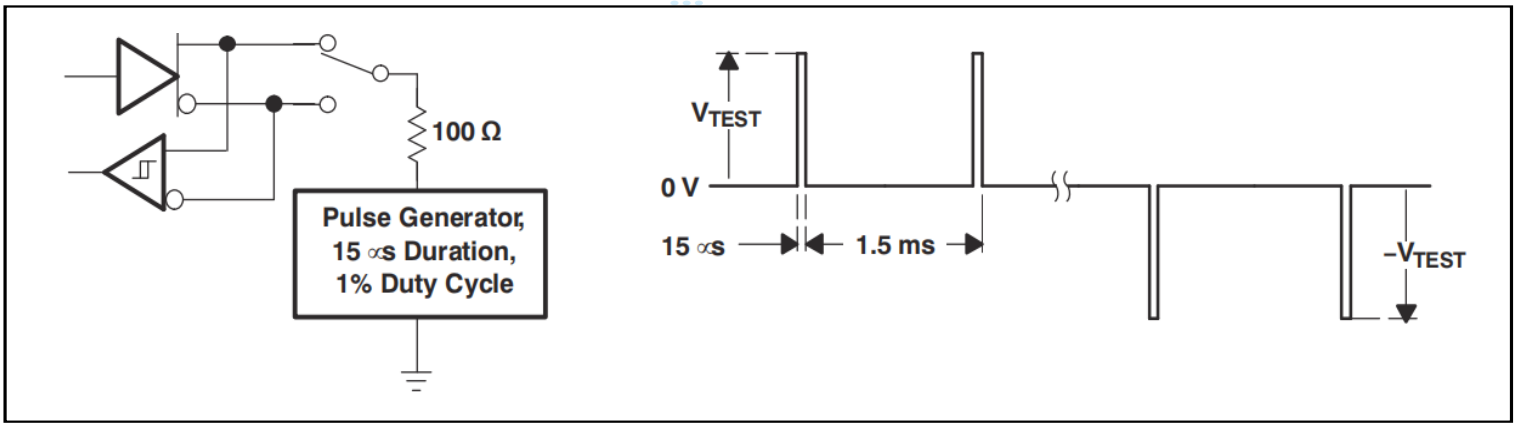


Figure 13. Test Circuit and Waveforms, Transient Over-Voltage Test

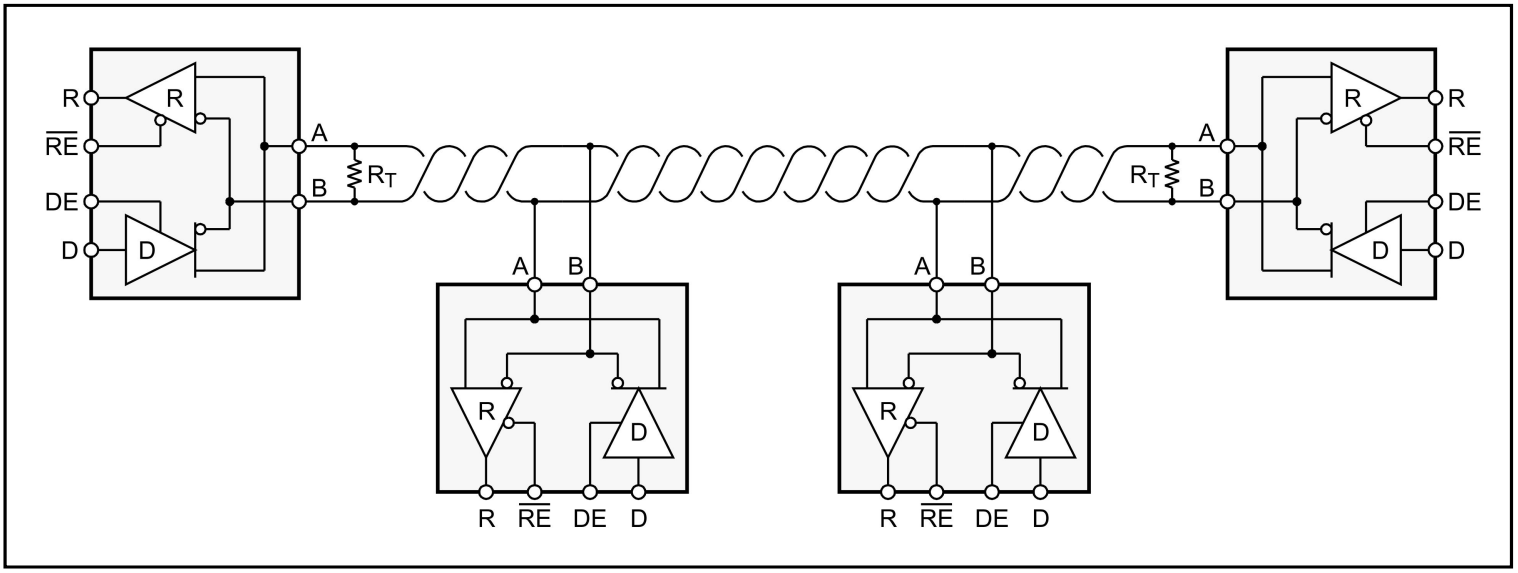


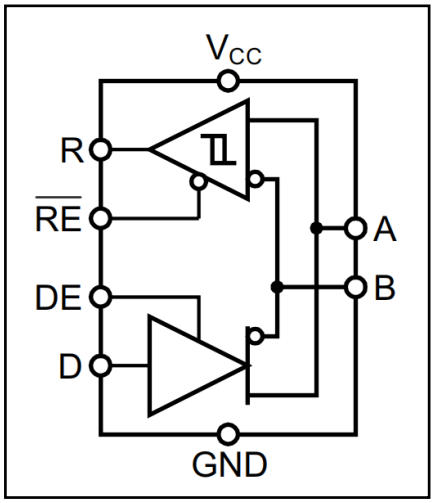
Figure 14.Typical Application Schematic

Detailed Description

Overview

The SN65HVD485E device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 10 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). Up to 64 units of the SN65HVD485E device can share a common RS-485 bus due to the low bus-input currents of the device. The device also features a high degree of ESD protection and low standby current consumption of 1 mA (maximum).

Functional Block Diagram



Feature Description

The SN65HVD485E device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A is low, and V_{OD} is negative. When DE is low, both outputs turn high impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus when left open, the driver is disabled (high impedance) by default. The D pin has an internal pullup resistor to V_{CC}; thus when left open while the driver is enabled, output A turns high and B turns low.

Driver Function Table

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin (RE) is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold (V_{IT+}) the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold (V_{IT-}), the receiver output (R) turns low. If $V_{ID}$is between V_{IT+} and V_{IT-}, the output is indeterminate. When RE is logic high or left open, the receiver output is high impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Receiver Function Table

DIFFERENTIAL INPUT VID=VA-VB	ENABLE RE	OUTPUT R	FUNCTION
$V_{IT+}<V_{ID}$	L	H	Receive valid bus High
$V_{IT-}<V_{ID}<V_{IT+}$	L	?	Indeterminate bus state
$V_{ID}<V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated)bus	L	H	Fail-safe high output

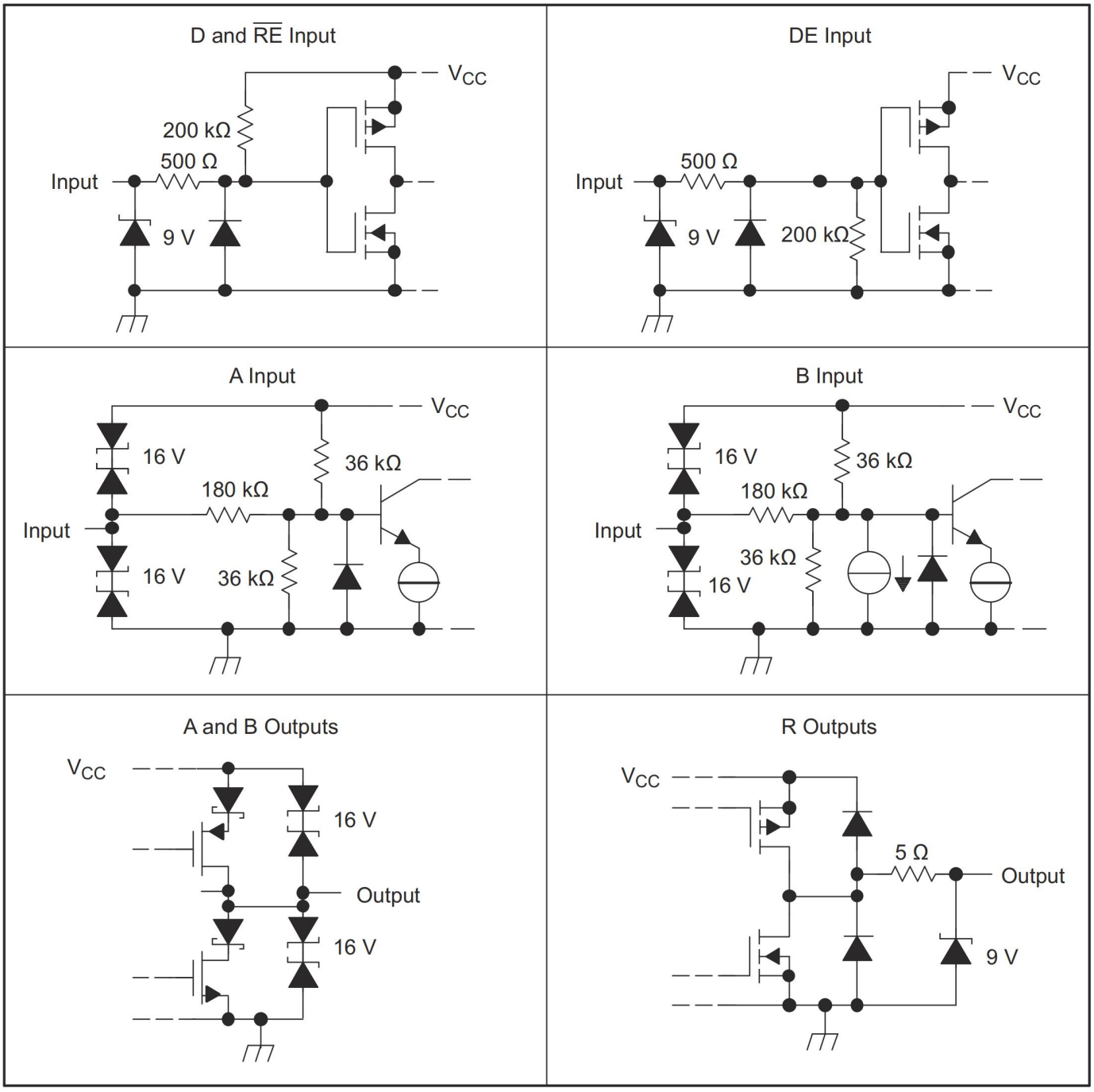


Figure 15.Equivalent Input and Output Schematic Diagrams

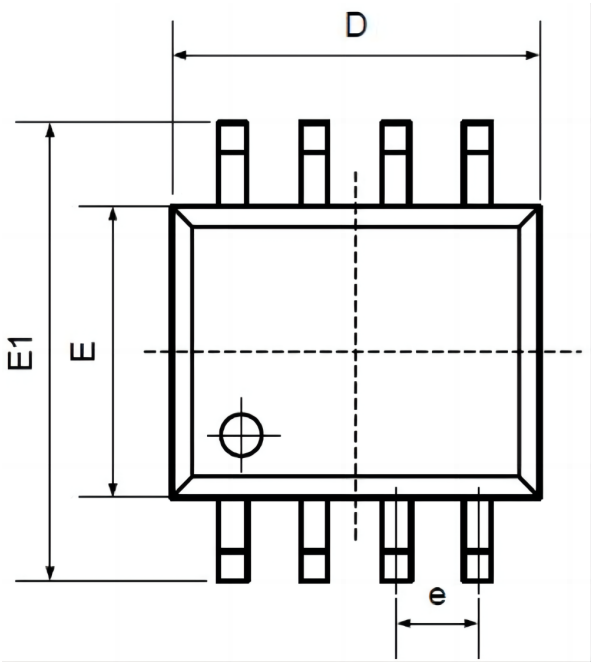
Order information

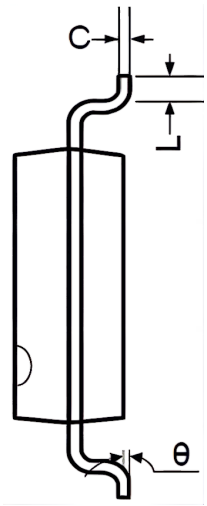
Order Number	Package	Package Quantity	Marking On The park	Temperature
SN65HVD485EDGKR-TUDI	MSOP8	Tape,Reel,4000	NWH	-40℃ to 85℃
			485G	
			NWJ	
SN65HVD485EDR-TUDI	SOP8	Tape,Reel,4000	VP485	
SN65HVD485EP-TUDI	DIP8	Tube,50,A box of 2000	65HVD485	

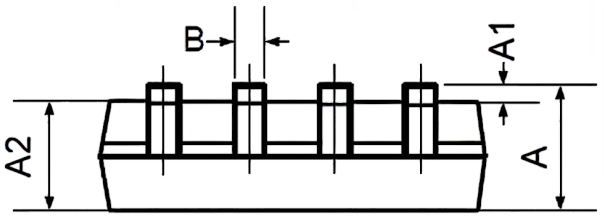
Revision history

	Date	Revision	Page
V1.0	2023/7	New	1-9
V1.1	2025/4	Update model and PDF template	1-21

Package SOP8

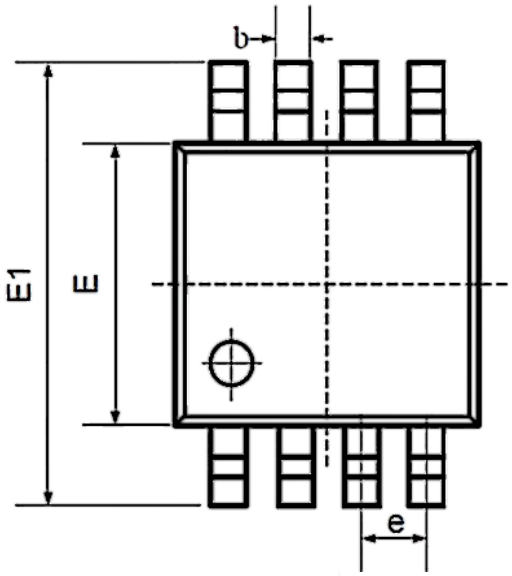


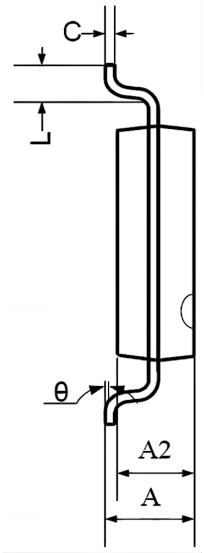


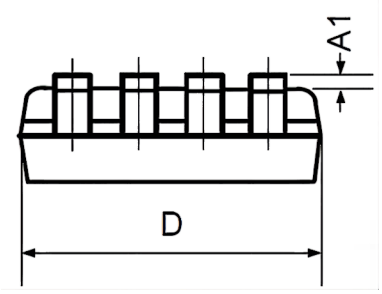


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package MSOP8

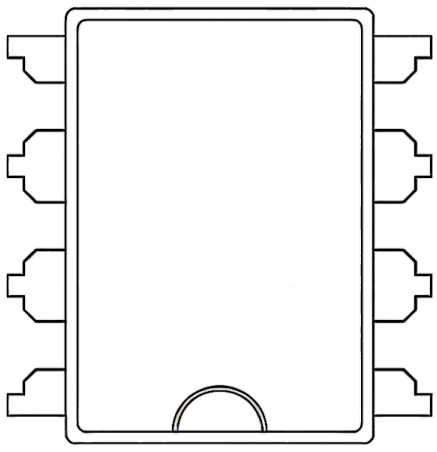


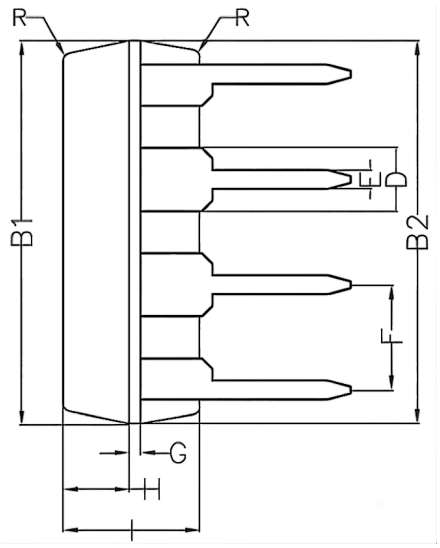


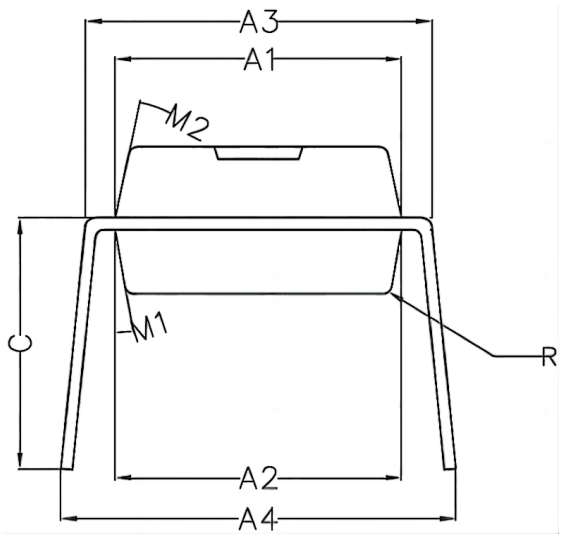


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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