1.8V 64M-BIT
SERIAL NOR FLASH MEMORY WITH
DUAL, QUAD SPI

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1. GENERAL DESCRIPTIONS

The W25Q64PW (64M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single W25Q64PW power supply with current consumption as low as 1mA active and 0.1µA for power-down. All devices are offered in space-saving packages.

The W25Q64PW array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q64PW has 2,048 erasable sectors and 128 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2)

The W25Q64PW supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 332MHz (133MHz x 2) for Dual I/O and MHz (133/166MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

The ECC enabled W25Q64PW device has additional features related to ECC and Reset functionality. These features are supplemented to support and enhance device performance in a highly intensive industrial environment. With ECC enabled feature, the device bit ECC every 16-byte alignment. Device offers internal ECC Status to monitor the ECC error.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q64PW: 64M-bit / 8M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - On-chip ECC(1-Bit correction every 16-Byte)(1)
  - Buffer Mode
- **Highest Performance Serial Flash**
  - 166MHz for Read instruction clocks with 12 and above dummy clocks
  - 83MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles(2)
  - More than 20-year data retention
- **Efficient "Continuous Read"**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
- **Low Power, Wide Temperature Range**
  - Single 1.65 to 1.95V supply
  - <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC 150/208-mil
  - 8-pad USON 4x3-mm / XSON 2x3/4x4-mm
  - 8-pad WSON 6x5-mm
  - 24-ball TFBGA 8x6-mm (5x5 ball array)
  - 12-ball WLCSP
  - Contact Winbond for KGD and other options

Note:

1. To maintain the ECC operation (ECC On Status) on aligned 16-byte memories across the full memory range (on LSB address A[3:0] = 0000b to 1111b) during reads, one time programming of one byte up to 16 bytes of data per aligned 16-Byte memory is required. More than one time programming on aligned 16-byte memories will turn off ECC functionality (ECC Off status) automatically on those affected aligned 16-byte memories during reads. An Erase is required to recover back ECC operations (ECC On Status) of these affected aligned memories during reads.
2. Tested with 16-byte aligned programming.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOIC 150-mil/208-mil

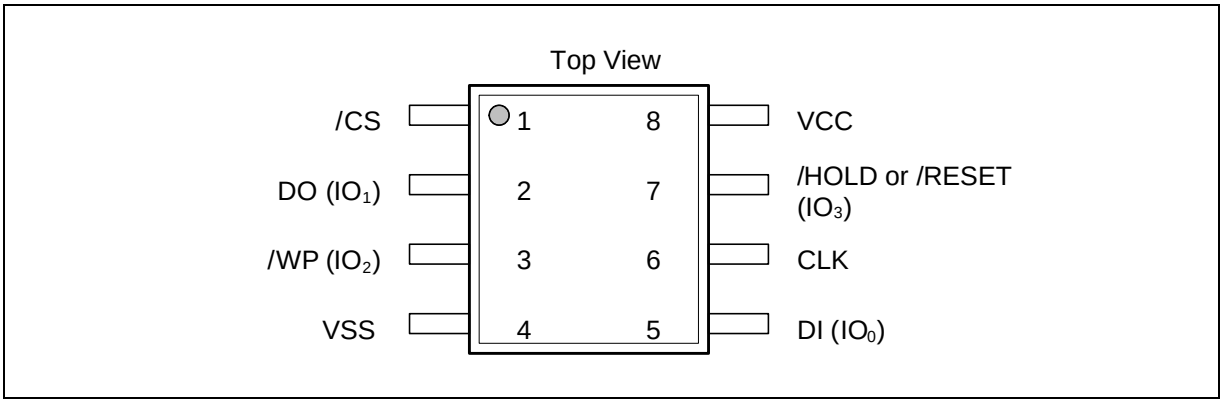


Figure 1a. W25Q64PW Pin Assignments, 8-pin SOIC 150/208-mil (Package Code SN/SS)

3.2 Pad Configuration XSON2x3/4x4-mm, USON4x3-mm, WSON 6x5-mm

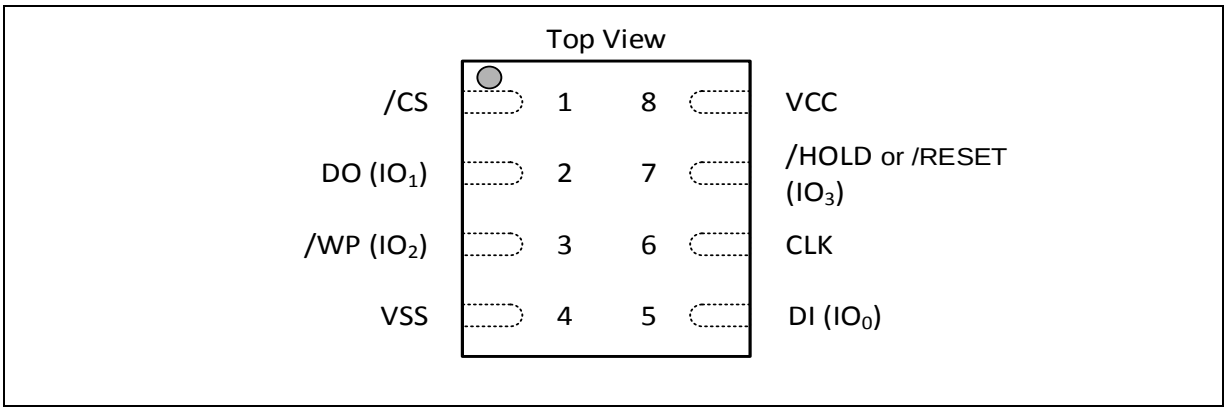


Figure 1b. W25Q64PW Pad Assignments XSON2x3/4x4-mm, USON4x3-mm, WSON 6x5-mm (Package Code XH,XG,UU, ZP)

3.3 Pin Description 150-mil/208-mil, XSON2x3/4x4-mm, USON4x3-mm, WSON 6x5-mm

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes: 1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

3.4 TFBGA 8x6-mm (5x5 Ball Array)

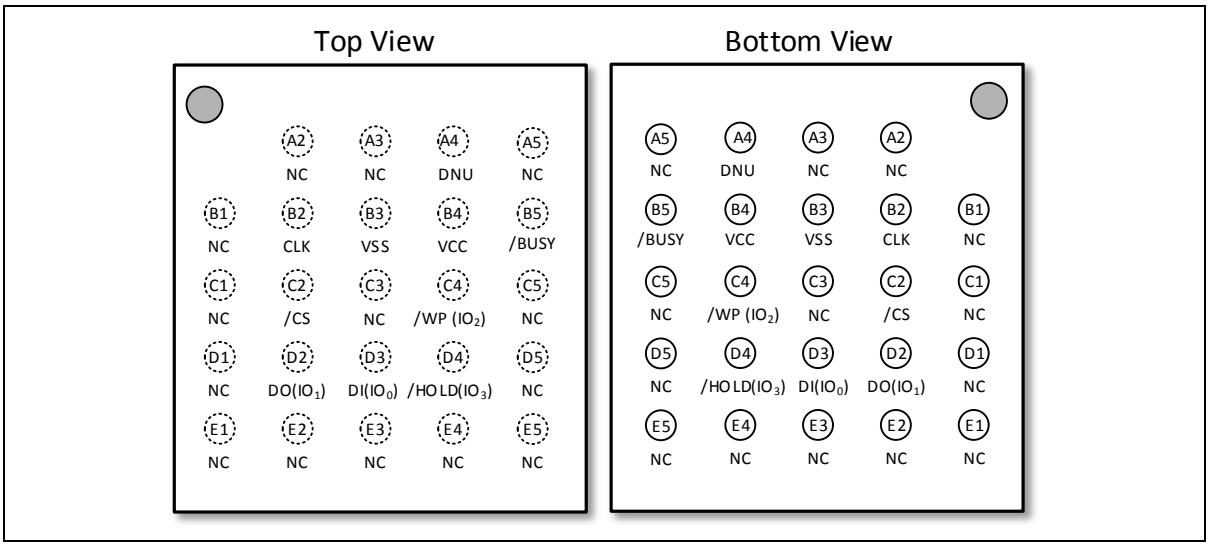


Figure 1c. W25Q64PWTBIH Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB)

3.5 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A4	DNU		Do not use. Leave floating is required.
B2	CLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
B5	/BUSY	O	/BUSY Output. Leave floating if not using(3)
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD (IO3) /RESET	I/O	Hold or Reset Input (Data Input Output 3)(2)
Multiple	NC		No Connect / DNU (Do Not Use)

Notes:
1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions (factory default for Quad Enabled part numbers with ordering option “IQ”).
3. The /BUSY pin is a dedicated hardware pin. If the function is not used, this pin can be left floating.

3.6 Ball Configuration WLCSP

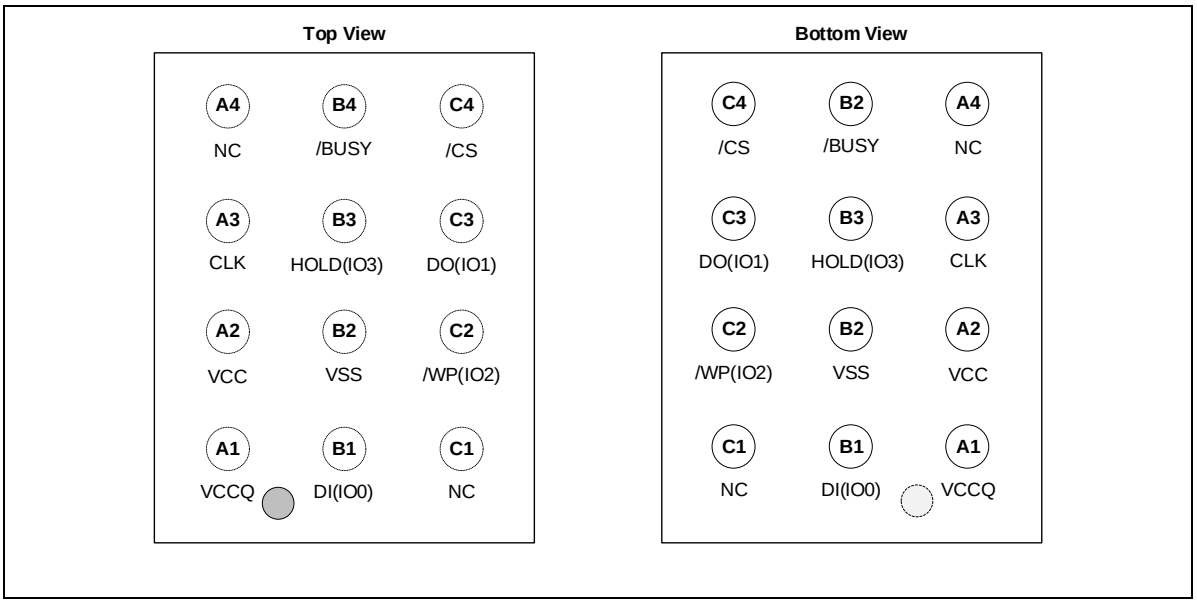


Figure 1d. W25Q64PWBYIH Ball Assignments, 12-ball WLCSP (Package Code BY)

3.7 Ball Description WLCSP12

PIN NO.	PIN NAME	I/O	FUNCTION
A1	VCCQ		1.8V Power Supply. Connect to 1.8V is needed
A2	VCC		Power Supply
A3	CLK	I	Serial Clock Input
B1	DI(IO0)	I/O	Data Input (Data Input Output 0)(1)
B2	VSS		Ground
B3	/HOLD (IO3)	I/O	Hold or Reset Input (Data Input Output 3)
B4	/BUSY	O	/BUSY Output(3)
C2	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)
C3	DO (IO1)	I/O	Data Output (Data Input Output 1)
C4	/CS	I	Chip Select Input
Multiple	NC		No connection

Notes:
1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions (factory default for Quad Enabled part numbers with ordering option “IQ”).
3. The /BUSY pin is a dedicated hardware pin. If the function is not used, this pin can be left floating.

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The 25Q64PW supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and the /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-c for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6 Busy PIN (/BUSY)

For the TFBGA/WLCSP/KGD package, W25Q64PW provides a dedicated /BUSY pin. The /BUSY pin is an asynchronous Ready/BUSY# signal. /BUSY pin has an open drain and an internally pulled up driver. /CS pin does not need to be asserted (device selected) to get the Ready/Busy# status. When /BUSY pin is low, the device is busy with internal program, erase, or write operation. When the /BUSY pin is high, the device is not performing any internal program, erase, or write operation.

5. BLOCK DIAGRAM

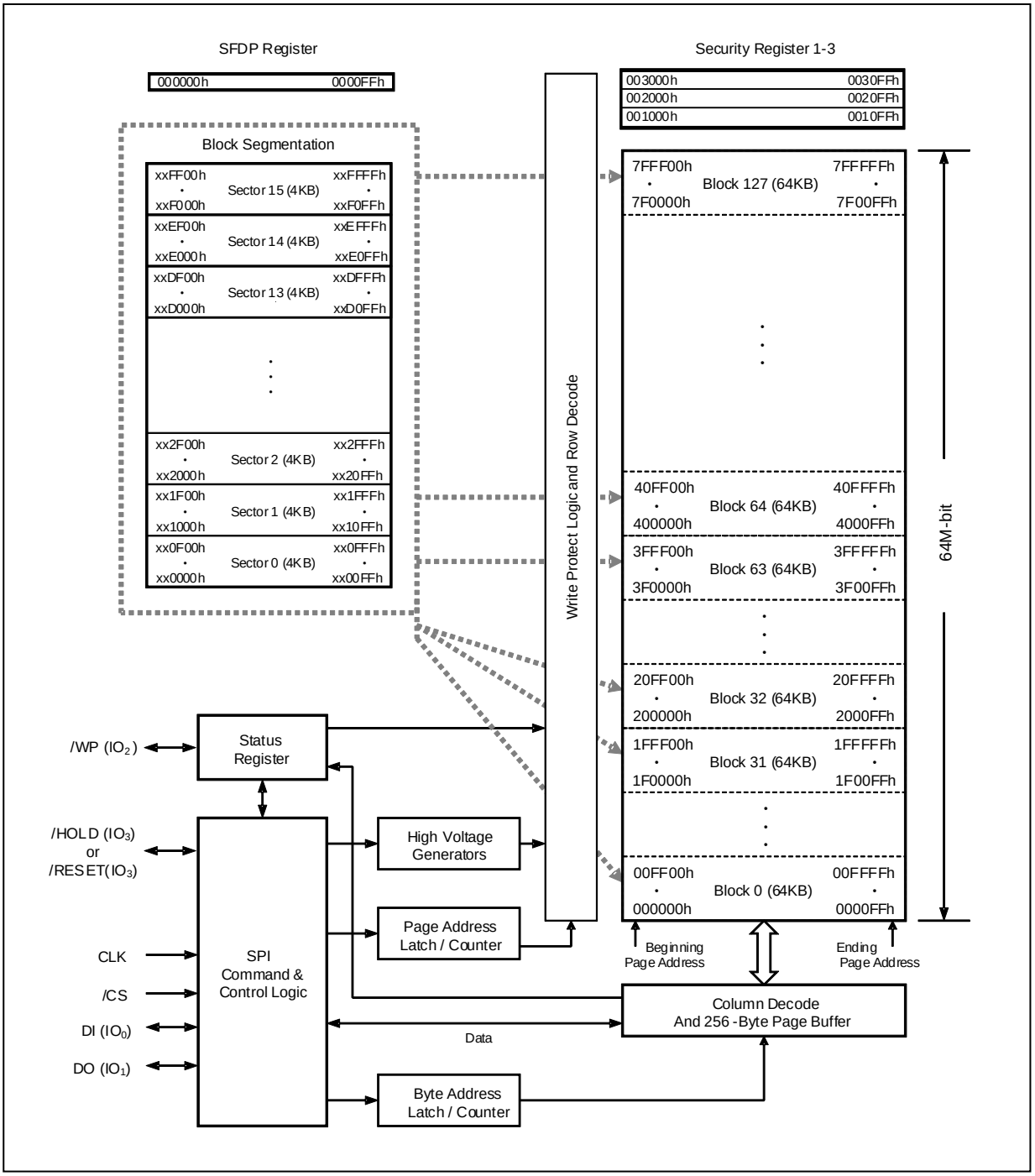


Figure 2. W25Q64PW Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1 Standard SPI Instructions

The W25Q64PW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.2 Dual SPI Instructions

The W25Q64PW supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.3 Quad SPI Instructions

The W25Q64PW supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. When using Quad SPI instructions, the DI and DO pins become bidirectional IO0 and IO1, with the additional I/O pins: IO2, IO3.

6.4 Software Reset

The W25Q64PW can be reset to the initial power-on state by a software Reset sequence. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset.

6.5 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q64PW provides several means to protect the data from inadvertent writing.

6.5.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * **Note**: This feature is available upon special flow. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q64PW will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 58). While reset, all operations are disabled, and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, TB, BP [2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

6.6 ECC Operation

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device lifetime operation and improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In W25Q64PW, the ECC calculation is done per aligned 16-byte memory address range partition (LSB A[3:0] = 0000b to 1111b) from the lowest address (00000000h) to the highest memory address (07FFFFFh). Every byte up to 16-byte memory data being programmed in the aligned 16-byte memory address array is checked by the internal ECC engine using Single Error Correction (SEC). Using 16-Byte ECC data granularity, ECC calculation latency time is minimized, while preserving the highest level of data integrity.

The W25Q64PW device has a ECC register, the ECC Status Register a, which controls the ECC settings and monitors the ECC event. The ECC Status Register has Single Error Correction (SEC), and ECC On/Off (ECCO) bits to monitor the ECC events.

The default value of all memory data is FFh (Erased) when the device is shipped from the factory. A “Page Program (02h or 12h)” or a “Quad Page Program (32h or 34h)” command can be used to program the user data into the memory array. ECC calculation is performed during the internal programming operation and the results are stored in the redundancy or spare area of the memory array. Error correction codes are calculated and stored based per 16-byte aligned address boundaries from LSB address A[3:0] = 0000b to 1111b and applicable across the full memory. Programming over previously programmed array are also tracked and monitored per aligned 16-byte memory. Every aligned 16-byte memory should be only programmed once with one byte up to 16 bytes of data, so ECC functionality (ECC On status or flag) will be maintained. If any of the aligned 16-byte memory is programmed more than once, the ECC functionality of those affected (targeted) 16-byte aligned memories will automatically be turned off (ECC Off status or flag) on read operations. Programming more than once on the same location from a single bit alteration up to the aligned 16-byte segment is accepted except the ECC functionality will automatically be turned off (ECC Off status or flag) during memory readings. ECC On/Off status is shown by ECC On/Off (ECCO) status bit of the ECC Status Register.

When ECC is active on an aligned 16-byte memory, read memory access to this address location is performed with the aid of the internal ECC engine which will check the ECC results stored in the spare area and apply necessary error correction or error detection to the memory array data being read out. The Single Error Correction (SEC) Bit in the ECC Status Register provides ECC status after the last Read operation to determine if the data read out has any errors or not. A Read operation can start from any byte address and continue through the entire memory array, it is not necessary to align the 16-Byte granularity boundary address to start a Read command. When ECC is inactive (disabled) on an aligned 16-byte memory, during read memory operations, read access will be directly to the memory array location without any internal ECC check for error correction or detection. Please contact Winbond for Application Note.

7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q64PW. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enable or disable, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, and output driver strength. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRL), the Write Enable instruction, and during Standard/Dual SPI operations.

7.1 Status Registers

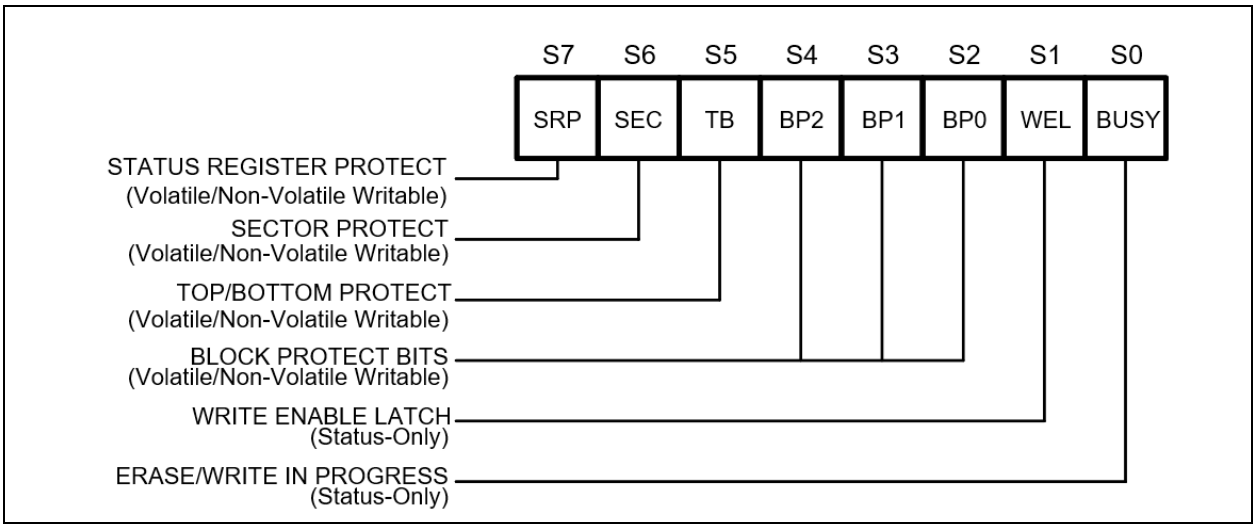


Figure 4a. Status Register-1

7.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP/SRL and WEL bits.

7.1.5 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, the previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.7 Status Register Protect (SRP, SRL) – *Volatile/Non-Volatile Writable*

Three Status and Configuration Registers are provided for W25Q64PW. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, and output driver strength, The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, output driver. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

SRL	SRP	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	X	X	One Time Program(2)	Status Register is permanently protected and cannot be written to. (**enabled by adding prefix command AAh, 55h)**

Note:

1. When SRL =1 , a power-down, power-up cycle will change SRL =0 state.
2. Please contact Winbond for details regarding the special instruction sequence.

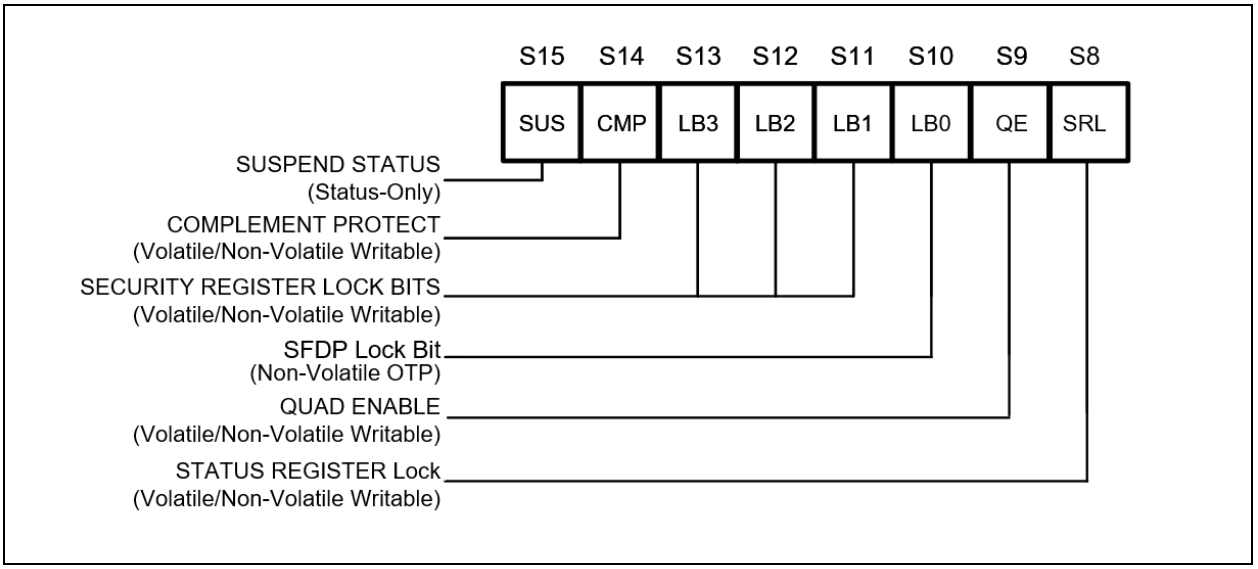


Figure 4b. Status Register-2

7.1.8 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9 Security Register Lock Bits (LB3, LB2, LB1, LB0) –*Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1, LB0) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11, S10) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-0 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

The default state of LB0 is 1, SFDP Register is locked.

7.1.10 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options "IM" & "IJ"), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option "IQ" & "IH"), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

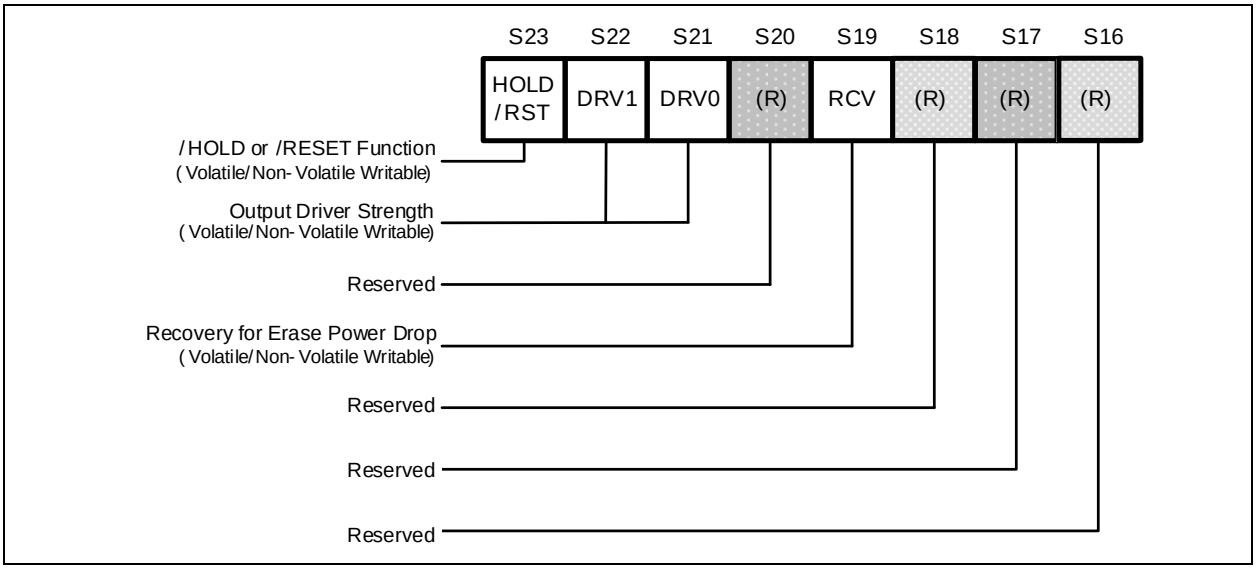


Figure 4c. Status Register-3

7.1.11 Recovery for Erase while power drop bit (RCV) - Volatile/Non-Volatile Writable

The Recovery for Erase while Power Drop Bit (RCV) is a non-volatile read/write bit located in the status register (S19). To enable this function, set S19 to 1 (enable). The default value is 0 (disable).

With conventional devices, there is a possibility that the erase operation may not be completed if a power drop occurs during the process. The RCV feature in W25Q64PW scans entire memory array whether a power drop has occurred before the completion of the erase operation after Flash power on. If the device detects an incomplete erase operation due to a power drop, it performs an internal recovery operation to prevent system data influence in non-erase areas. However, the areas affected by the incomplete erase will still require an additional erase before they can be used.

After enabling this feature, W25Q64PW automatically starts the Recovery for Erase while power drop for each power on. There is an extra tRCV time consumed after tVSL, which is mentioned in chapter “AC Electrical Characteristics”. During progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Recovery for Erase while the power drop cycle and 0 when the cycle is finished and ready to accept other instructions again.

7.1.12 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Resistor
0, 0	25-ohm
0, 1	33-ohm
1, 0	50-ohm(default)
1, 1	100-ohm

7.1.13 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

7.1.14 Status Register Memory Protection (CMP = 0)

STATUS REGISTER[1]					W25Q64PW (64M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 and 127	7E0000h – 7FFFFFh	128KB	Upper 1/64
0	0	0	1	0	124 thru 127	7C0000h – 7FFFFFh	256KB	Upper 1/32
0	0	0	1	1	120 thru 127	780000h – 7FFFFFh	512KB	Upper 1/16
0	0	1	0	0	112 thru 127	700000h – 7FFFFFh	1MB	Upper 1/8
0	0	1	0	1	96 thru 127	600000h – 7FFFFFh	2MB	Upper 1/4
0	0	1	1	0	64 thru 127	400000h – 7FFFFFh	4MB	Upper 1/2
0	1	0	0	1	0 and 1	000000h – 01FFFFh	128KB	Lower 1/64
0	1	0	1	0	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/32
0	1	0	1	1	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/16
0	1	1	0	0	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/8
0	1	1	0	1	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/4
0	1	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
X	X	1	1	1	0 thru 127	000000h – 7FFFFFh	8MB	ALL
1	0	0	0	1	127	7FF000h – 7FFFFFh	4KB	U – 1/2048
1	0	0	1	0	127	7FE000h – 7FFFFFh	8KB	U – 1/1024
1	0	0	1	1	127	7FC000h – 7FFFFFh	16KB	U – 1/512
1	0	1	0	X	127	7F8000h – 7FFFFFh	32KB	U – 1/256
1	1	0	0	1	0	000000h – 000FFFh	4KB	L – 1/2048
1	1	0	1	0	0	000000h – 001FFFh	8KB	L – 1/1024
1	1	0	1	1	0	000000h – 003FFFh	16KB	L – 1/512
1	1	1	0	X	0	000000h – 007FFFh	32KB	L – 1/256

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.15 Status Register Memory Protection (CMP = 1)

STATUS REGISTER[1]					W25Q64PW (64M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	0 thru 127	000000h – 7FFFFFh	8MB	ALL
0	0	0	0	1	0 thru 125	000000h – 7DFFFFh	8,064KB	Lower 63/64
0	0	0	1	0	0 thru 123	000000h – 7BFFFFh	7,936KB	Lower 31/32
0	0	0	1	1	0 thru 119	000000h – 77FFFFh	7,680KB	Lower 15/16
0	0	1	0	0	0 thru 111	000000h – 6FFFFFh	7MB	Lower 7/8
0	0	1	0	1	0 thru 95	000000h – 5FFFFFh	6MB	Lower 3/4
0	0	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
0	1	0	0	1	2 thru 127	020000h – 7FFFFFh	8,064KB	Upper 63/64
0	1	0	1	0	4 thru 127	040000h – 7FFFFFh	7,936KB	Upper 31/32
0	1	0	1	1	8 thru 127	080000h – 7FFFFFh	7,680KB	Upper 15/16
0	1	1	0	0	16 thru 127	100000h – 7FFFFFh	7MB	Upper 7/8
0	1	1	0	1	32 thru 127	200000h – 7FFFFFh	6MB	Upper 3/4
0	1	1	1	0	64 thru 127	400000h – 7FFFFFh	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 127	000000h – 7FEFFFh	8,188KB	L – 2047/2048
1	0	0	1	0	0 thru 127	000000h – 7FDFFFh	8,184KB	L – 1023/1024
1	0	0	1	1	0 thru 127	000000h – 7FBFFFh	8,176KB	L – 511/512
1	0	1	0	X	0 thru 127	000000h – 7F7FFFh	8,160KB	L – 255/256
1	1	0	0	1	0 thru 127	001000h – 7FFFFFh	8,188KB	L – 2047/2048
1	1	0	1	0	0 thru 127	002000h – 7FFFFFh	8,184KB	L – 1023/1024
1	1	0	1	1	0 thru 127	004000h – 7FFFFFh	8,176KB	L – 511/512
1	1	1	0	X	0 thru 127	008000h – 7FFFFFh	8,160KB	L – 255/256

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.2 Error Code Correction (ECC) Registers

7.2.1 ECC Status Register – Volatile Writable and Readable

The W25Q64PW provides a volatile ECC Status Register which consists of the configuration bits for advanced features for error correction, advance flash memory cell abnormality detection. Upon power up or after the execution of a Software Reset, the ECC Status Register bits will be reset to their default value – SEC and ECCO bits default value is 0 and ECC bit default value is 1.

The remaining ECC Register bits namely Single Error Correction bit (ER7), and ECC On/Off bit (ER0) are read status only bits. The Read ECC Status Register instruction (25h) is used to read the ECC Status Register.

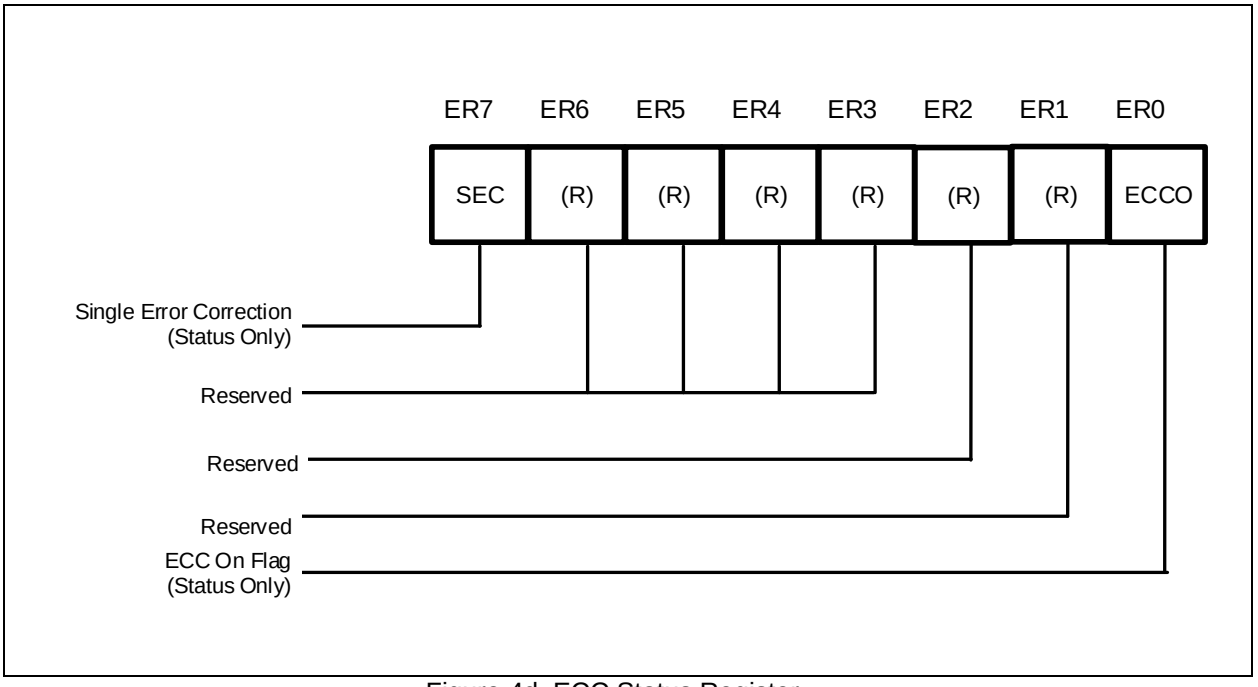


Figure 4d. ECC Status Register

7.2.1.1. ECC Status Bits (SEC) – *Status Only*

SEC (Single Error Correction) Status Bit is used to show the ECC results for the last Read operation. SEC bit will be cleared to 0 once the device accepts a new Read command.

SEC	Definitions
0	No ECC events in all aligned 16-Byte granularities.
1	SEC events in single or multiple 16-Byte granularities, data is OK to use (unless it's odd bits error in 16-Byte granularity).

7.2.1.2. ECC On/Off (ECCO) – Status Only

The ECC On/Off bit is a status indicator if the ECC function is active or inactive (disabled) on any of the 16-byte aligned memory from the last memory read operation. When ECC On/Off bit is '0' (default), the ECC function is active in all the 16-byte aligned memory from the last memory read operation. When ECC On/Off bit is '1', the ECC function has been turned off (disabled) in one of the 16-byte aligned memory from the last memory read operation. The ECC On/Off bit is automatically turned off (disabled) if any of the aligned 16-byte memory address ranges are programmed more than once before an erase operation.

7.3 Page Buffer

In Standard SPI mode, one of the new powerful features of the W25Q64PW is the integrated Serial SRAM buffer and its associated Program Buffer. Together, the 256-byte Serial SRAM provides usable SRAM storage. The SRAM can be used in conjunction with the Flash memory or independently. The main purpose of the Serial SRAM is to serve as the primary buffer for data to be written into the Serial Flash memory array. In case of need, it can help to transform random Byte Write to page Program Buffer.

Using the Write Buffer instruction, data is first shifted into the SRAM from the SPI bus. When the instruction sequence has been completed, the entire 256-bytes is transferred to the Program Buffer. The Program Buffer supports the array during the Erase/Write cycle (tWP), freeing the SRAM to accept new data. This double-buffering scheme increases erase/write transfer rates and can eliminate the need for external RAM buffers (Figure 4e). The SRAM is fully byte-addressable. Thus, the entire 256-bytes, a single byte, or a sequence of bytes can be read from or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The Transfer Sector to SRAM instruction allows the con- tents of a specified sector of Flash memory to be moved to the SRAM. This can be useful when only a portion of a sector needs to be altered. In this case the sector is first transferred to the SRAM, where modifications are made using the Write to SRAM instruction. Once complete, a Transfer SRAM to Sector instruction is used to update the sector.

Page Buffer control instruction as below:

- Clear Buffer(81h): Reset all the bit in the Page Buffer becomes '1'.
- Write Buffer(82h): Write the data into the Page Buffer, from the 1st byte to the 256th byte.
- Read Buffer(83h): Read out the data from Page Buffer.
- Program Buffer(8Ah): Write the Page Buffer data into the specified Flash Physical memory page.
- Load Buffer(8Bh): Read the data from the specified Flash Physical memory page into the Page Buffer.

Upon power off or the execution of a reset, all bits in the Page Buffer become '1', effectively clearing the buffer. After Release Power-down(ABh), a clear buffer command must be issued."

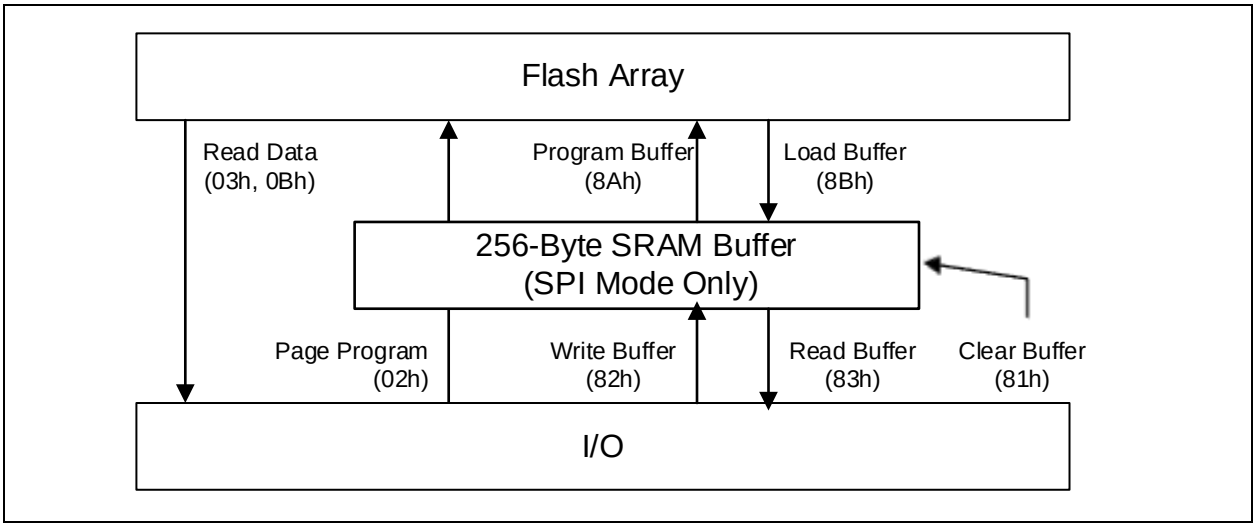


Figure.4e Serial Flash Buffer Mode

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q64PW consists of 48 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 6 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q64PW-Q/H	16h	6017h
W25Q64PW-M/J(1)	16h	8017h

Note: For DTR, QPI supporting, please refer to W25Q64PW-M DTR datasheet.

8.1.2 Instruction Set Table 1 (Standard SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down	**ABh**						
Read ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Chip Erase	**C7h/60h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1	**01h**	(S7-S0)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-S16)(2)					
Write Status Register-3	**11h**	(S23-S16)					
Read ECC Status Register	**25h**	(ER7-ER0) (2)					
Read SFDP Register	**5Ah**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register(4)	**44h**	A23-A16	A15-A8	A7-A0			
Program Security Register(4)	**42h**	A23-A16	A15-A8	A7-A0	D7-D0(3)		
Read Security Register(4)	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Set Read Parameters	**C0h**	P7-P0					
Enable Reset	**66h**						
Reset Device	**99h**						
Recovery for Erase	**A8h**						

8.1.3 Instruction Set Table 2 (Dual/Quad SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)		
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual I/O	**BBh**	A23-A16(6)	A15-A8(6)	A7-A0(6)	Dummy(11)	(D7-D0)(7)			
Mftr./Device ID Dual I/O	**92h**	A23-A16(6)	A15-A8(6)	00(6)	Dummy(11)	(MF7-MF0)	(ID7-ID0)(7)		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(10)
Number of Clock(1-4-4)	**8**	**2**(8)	**2**(8)	**2**(8)	**2**	**2**	**2**	**2**	**2**
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	00	Dummy(11)	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	Dummy(12)	(D7-D0)	
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can’t be used to program Status Register-2,.
5. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
9. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
10. Fast Read Quad I/O data output format:
    IO0 = (x, x, x, x, D4, D0, D4, D0)
    IO1 = (x, x, x, x, D5, D1, D5, D1)
    IO2 = (x, x, x, x, D6, D2, D6, D2)
    IO3 = (x, x, x, x, D7, D3, D7, D3)
11. The first dummy is M7-M0 should be set to Fxh.
12. Set Read Parameters" instruction (C0h) can set the number of dummy clocks.

8.2 Instruction Descriptions

8.2.1 Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

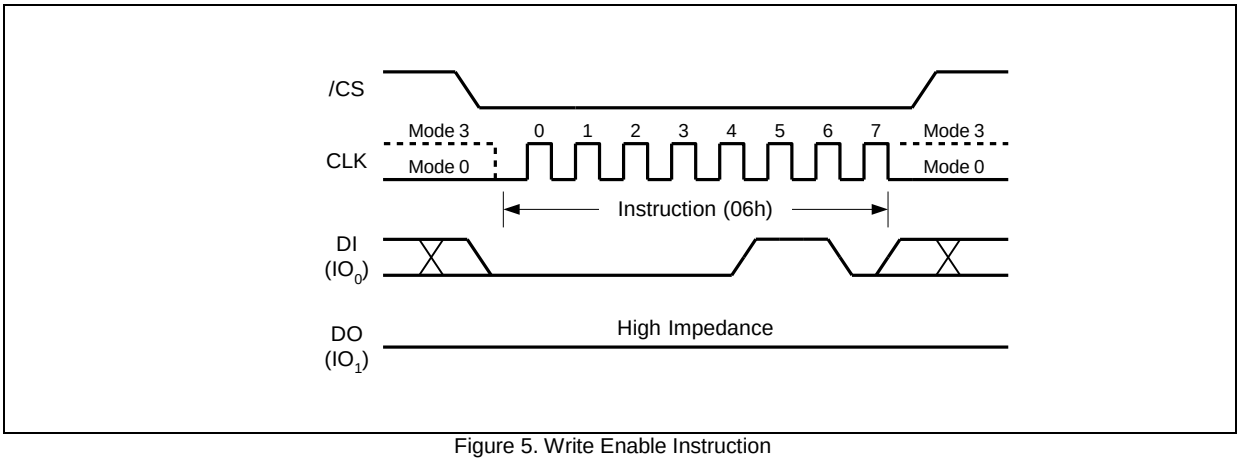


Figure 5. Write Enable Instruction

8.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 6) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

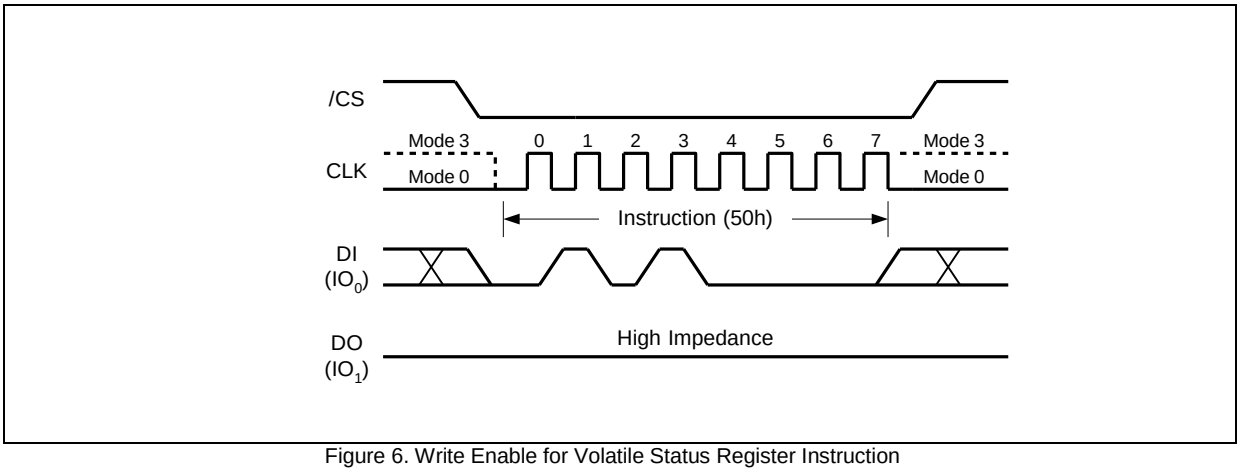


Figure 6. Write Enable for Volatile Status Register Instruction

8.2.3 Write Disable (04h)

The Write Disable instruction (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

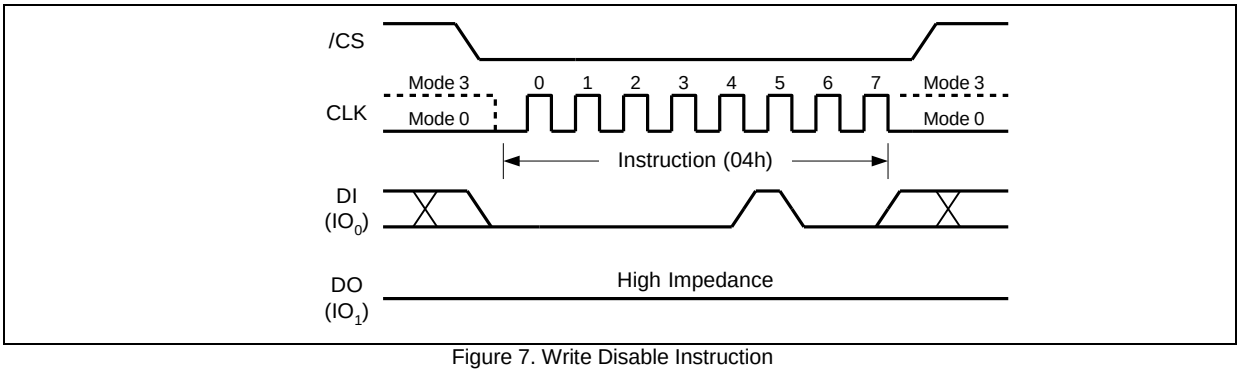


Figure 7. Write Disable Instruction

8.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 8. Refer to section 7.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 8. The instruction is completed by driving /CS high.

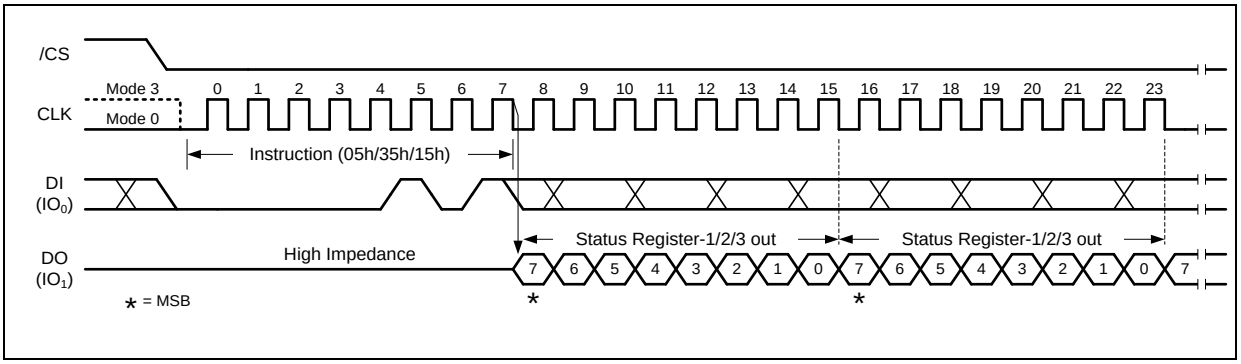


Figure 8. Read Status Register Instruction

8.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; DRV1, DRV0 in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 9a.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset instruction, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

Refer to section 7.1 for Status Register descriptions.

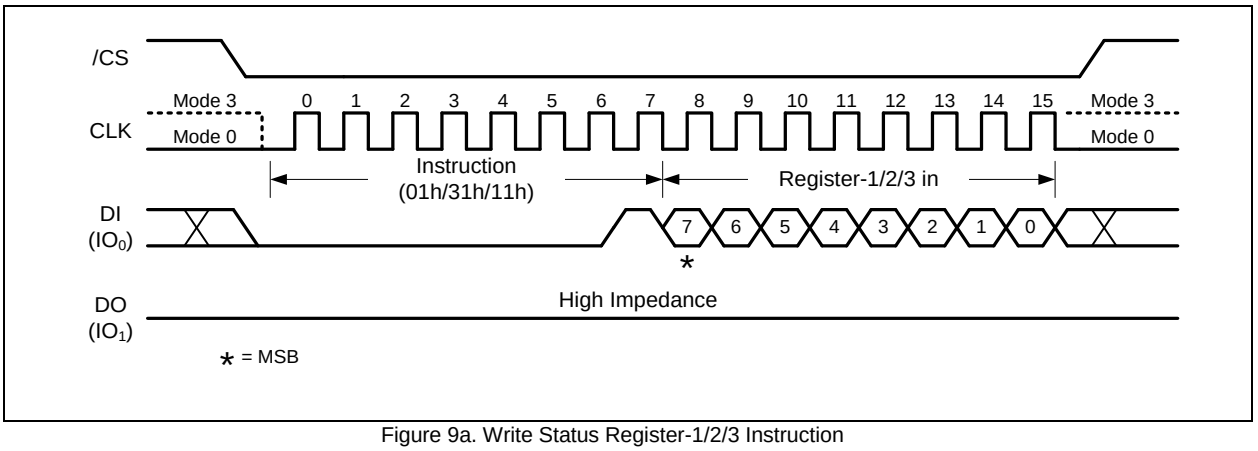


Figure 9a. Write Status Register-1/2/3 Instruction

8.2.6 Read ECC Status Register (25h)

ECC Status Register contains bits including SEC and ECC ON/OFF bits as described in Section 7.2 ” Read ECC Status Register”. The Read ECC Status Register instruction is entered by driving /CS low and shifting the instruction code “25h” into the DI pin on the rising edge of CLK. The ECC Status Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 11a. Please contact Winbond for Application Note.

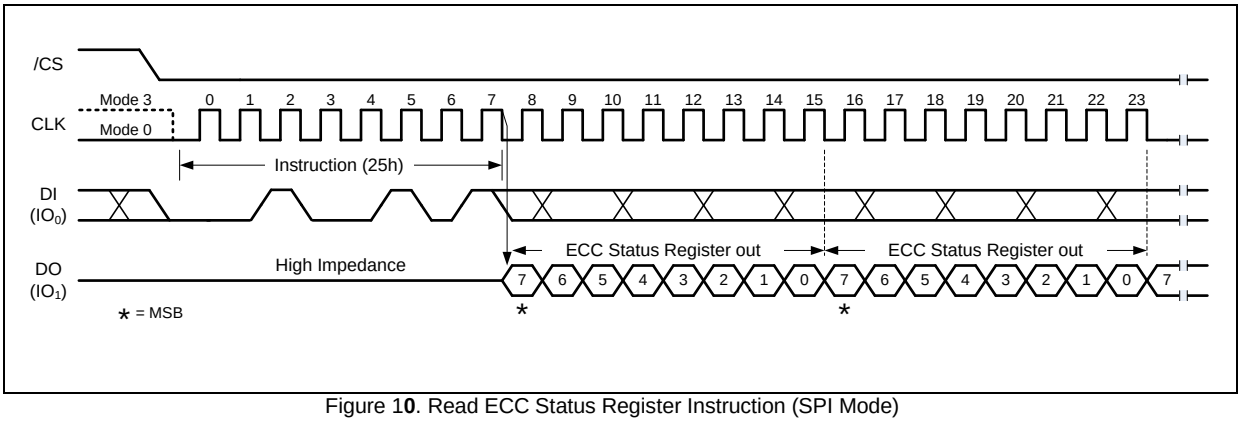


Figure 10. Read ECC Status Register Instruction (SPI Mode)

8.2.7 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

he Read Data instruction sequence is shown in Figure 11. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

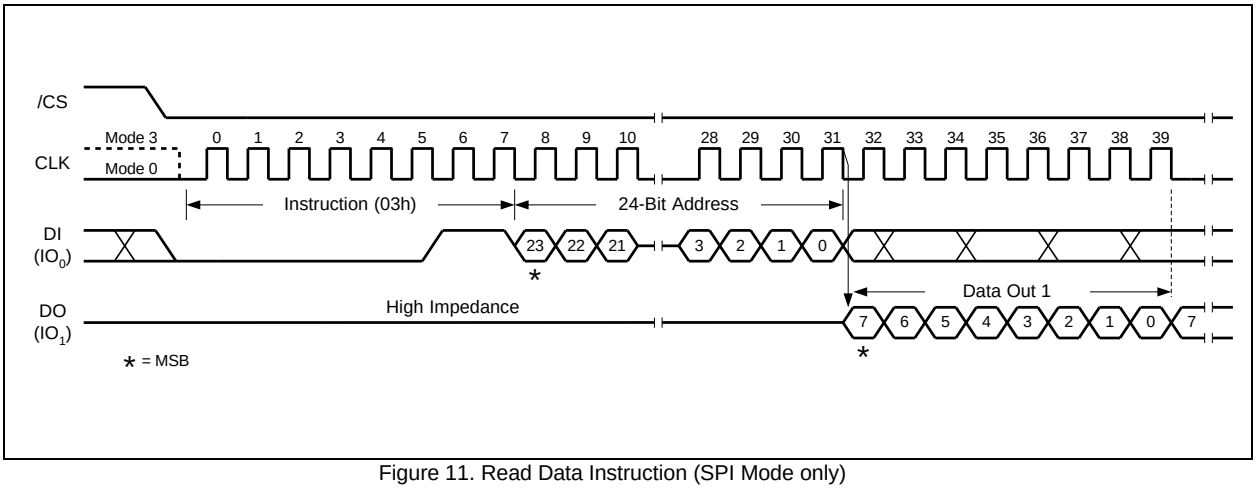


Figure 11. Read Data Instruction (SPI Mode only)

8.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 12. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

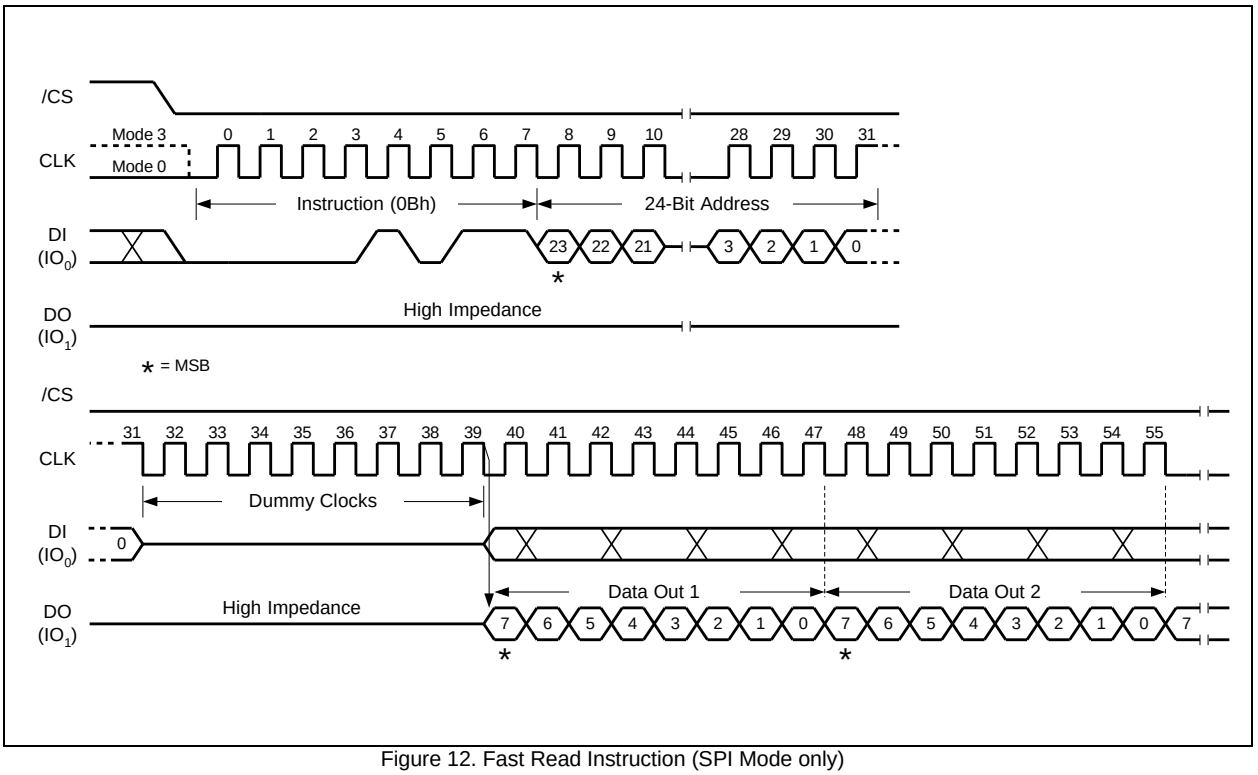


Figure 12. Fast Read Instruction (SPI Mode only)

8.2.9 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of Fr (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 13. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

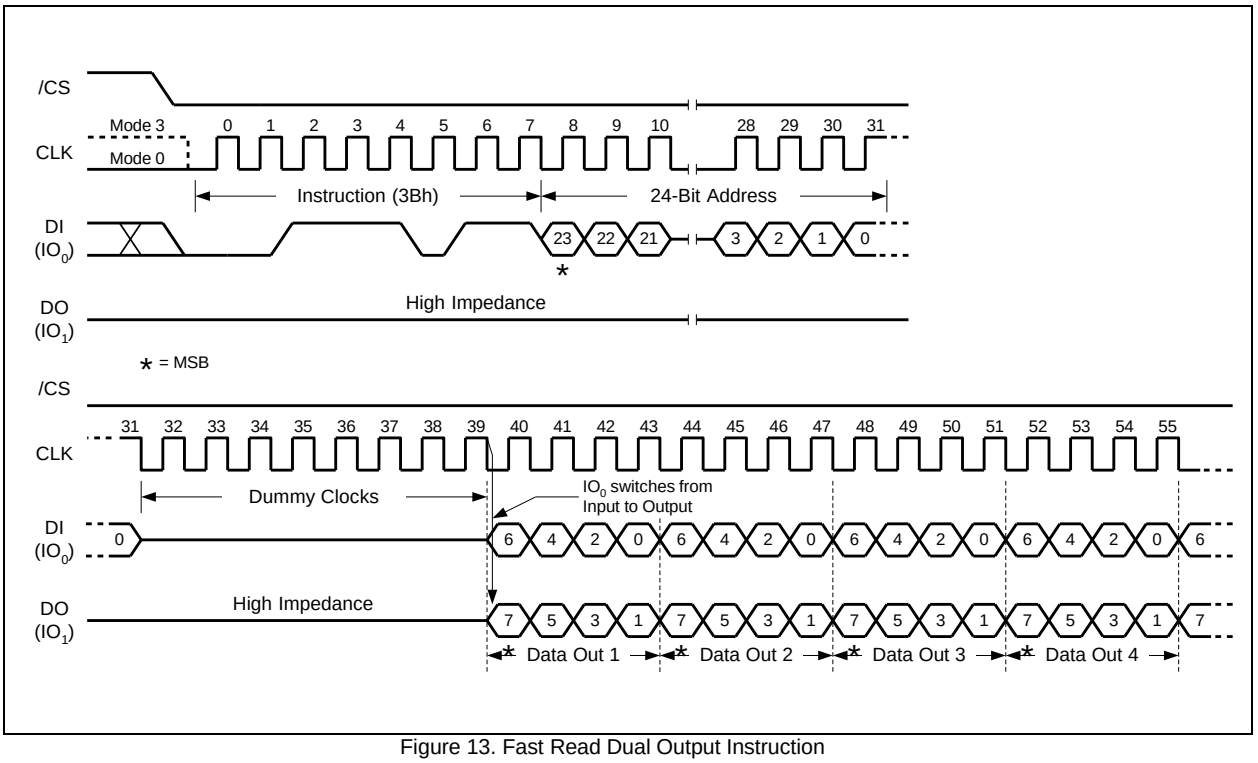


Figure 13. Fast Read Dual Output Instruction

8.2.10 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 14. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

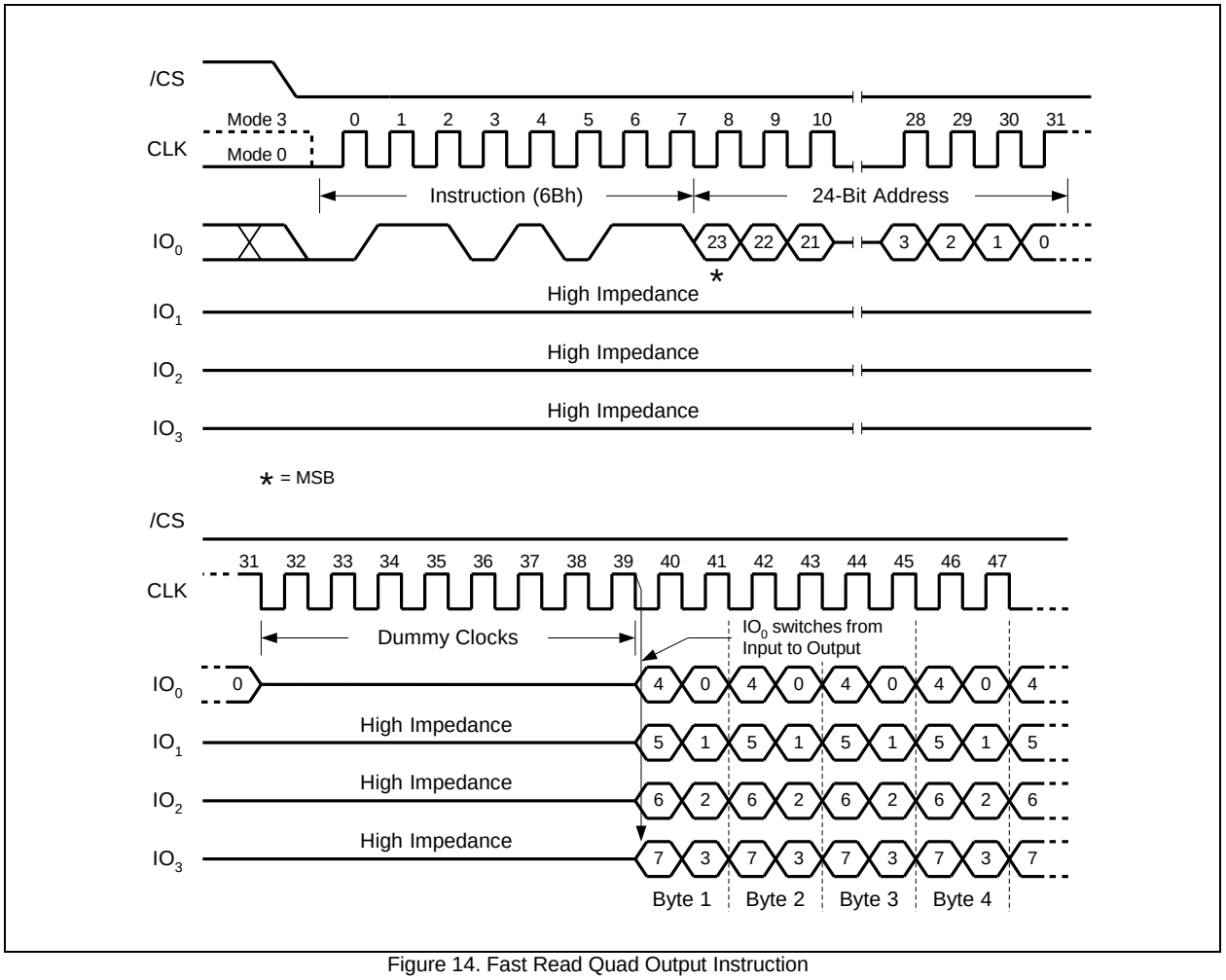


Figure 14. Fast Read Quad Output Instruction

8.2.11 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Similar to the Fast Read Dual Output (3Bh) instruction, the Fast Read Dual I/O instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding four “dummy” clocks after the 24-bit address as shown in Figure 15. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

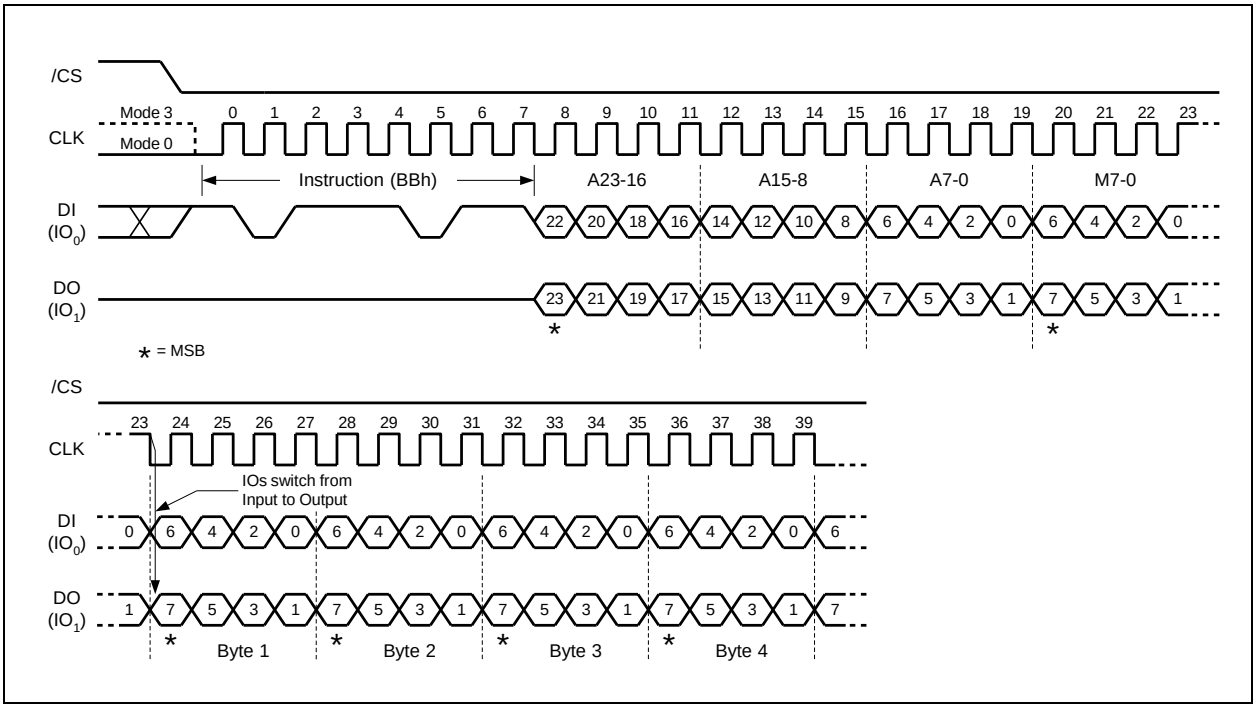


Figure 15. Fast Read Dual I/O Instruction (M7-M0 should be set to Fxh)

8.2.12 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

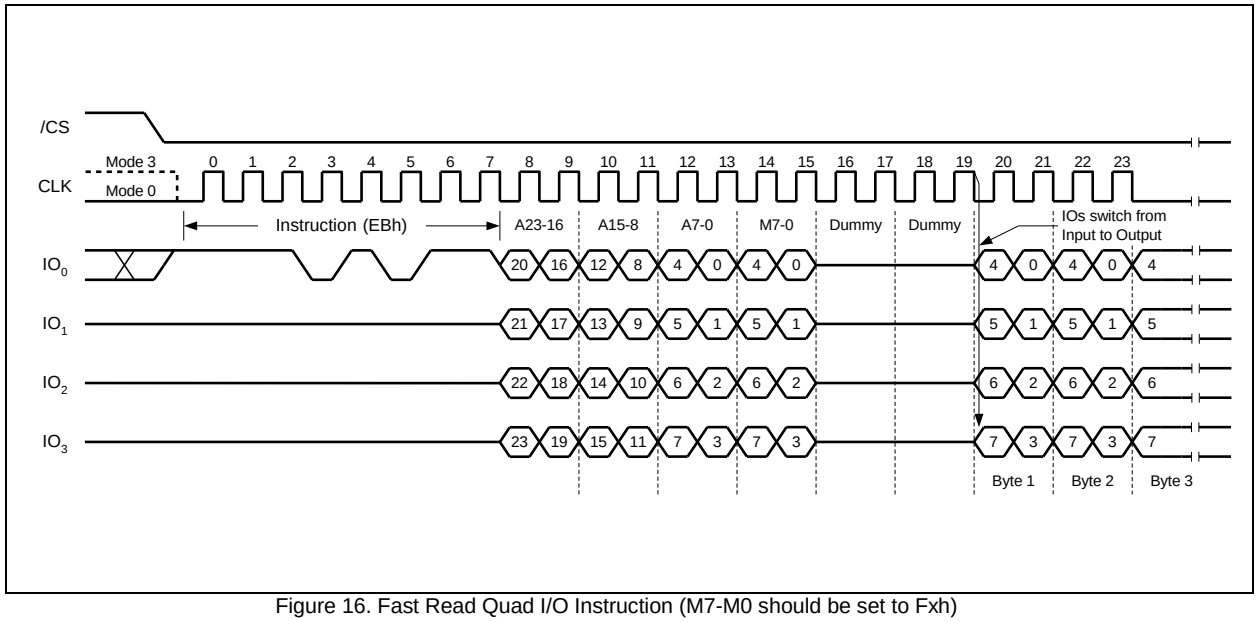


Figure 16. Fast Read Quad I/O Instruction (M7-M0 should be set to Fxh)

* "Set Read Parameters" instruction (C0h) can set the number of dummy clocks.

8.2.13 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 17. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

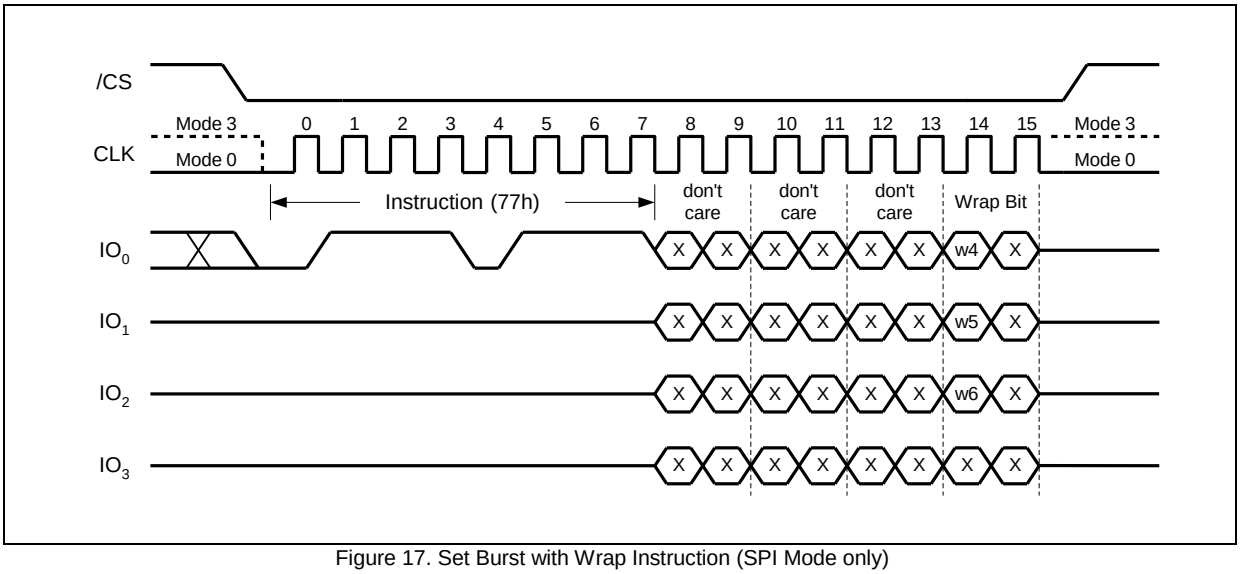


Figure 17. Set Burst with Wrap Instruction (SPI Mode only)

8.2.14 Set Read Parameters (C0h)

"Set Read Parameters (C0h)" instruction is used to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency. This is accomplished by setting the number of dummy clocks and wrap length configurations for set of selected instructions. Set Read Parameters (C0h) instruction writes to the Read Parameter Register (P[7:0]).

SPI Set Read Parameters (C0h)" instruction writes to 'Dummy Clocks' P[6:4] bits only, while it will ignore P[3:0] bits input as they are don't care in SPI mode. The Set Read Parameters instruction sequence is shown in Figure 18.

The dummy clocks for various Fast Read instructions in SPI mode are fixed, except for "Fast Read Quad I/O (EBh)" instructions. Please refer to the Instruction Tables 1 and 2 for details. "Wrap Length" for the SPI "Fast Read Quad I/O (EBh)" instruction is set by W6-4 bit with the "Set Burst with Wrap (77h)" instruction.

The default Parameter Read "Dummy Clocks" and "Wrap Length" settings for selected SPI read instructions after power up or reset are defined on the tables below. After power up or reset, Read Parameter bits are reset to 00h.

Detailed Read Parameter bits configuration are also shown below.

SPI –EB P6 P5 P4	DUMMY CLOCKS	MAXIMUM READ FREQ.
0 0 0	6(default)	133MHz
0 0 1	6	133MHz
0 1 0	6	133MHz
0 1 1	8	133MHz
1 0 0	10	133MHz
1 0 1	12	166MHz
1 1 0	14	166MHz
1 1 1	16	166MHz

Notes:

1. Default from power up

2. Required address alignment and start address for Reads: LSB A[1:0]=00b

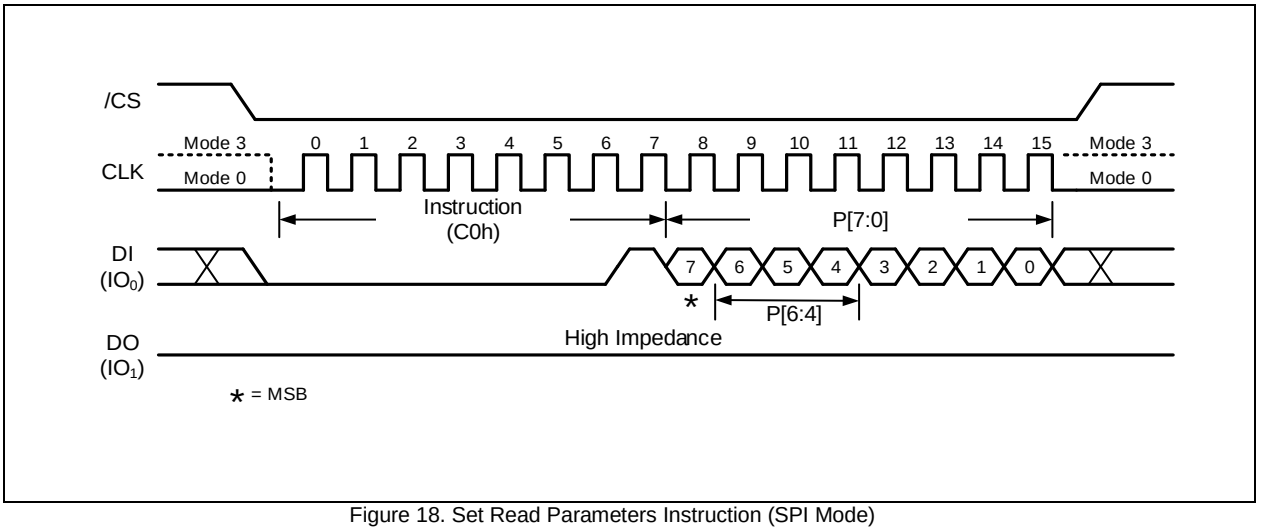


Figure 18. Set Read Parameters Instruction (SPI Mode)

8.2.15 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 19.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

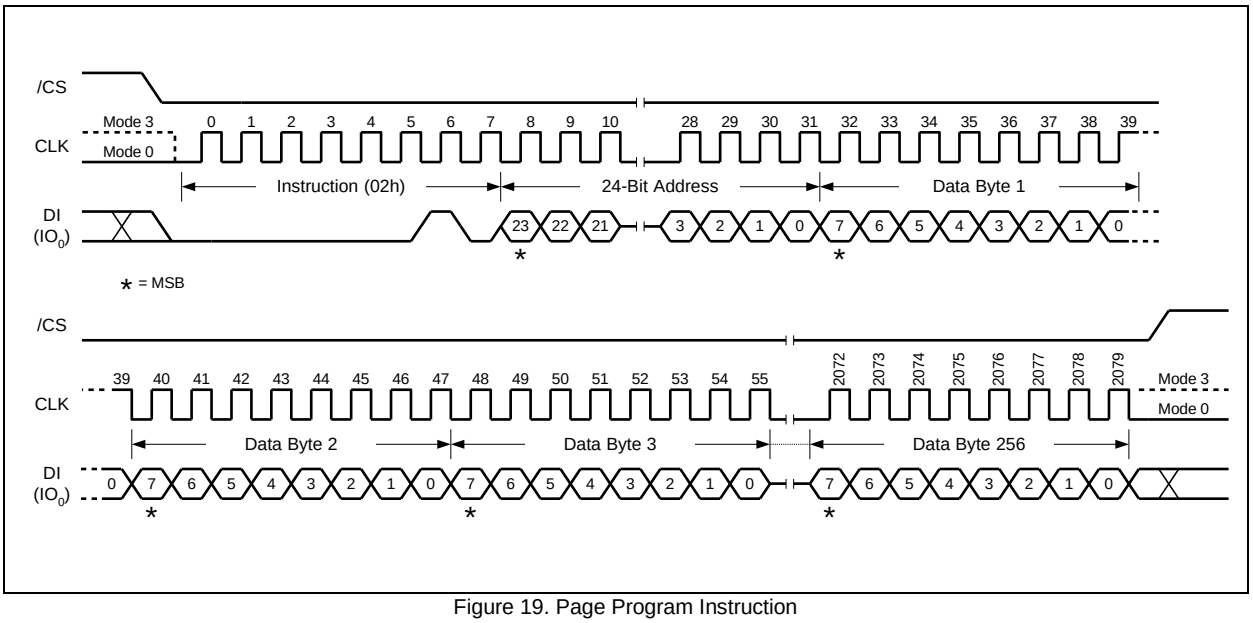


Figure 19. Page Program Instruction

8.2.16 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 20.

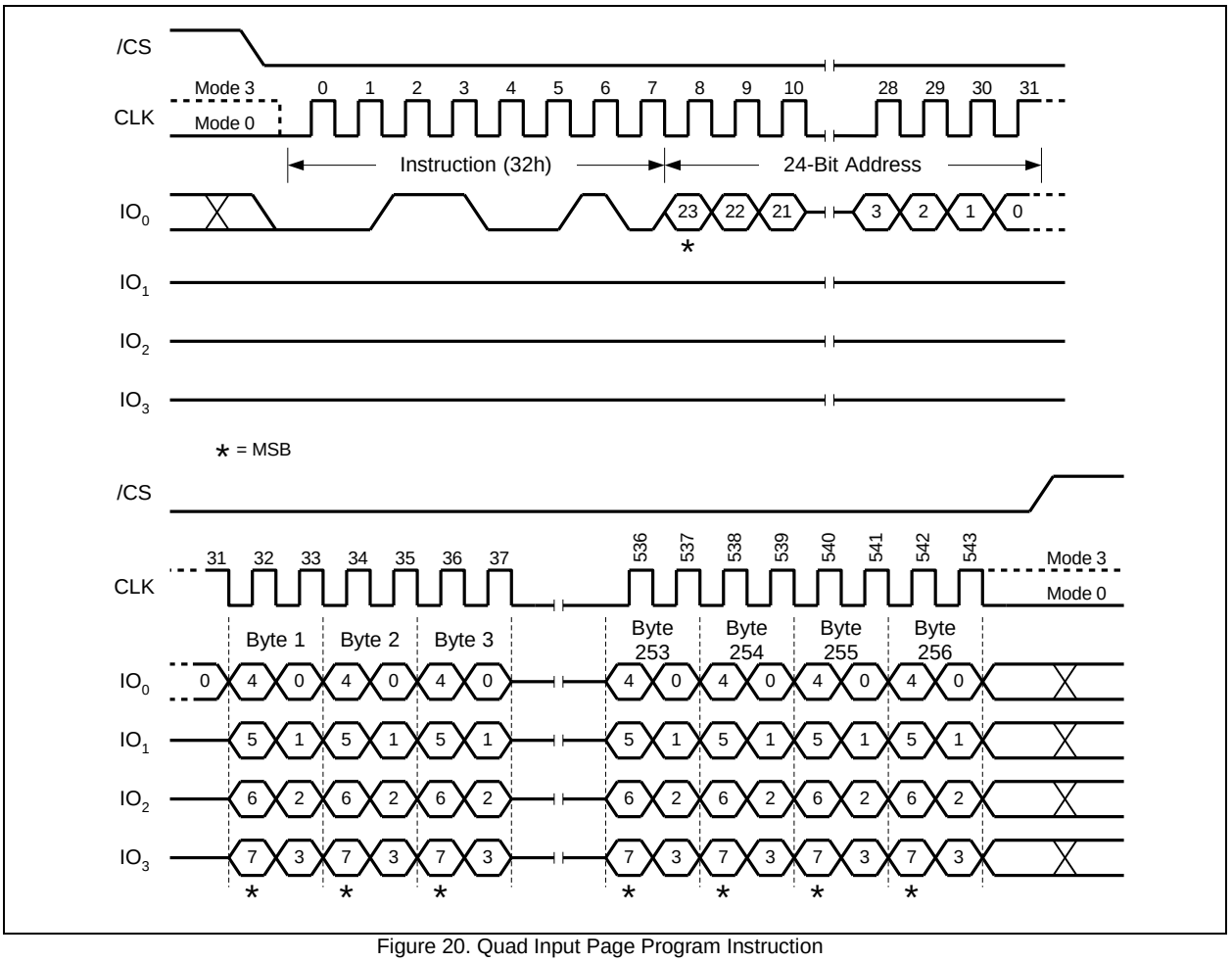


Figure 20. Quad Input Page Program Instruction

8.2.17 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 21.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

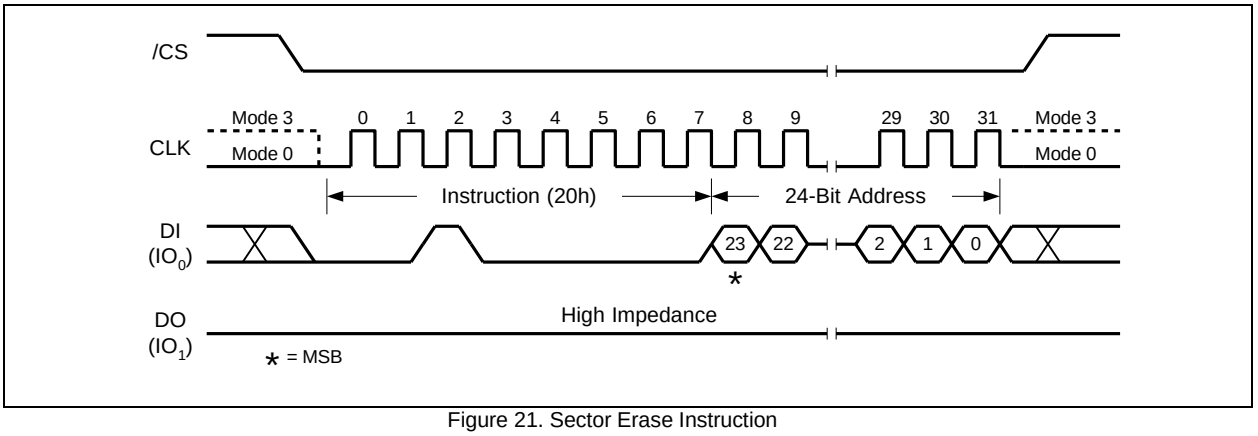


Figure 21. Sector Erase Instruction

8.2.18 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 22.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

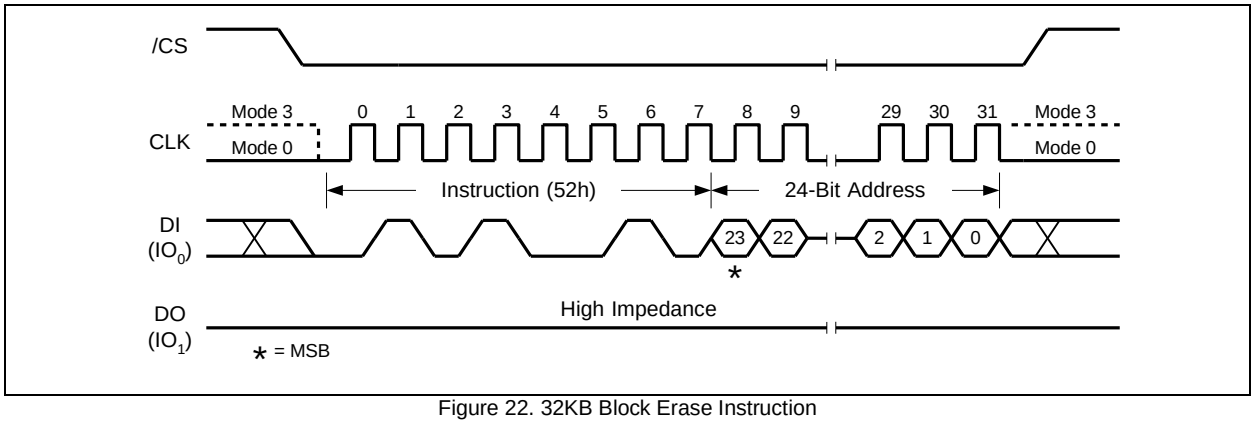


Figure 22. 32KB Block Erase Instruction

8.2.19 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 23.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

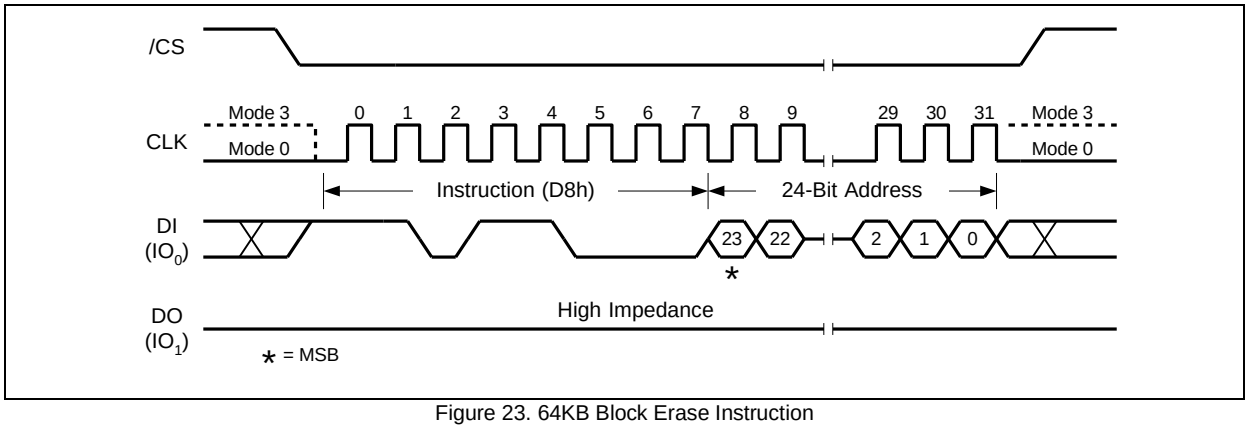


Figure 23. 64KB Block Erase Instruction

8.2.20 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 24.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

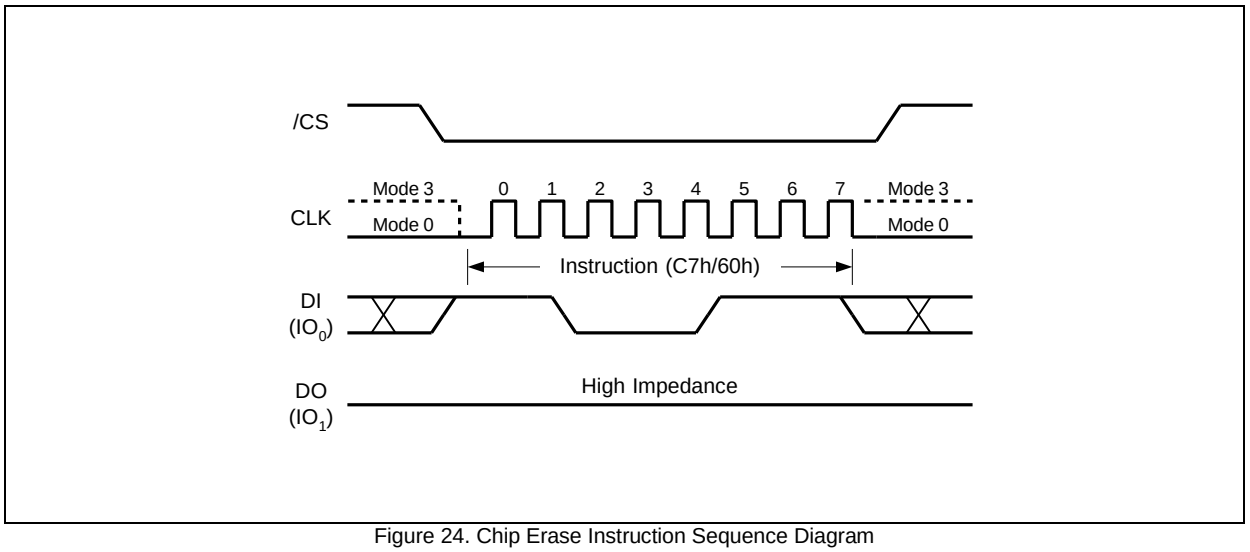


Figure 24. Chip Erase Instruction Sequence Diagram

8.2.21 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 25.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “t_{SUS}” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “t_{SUS}” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

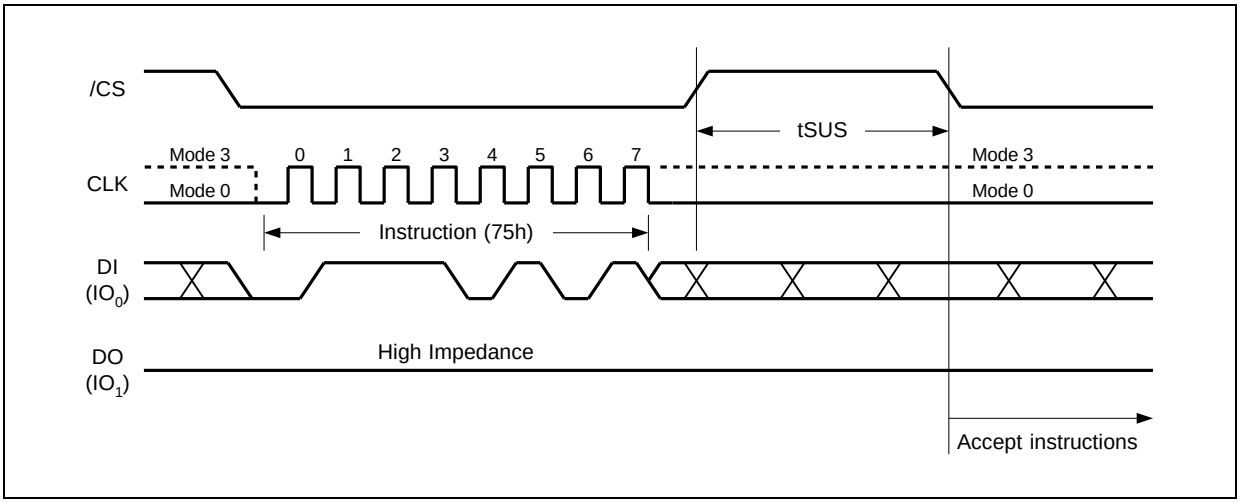


Figure 25. Erase/Program Suspend Instruction

8.2.22 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 26.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

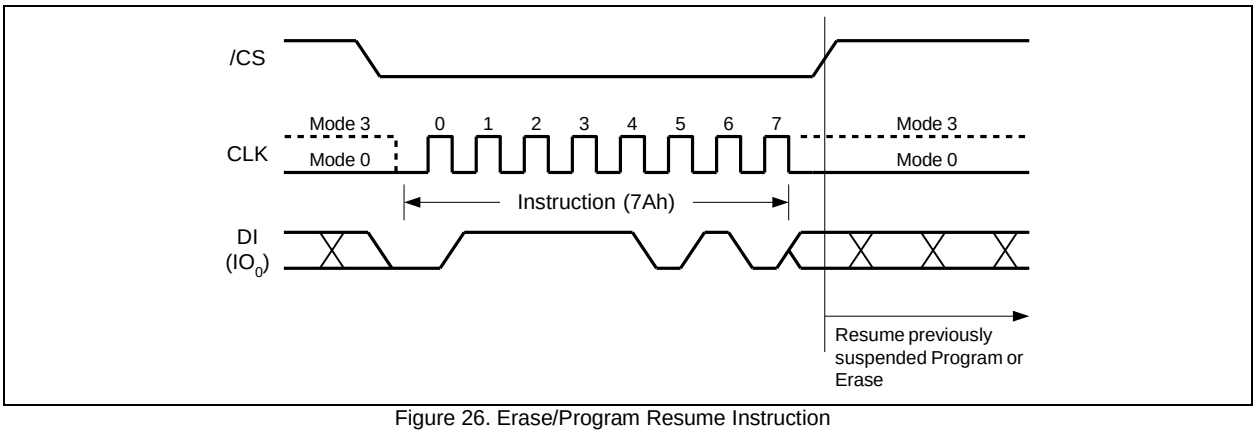


Figure 26. Erase/Program Resume Instruction

8.2.23 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 27.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release Power-down (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

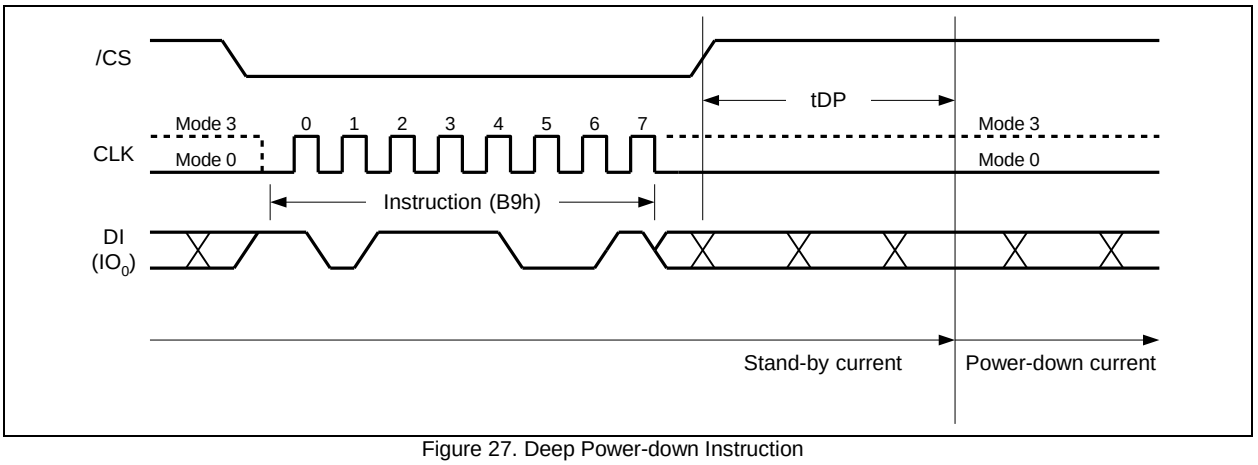


Figure 27. Deep Power-down Instruction

8.2.24 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 28a. Release from power-down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the W25Q64PW is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

If the Release from Power-down instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

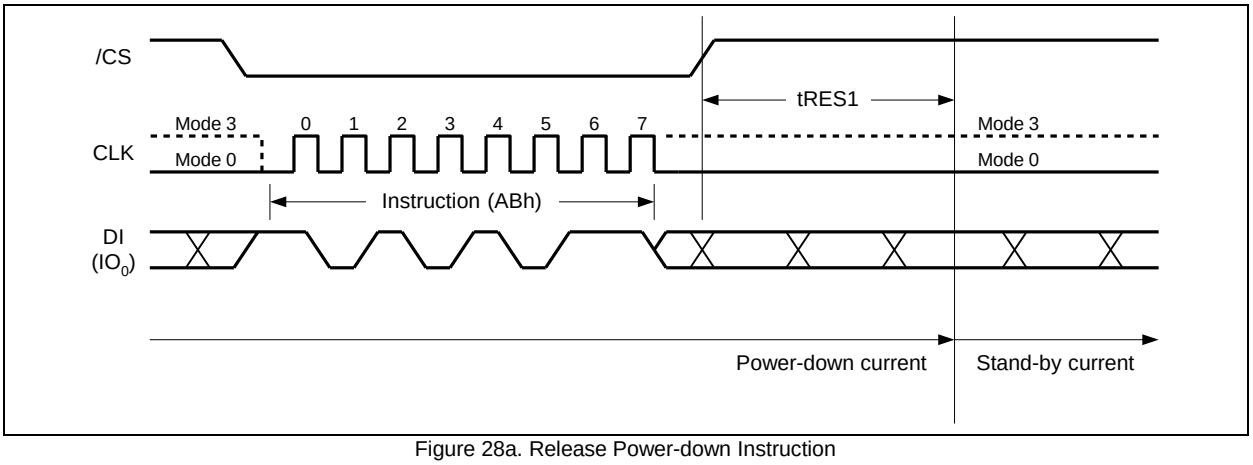


Figure 28a. Release Power-down Instruction

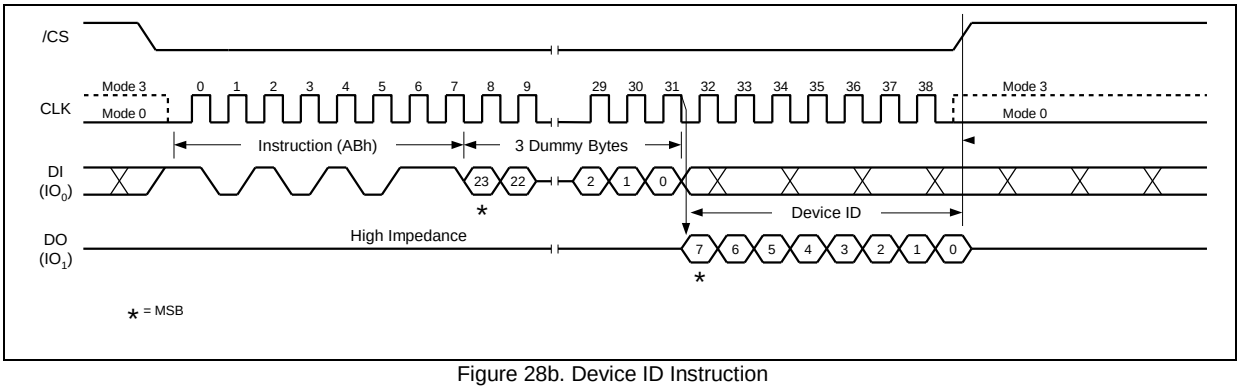


Figure 28b. Device ID Instruction

8.2.25 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 29. The Device ID values for the W25Q64PW are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

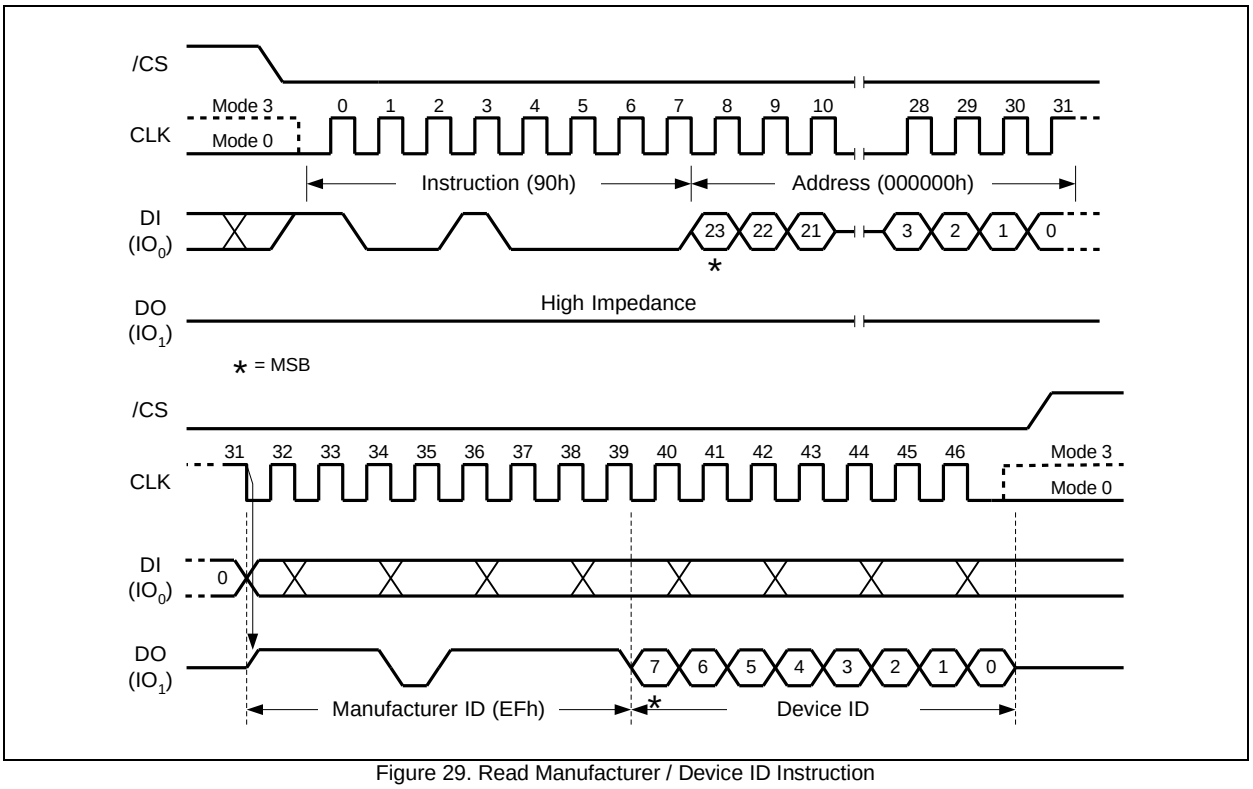


Figure 29. Read Manufacturer / Device ID Instruction

8.2.26 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 30. The Device ID values for the W25Q64PW are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

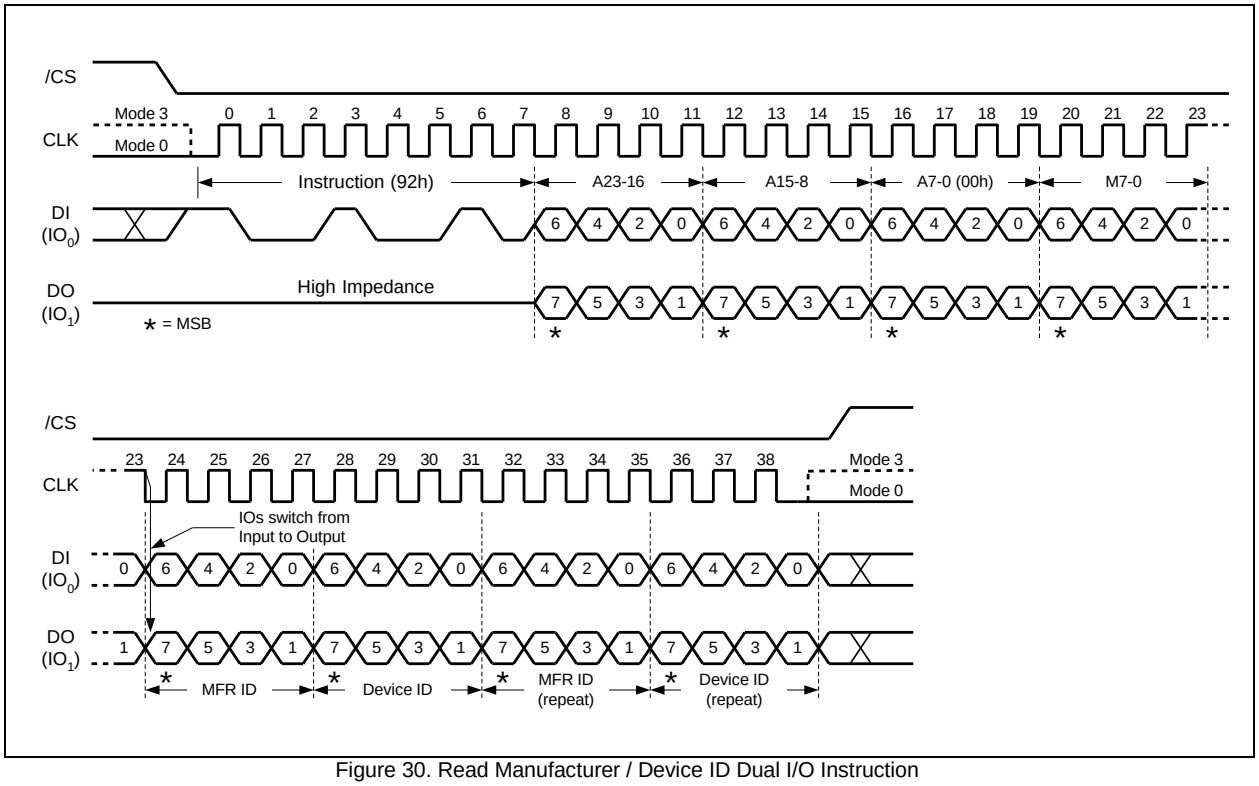


Figure 30. Read Manufacturer / Device ID Dual I/O Instruction

Note:

The bits M(7-0) must be set to Fxh o be compatible with Fast Read Dual I/O instruction.

8.2.27 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 31. The Device ID values for the W25Q64PW are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

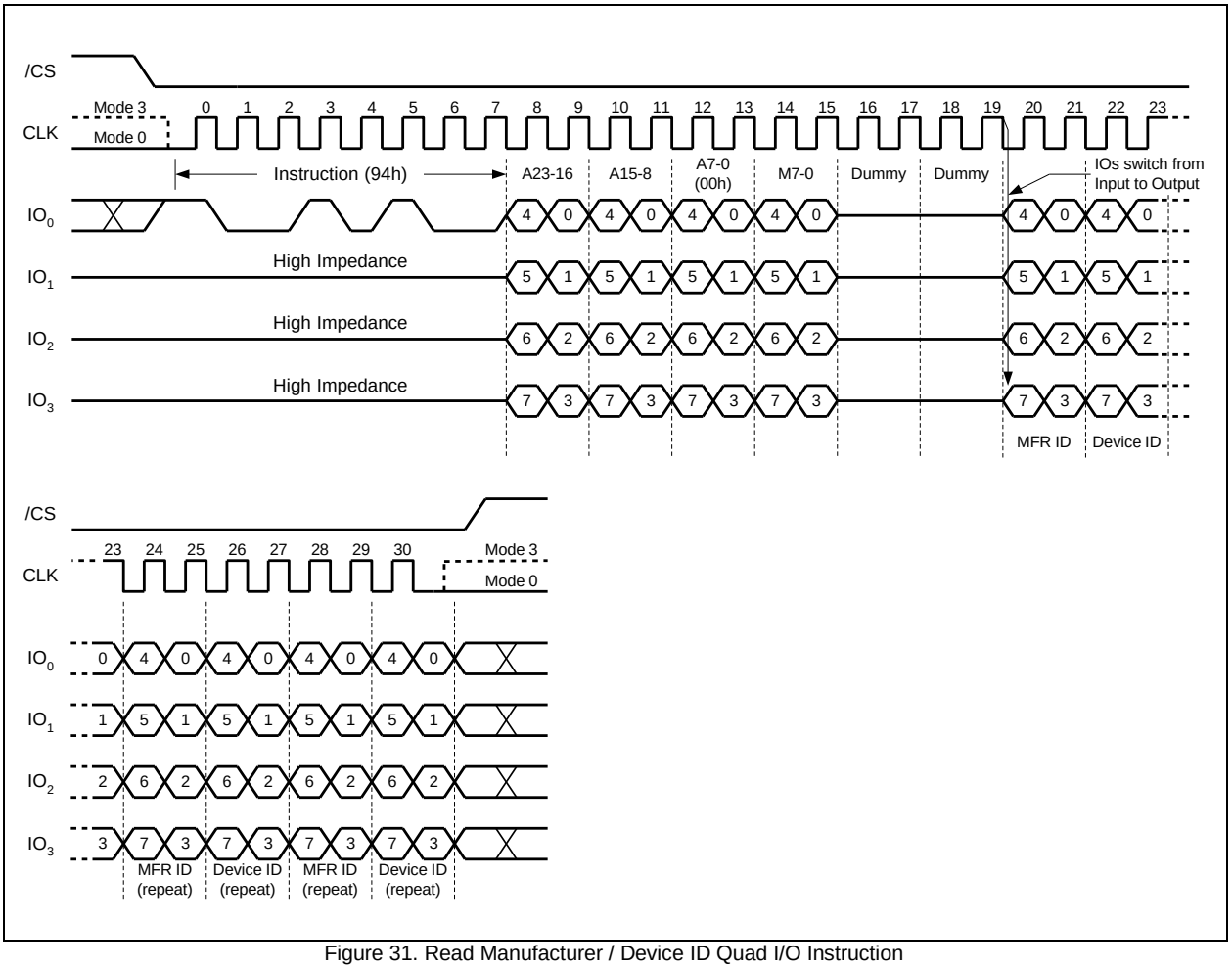


Figure 31. Read Manufacturer / Device ID Quad I/O Instruction

Note:
The “Continuous Read Mode” bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

8.2.28 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q64PW device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 32.

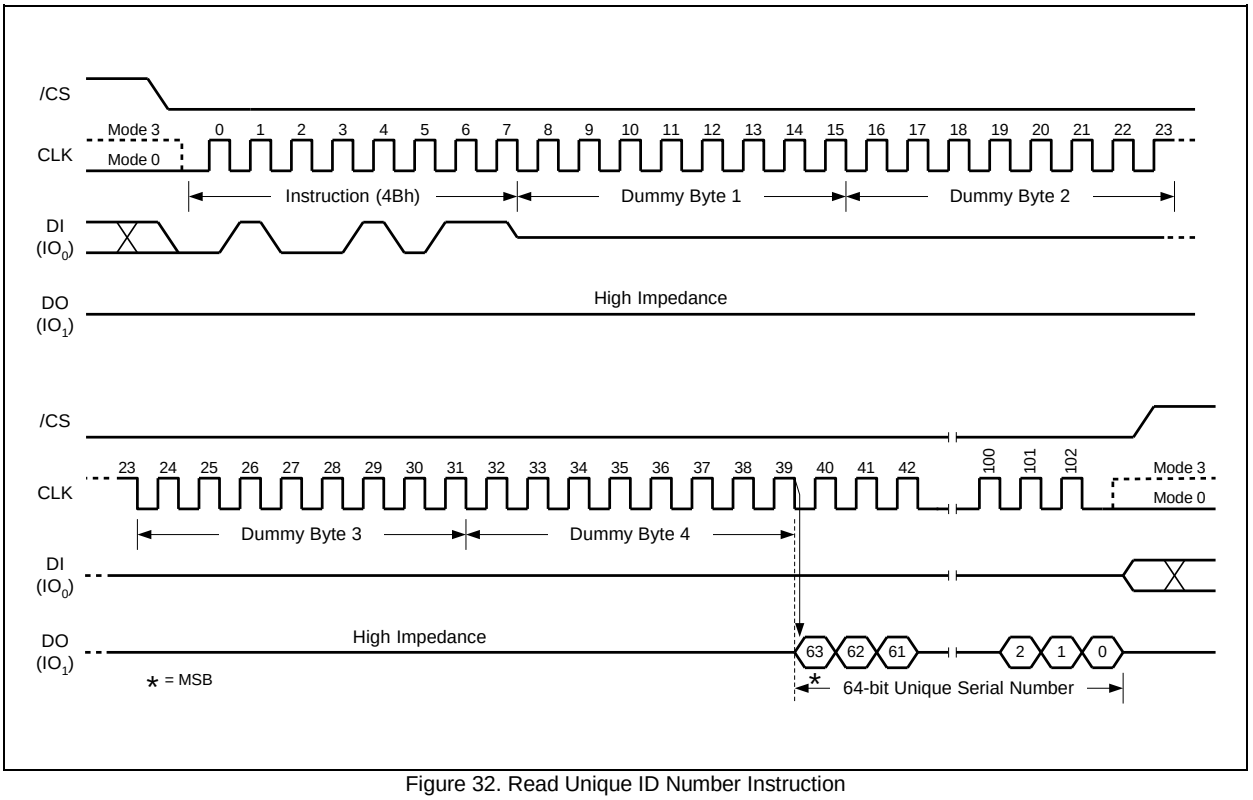


Figure 32. Read Unique ID Number Instruction

8.2.29 Read JEDEC ID (9Fh)

For compatibility reasons, the W25Q64PW provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 33. For memory type and capacity values refer to Manufacturer and Device Identification table.

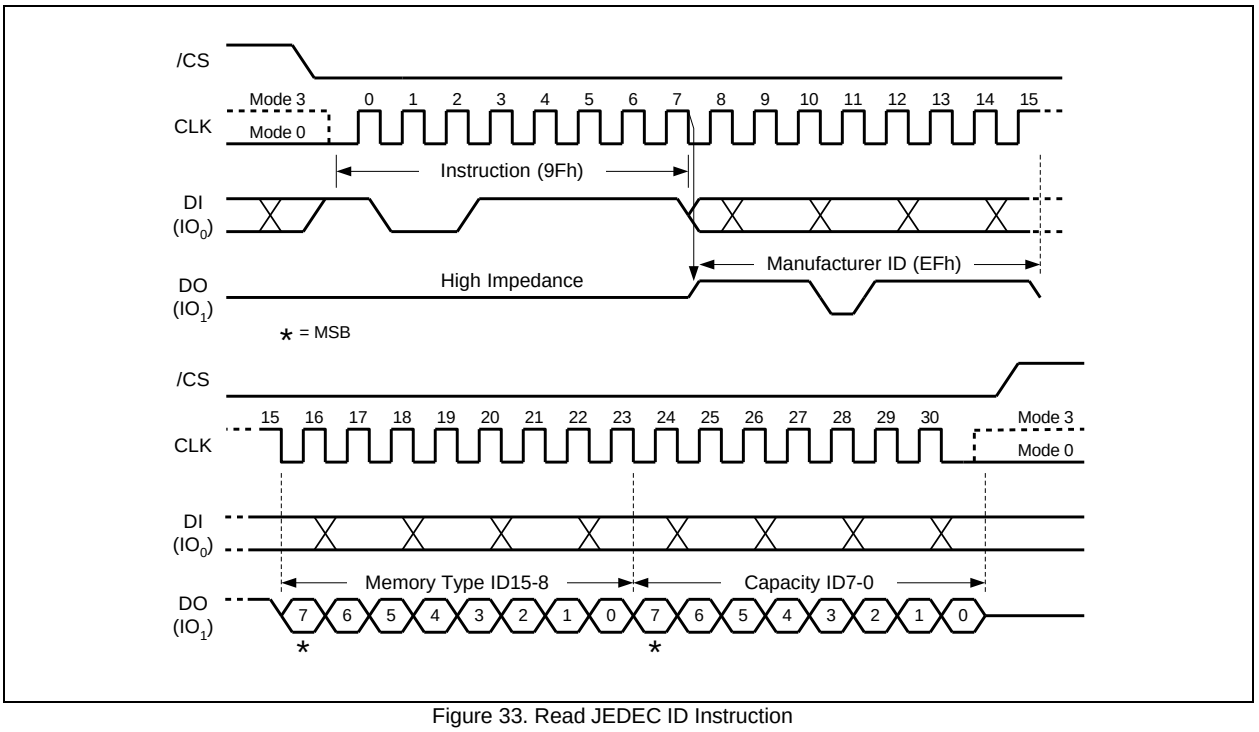


Figure 33. Read JEDEC ID Instruction

8.2.30 Read SFDP Register (5Ah)

The W25Q64PW features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216-serials that is published in 2011. Most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 34. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

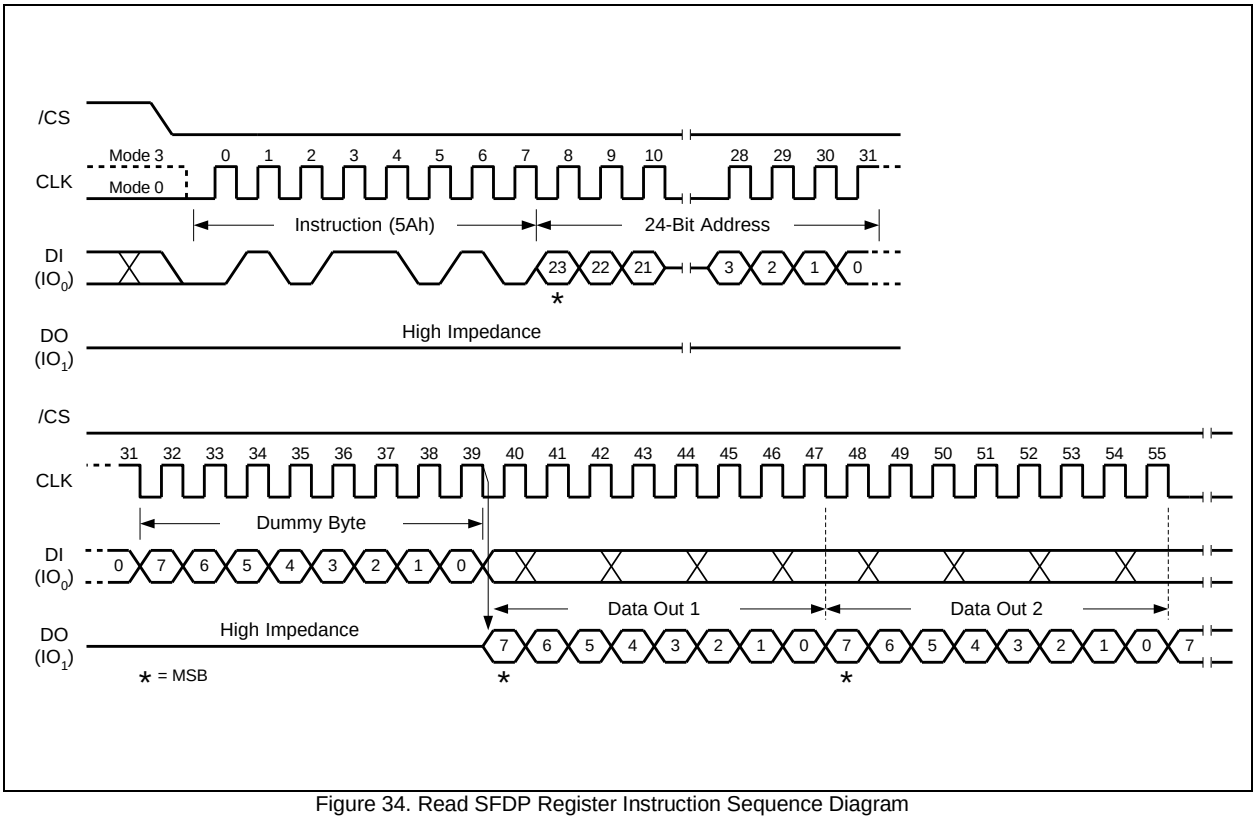


Figure 34. Read SFDP Register Instruction Sequence Diagram

8.2.31 Erase Security Registers (44h)

The W25Q64PW offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don't Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don't Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don't Care

The Erase Security Register instruction sequence is shown in Figure 35. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 7.1.9 for detail descriptions).

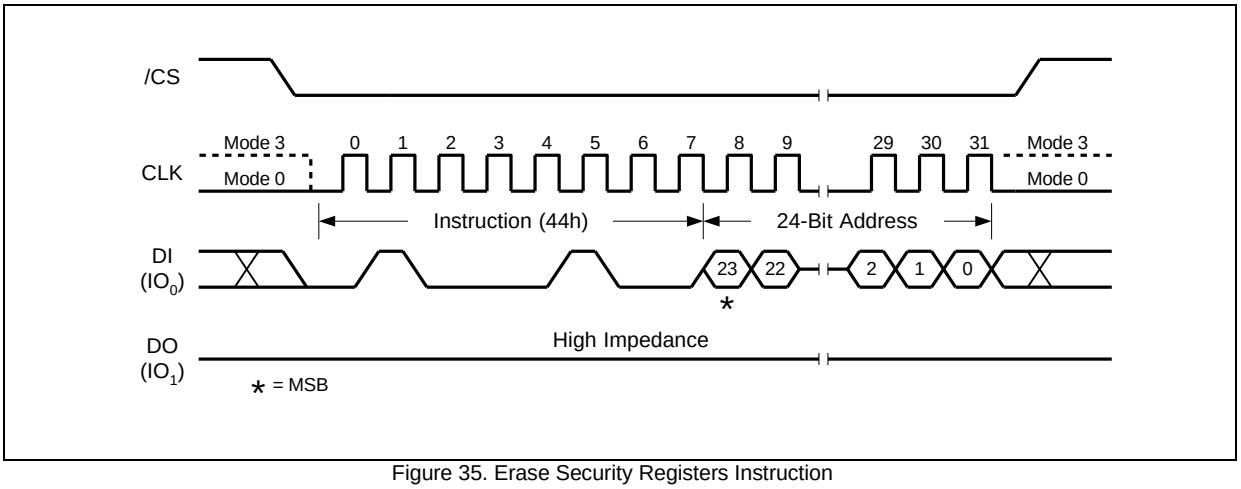


Figure 35. Erase Security Registers Instruction

8.2.32 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 36. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See “Security Register Lock” for detail descriptions).

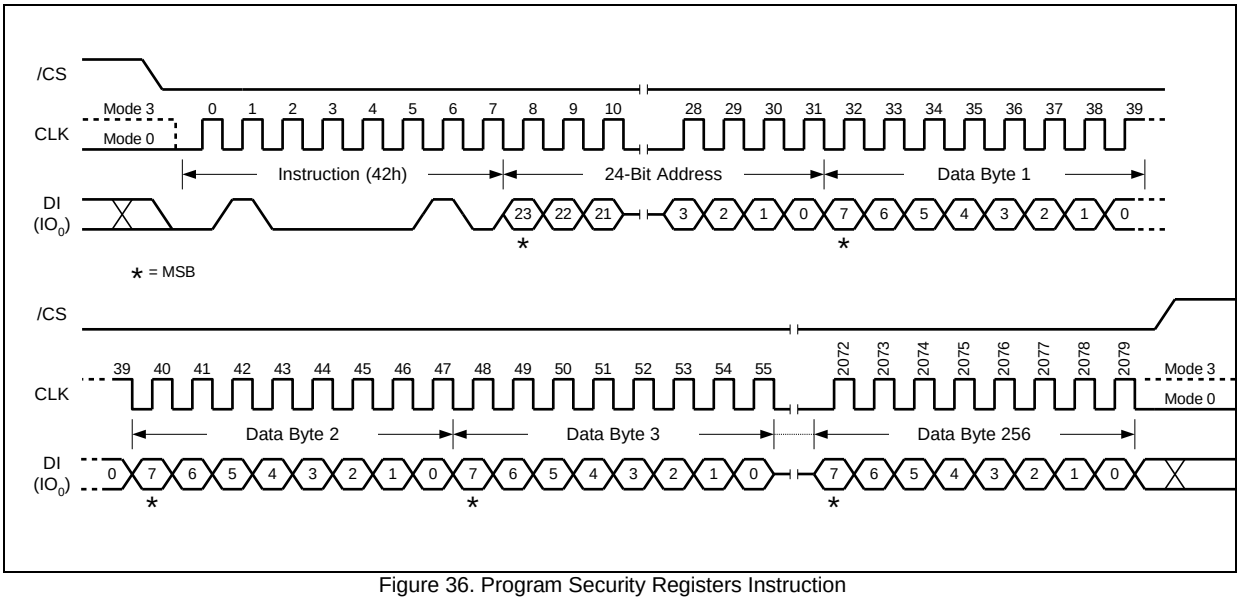


Figure 36. Program Security Registers Instruction

8.2.33 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 37. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of F_R (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

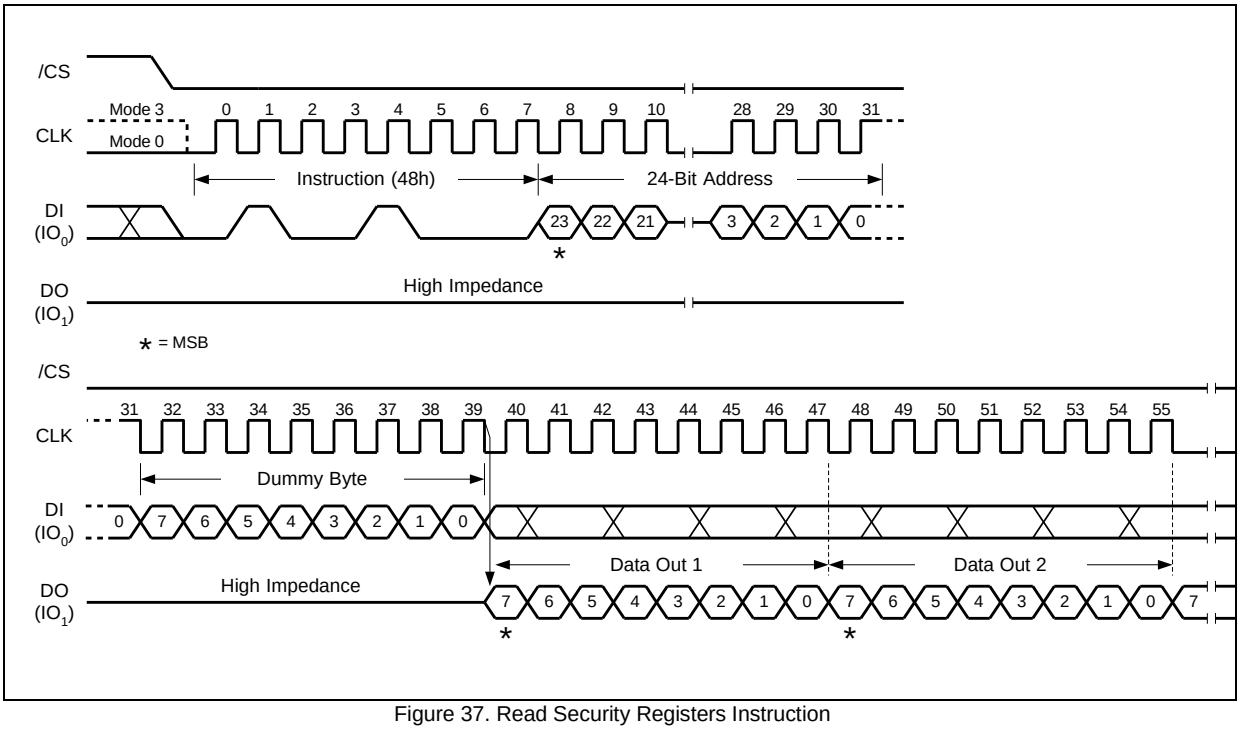


Figure 37. Read Security Registers Instruction

8.2.34 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25Q64PW provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0).

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in SPI. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

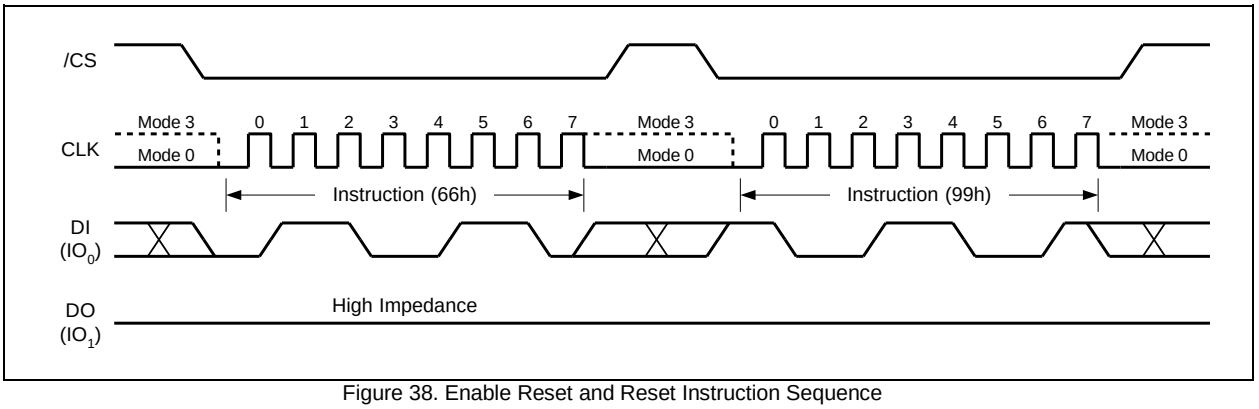


Figure 38. Enable Reset and Reset Instruction Sequence

8.2.35 Recovery for Erase (A8h)

The Recovery for Erase instruction identifies whether a power drop has occurred before completing the erase operation. Upon scanning and detecting an incomplete erase due to a power drop, the device performs an internal recovery process to prevent Flash data influence in non-erase areas.

A Write Enable instruction must be executed prior to accepting the Recovery for Erase instruction (Status Register bit WEL must equal 1). The instruction begins by driving the /CS pin low and shifting the instruction code “A8h”. The sequence for the Recovery for Erase instruction is illustrated in Figure 39.

Once /CS is driven high, the self-timed Recovery for Erase instruction initiates for a duration of tRCV (See AC Characteristics). During the Recovery for Erase cycle, the Read Status Register instruction can still be accessed to check the BUSY bit status. The BUSY bit remains at 1 during the Recovery for Erase and switches to 0 once the cycle completes, indicating the device is ready for other instructions. After the Recovery for Erase cycle concludes, the Write Enable Latch (WEL) bit in the Status Register is reset to 0.

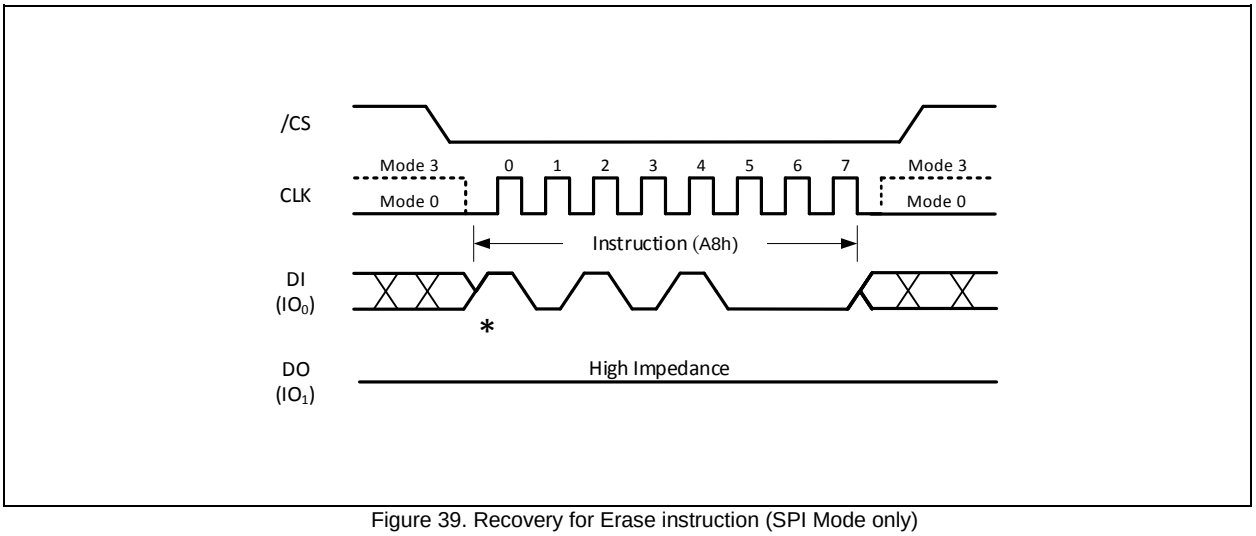


Figure 39. Recovery for Erase instruction (SPI Mode only)

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 2.5	V
Voltage Applied to Any Pin	VIO	Respect to VSS	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Respect to VSS	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	FR = 166MHz with 16T dummy FR = 133MHz, fR = 104MHz	1.65	1.95	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

9.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	20		µs
Time Delay Before Write Instruction	t_{PUW}[1]	5		ms
Write Inhibit Threshold Voltage	V_{WI}[1]	1.0	1.4	V
The minimum duration for ensuring initialization will occur	t_{PWD}[1]	100		µs
VCC voltage needed to below V_{PWD} for ensuring initialization will occur	V_{PWD}[1]		0.8	V

Note:

1. These parameters are characterized only.

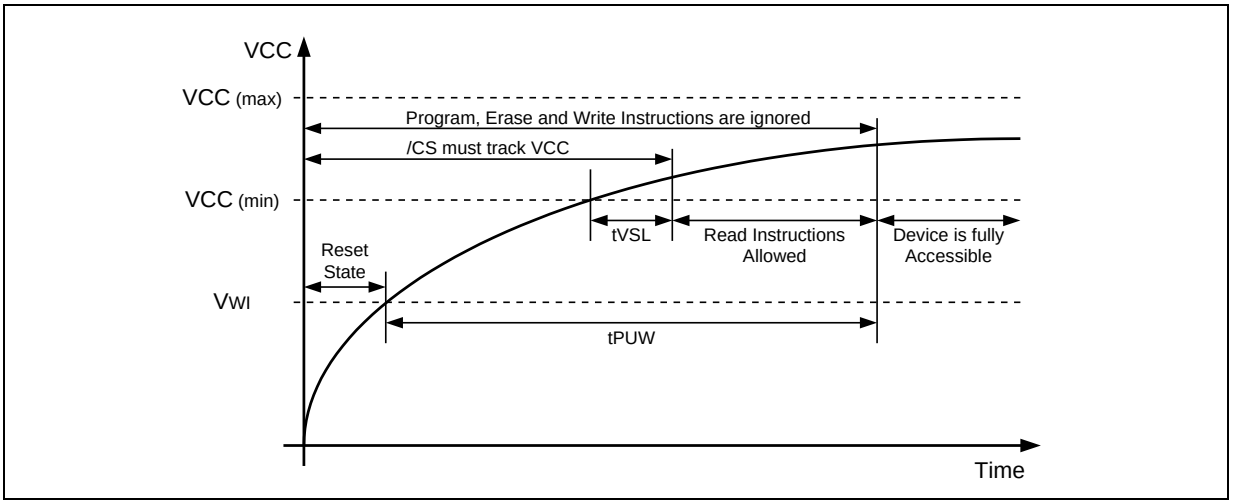


Figure 58a. Power-up Timing and Voltage Levels

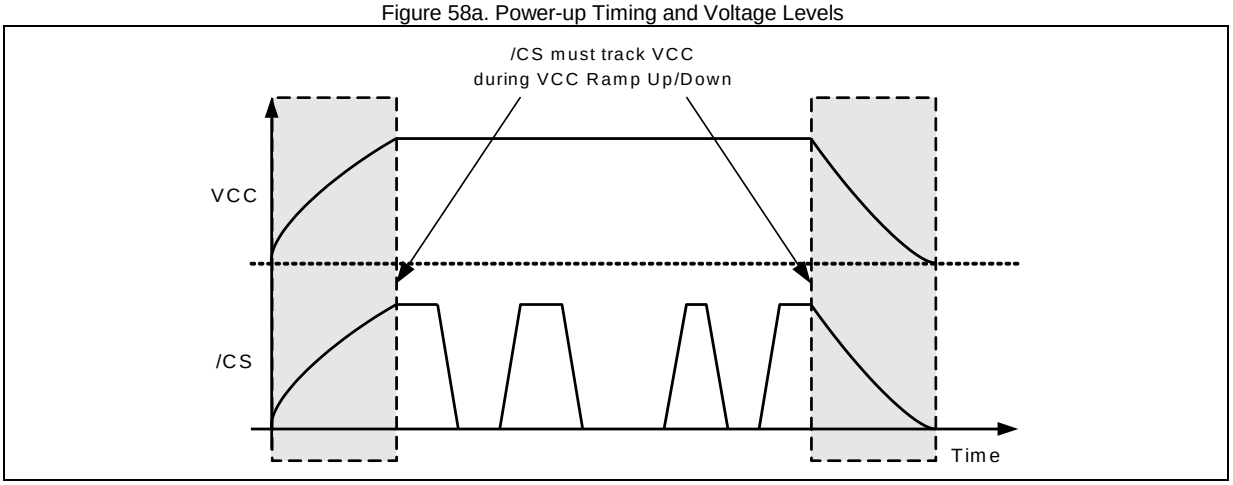


Figure 58b. Power-up, Power-Down Requirement

9.3.1 Power Cycle Requirement

For power cycle, the system must not initial the power-up sequence until Vcc drops down to V_{PWD} and keeps a t_{PWD} for device to initialize correctly.

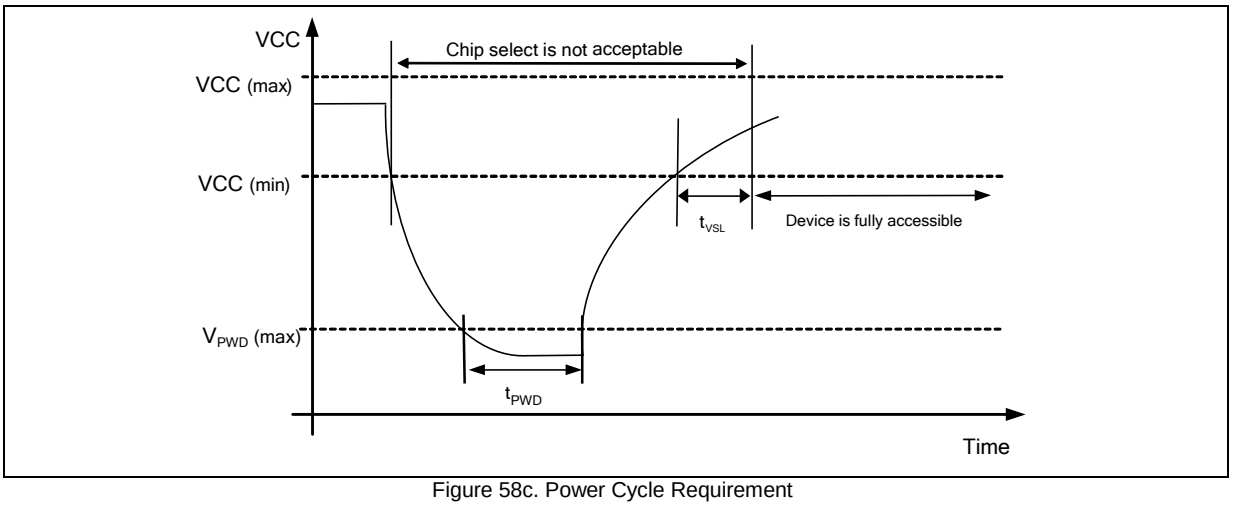


Figure 58c. Power Cycle Requirement

9.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V			6	pF
Output Capacitance	C_{OUT}(1)	V_{OUT} = 0V			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = VSS or VCC		10	30	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = VSS or VCC		0.1	1	µA
Read Data / Dual /Quad 50MHz Current	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		3	6	mA
Current Read Data / Dual /Quad 84MHz Current	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		3.5	5	mA
Read Data / Dual Output / Quad Output Read 104MHz Current	Icc3	C = 0.1 VCC / 0.9 VCC DO = Open		4	8	mA
Read Data / Dual Output / Quad Output Read 133MHz Current	Icc3	C = 0.1 VCC / 0.9 VCC DO = Open		5	9	mA
Read Data / Dual Output / Quad Output Read 166MHz Current	Icc3	C = 0.1 VCC / 0.9 VCC DO = Open		6	10	mA
Current Write Status Register	Icc4(2)	/CS = VCC		8	15	mA
Current Page Program	Icc5	/CS = VCC		8	15	mA
Current Sector/Block Erase	Icc6	/CS = VCC		8	15	mA
Current Chip Erase	Icc7	/CS = VCC		8	15	mA
Input Low Voltage	Vil		-0.5		VCC x 0.3	V
Input High Voltage	Vih		VCC x 0.7			V
Output Low Voltage	Vol	Iol = 100 µA			0.2	V
Output High Voltage	Voh	Ioh = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.
2. Checker Board Pattern.

9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

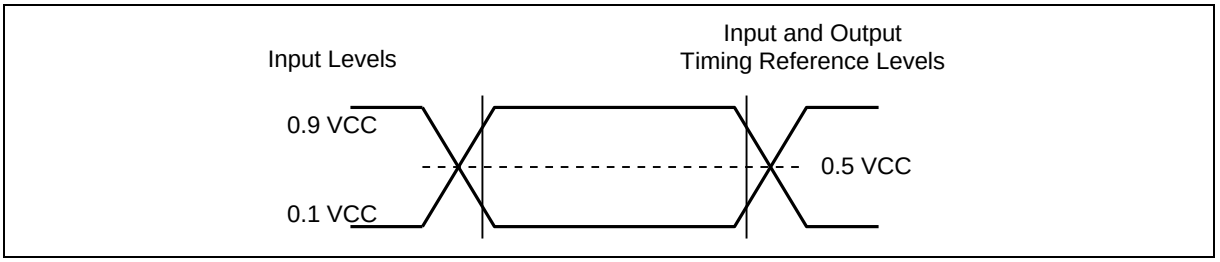


Figure 59. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics[5,6]

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for QSPI-EBh dummy 12-16T[8]	F_R	f_{C1}	D.C.		166[6]	MHz
Clock frequency except for Read Data (03h) & instructions	F_R	f_{C1}	D.C.		133[6]	MHz
Clock frequency for Read Data instruction (03h)	f_R		D.C.		104[6]	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	t_{CLH}, t_{CLL}[1]		45%PC			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}[1]		45%PC			ns
Clock Rise Time peak to peak	t_{CLCH}[2]		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}[2]		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		3			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	2			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50			ns
/CS Deselect Time (for program/erase) to /BUSY Low	t_{SHBL}				80	ns
/BUSY high to /CS Active	t_{BHSL}			0		ns
Output Disable Time	t_{SHQZ}[2]	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			4.5	ns
Output Hold Time	t_{CLQX}	t_{HO}	1			ns

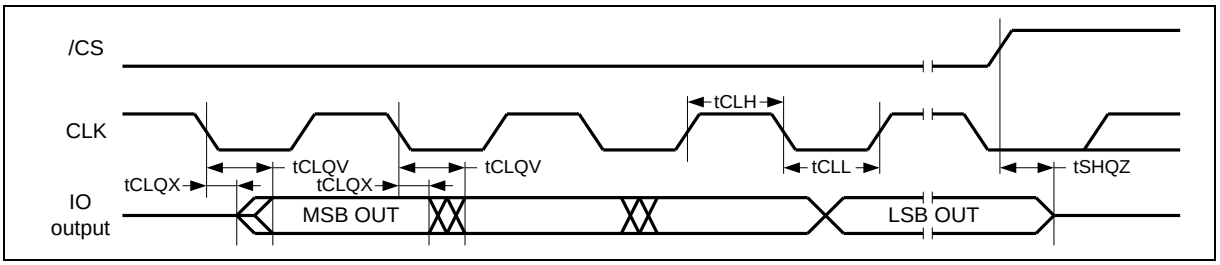
Continued – next page

AC Electrical Characteristics (cont'd)

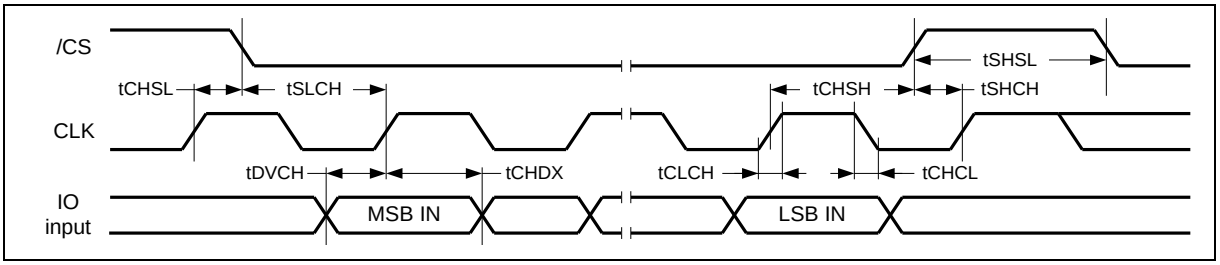
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				3	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
Write Status Register Time	t_W			1	15	ms
Page Program Time	t_{PP}			0.12	1.5	ms
Sector Erase Time (4KB)	t_{SE}			30	250	ms
Block Erase Time (32KB)	t_{BE_1}			90	800	ms
Block Erase Time (64KB)	t_{BE_2}			120	1000	ms
Chip Erase Time	t_{CE}			7	50	s
Recovery for Erase Time(9)	t_{RCV}			2.5	5	s

Notes:
1. Clock high or Clock low must be more than or equal to 45%Pc. $Pc=1/fc_{(MAX)}$
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. TYP. value tested on sample basis and specified through design and characterization data. T_A = 25° C, VCC = 1.8V driver strength.
6. 4-bytes address alignment for Read, start address from [A1,A0]=(0,0).
7. Tested with 55h/AAh pattern
8. Please refer to the Set Read Parameters(C0h) section.
9. The maximum value represents Revery for a signal power drop during erase event.

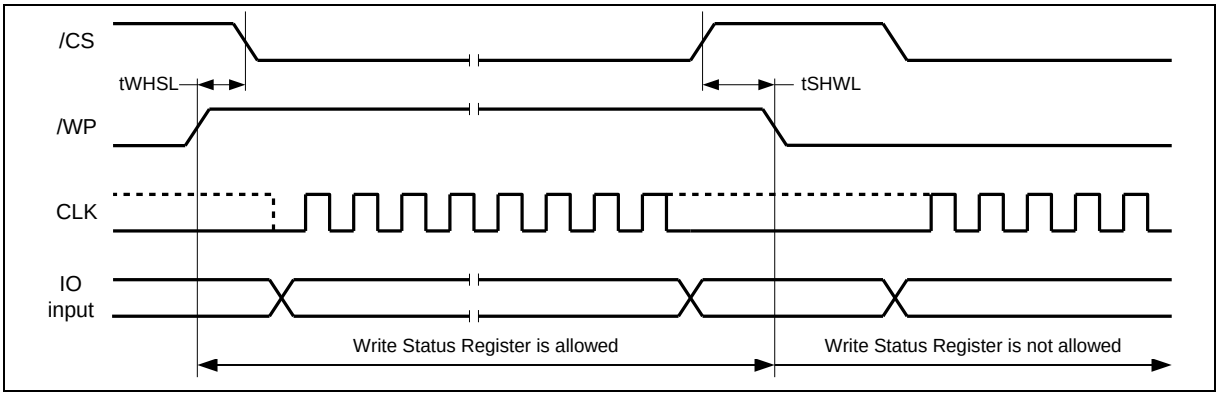
9.7 Serial Output Timing



9.8 Serial Input Timing

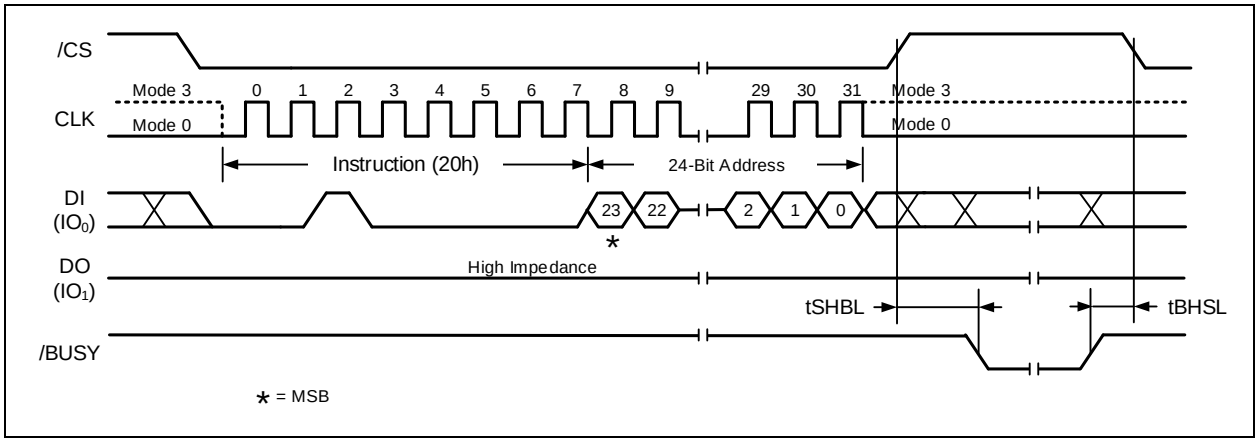


9.9 /WP Timing



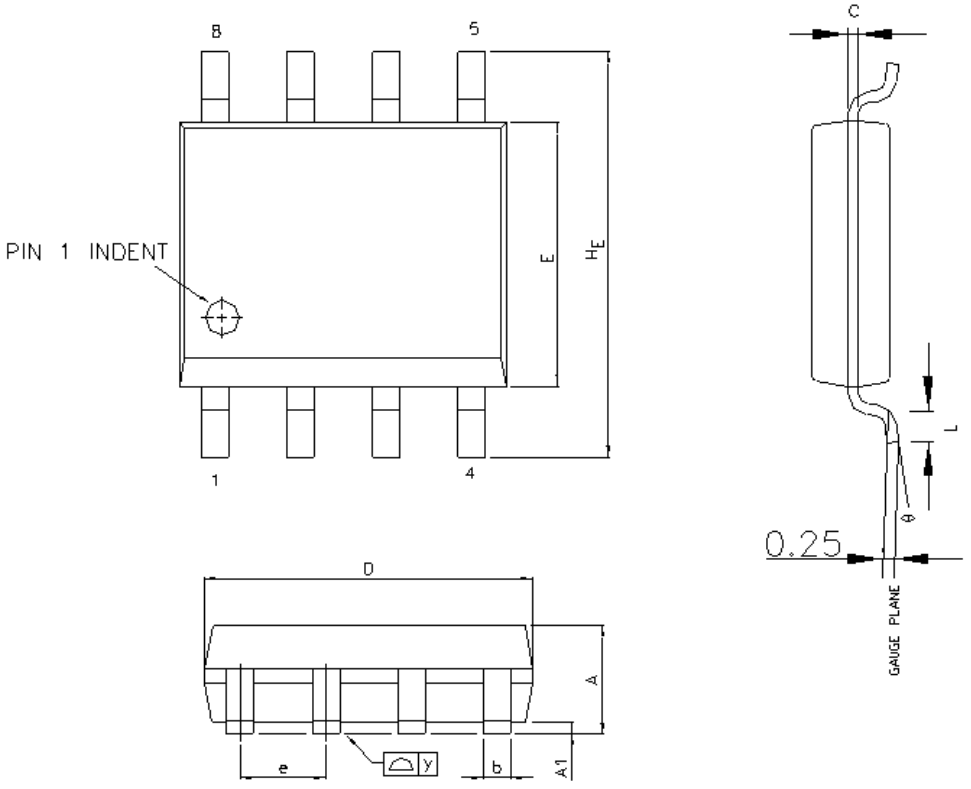
9.10 /Busy Timing

The following timing diagram illustrates /BUSY signal behavior during Sector Erase (20h) instruction.
All other *Erase and Program* instructions have similar timing relationship between /CS and /BUSY.



10. PACKAGE SPECIFICATIONS

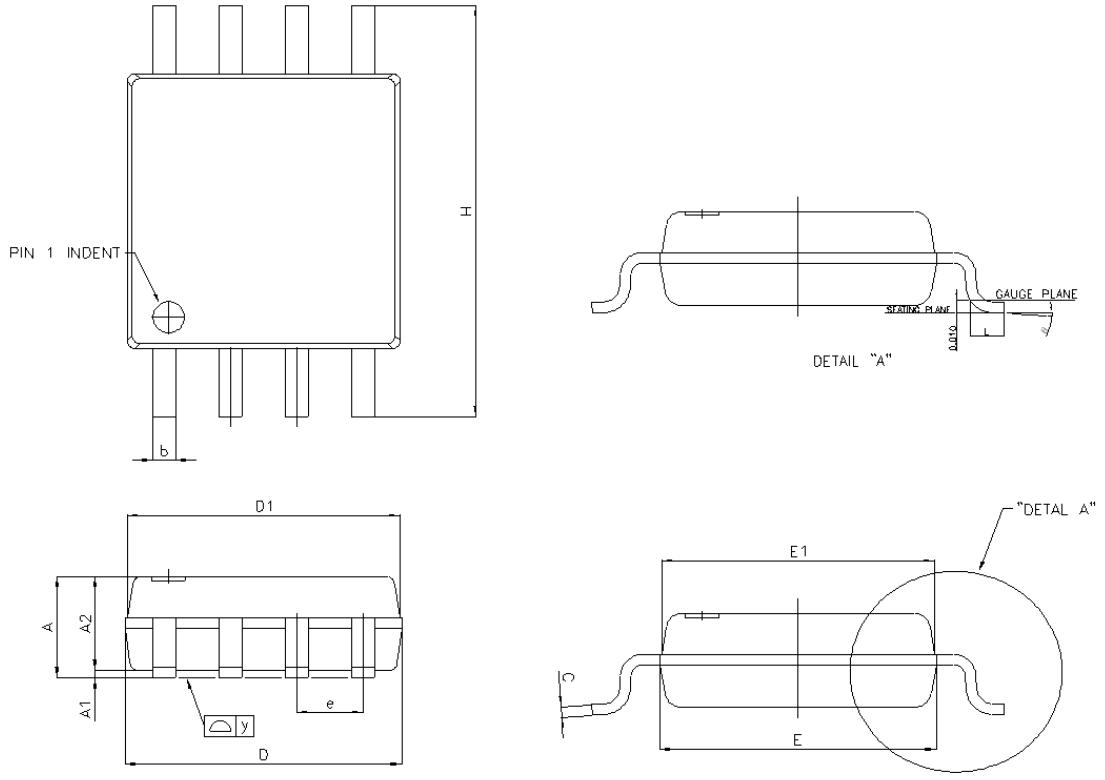
10.1 8-Pin SOIC 150-mil (Package Code SN)



SYMBOL	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.60	1.75	0.053	0.062	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.0078	0.0098
D	4.80	4.85	5.00	0.188	0.190	0.197
E	3.80	3.90	4.00	0.150	0.153	0.157
H_E	5.80	6.00	6.20	0.288	0.236	0.244
e	1.27BSC			0.050BSC		
L	0.40	0.71	1.27	0.016	0.027	0.050
y	---	---	0.10	---	---	0.004
θ°	0°	---	10°	0°	---	10°

Note:
1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

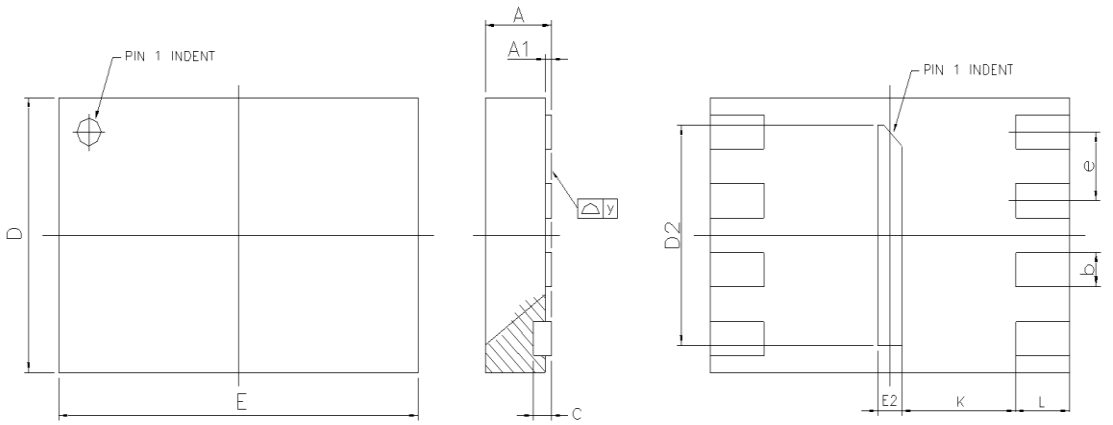
10.2 8-Pin SOIC 208-mil (Package Code SS)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
D1	5.13	5.23	5.33	0.202	0.206	0.210
E	5.18	5.28	5.38	0.204	0.208	0.212
E1	5.13	5.23	5.33	0.202	0.206	0.210
e	1.27 BSC			0.050 BSC		
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

Note:
1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

10.3 8-Pad XSON 2x3x0.4-mm (Package Code XH)

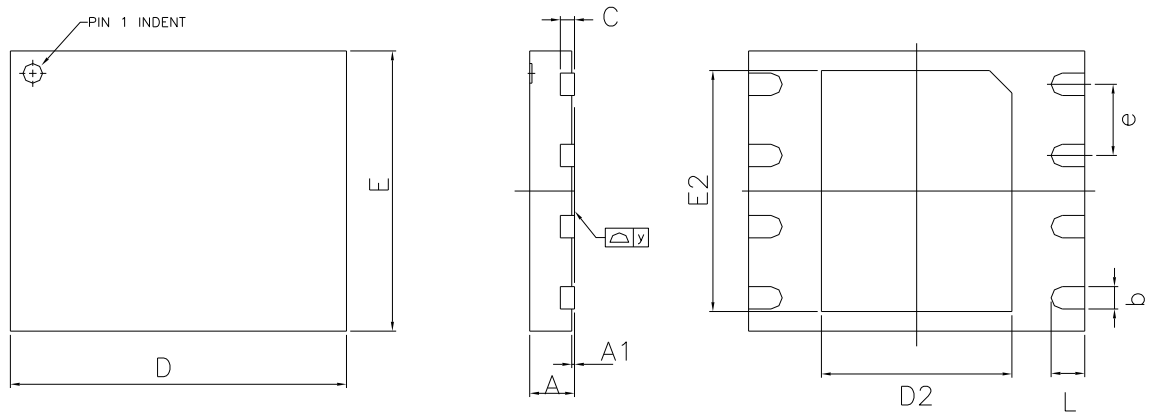


Symbol	Millimeters		
	Min	Nom	Max
A	0.30	0.35	0.40
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C	---	0.127 Ref.	---
D	1.90	2.00	2.10
D2	1.55	1.60	1.65
E	2.90	3.00	3.10
E2	0.15	0.20	0.25
e	---	0.50	---
K	0.95 Ref.		
L	0.40	0.45	0.50
y	0.00	---	0.075

Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

10.4 8-Pad WSON 6x5-mm (Package Code ZP)

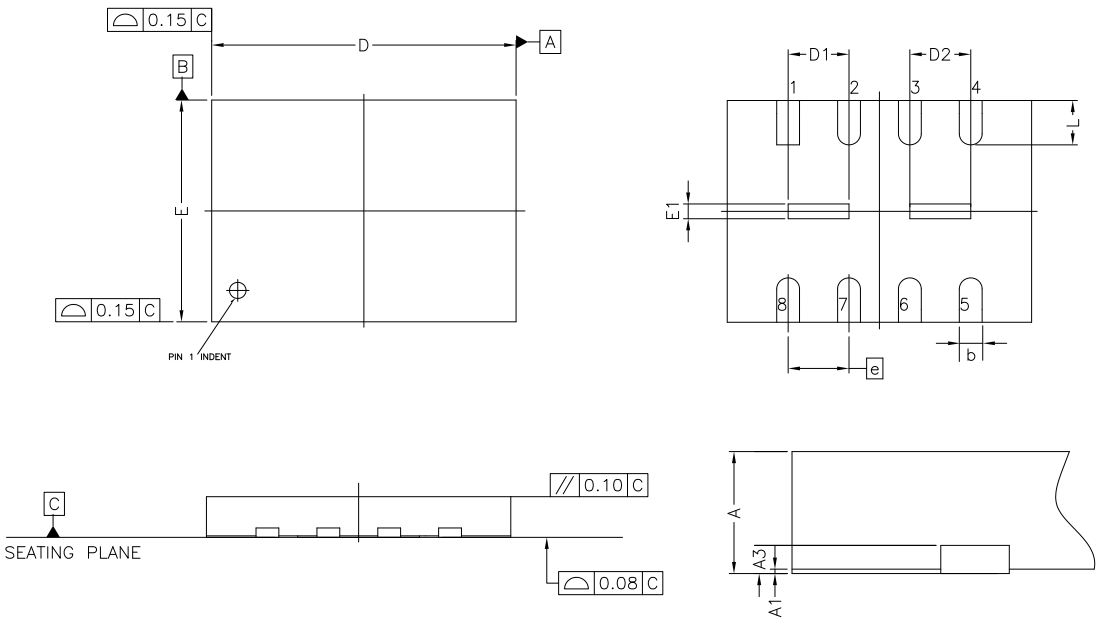


Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	1.27 BSC			0.050 BSC		
L	0.55	0.60	0.65	0.022	0.024	0.026
y	0.00	---	0.075	0.000	---	0.003

Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

10.5 8-Pad USON 4x3-mm (Package Code UU)

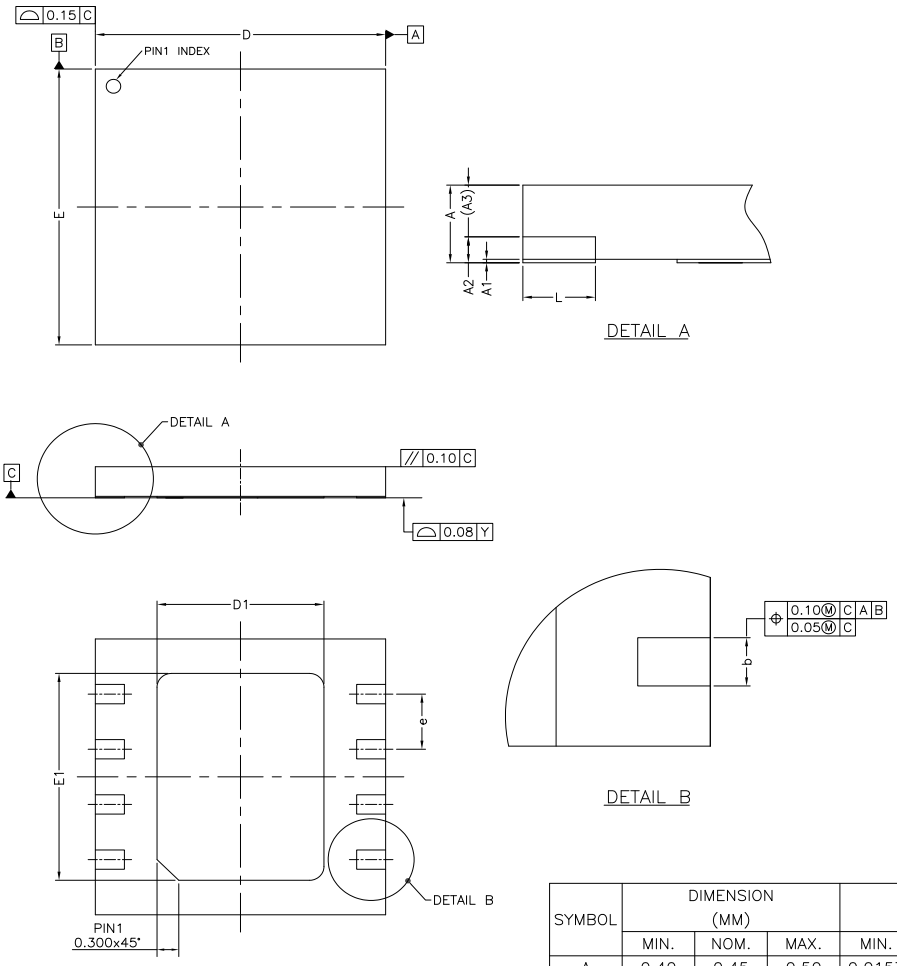


Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	---	0.15	---	---	0.006	---
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.70	0.80	0.90	0.027	0.031	0.035
D2	0.70	0.80	0.90	0.027	0.031	0.035
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.10	0.20	0.30	0.004	0.008	0.012
e	0.80 BSC			0.031 BSC		
L	0.55	0.60	0.65	0.022	0.024	0.026

Note:

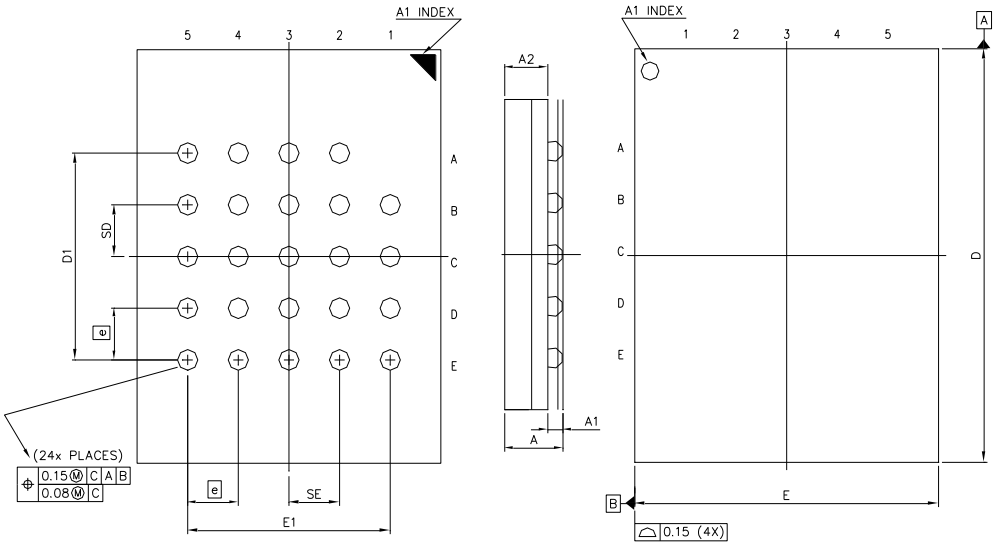
The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

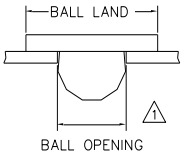
10.6 8-Pad XSON 4x4x0.45-mm (Package Code XG)



SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.40	0.45	0.50	0.0157	0.0177	0.0196
A1	0.00	0.02	0.05	0	0.0007	0.0019
A2	–	0.15	–	–	0.0059	–
A3	0.25	0.30	0.35	0.0098	0.0118	0.0137
b	0.25	0.30	0.35	0.0098	0.0118	0.0137
D	3.90	4.00	4.10	0.1535	0.1574	0.1614
D1	2.20	2.30	2.40	0.0866	0.0905	0.0944
E	3.90	4.00	4.10	0.1535	0.1574	0.1614
E1	2.90	3.00	3.10	0.1141	0.1181	0.1220
e	0.80 BSC			0.0314 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177

10.7 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 ball array)

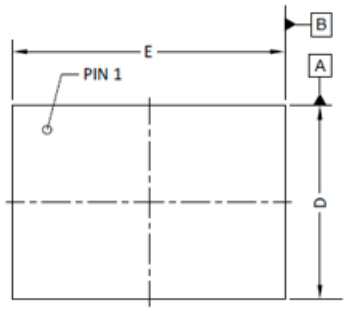




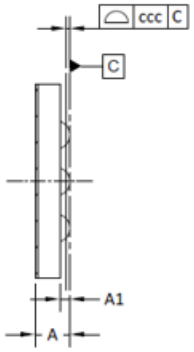
Note:
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.26	0.31	0.36	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		

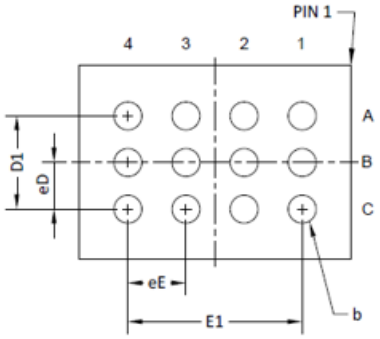
10.8 WLCSP 12Ball(Ball pitch : 0.50mm)



TOP VIEW



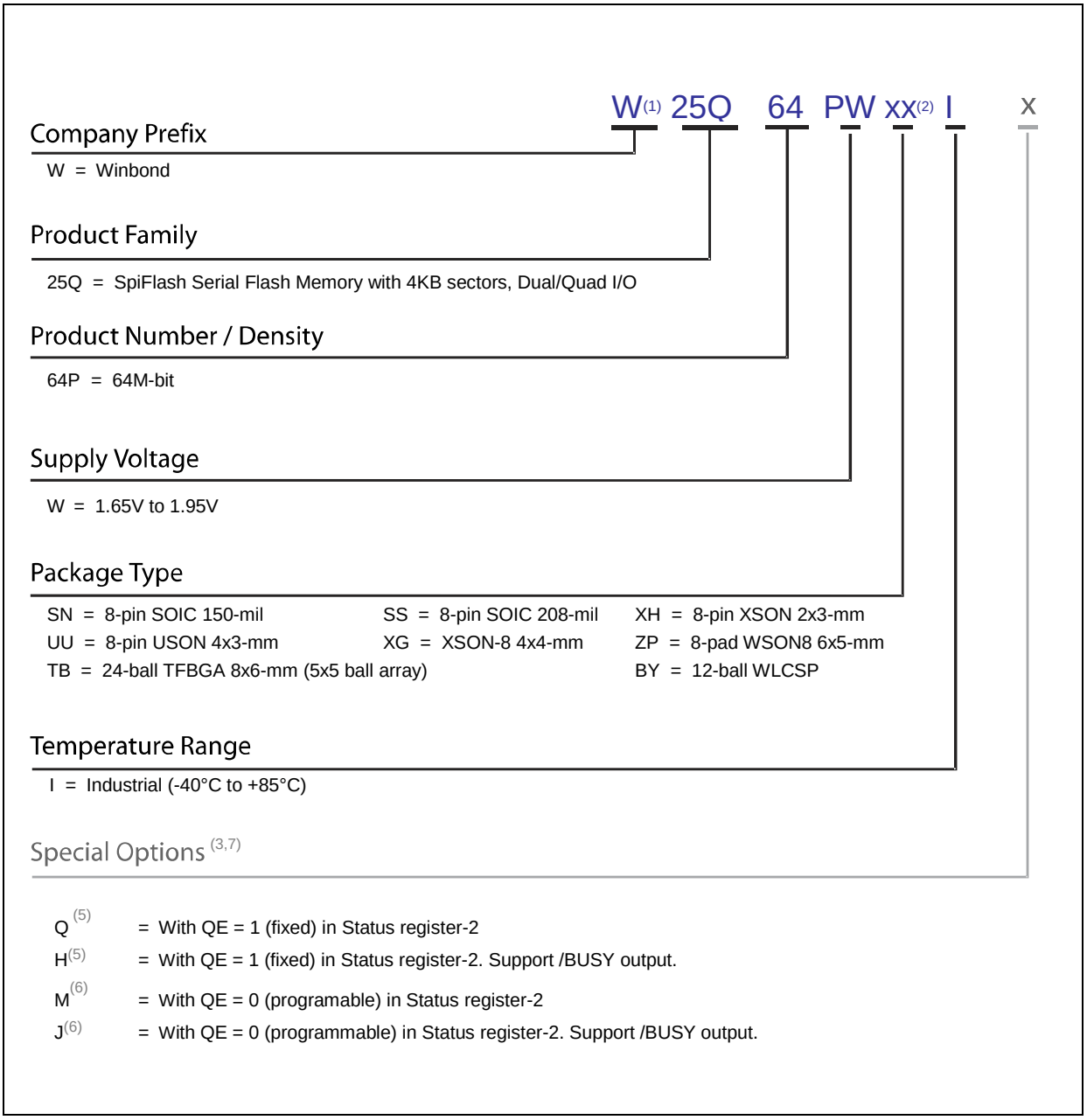
SIDE VIEW



BOTTOM VIEW

Symbol	Millimeters			Inches		
	Min	Nom	MAX.	Min	Nom	MAX.
A	0.264	0.297	0.330	0.010	0.012	0.013
A1	0.075	0.085	0.095	0.003	0.003	0.004
D1	0.800 BSC			0.031 BSC		
E1	1.500 BSC			0.059 BSC		
eD	0.400 BSC			0.016 BSC		
eE	0.500 BSC			0.020 BSC		
b	0.210	0.240	0.270	0.008	0.009	0.011
ccc	0.05 BSC			0.001 BSC		

11. ORDERING INFORMATION



Notes:

1. The "W" prefix is not included on the part marking.
2. Only the 2nd letter is used for the part marking; WSON package type ZP is not used for the part marking.
3. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
4. For shipments with OTP feature enabled, please specify when placing orders.
5. /HOLD function is disabled to support Standard, Dual and Quad I/O without user setting.
6. For DTR, QPI supporting, please refer to W25Q64PW-M DTR datasheet.
7. All devices are in compliance with RoHs, Halogen free, TSCA, and REACH.

11.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25Q64PW SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

W25Q64PW-IQ(-40°C to +85°C) valid part numbers:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150mil	64M-bit	W25Q64PWSNIQ	25Q64PWNIQ
SS SOIC-8 208-mil	64M-bit	W25Q64PWSSIQ	25Q64PWSIQ
XH XSON-8 2x3mm	64M-bit	W25Q64PWXHIQ	●WCywH(2) IQxxxx
UU USON-8 4x3mm	64M-bit	W25Q64PWUUIQ	Q64PWUUIQ
XG XSON-8 4x4x0.45-mm	64M-bit	W25Q64PWXGIQ	Q64PWXGIQ
ZP WSON-8 6x5-mm	64M-bit	W25Q64PWZPIQ	25Q64PWIQ

W25Q64PW-IH(3) (-40°C to +85°C) valid part numbers:

TB TFBGA-24 8x6-mm (5x5 Ball Array)	64M-bit	W25Q64PWTBIH	25Q64PWBIH
BY(1) 8-ball WLCSP	64M-bit	W25Q64PWBYIH	*6AP IHyw(2)

Note:

1. These package types are special order, please contact Winbond for more information
2. yw: year/ week ; xxxx=lot ID
3. The ordering number that ends with “H” or “J” is includes a /BUSY pin.
4. For DTR, QPI supporting, please refer to W25Q64PW-M DTR datasheet.

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	10/15/2024	61-62	New Create “Preliminary” Updated tSLCH , tHO, tCE
B	04/30/2025	All 24 6 - 8, 69 - 78 18, 60, 67	Removed “Preliminary” Added Buffer Mode Updated valid part numbers Added RCV bit and A8h instruction information

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