

钍地半导体
Tudi Semiconductor

# Product Specification

## TUDI-CAT24C01/02/04/08/16

1-Kb, 2-Kb, 4-Kb, 8-Kb and 16-Kb $I^2C$ CMOS Serial EEPROM

网址 www.sztdbdt.com

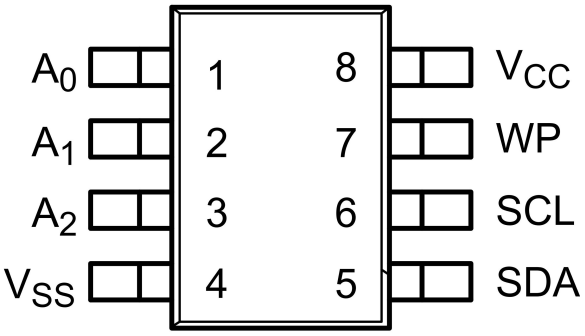
**用芯智造·卓越品质**

**semiconductor device manufacturer**

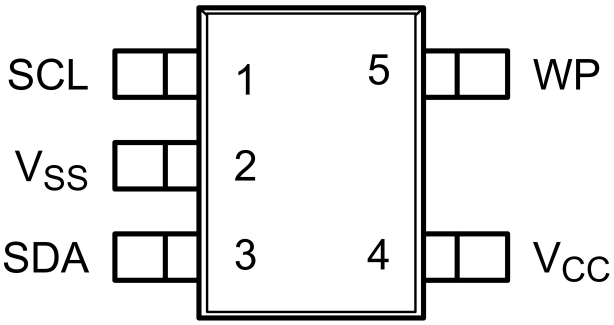
- Design
- research and development
- production
- and sales

## Features

- Supports Standard and Fast $I^2C$ Protoco
- 1.7 V to 5.5 V Supply Voltage Range
- 16-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on $I^2C$ Bus Inputs (SCL and SDA)
- Low power CMOS Technology
- More than 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



SOP8/DIP8/TSSOP8



SOT23-5

## Description

The CAT24C01/02/04/08/16 are 1-Kb, 2-Kb, 4-Kb, 8-Kb and 16-Kb respectively CMOS Serial EEPROM devices organized internally as 8/16/32/64 and 128 pages respectively of 16 bytes each. All devices support both the Standard (100 kHz) as well as Fast (400 kHz) $I^2C$ protocol.

Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non-volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight CAT24C01 or CAT24C02, four CAT24C04, two CAT24C08 and one CAT24C16 device on the same bus.

## Table 1.PIN FUNCTION

| Pin Namet | Function |
|---|---|
| A0,A1,A2 | Device Address Input |
| SDA | Serial Data Input/Output |
| SCL | Serial Clock Input |
| WP | Write Protect Input |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |
| NC | No Connect |

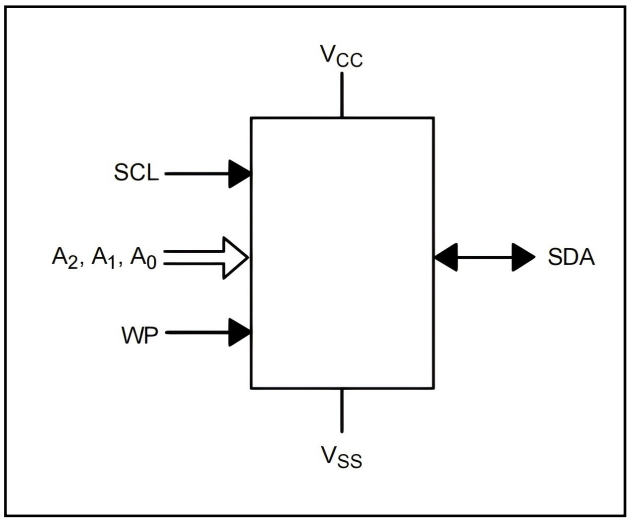



Figure 1. Functional Symbol

## Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameters | Ratings | Units |
|---|---|---|
| Storage Temperature | -65 to+150 | ℃ |
| Voltage on any pin with respect to Ground (Note 1) | -0.5 to+6.5 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. During input transitions, voltage undershoot on any pin should not exceed-1 V for more than 20 ns. Voltage overshoot on pins $A_0$, $A_1$, $A_2$ and WP should not exceed $V_{CC}$ + 1 V for more than 20 ns, while voltage on the $I^2C$ bus pins, SCL and SDA, should not exceed the absolute maximum ratings, irrespective of $V_{CC}$.

## Table 3. RELIABILITY CHARACTERISTICS (Note 2)

| Symbol | Parameter | Min | Units |
|---|---|---|---|
| $N_{END}$(Note 3) | Endurance | 1,000,000 | Program/Erase Cycles |
| $T_{DR}$ | Data Retention | 100 | Years |

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, $V_{CC}$ = 5 V, 25°C.

## Table 4. D.C. OPERATING CHARACTERISTICS

($V_{CC}$ = 1.8 V to 5.5 V, $T_A$ = -40°C to +125°C and $V_{CC}$ = 1.7 V to 5.5 V, $T_A$ = -40°C to +85°C, unless otherwise specified.)

| Symbol | Parameter | Test Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CCR}$ | Read Current | Read,$f_{SCL}$=400 kHz | | | 1 | mA |
| $I_{CCW}$ | Write Current | Write,$f_{SCL}$=400 kHz | | | 2 | mA |
| $I_{SB}$ | Standby Current | All I/O Pins at GND or $V_{CC}$ | $T_A$=-40℃ to +85℃ $V_{CC}\leq$3.3V | | 1 | μA |
| | | | $T_A$=-40℃ to+85℃ $V_{CC}$>3.3V | | 3 | |
| | | | $T_A$=-40℃ to+125℃ | | 5 | |
| $I_L$ | I/O Pin Leakage | Pin at GND or $V_{CC}$ | | | 2 | μA |
| $V_{IL}$ | Input Low Voltage | | | -0.5 | 0.3×$V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage | $A_0$,$A_1$,$A_2$ and WP | | 0.7×$V_{CC}$ | $V_{CC}$+0.5 | V |
| | | SCL and SDA | | 0.7×$V_{CC}$ | 5.5 | |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$>2.5V,$I_{OL}$=3 mA | | | 0.4 | |
| | | $V_{CC}$<2.5 V,$I_{OL}$=1 mA | | | 0.2 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## Table 5. PIN IMPEDANCE CHARACTERISTICS

($V_{CC}$ = 1.8 V to 5.5 V, $T_A$ = -40°C to +125°C and $V_{CC}$ = 1.7 V to 5.5 V, $T_A$ = -40°C to +85°C, unless otherwise specified.)

| Symbol | Parameter | Conditions | Max | Units |
|---|---|---|---|---|
| $C_{IN}$(Note 4) | SDA Pin Capacitance | $V_{IN}$=0V,f=1.0 MHz,$V_{cc}$=5.0V | 8 | pF |
| | Other Pins | | 6 | pF |
| $I_{WP}$(Note 5) | WP Input Current | $V_{IN}<V_{IH}$,$V_{cc}$=5.5V | 130 | μA |
| | | $V_{IN}<V_{IH}$,$V_{cc}$=3.3V | 120 | |
| | | $V_{IN}<V_{IH}$,$V_{cc}$=1.7V | 80 | |
| | | $V_{IN}>V_{IH}$ | 2 | |
| $I_A$(Note 5) | Address Input Current (A0,A1,A2)Product Rev H:CAT24C02 Product Rev K:CAT24C04, CAT24C08,CAT24C16 | $V_{IN}<V_{IH}$,$V_{cc}$=5.5V | 50 | μA |
| | | $V_{IN}<V_{IH}$,$V_{cc}$=3.3V | 35 | |
| | | $V_{IN}<V_{IH}$,$V_{cc}$=1.7V | 25 | |
| | | $V_{IN}>V_{IH}$ | 2 | |

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x VCC), the strong pull-down reverts to a weak current source.

# Table 6. A.C. CHARACTERISTICS

(Note 6) ($V_{CC}$ = 1.8 V to 5.5 V, $T_A$ = -40°C to +125°C and $V_{CC}$ = 1.7 V to 5.5 V, $T_A$ = -40°C to +85°C, unless otherwise specified.)

| Symbol | Parameter | Standard | | Fast | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCL}$ | Clock Frequency | | 100 | | 400 | kHz |
| $t_{HD:STA}$ | START Condition Hold Time | 4 | | 0.6 | | μ s |
| $t_{LOW}$ | Low Period of SCL Clock | 4.7 | | 1.3 | | μ s |
| $t_{HIGH}$ | High Period of SCL Clock | 4 | | 0.6 | | μs |
| $t_{SU:STA}$ | START Condition Setup Time | 4.7 | | 0.6 | | μs |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | 0 | | μ s |
| $t_{SU:DAT}$ | Data In Setup Time | 250 | | 100 | | ns |
| $t_R$ | SDA and SCL Rise Time | | 1000 | | 300 | ns |
| $t_F$(Note 6) | SDA and SCL Fall Time | | 300 | | 300 | ns |
| $t_{SU:STO}$ | STOP Condition Setup Time | 4 | | 0.6 | | μs |
| $t_{BUF}$ | Bus Free Time Between STOP and START | 4.7 | | 1.3 | | μ s |
| $t_{AA}$ | SCL Low to Data Out Valid | | 3.5 | | 0.9 | μ s |
| $t_{DH}$ | Data Out Hold Time | 100 | | 100 | | ns |
| $T_i$(Note 6) | Noise Pulse Filtered at SCL and SDA Inputs | | 100 | | 100 | ns |
| $t_{SU:WP}$ | WP Setup Time | 0 | | 0 | | μ s |
| $t_{HD:WP}$ | WP Hold Time | 2.5 | | 2.5 | | μs |
| $t_{WR}$ | Write Cycle Time | | 5 | | 5 | ms |
| $t_{PU}$(Notes7,8) | Power-up to Ready Mode | | 1 | | 1 | ms |

6. Test conditions according to “ AC Test Conditions ” table.
7. Tested initially and after a design or process change that affects this parameter.
8. tPU is the delay between the time VCC is stable and the device is ready to accept commands.

## Table 7. A.C. TEST CONDITIONS

| Input Drive Levels | Input Rise and Fall Time | Input Reference Levels | Output Reference Level | Output Test Load |
|---|---|---|---|---|
| 0.2×Vcc to 0.8×Vcc | ≤50 ns | 0.3×Vcc,0.7×Vcc | 0.5×Vcc | Current Source<br>$I_{OL}$=3 mA(Vcc≥2.5V);<br>$I_{OL}$=1 mA(Vcc<2.5V);<br>CL=100 pF |

**Power-On Reset (POR):**Each CAT24Cxx* incorporates Power-On Reset (POR) circuitry which protects the internal logicagainst powering up in the wrong state.

A CAT24Cxx device will power up into Standby mode after $V_{CC}$ exceeds the POR trigger level and will power down into Reset mode when $V_{CC}$ drops below the POR trigger level. This bi-directional POR feature protects the device against ‘brown-out’ failure following a temporary loss of power.

For common features, the CAT24C01/02/04/08/16 will be referred to as CAT24Cxx.

**Pin Description**

**SCL:** The Serial Clock input pin accepts the Serial Clock generated by the Master.

**SDA:** The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

**A0, A1 and A2:** The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

**WP:** The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

**Functional Description:**The CAT24Cxx supports the Inter-Integrated Circuit (I2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24Cxx acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

**I 2C Bus Protocol:**The I2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the VCC supply via pull-up resistors. Master and Slave devices connect to the 2? wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see AC Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is high. An SDA transition while SCL is high will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake-up’ call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

NOTE: The I/O pins of CAT24Cxx do not obstruct the SCL and SDA lines if the VCC supply is switched off. During power-up, the SCL and SDA pins (connected with pull-up resistors to VCC) will follow the VCC monotonically from VSS (0 V) to nominal VCC value, regardless of pull-up resistor value. The delta between the VCC and the instantaneous voltage levels during power ramping will be determined by the relation between bus time constant (determined by pull-up resistance and bus capacitance) and actual VCC ramp rate.

**Device Addressing:**The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8_bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/W, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 3. A2, A1and A0 must match the state of the external address pins, and a10, a9 and a8 are internal address bits.

**Acknowledge:**After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9$^{th}$ clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

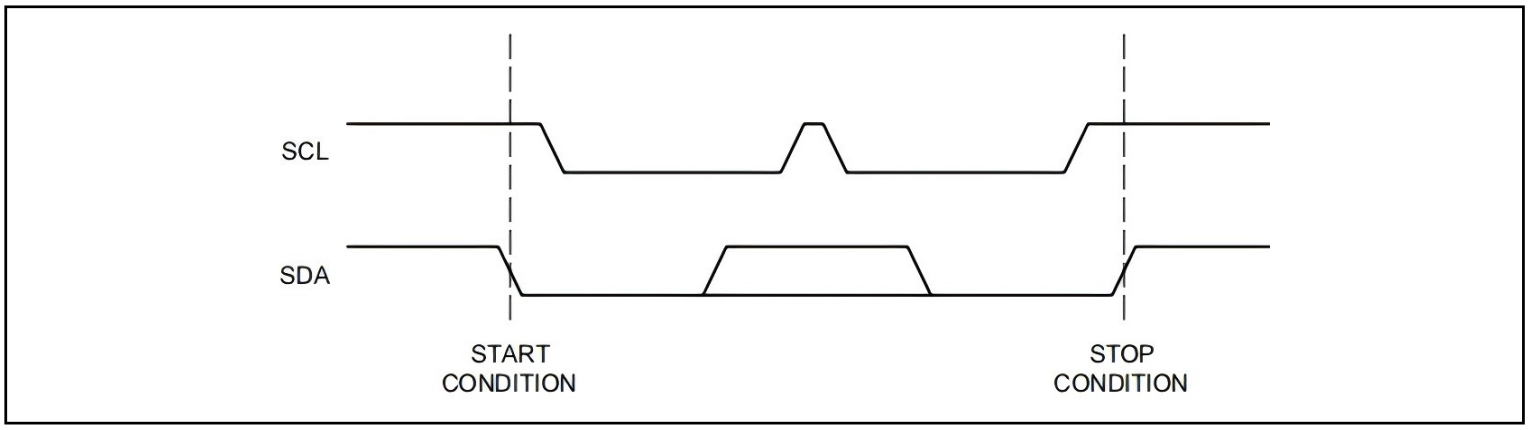



Figure 2. Start/Stop Timing

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | $A_2$ | $A_1$ | $A_0$ | R/$\overline{W}$ | CAT24C01 and CAT24C02 |
| 1 | 0 | 1 | 0 | $A_2$ | $A_1$ | $a_8$ | R/$\overline{W}$ | CAT24C04 |
| 1 | 0 | 1 | 0 | $A_2$ | $a_9$ | $a_8$ | R/$\overline{W}$ | CAT24C08 |
| 1 | 0 | 1 | 0 | $a_{10}$ | $a_9$ | $a_8$ | R/$\overline{W}$ | CAT24C16 |

Figure 3. Slave Address Bits

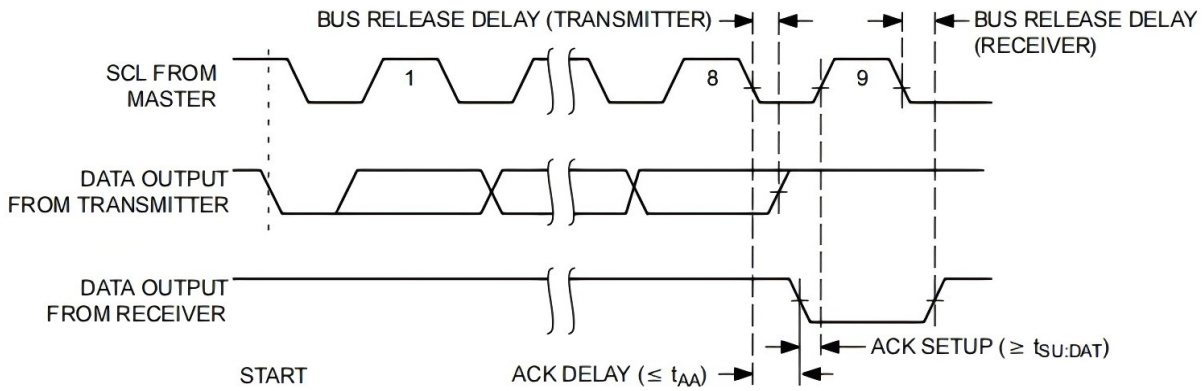



Figure 4. Acknowledge Timing

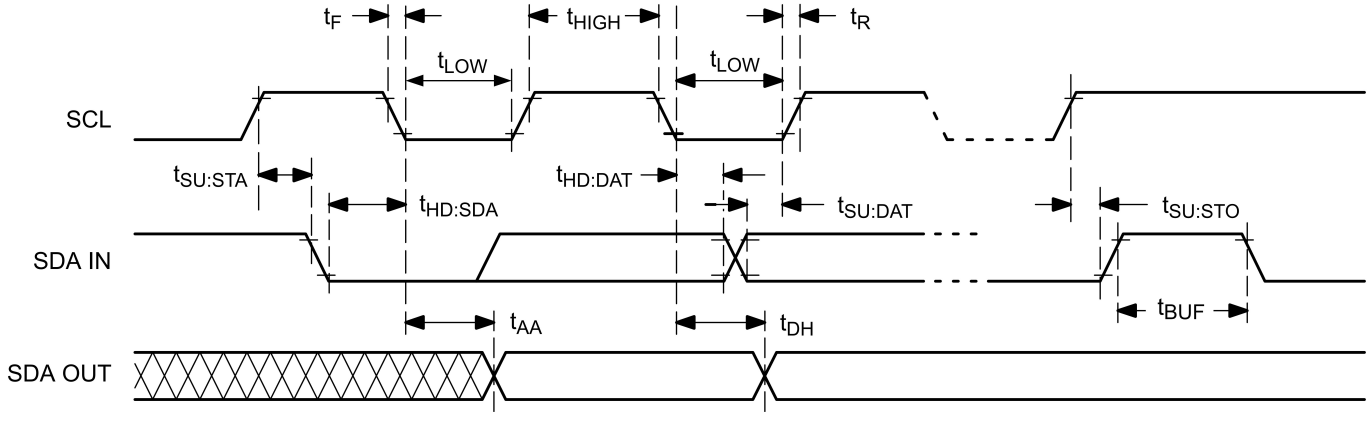



Figure 5. Bus Timing

## WRITE OPERATIONS

**Byte Write:**In Byte Write mode, the Master sends the START condition and the Slave address with the R/W bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24Cxx. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAT24Cxx device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 6). While this internal cycle is inprogress (tWR), the SDA output will be tri-stated and the CAT24Cxx will not respond to any request from the Master device (Figure 7).

**Page Write :**The CAT24Cxx writes up to 16 bytes of data in a single write cycle, using the Page Writeoperation (Figure 8). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send upto fifteen additional bytes. After each byte has been transmitted the CAT24Cxx will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter wraps around ’ to the beginning of page and previously transmitted data will be overwritten. Once allsixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAT24Cxx in a single write cycle.

**Acknowledge Polling:**The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host ’ s write operation, the CAT24Cxx initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24Cxx is still busy with the write operation, NoACK will be returned. If the CAT24Cxx has completed the internal write operation, an ACK will be returned and the host can then proceed withthe next read or write operation.

**Hardware Write Protection :**With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24Cxx. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24Cxx will not acknowledge the data byteand the Write request will be rejected.

**Delivery State:**The CAT24Cxx is shipped erased, i.e., all bytes are FFh.

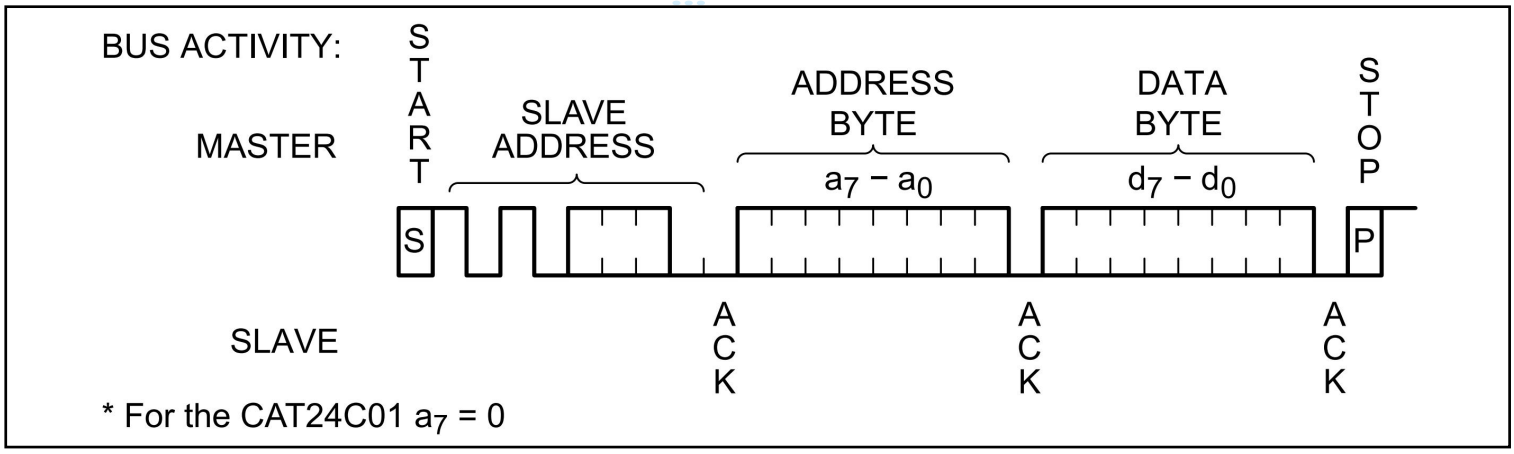



Figure 6. Byte Write Sequence

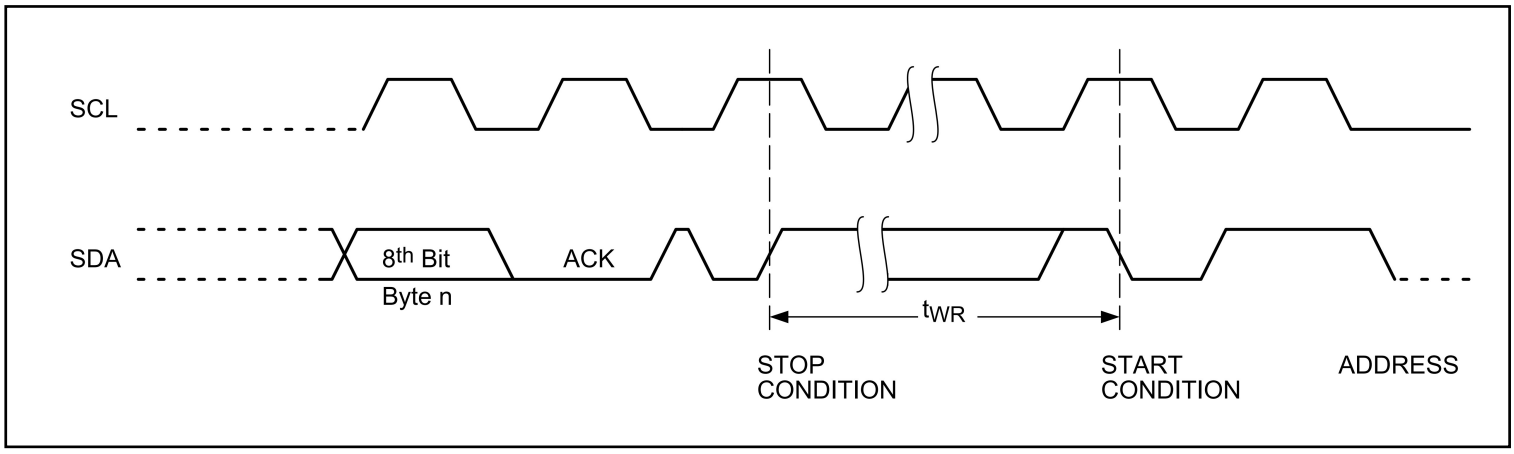



Figure 7. Write Cycle Timing

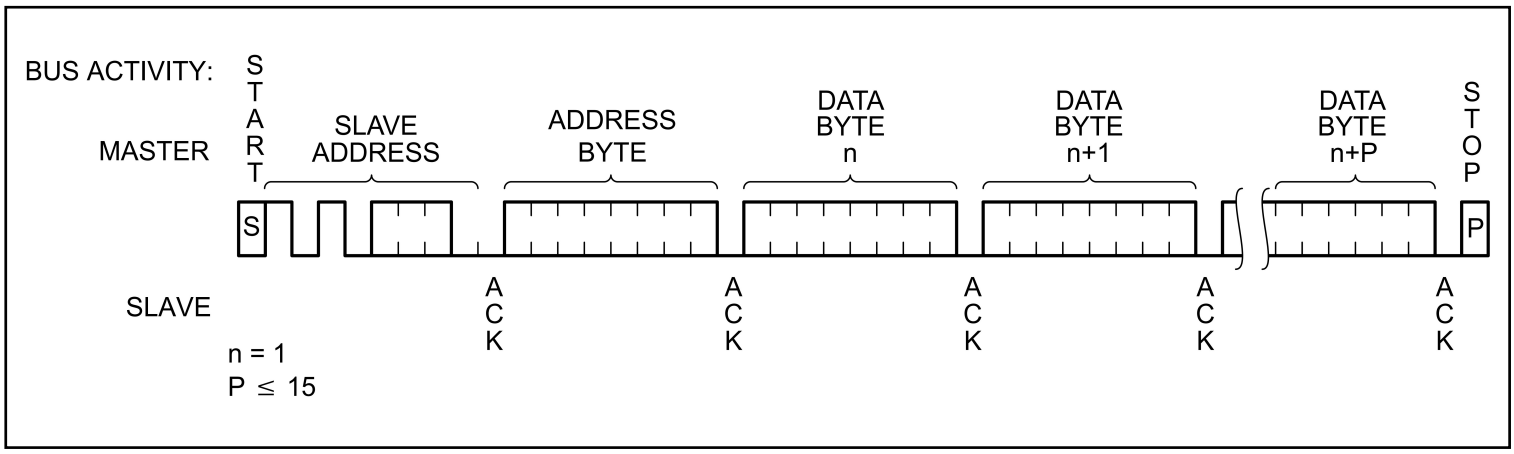



Figure 8. Page Write Sequence

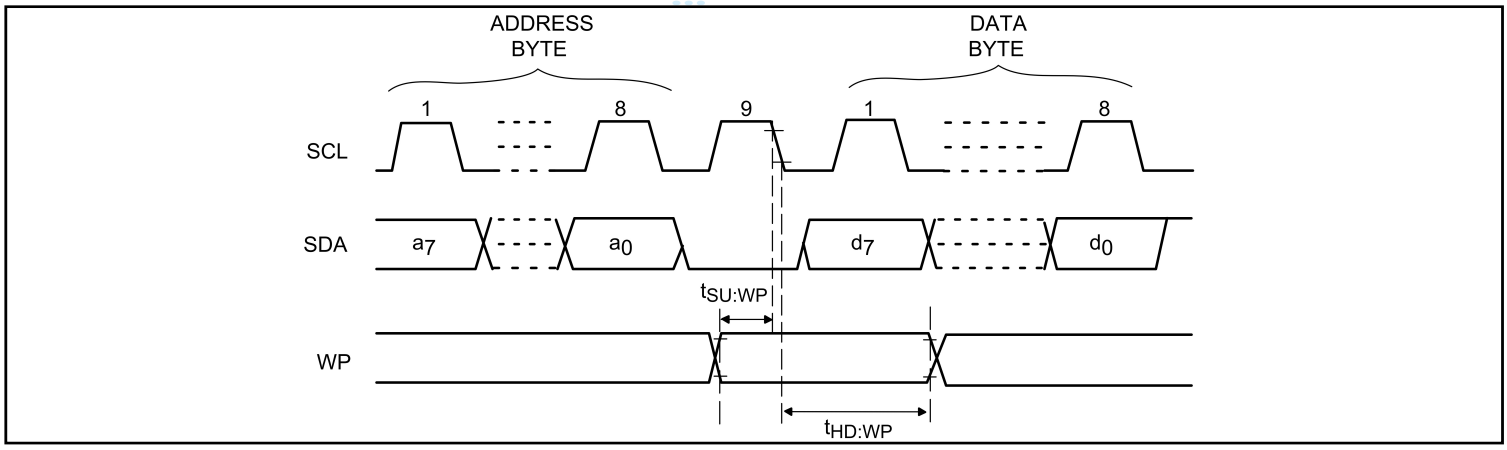



Figure 9. WP Timing

## READ OPERATIONS

**Immediate Read:**Upon receiving a Slave address with the R/W bit set to ‘1’, the CAT24Cxx will interpret this as arequest for data residing at the current byte address in memory. The CAT24Cxx willacknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24Cxx returns to Standby mode.

**Selective Read:**Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte address of the location it wishes to read. After theCAT24Cxx acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/W bit set to one. The CAT24Cxx then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

**Sequential Read:**If during a Read session, the Master acknowledges the 1st data byte, then the CAT24Cxx will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wraparound at end of memory (rather than end of page). In the CAT24C01, the internal address count will not wrap around at the end of the 128 byte memory space.

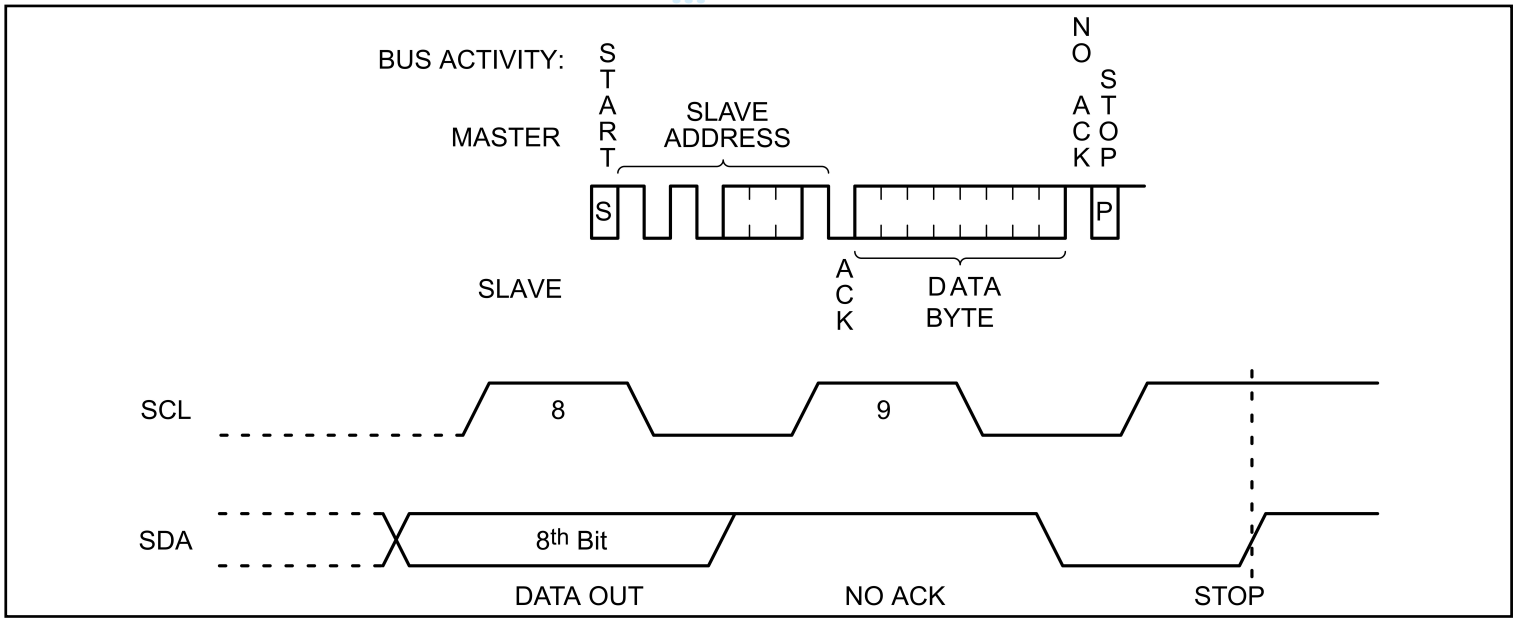



Figure 10. Immediate Read Sequence and Timing

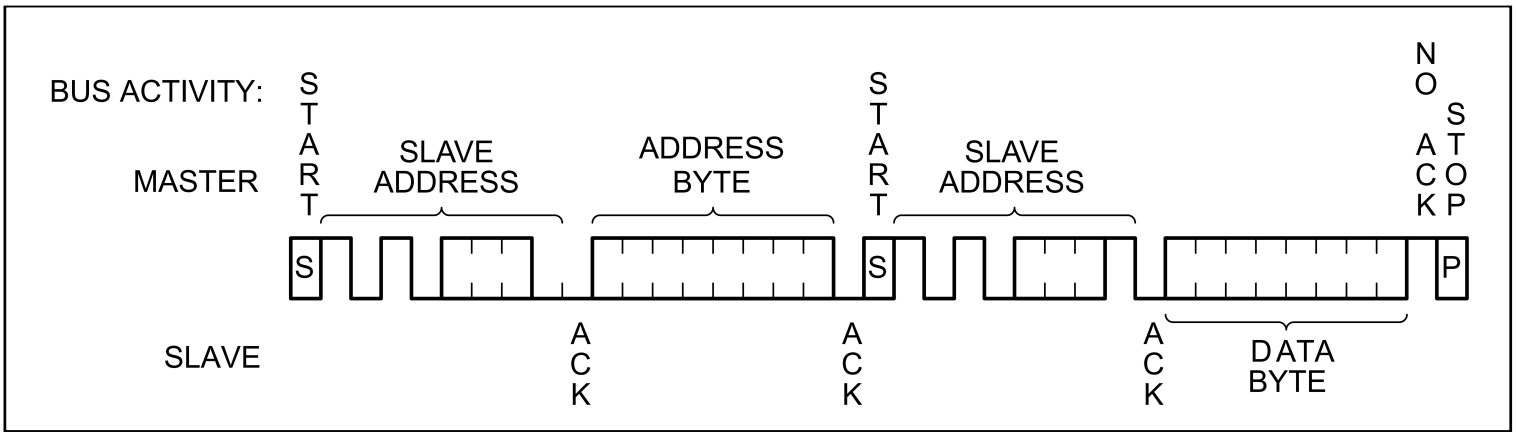



Figure 11. Selective Read Sequence

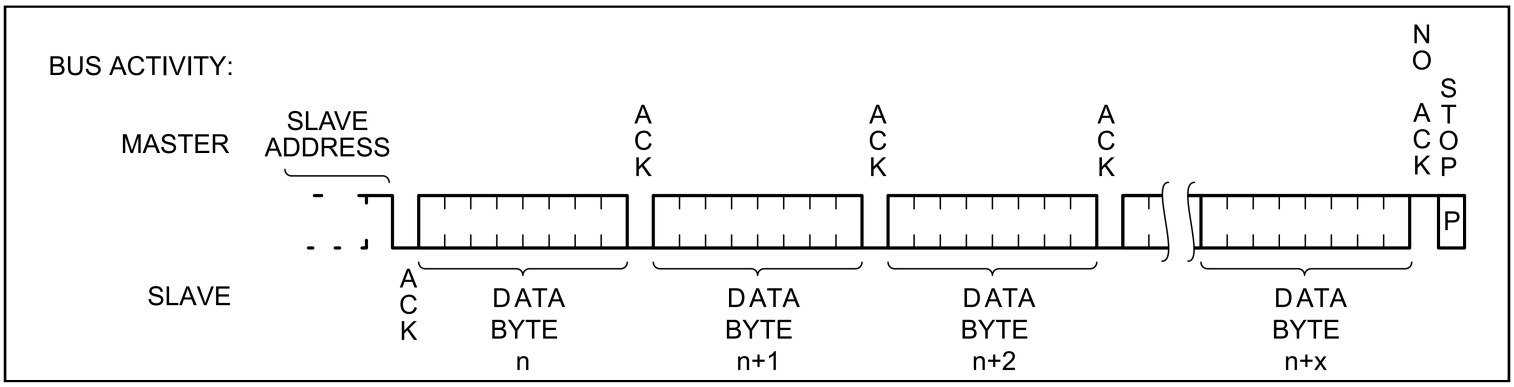



Figure 12. Sequential Read Sequence

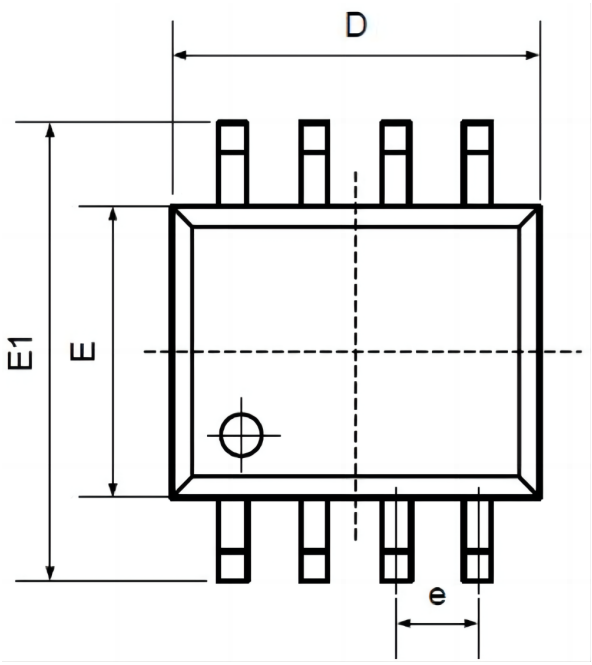
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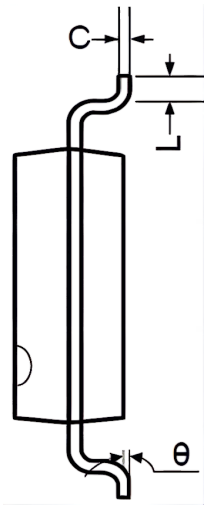
| Order Number | Package | Package Quantity | Marking On The park | Temperature |
|---|---|---|---|---|
| CAT24C01TDI-GT3-TUDI | SOT23 | Tape,Reel,3000 | MM | -40°C to 85°C |
| CAT24C01WI-GT3-TUDI | SOP8 | Tape,Reel,4000 | 24C01WI | |
| CAT24C01YI-GT3A-TUDI | TSSOP8 | Tape,Reel,4000 | 24C01Y | |
| CAT24C02TDI-GT3A-TUDI | SOT23 | Tape,Reel,3000 | C01 | |
| CAT24C02WI-GT3-TUDI | SOP8 | Tape,Reel,4000 | 24C02WI | |
| | | | 24C02H | |
| CAT24C02YI-GT3A-TUDI | TSSOP8 | Tape,Reel,4000 | 24C02Y | |
| | | | C02H | |
| CAT24C04WI-GT3-TUDI | SOP8 | Tape,Reel,4000 | 24C04WI | |
| | | | 24C04K | |
| CAT24C04YI-GT3A-TUDI | TSSOP8 | Tape,Reel,4000 | 24C04Y | |
| CAT24C08WI-GT3-TUDI | SOP8 | Tape,Reel,4000 | 24C08WI | |
| | | | 24C08K | |
| CAT24C08YI-GT3A-TUDI | TSSOP8 | Tape,Reel,4000 | 24C08Y | |
| CAT24C16WI-GT3-TUDI | SOP8 | Tape,Reel,4000 | 24C16WI | |
| | | | 24C16K | |
| CAT24C16YI-GT3A-TUDI | TSSOP8 | Tape,Reel,4000 | 24C16Y | |

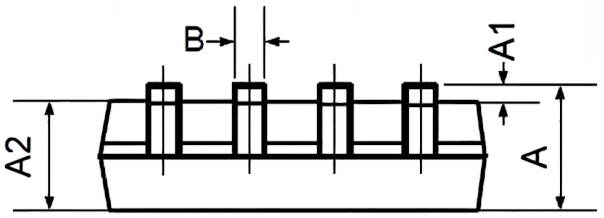
# Revision history

| | Date | Revision | Page |
|---|---|---|---|
| V1.0 | 2022/12 | New | 1-18 |
| V1.1 | 2024/8 | Update model and PDF template | 1-18 |

# Package SOP8

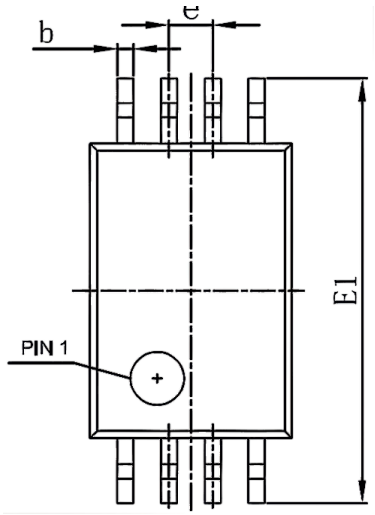


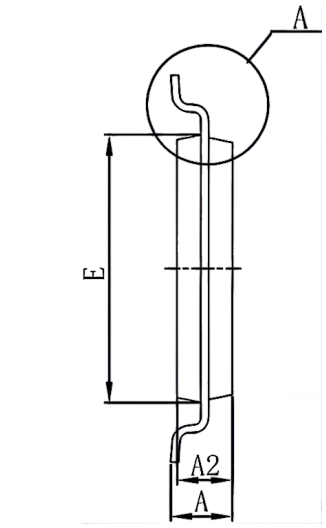



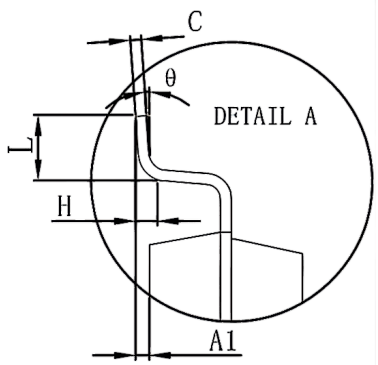



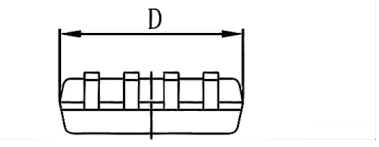

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| B | 0.330 | 0.510 | 0.013 | 0.020 |
| C | 0.190 | 0.250 | 0.007 | 0.010 |
| D | 4.780 | 5.000 | 0.188 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.248 |
| e | 1.270TYP | | 0.050TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

# Package TSSOP8



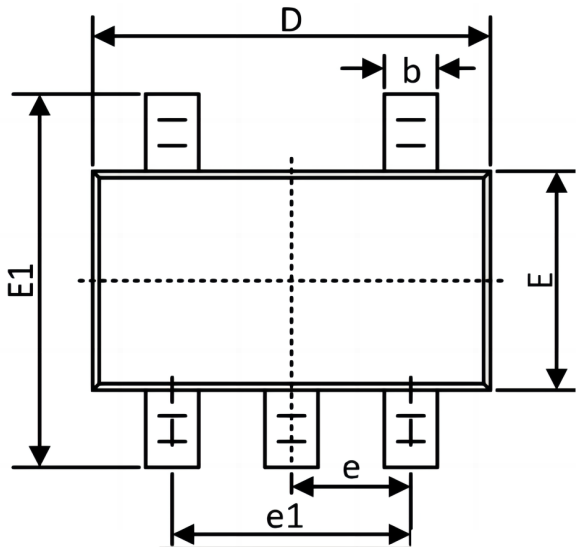



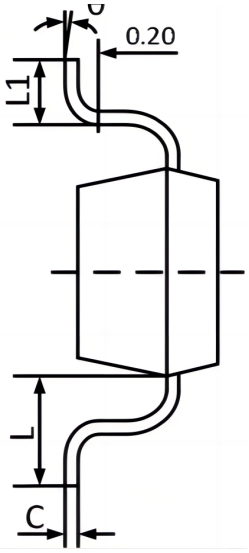



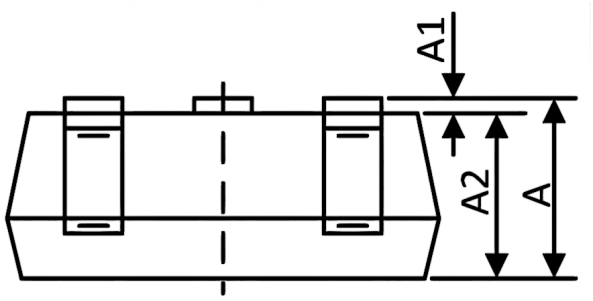




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 4.300 | 4.500 | 0.169 | 0.177 |
| b | 0.190 | 0.300 | 0.007 | 0.012 |
| C | 0.090 | 0.200 | 0.004 | 0.008 |
| E1 | 6.250 | 6.550 | 0.246 | 0.258 |
| A | | 1.200 | | 0.047 |
| A2 | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| e | 0.65(BSC) | | 0.026(BSC) | |
| L | 0.500 | 0.700 | 0.020 | 0.028 |
| H | 0.25(TYP) | | 0.01(TYP) | |
| θ | 1° | | 1° | |

# Package SOT23-5




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.050 | 1.250 | 0.041 | 0.049 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 1.050 | 1.150 | 0.041 | 0.045 |
| b | 0.300 | 0.400 | 0.012 | 0.016 |
| C | 0.100 | 0.200 | 0.004 | 0.008 |
| D | 2.820 | 3.020 | 0.111 | 0.119 |
| E | 1.500 | 1.700 | 0.059 | 0.067 |
| E1 | 2.650 | 2.950 | 0.104 | 0.116 |
| e | 0.950TYP | | 0.037TYP | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.700REF | | 0.028REF | |
| L1 | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

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