NOVOSENSE

NSOPA240x
36-V Rail-to-Rail Input/Output, Automotive Operational Amplifier with High Current Output for Resolver Drive

Datasheet (EN) 1.1

Product Overview

The NSOPA2401/NSOPA2402 are single/dual CMOS operational amplifier combined full swing input and output. Current limiting and over temperature detection enhance overall system robustness when driving analog signals over wires that are susceptible to faults.

It outputs typically up to 400mA of peak-to-peak current to drive low resistance load including inductance load such as angle resolver, lineout cable and piezo actuator. In addition, it has enhanced RF noise immunity.

Key Features

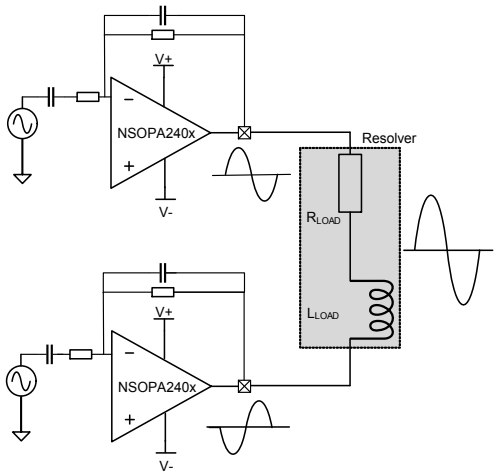
- AEC Q-100 Qualified for Grade 1: T_A from –40 °C to 125 °C
- Wide power supply voltage range: 4.5V to 36V
- High output current drive: 400mA continuous, Replaces discrete op amps and transistors
- Output current limit
- Over current alarm (NSOPA2402 only)
- Over temperature shutdown
- Shutdown pin for low I_Q application
- 7.5MHz gain bandwidth with 5.5V/µs slew rate
- Internal RF/EMI filter
- Package: 14-pin HTSSOP, 5-pin TO252
- RoHS and REACH compliance

Device Information

Part Number	Package	Body Size
NSOPA2401-Q1TOAR	TO-252-5L	6.54 mm × 6.04mm
NSOPA2402-Q1HTSKR	HTSSOP14	5.00 mm × 4.40 mm

Typical Application

- Resolver-based automative applications
- Inverter and motor control
- Motor driver
- Liner power booster
- Servo drive power stage module



Typical Resolver Excitation Circuit

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1. Pin Configuration and Functions

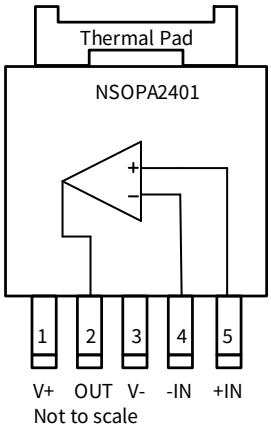

Figure 1-1 NSOPA2401 5-Pin TO252 Package Top View

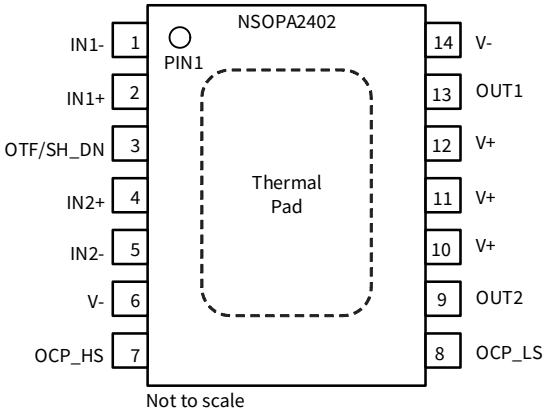

Figure 1-2 NSOPA2402 14-pin HTSSOP Package Top View

Table 1-1 NSOPA240x Pin Configuration and Description

Symbol	5-Pin TO252	14-Pin HTSSOP	*Function*
	NO.		
V-	3	6,14	Negative supply pin
IN1+	-	2	Noninverting input terminal 1
IN2+	-	4	Noninverting input terminal 2
IN1-	-	1	Inverting input terminal 1
IN2-	-	5	Inverting input terminal 1
IN+	5	-	Noninverting input terminal
IN-	4	-	Inverting input terminal
OCP_HS	-	7	Over current protection flag
OCP_LS	-	8	Over current protection flag
OTF/SH_DN	-	3	Over temperature flag and shutdown
OUT1	-	13	Amplifier output 1
OUT2	-	9	Amplifier output 2
OUT	2	-	Amplifier output
V+	1	10,11,12	Positive supply pin
Thermal pad	-	-	Connect the thermal pad to (V-) pin internally

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2. Absolute Maximum Ratings[1]

Parameters	Symbol	Min	Max	Unit
Supply Voltage	$V_S = (V_+)–(V_-)$	-0.3	40	V
Differential Input Voltage between IN+ and IN-	V_{ID}		V_S +0.3	V
Common-mode Input Voltage	V_{CM}	(V_-) - 0.3	(V_+) + 0.3	V
OTF/SH_DN pin, OCP_HS and OCP_LS voltage range	V_{OTF/SH_DN} V_{OCP_HS} V_{OSP_LS}	(V_-) - 0.3	(V_-) + 7	V
Input Current	I_{IN}	-10	+10	mA
Output Voltage	V_O	(V_-) - 0.3	(V_+) + 0.3	V
Junction Temperature	T_j	-40	150	°C
Storage Temperature	T_{stg}	-55	150	°C

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic Discharge	Human body model (HBM), AEC Q100-002	±3000	V
	Charged device model (CDM), AEC Q100-011	±2000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Supply Voltage	$V_S = (V_+) – (V_-)$	4.5	36	V
Flag Pin Voltage		2	5	V
Operating Free-Air Temperature	T_A	-40	125	°C

[1] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

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5. Thermal Information

Parameters	Symbol	HTSSOP14	TO-252-5L	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	40	35	°C/W
Junction-to-case (top) Thermal Resistance	$\theta_{JC(TOP)}$	39.9	34.6	°C/W
Junction-to-case (bottom) Thermal Resistance	$\theta_{JC(BOT)}$	2.2	9.1	°C/W
Junction-to-board Thermal Resistance	θ_{JB}	16.8	12.6	°C/W
Junction-to-top Characterization Parameter	Ψ_{JT}	3.5	6.1	°C/W
Junction-to-board Characterization Parameter	Ψ_{JB}	17.2	12	°C/W

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6. Electrical Characteristics

For $V_S = (V_+) - (V_-) = 4.5V$ to 36 V (±2.25V to ±18 V) at $T_A = 25°C$, $R_L = 10\ k\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

Parameters	*Symbol*	*Condition*		*Min*	*Typ*	*Max*	*Unit*
Input							
Input Offset Voltage	V_{OS}	$V_{CM} = (V_-)$			±1	±3.8	mV
			T_A = -40°C to 125°C			±4.3	
Input Offset Voltage Drift	dV_{OS}/dT	T_A = -40°C to 125°C			7		μV/°C
Common-Mode Input Range	V_{CM}			(V_-)		(V_+)	V
Common-Mode Rejection Ratio	CMRR	$(V_-) < V_{CM} < (V_+) - 3.5V$, $V_S = 36V$		100	125		dB
			T_A = -40°C to 125°C	90			
		$(V_-) < V_{CM} < (V_+) - 3.5V$, $V_S = 12V$		90	117		
			T_A = -40°C to 125°C	80			
		$(V_-) < V_{CM} < (V_+)$, V_S = 12 to 36V	T_A = -40°C to 125°C	60			
Input Bias Current	I_B				±500		pA
		T_A =-40°C to 125°C			±10		nA
Input Offset Current	I_{OS}				±100		pA
		T_A =-40°C to 125°C			±10		nA
Input Impedance	Z_{ID}	Common-mode			30||4		GΩ || pF
	Z_{ICM}	Differential			0.3||5		
Open-Loop Gain							
Open-loop Voltage Gain	A_{OL}	$(V_-)+0.5V < V_O < (V_+)-0.5V$, $V_S = 36V$		108	125		dB
			T_A =-40°C to 125°C	95			
		$(V_-)+0.5V < V_O < (V_+)-0.5V$, $V_S = 12V$		106	118		
			T_A =-40°C to 125°C	88			
Power Supply							
Operating Voltage Range	V_S			4.5		36	V
Power Supply Rejection Ratio	PSRR	V_S = 4.5 to 36V, $V_{CM} = (V_-)$		95	113		dB
			T_A =-40°C to 125°C	85			
		V_S = 4.5 to 12V, $V_{CM} = (V_-)$		95	110		
			T_A =-40°C to 125°C	80			
Quiescent Current Per Channel	I_q	I_O =0A, $V_{CM} = (V_-)$			5.1	8	mA
			T_A =-40°C to 125°C			8.8	
		V_{OTF/SH_DN} = 0V	T_A =-40°C to 125°C		0.5		

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Electrical Characteristics (continued)

For $V_S = (V_+) - (V_-) = 4.5V$ to 36 V (±2.25V to ±18 V) at $T_A = 25°C$, $R_L = 10\ k\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

Parameters	Symbol	Condition			Min	Typ	Max	Unit
Output								
Voltage output swing from positive rail	V_O	V_{ID} = 500mV V_S = 12 to 36V	No load, T_A =-40°C to 125°C				5	mV
			I_O =100mA			140		
				T_A =-40°C to 125°C			290	
			I_O =200mA			280		
				T_A =-40°C to 125°C			540	
Voltage output swing from negative rail	V_O	V_{ID} = 500mV V_S = 12 to 36V	No load, T_A =-40°C to 125°C				5	
			I_O =100mA			105		
				T_A =-40°C to 125°C			200	
			I_O =200mA			210		
				T_A =-40°C to 125°C			450	
Short-circuit current	I_{SC}	Sink, Vs = 36V				630		mA
		Source, Vs = 36V				640		
Noise (Input Referred)								
Input voltage noise density	e_n	f = 1kHz				58		nV/$\sqrt{Hz}$
		f = 10kHz				20		
Input voltage noise	e_{np-p}	f =0.1Hz to 10Hz				20		µVpp
Frequency Response								
Gain-bandwidth product	GBP	V_S =36V, R_L = 100Ω				7.5		MHz
Phase margin	PM	G =+1, C_L = 10pF				75		degree
Settling time	t_S	To 0.1% 10V step, G = +1, C_L = 10pF				2.5		µs
		To 0.1% 10V step, G = -1, C_L = 10pF				2.5		
Slew rate	SR	V_S = 36V, G = +1,10V step, R_L = 100Ω				5.5		V/µs
Total harmonic distortion + noise	THD+N	V_O = 10Vpp, G =+1, f = 10 kHz, R_L = 100 Ω				-95		dB
Overload recovery time		V_{IN} × Gain > V_S				0.65		µs
EMI rejection ratio	EMIRR	f = 1GHz				90		dB
Temperature								
Thermal shutdown						173		°C
Thermal shutdown recovery						155		
Flag Pin								
Enable input voltage	V_{IH_OTF}	V_{PULL_UP} = (V-) + 5V, R_{PULL_UP} = 2.5kΩ			1			V
Disable input voltage	V_{IL_OTF}	V_{PULL_UP} = (V-) + 5V, R_{PULL_UP} = 2.5kΩ					0.3	
Over temperature and current pin output flag low voltage	V_{OL_Flag}	V_{PULL_UP} = (V-) + 5V, R_{PULL_UP} = 2.5kΩ					0.3	

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7. Typical Performance Characteristics

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

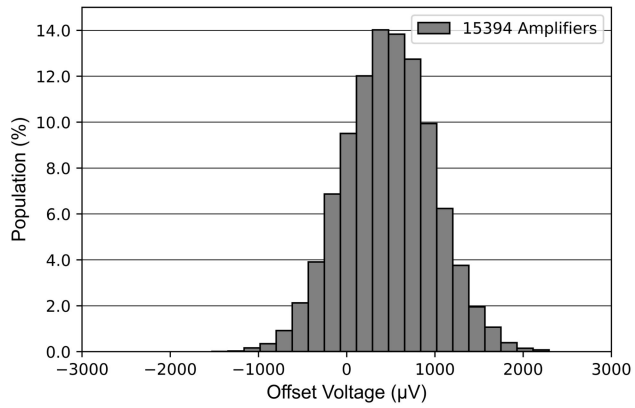

Figure 7-1 offset Voltage distribution, $V_{CM} = (V_-)$

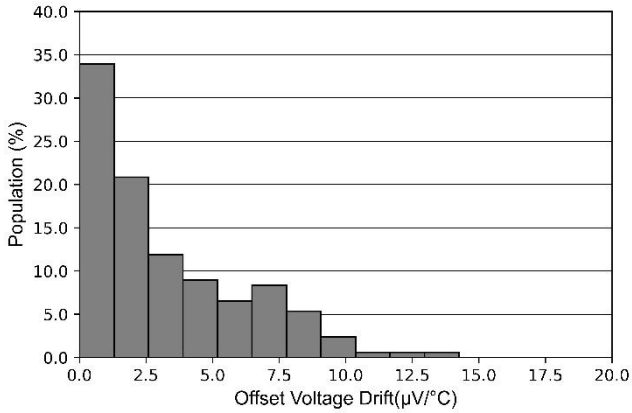

Figure 7-2 Offset Voltage Drift Distribution, $V_{CM} = (V_-)$

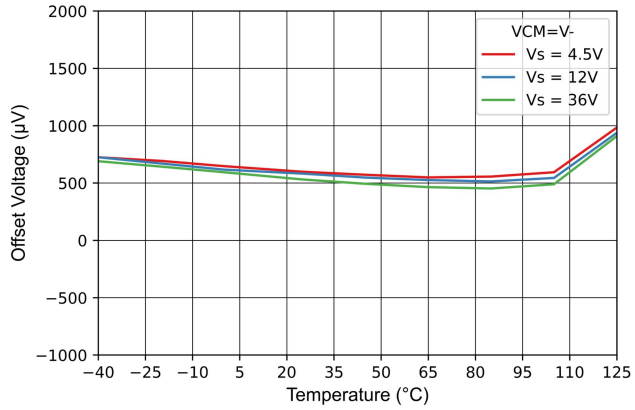

Figure 7-3 Offset Voltage vs Temperature

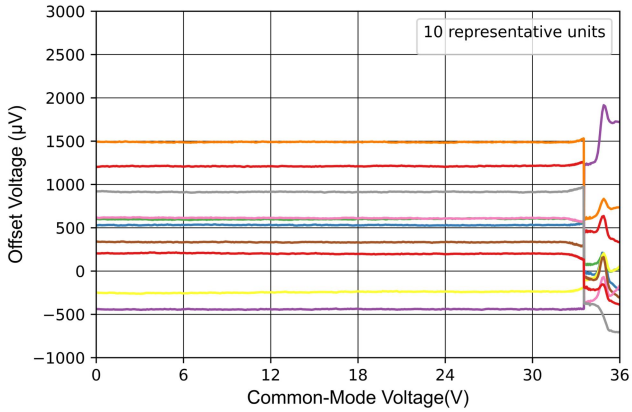

Figure 7-4 Offset Voltage vs Common-Mode Voltage

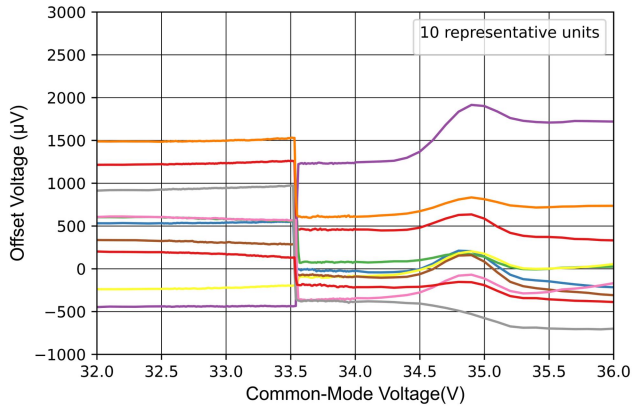

Figure 7-5 Offset Voltage vs Common-Mode Voltage, Transition

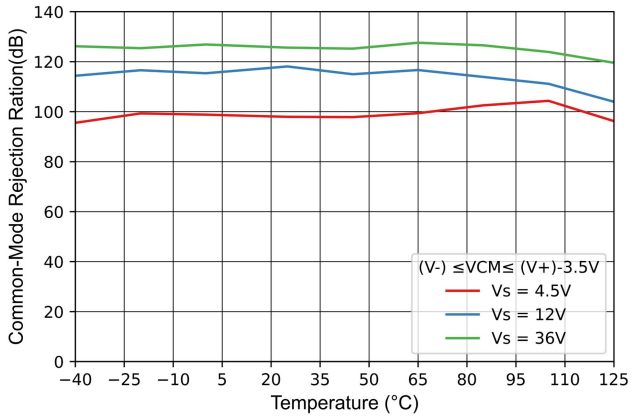

Figure 7-6 Common-Mode Rejection Ration vs Temperature

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

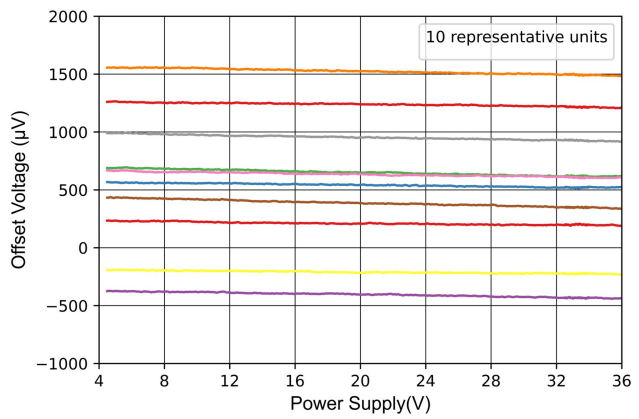

Figure 7-7 Offset Voltage vs Supply Voltage

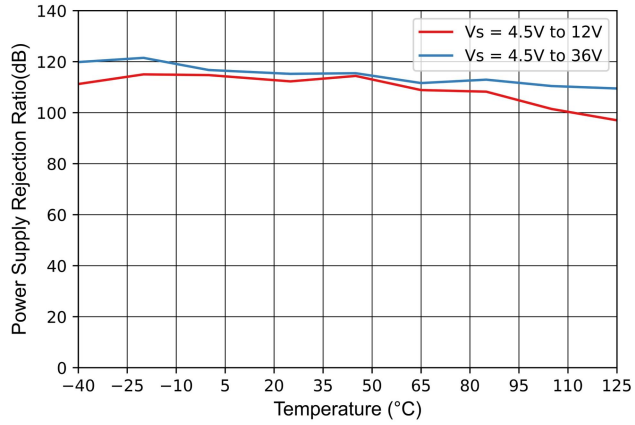

Figure 7-8 Power Supply Rejection Ratio vs Temperature

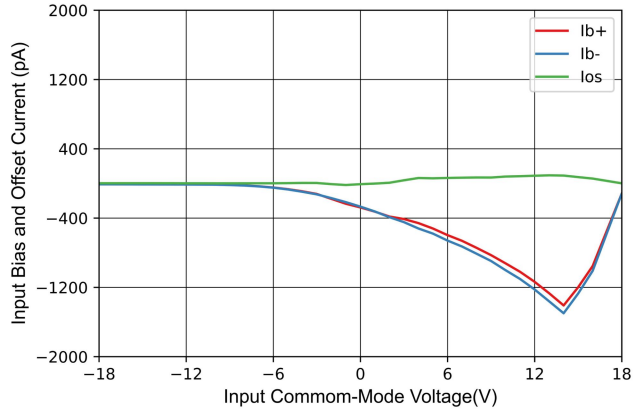

Figure 7-9 Input Bias Current vs Common-Mode

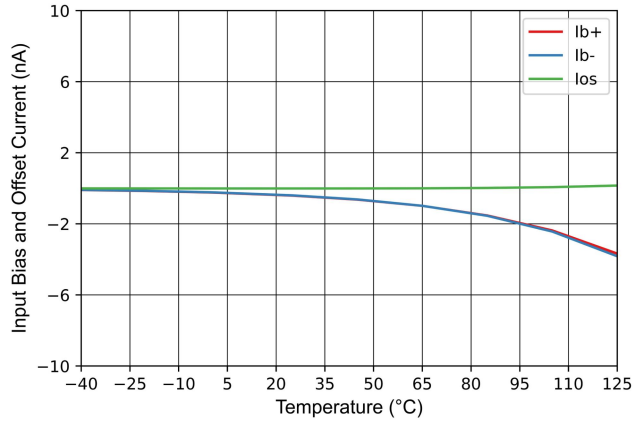

Figure 7-10 Input Bias Current vs Temperature

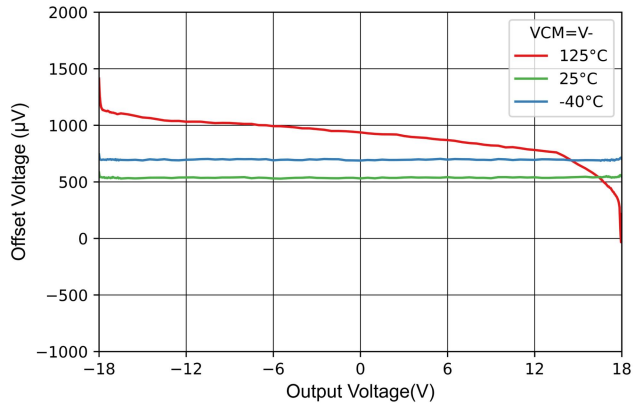

Figure 7-11 Offset Voltage vs Output Voltage

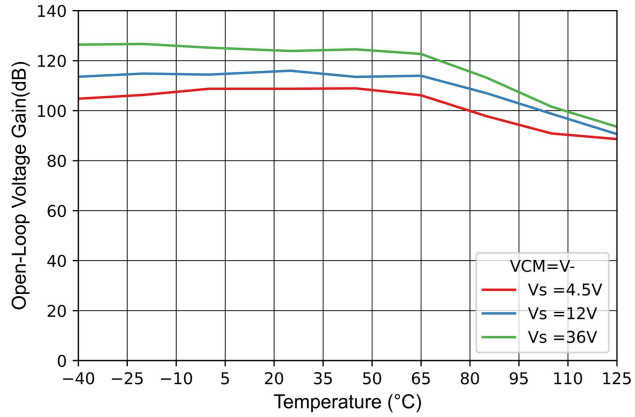

Figure 7-12 Open-Loop Voltage Gain vs Temperature

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

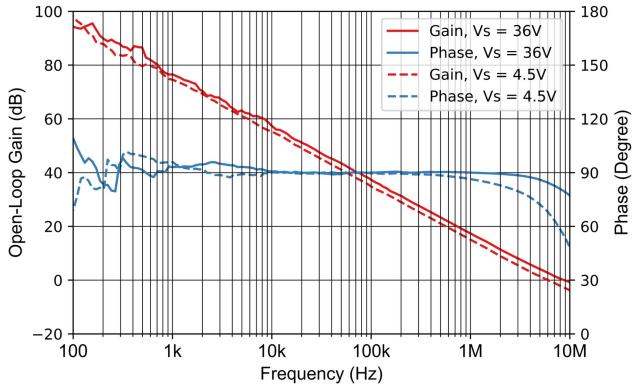

Figure 7-13 Open-Loop Gain vs Frequency

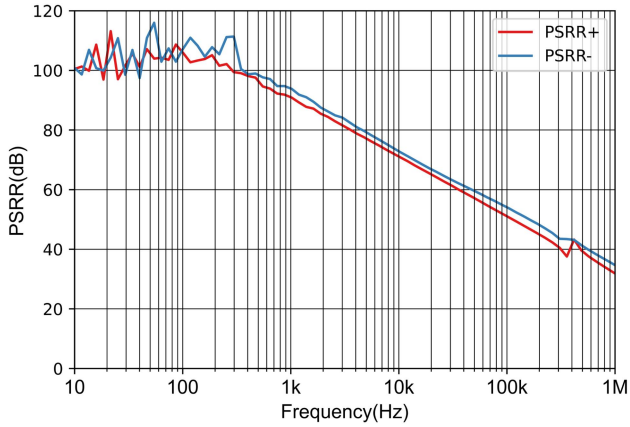

Figure 7-14 PSRR vs Frequency

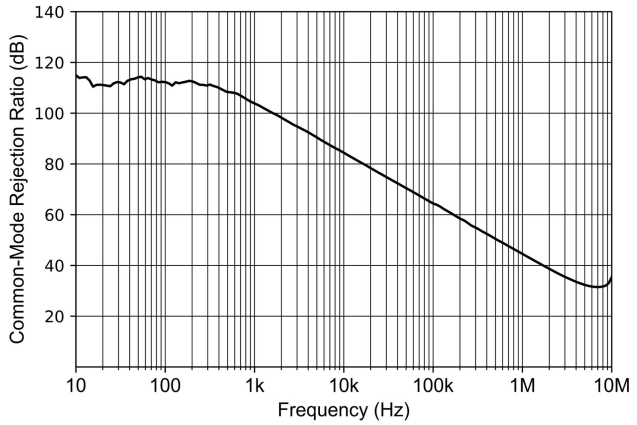

Figure 7-15 CMRR vs Frequency

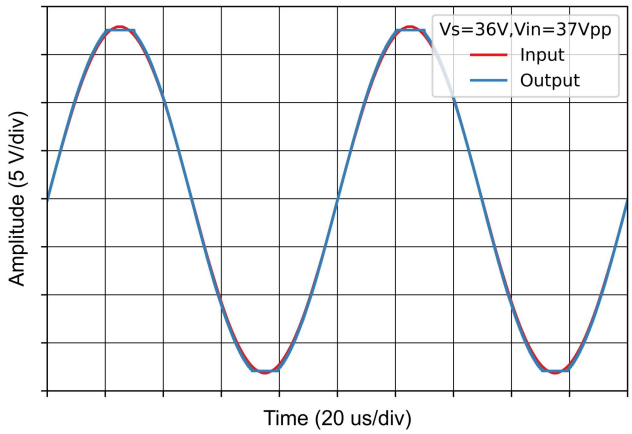

Figure 7-16 No Phase Reversal

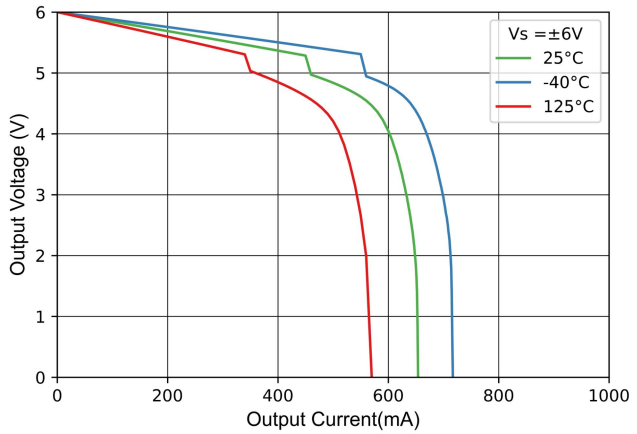

Figure 7-17 Output Voltage Swing vs Output Source Current

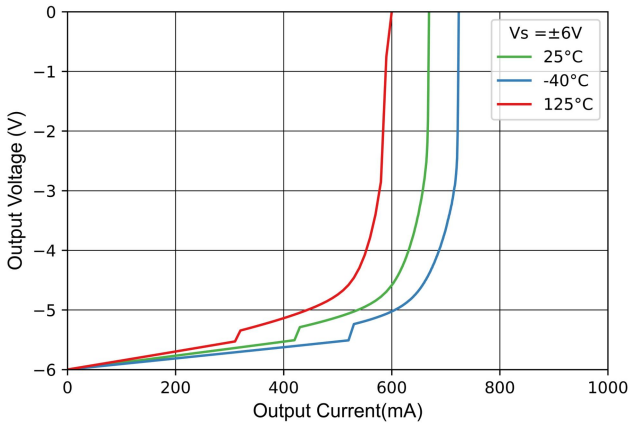

Figure 7-18 Output Voltage Swing vs Output Sink Current

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Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

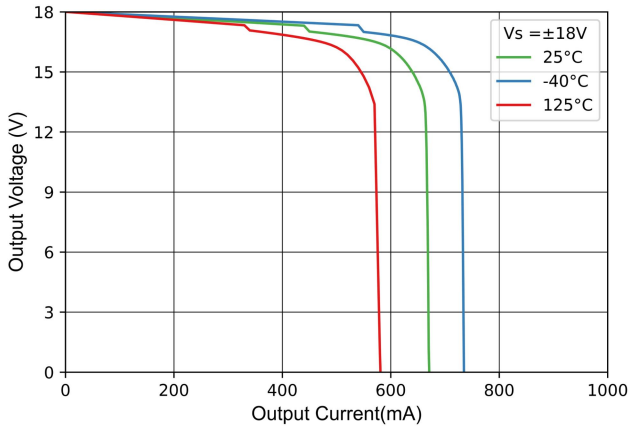

Figure 7-19 Output Voltage Swing vs Output Source Current

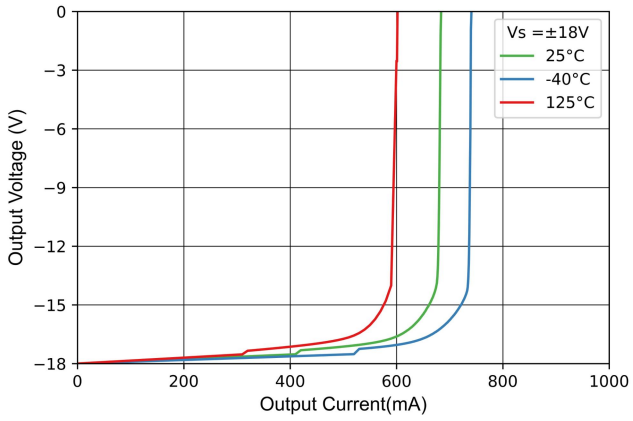

Figure 7-20 Output Voltage Swing vs Output Sink Current

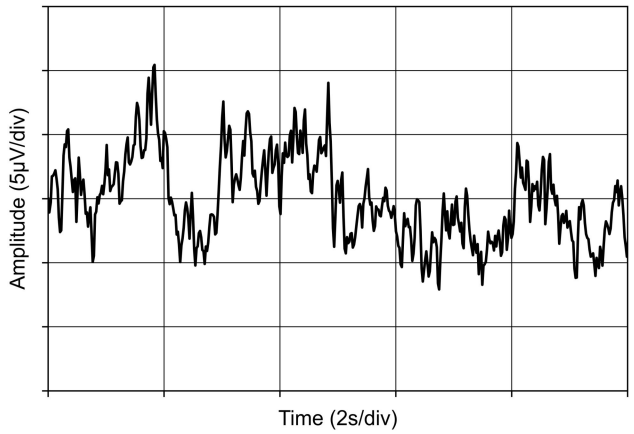

Figure 7-21 0.1 to 10 Hz noise

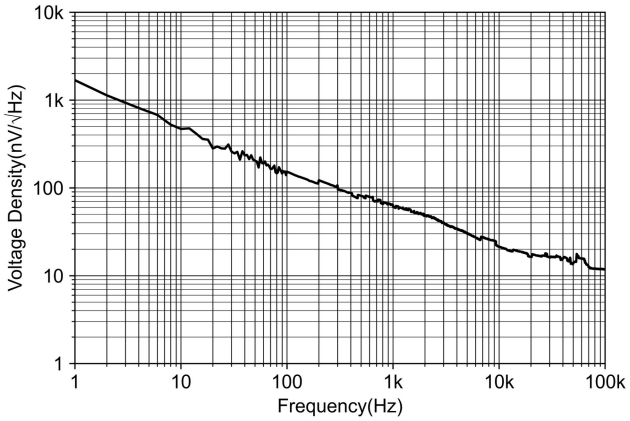

Figure 7-22 Input Voltage spectral Density

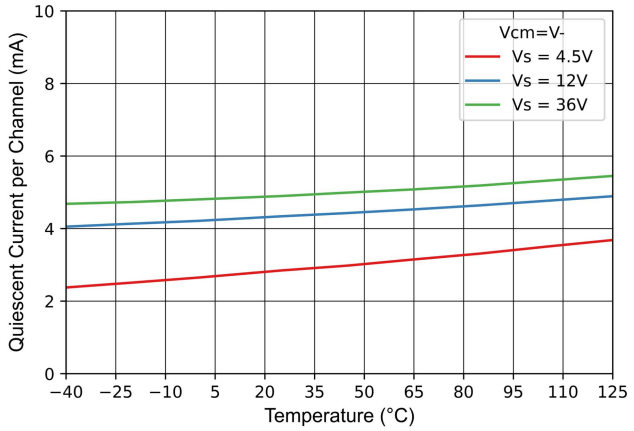

Figure 7-23 Quiescent Current vs Temperature

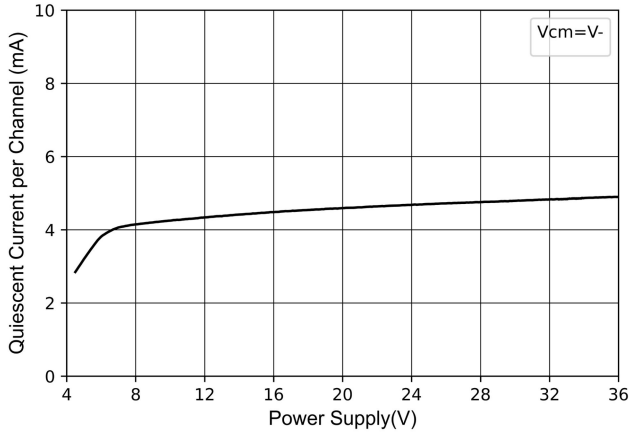

Figure 7-24 Quiescent Current vs Supply Power

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Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

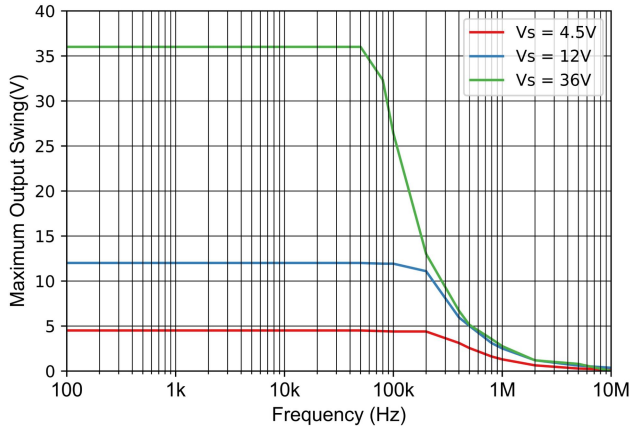

Figure 7-25 Maximum Output Voltage vs Frequency

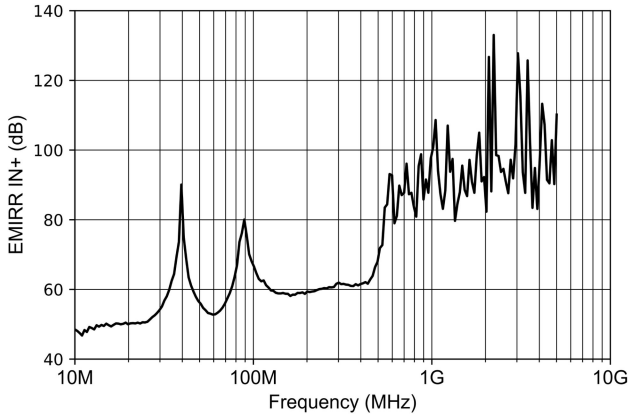

Figure 7-26 EMIRR vs Frequency

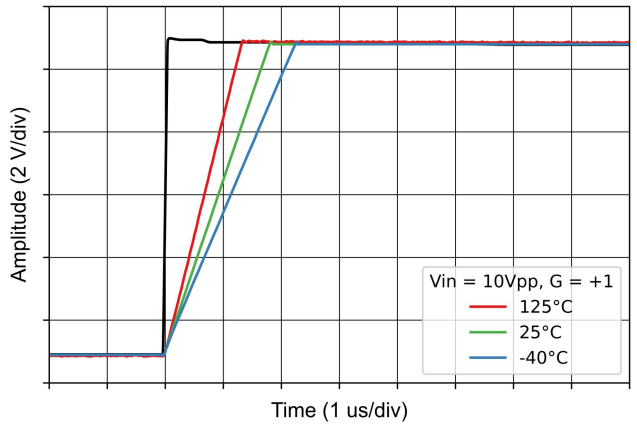

Figure 7-27 Large-Signal Step Response (Rising)

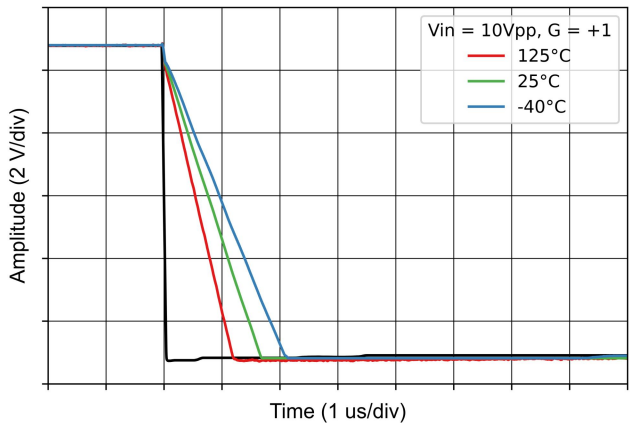

Figure 7-28 Large-Signal Step Response (Falling)

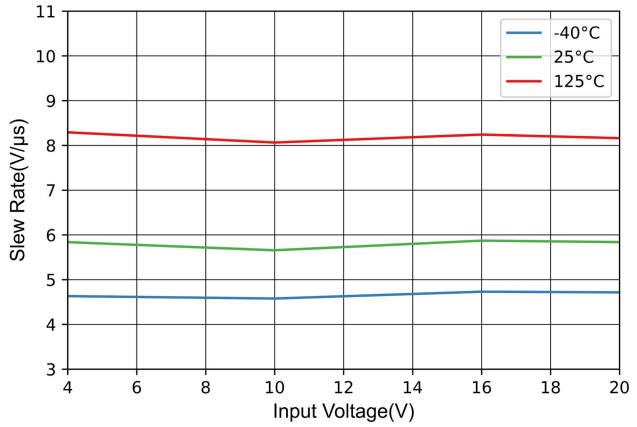

Figure 7-29 Slew Rate vs Input Amplitude

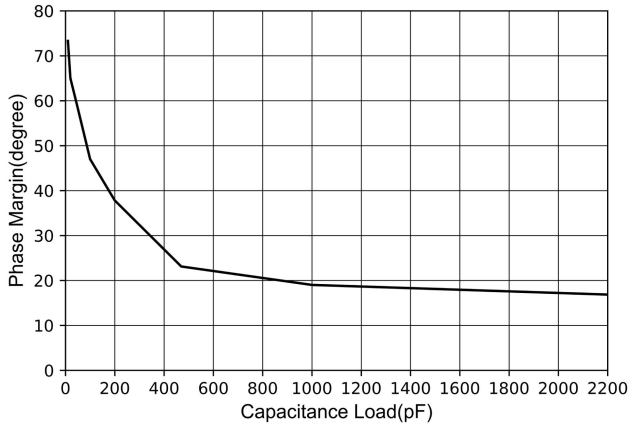

Figure 7-30 Phase Margin vs Capacitance Load

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Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 36$ V (±18 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

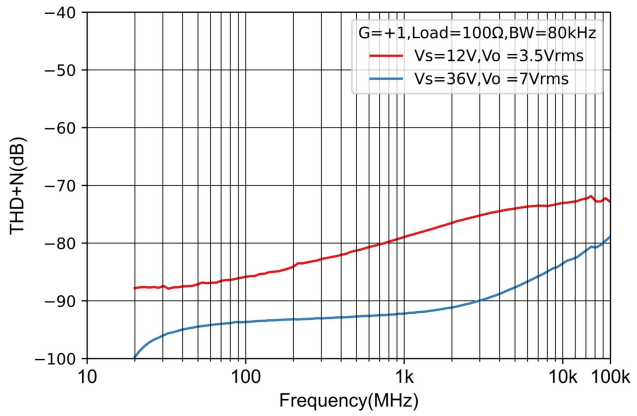

Figure 7-31 THD + N vs Frequency

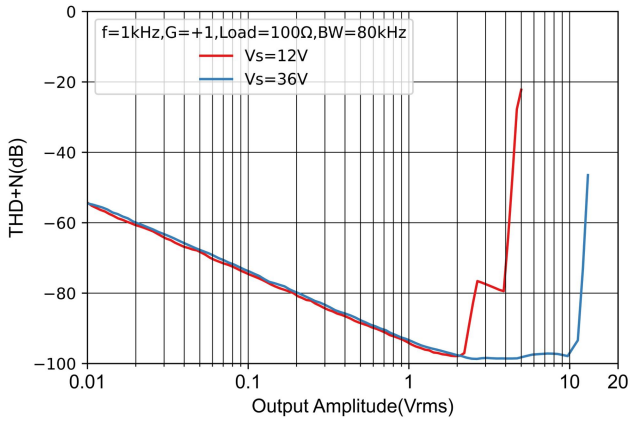

Figure 7-32 THD + N vs Amplitude

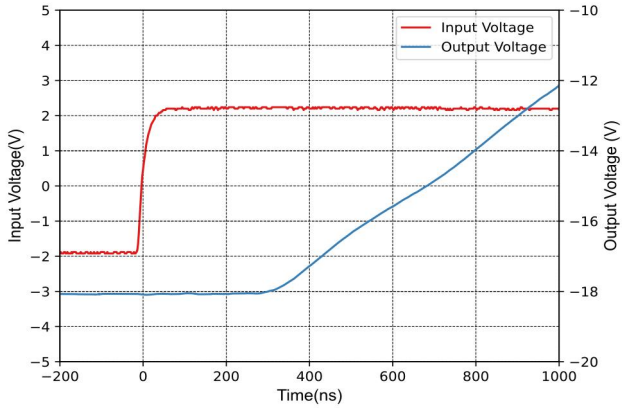

Figure 7-33 Overload Recovery Time (positive edge)

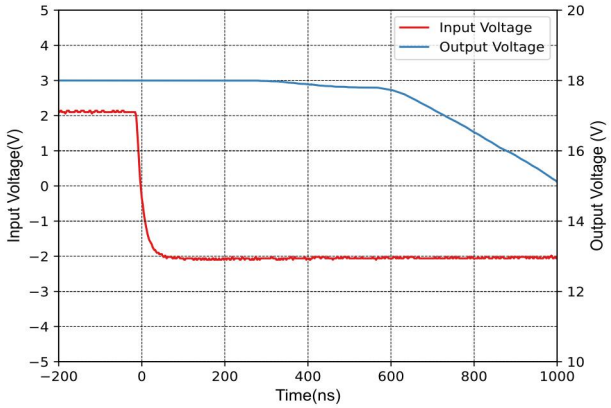

Figure 7-34 Overload Recovery Time (negative edge)

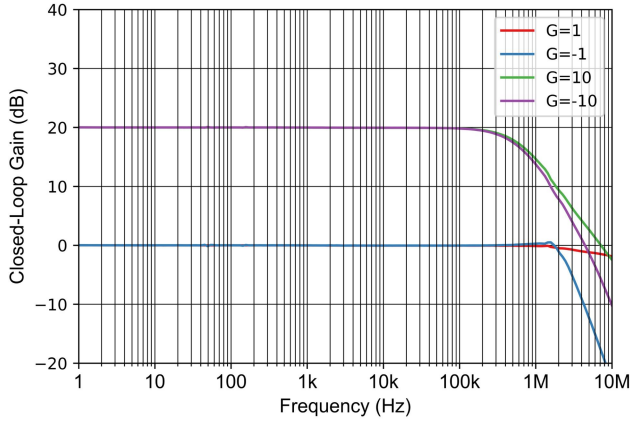

Figure 7-35 Close-Loop Gain vs Frequency

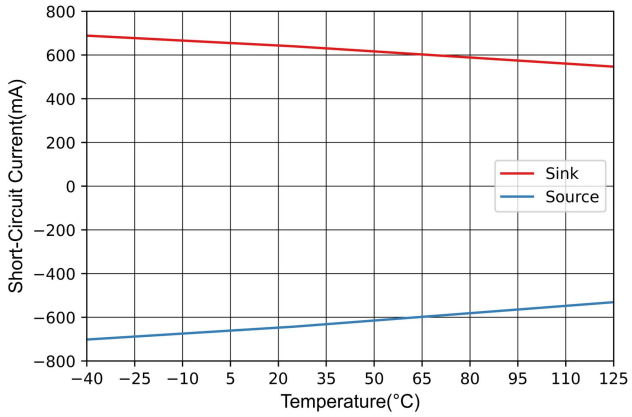

Figure 7-36 Output Short-Circuit Current vs Temperature

8. Function Description

8.1. Overview

NSOPA240x is power op amp which is dedicated for automotive applications. High output current and FPBW capability are the key features. In addition, protection functionality makes it safe in the overtemperature and overcurrent application.

8.2. Functional Block Diagram

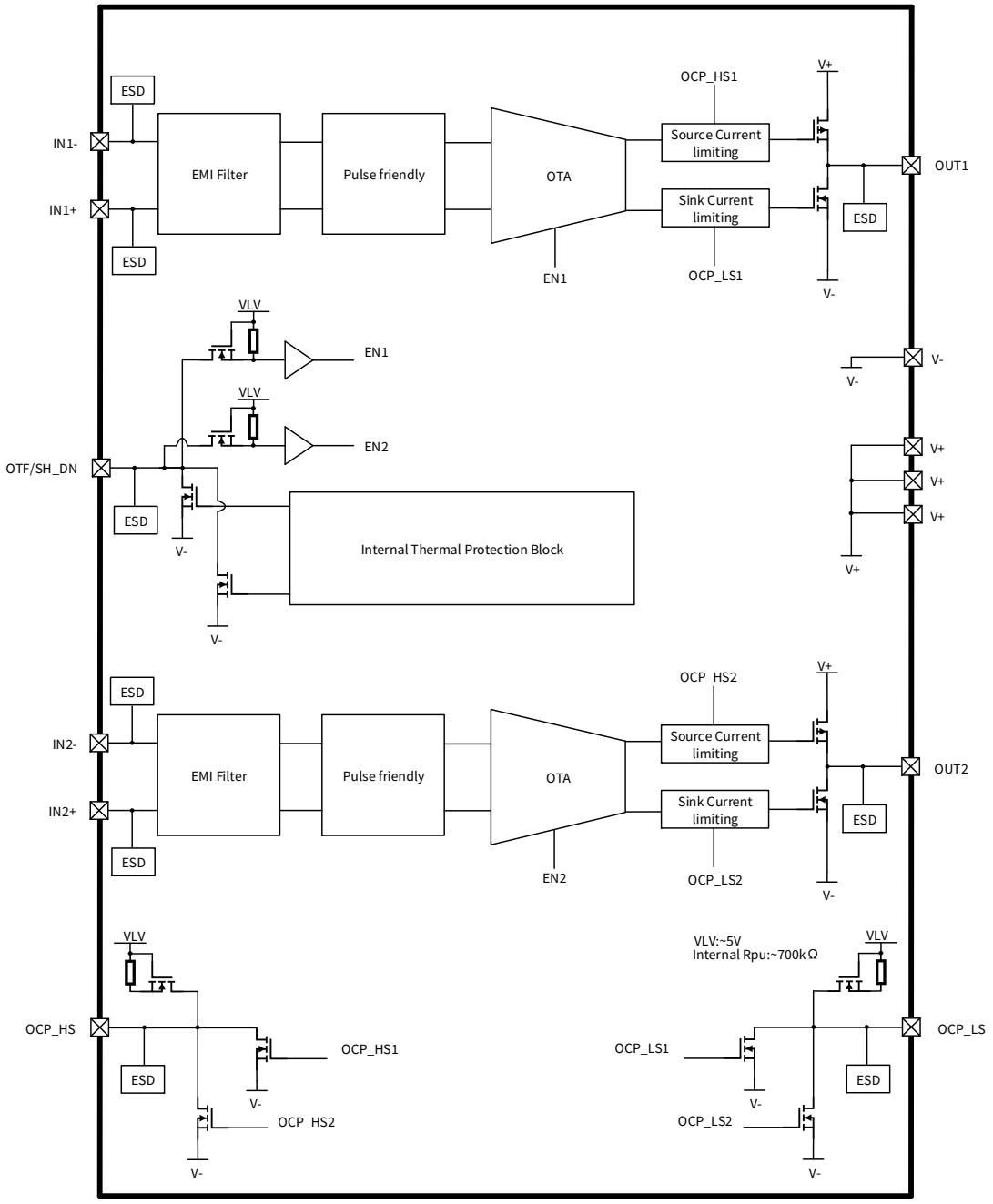

Figure 8-1 NSOPA2402 Functional Block Diagram

8.3. Feature Description

8.3.1. Pulse Friendly

Traditional op amps use back-to-back diode input stages to limit the differential input range. If the device operates in open-loop conditions, once the voltage between the two input pins exceeds the limit voltage, unexpected current will flow into the device and may cause device damage.

Using new input stage topology, NSOPA240x provides full 36V differential input range. when it works in open-loop case, it will not sink large current from source and behave as the comparator for most applications.

A majority of electrical characteristics are verified in negative feedback, closed-loop configurations. Certain dc electrical characteristics, like offset, may have a higher drift across temperature and lifetime when continuously operated in open loop over the lifetime of the device.

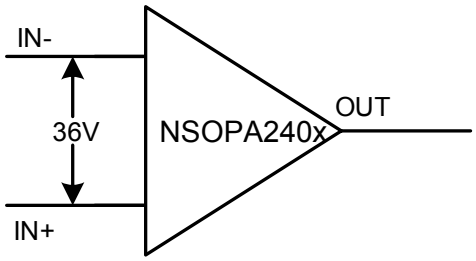

Figure 8-2 NSOPA240x Input Stage

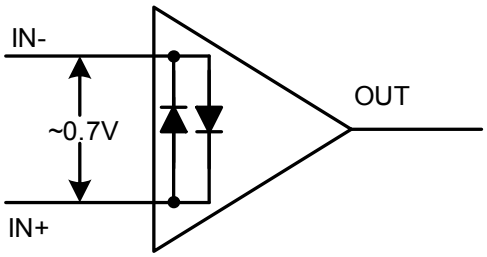

Figure 8-3 Traditional op-amp Input Stage

8.3.2. Common-Mode Input Stage

The NSOPA240x is a 36V true rail-to-rail input op amp with an input common-mode range of 100mV beyond either supply rail. This wide range is achieved by paralleling complementary N-channel and P-channel differential input pairs, as shown in Figure 8-4. N-channel pairs are active when the input voltage is close to the positive supply rail, typically – 1 V to 100 mV above the positive supply (V+). The P-channel pair is active over an input range from 100 mV below the negative supply to approximately (V+) – 2.5 V. There is a small transition region, typically (V+) – 2.5 V to (V+) – 1 V, where both input pairs are on. This transition region will vary slightly with process variations, and within this region, PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

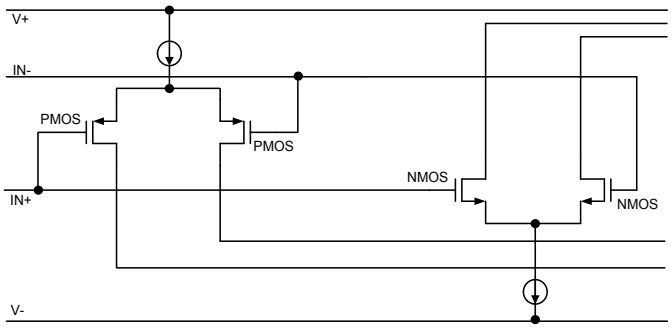

Figure 8-4 NSOPA240x Rail-to-rail Input Stage

8.3.3. EMI Rejection

The NSOPA240x uses integrated electromagnetic interference (EMI) filtering to reduce the impact of EMI from sources such as wireless communications and densely populated circuit boards that mix analog signal chains and digital components. The advantage of NSOPA240x is that EMI immunity can be improved through circuit design technology. Figure 8-5 shows the test results on NSOPA240x.

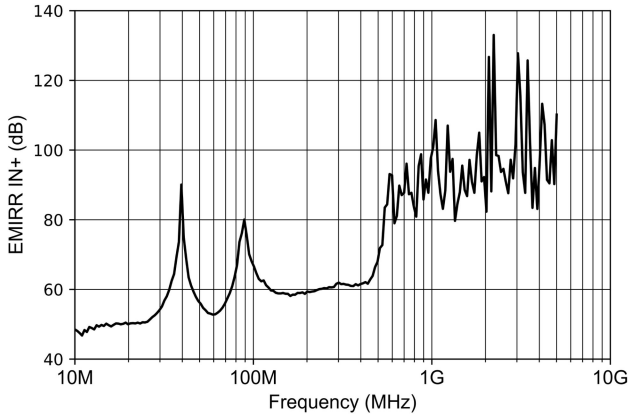

Figure 8-5 NSOPA240x EMIRR vs Frequency

8.3.4. Drive Capacitive Load

The NSOPA240x has a resistive output stage capable of driving moderate capacitive loads, and by utilizing isolation resistors, the device can be easily configured to drive large capacitive loads. The specific op amp circuit configuration, layout, gain, and output loading are important factors in determining whether the amplifier will operate stably Some factors to consider.

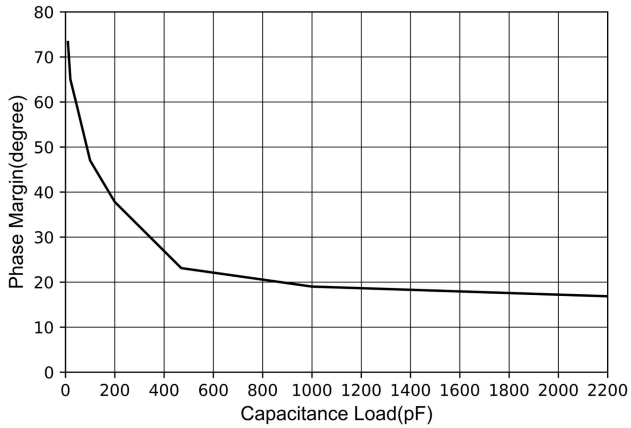

Figure 8-6 NSOPA240x Phase Margin vs Capacitive Load

To obtain additional drive capability in a unity-gain configuration, capacitive load drive can be improved by inserting a small resistor, R_{ISO}, in series with the output, as shown in Figure 8-7. This resistor significantly reduces ringing and maintains DC performance under purely capacitive loads. However, if a resistive load is placed in parallel with a capacitive load, a voltage divider is created, which introduces a gain error at the output and slightly reduces the output swing. The error introduced is proportional to the ratio R_{ISO}/R_L and is usually negligible at low voltage output levels.

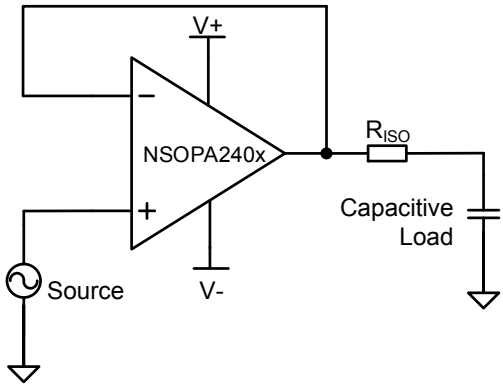

Figure 8-7 Insert isolation Resistor to drive large Capacitive Load

8.3.5. Current-Limit and Short-Circuit Protection

NSOPA240x has separate internal current limiting for the PMOS (high-side) and NMOS (low-side) output transistors.
If the output is shorted to ground, then the PMOS (high-side) current limit is activated, and limits the current to about 550 mA. OCP_HS pin (pin7 of NSOPA2402) goes low to alert that the high side current-limit event occurs, and released after current-limit has removed.
If the output is shorted to supply, then the NMOS (low-side) current limit is activated and limits the current to about 550 mA. OCP_LS pin (pin 8 of NSOPA2402) goes low to alert that the low side current-limit event occurs, and released after current-limit has removed.
The OCP pins can be monitored to determine if the device is in current limit state. Pull-up resistors not less than 2kΩ are needed because of its open-drain structure. These pins can be floating configuration if this function is not used.
When current is limited, the safe limits for the die temperature must be taken in to account. With too much power dissipation, the die temperature can surpass thermal shutdown limits; the op amp shuts down and reactivates after the die has fallen below thermal limits.

8.3.6. Thermal Protection and OTP/SH_DN Alarm Flag

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called self-heating. The absolute maximum junction temperature of the NSOPA240x is 150°C. Exceeding this temperature may damage the device. The NSOPA240x features thermal protection to reduce damage caused by self-heating. This protection is achieved by monitoring the device temperature and turning off the op amp output drive when the temperature is above 173°C.

Figure 8-8 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 10V. When self-heating causes the device junction temperature to rise above internal limits, thermal protection forces the output into a high-impedance state and pulls the output to ground through resistor R_L.

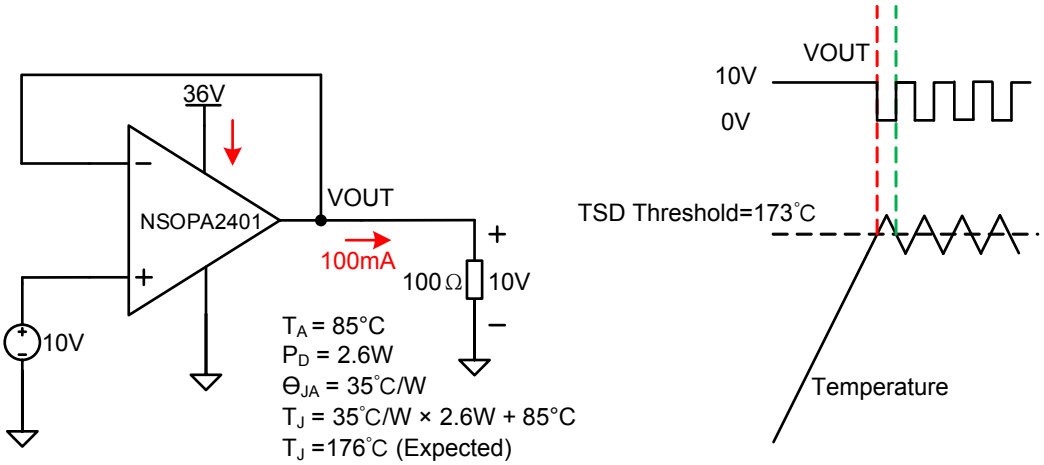

Figure 8-8 Thermal Shut Down and Recovery

If the die temperature exceeds safe limits, all outputs are disabled, and OTF/SH_DN pin (pin3 of NSOPA2402) is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The OTF/SH_DN pin is released after operation has resumed. OTF/SH_DN pin is bidirectional that allows both op amps to be put into a low IQ state when forced low.

As a result of this pin being bidirectional, and the respective enable and disable functionality, this pin must be pulled high through a pull up resistor not less than 2kΩ (Although the chip has internal weak pull-up resistor, it is strongly recommended to use external strongly pull-up resistor)

CAUTION

Do not continuously operate the device in thermal hysteresis for long periods of time because this action may cause irreversible damage to the device.

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8.3.7. Current Limit and OCP Alarm Flag

NSOPA240X has internal current limit functionality to protect device in case of overcurrent event. Once the OCP function is trigged, current limit will be valid and limit the output current when the current reaches 400mA.

The pin 7 and 8 of NSOPA2402 are designed for the over-current protect (OCP) function. Corresponding to traditional class A-B output stage of NSOPA2402, pin 7(OCP_HS) and pin 8 (OCP_LS) can be trigged independently to indicated where the overcurrent event locates. When the output current exceeds the limit (~400mA typ), these pins go low to alert that the output-current event occurs. OCP_HS pin goes low means over current event occurs in the high side of output stage. OCP_LS pin goes low means over current event occurs in the low side of output stage.

OCP pins are only output pin used to detecting the internal overcurrent status. If customer need this function, pull-up resistor not less than 2kΩ is installed because of its open-drain structure. In addition, it can be floating configuration if customer do not need this functionality.

8.3.8. Electrical Overstress

Always, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 8-9 shows an illustration of the ESD circuits contained in the NSOPA240x (indicated by the dotted area area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

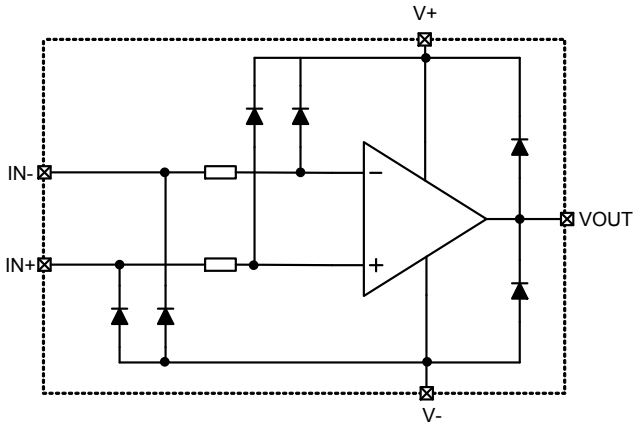

Figure 8-9 Internal ESD Equipment Model

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin.

Electrostatic Discharge (ESD) is defined the transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is regarded as a high voltage(kV), short duration event(1-100ns). Besides, it is fast edges and lower power event.

But unlike ESD problems, EOS is another common device problem. Electrical Over Stress (EOS) is defined the exposure of an item to current or voltage beyond its maximum ratings.

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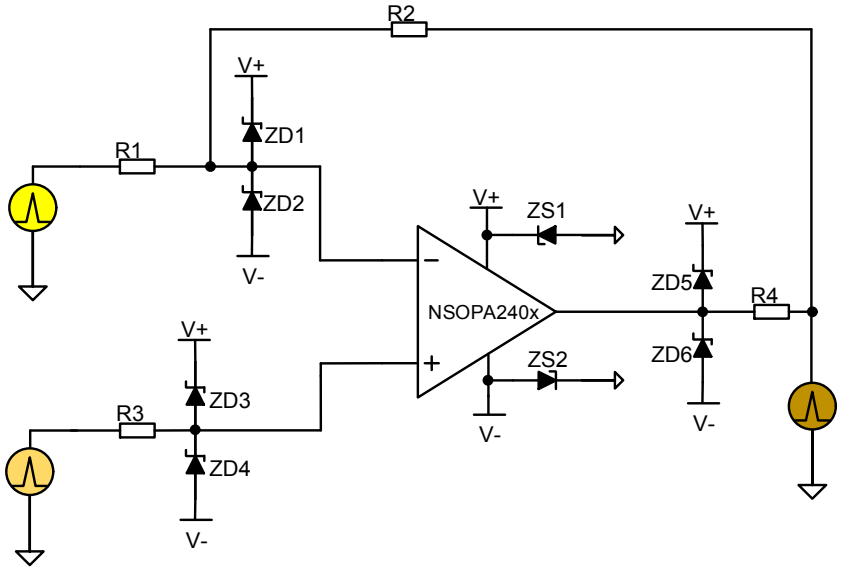

Figure 8-10 External Component to Enhance EOS Performance

Figure 8-10 shows how to use external components to enhance the circuitry robustness.

1. SDx are small signal Schottky diodes. Using power Schottky for power operational amplifier. Diodes limits EOS Voltage to [(V+) +0.3V] or [(V-)-0.3V].
2. ZS1 and ZS2 are Zener diodes or unipolar semiconductor Transient Voltage Suppressors (TVS). They prevent device supply over-voltage, provide reverse polarity protection, and provide a current path for Iq if one supply floats.
3. R1, R2 limit current through SD1, SD2.
4. R3 limits current through SD3, SD4.
5. R4 limits current through SD5, SD6.R4 is inside the feedback loop adding little error at output voltage.
6. **Check Absolute Maximum Ratings before using NSOPA240x and never violate the Absolute Maximum Ratings.**

9. Application

9.1. Resolver Driver Power Amplifier Power Dissipation

NSOPA240x is designed to drive resolver in automative applications. It's recommended to use differential mode. Because of the relatively low impedance of the resolver and the large VCC voltage, it is important to estimate temperature of device. The dissipation power is determined by the type of loads. Always, the typical resolver can be regarded as resistive and inductance load.

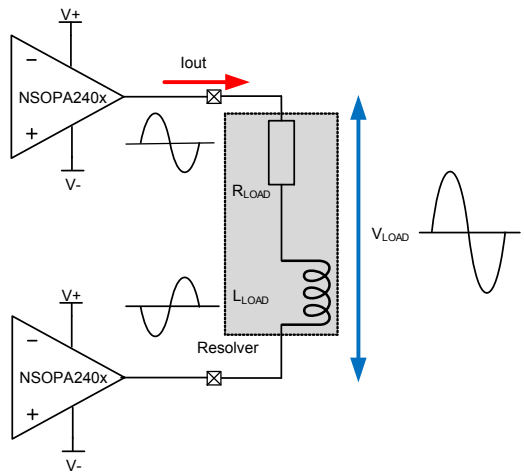

Figure 9-1 Equivalent Circuit for Calculating Power Supply Current

The dissipation power of the amp (P_{AMP}) is calculated by subtracting the power dissipated in the load (P_{LOAD}), from the power supply (P_{SUPPLY})

$$P_{AMP} = P_{SUPPLY} - P_{LOAD}$$

The equivalent load impedance of the resolver rotor winding is equal to:

$$Z = R + jX_L$$

where $XL = \omega L$

The magnitude of the impedance is:

$$|Z| = \sqrt{R^2 + X_L^2}$$

The signal applied to the rotor winding is $v(t) = A\ sin\omega t$, The rms voltage applied to Z is $V = A/\sqrt{2}$. The rms current through Z is given by:

$$I = \frac{V}{|Z|} = \frac{A/\sqrt{2}}{|Z|}$$

the power dissipated in the load is:

$$P_{LOAD} = V * I * \cos\theta = \frac{A^2}{2 * |Z|} * \frac{R}{|Z|}$$

Where $\cos\theta = \frac{R}{|Z|}$ is the power factor.

The average current from the supply is:

$$I_{AVG} = \frac{I_{PEAK}}{\pi} = \frac{A}{\pi * |Z|}$$

Because this current must be supplied by each rail,

$$P_{SUPPLY} = 2 * V_{SUPPLY} * I_{AVG} = V_{SUPPLY} * \frac{A}{\pi * |Z|}$$

We can now calculate P_{AMP}:

$$P_{AMP} = P_{SUPPLY} - P_{LOAD}$$
$$= (2 * V_{SUPPLY} * \frac{A}{\pi * |Z|}) - (\frac{A^2}{2 * |Z|} * \frac{R}{|Z|})$$

When using Tamagawa TS2620N21E11 resolver, the impedance is 70 Ω+j100 Ω at 10 kHz. In the typical use case (VCC = 12 V, A = 10 V).

Calculating the power dissipation by using the derived equation:

$$P_{AMP} = (2 * V_{SUPPLY} * \frac{A}{\pi * |Z|}) - (\frac{A^2}{2 * |Z|} * \frac{R}{|Z|})$$
$$= (2 * 12V * \frac{10V}{\pi * 122\Omega}) - (\frac{10V^2}{2 * 122\Omega} * \frac{70\Omega}{122\Omega}) = 0.39w$$

when NSOPA2402 is adopted, the thermal resistance to ambient (θ_{JA}) of NSOPA2402 (HTSSOP14) is 40°C/W and therefore the junction temperature rise above ambient is:

$$\Delta t = 40°C/W \times 0.39W = 15.6°C$$

when two NSOPA2401 are adopted, the thermal resistance to ambient (θ_{JA}) of NSOPA2401 (TO-252-5L) is 35°C/W and therefore the junction temperature rise above ambient is:

$$\Delta t = 35°C/W \times \frac{0.39W}{2} = 6.8°C$$

9.2. Safe Operation Area

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistors, VS − VO. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$.

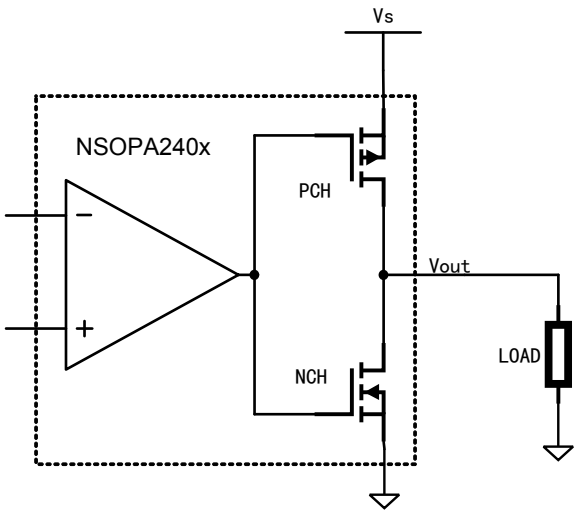

Figure 9-2 Simple Power Amplifier Circuit

The maximum operating junction temperature is recommended to exceed 150 degrees, so we derive maximum dissipate power under given conditions.

$$T_J(\max) = T_A + p_D \times R_{\theta JA} \#1$$

The Safe Operating Area (SOA curve, Figure 9-3) illustrates the permissible range of voltage and current.

The curves shown represent devices soldered to a printed circuit board (PCB) with no heat sink (JEDEC standard).

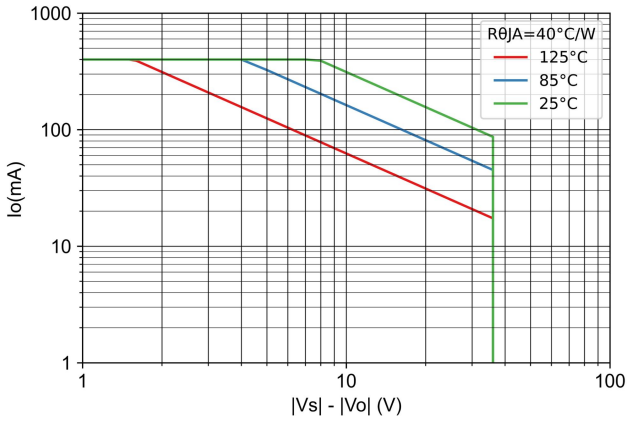

Figure 9-3 HTSSOP14 SOA Curve

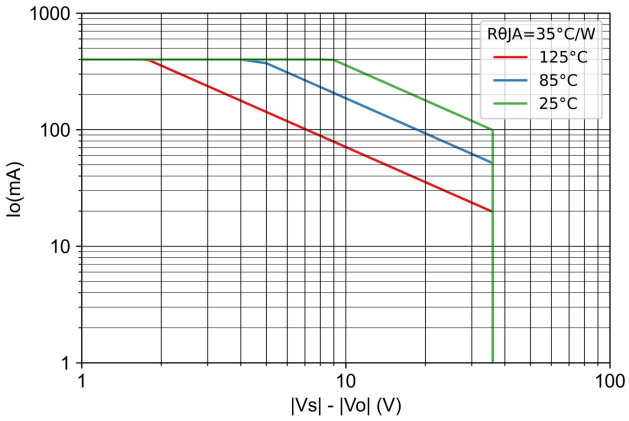

Figure 9-4 TO252 SOA Curve

Increasing printed circuit trace area or the use of a heat sink can significantly reduce thermal resistance, resulting in increased output current for a given output voltage.

The safe output current decreases as $V_S - V_O$ increases. Output short-circuits are a very demanding case for SOA. This exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, a heat sink is required.

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10. Layout Guidance

10.1. Guidelines

Poor op amp PCB layout will deteriorate the chip parameters, or even worse, cause it to work abnormally. For better performance, some tips should be considered.

• Noise can propagate into the analog circuitry through the board's power connections and to the power pins of the op amp itself. Bypass capacitors are used to reduce coupled noise by providing a low impedance path to ground.

– Connect a low ESR 0.1µF ceramic bypass capacitor between each supply pin and ground as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single-supply applications.

• To reduce parasitic coupling, keep input traces as far away from power supply or output traces as possible. If these traces cannot be kept separate, route them at a 90-degree angle

It's much better to run overly sensitive traces than to run traces parallel to noisy traces.

• External components should be located as close to the device as possible, as shown in following figure. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.

• Keep input traces as short as possible. Remember, the input traces are the most sensitive parts of the circuit.

• For best performance, cleaning is recommended after PCB board assembly.

10.2. Example

A single channel is shown as follow. The rest channels should be handled with identical way but not shown in the figure.

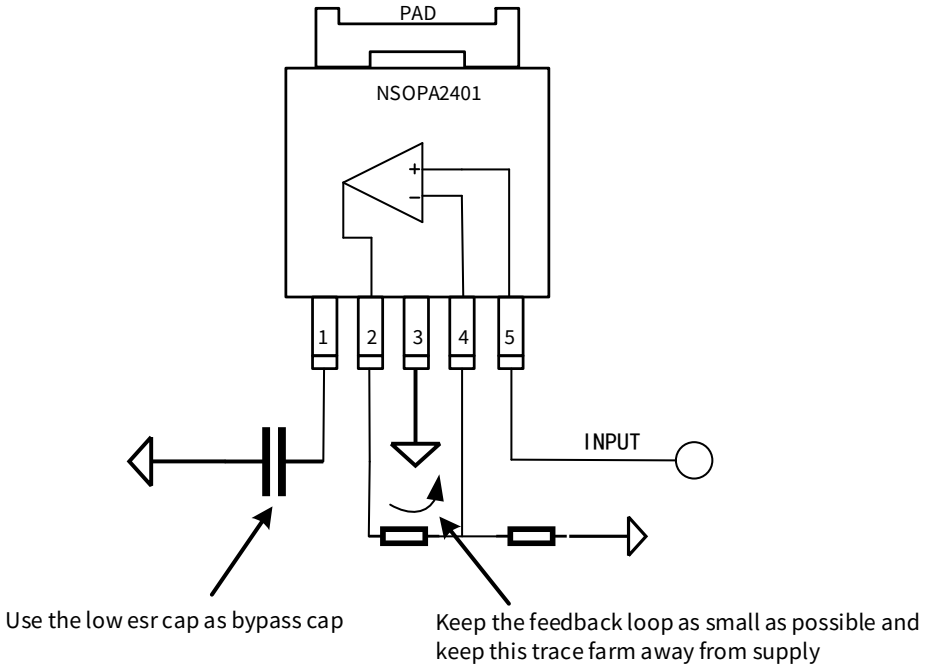


Figure 10-1 Layout example

10.3. PCB processing

The following recommendations can be used as guidelines for designing PCB for thermal testing or functional evaluation.

- Connect thermal Pad to V- net
- Use large and multi-layer PCB boards (at least 4 layers) if possible.
- When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer.
- It is recommended, but not required, to place a small number of the holes under the package, but outside the thermal pad area. These holes provide additional heat path between the copper land and ground plane and are 25 mils in diameter. They may be larger because they are not in the area to be soldered, so wicking is not a problem. This is illustrated in Figure 10-3
- Use the heat sink if possible.

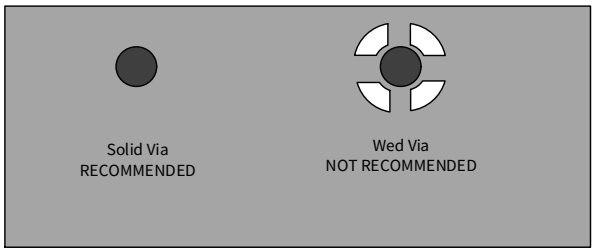


Figure 10-2 Via Style

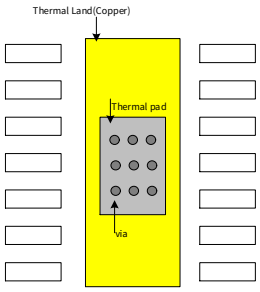
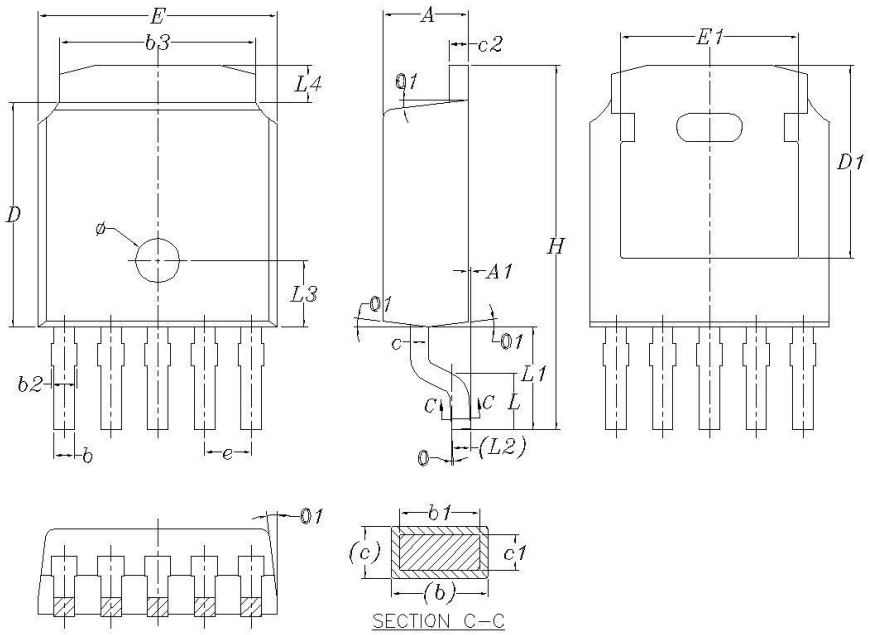


Figure 10-3 Via and Thermal land

11. Package Information

11.1. TO-252-5L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.184	2.387	0.0860	0.0940
A1	0.000	0.127	0.0000	0.0050
A2	1.450	1.850	0.0571	0.0728
b	0.508	0.711	0.0200	0.0280
b1	0.508	0.660	0.0200	0.0260
b2	0.610	0.787	0.0240	0.0310
b3	5.184	5.461	0.2041	0.2150
c	0.460	0.610	0.0181	0.0240
c1	0.406	0.559	0.0160	0.0220
c2	0.460	0.610	0.0181	0.0240
D	6.000	6.223	0.2362	0.2450
D1	5.050	/	0.1988	/
E	6.350	6.731	0.2500	0.2650
E1	4.318	/	0.1700	/
e	1.170	1.370	0.0461	0.0539
H	9.500	10.300	0.3740	0.4055
L	1.397	1.778	0.0550	0.0700
L1	2.400	3.000	0.0945	0.1181
L2	0.508 REF		0.020 REF	
L3	1.600	2.000	0.0630	0.0787
L4	0.889	1.270	0.0350	0.0500
θ	0°	10°	0°	10°
θ1	0°	15°	0°	15°
Φ	1.05	1.35	0.0413	0.0531

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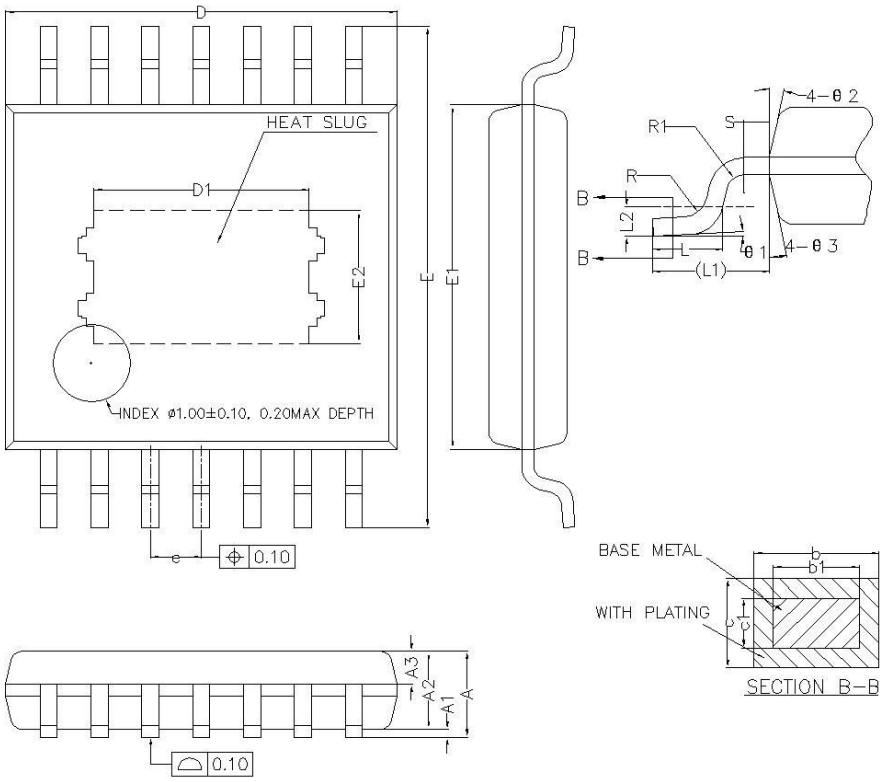
11.2. HTSSOP14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.20	— —	0.0472
A1	0.05	0.15	0.0020	0.0059
A2	0.90	1.05	0.0354	0.0413
A3	0.32	0.52	0.0126	0.0205
b	0.20	0.29	0.0079	0.0114
b1	0.19	0.25	0.0075	0.0098
c	0.15	0.20	0.0059	0.0079
c1	0.14	0.16	0.0055	0.0063
D	4.90	5.10	0.1929	0.2008
D1	2.65	2.85	0.1043	0.1122
E	6.20	6.60	0.2441	0.2598
E1	4.30	4.50	0.1693	0.1772
E2	1.60	1.80	0.0630	0.0709
e	0.55	0.75	0.0217	0.0295
L	0.45	0.75	0.0177	0.0295
L1	1.00REF			
L2	0.25BSC			
R	0.09	— —	0.0035	— —
R1	0.09	— —	0.0035	— —
S	0.20	— —	0.0079	— —
θ1	0°	8°	0°	8°
θ2	10°	14°	10°	14°
θ3	10°	14°	10°	14°

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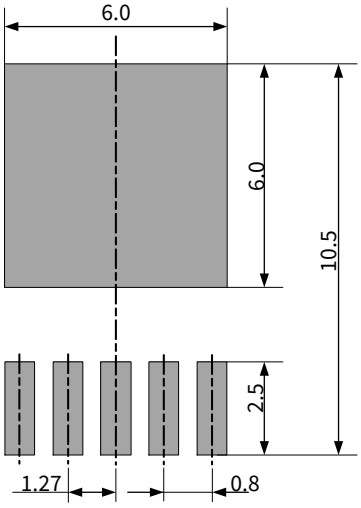
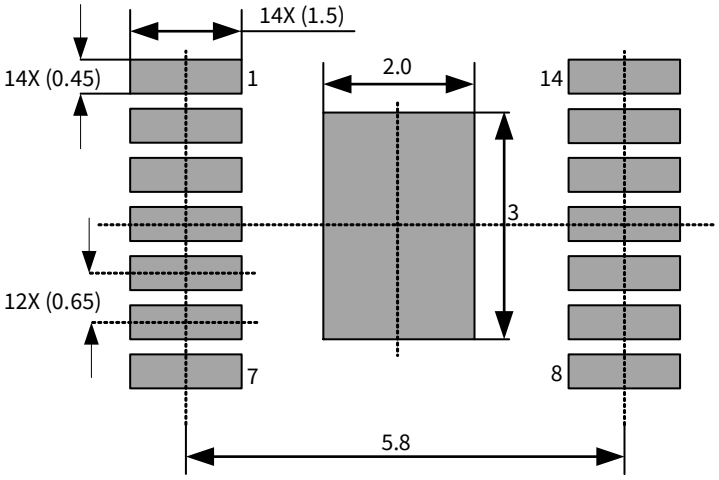
11.3. Example of Solder Pads Dimensions





Note:

1. Unit: mm.

12. Ordering Information

Part Number	*Package*	*MSL Level*	*Op Temp (°C)*	*SPQ*
NSOPA2401-Q1TOAR	TO-252-5L	3	-40~+125	2000
NSOPA2402-Q1HTSKR	HTSSOP (14)	1	-40~+125	4000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

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13. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NSOPA2401-Q1TOAR			
NSOPA2402-Q1HTSKR			

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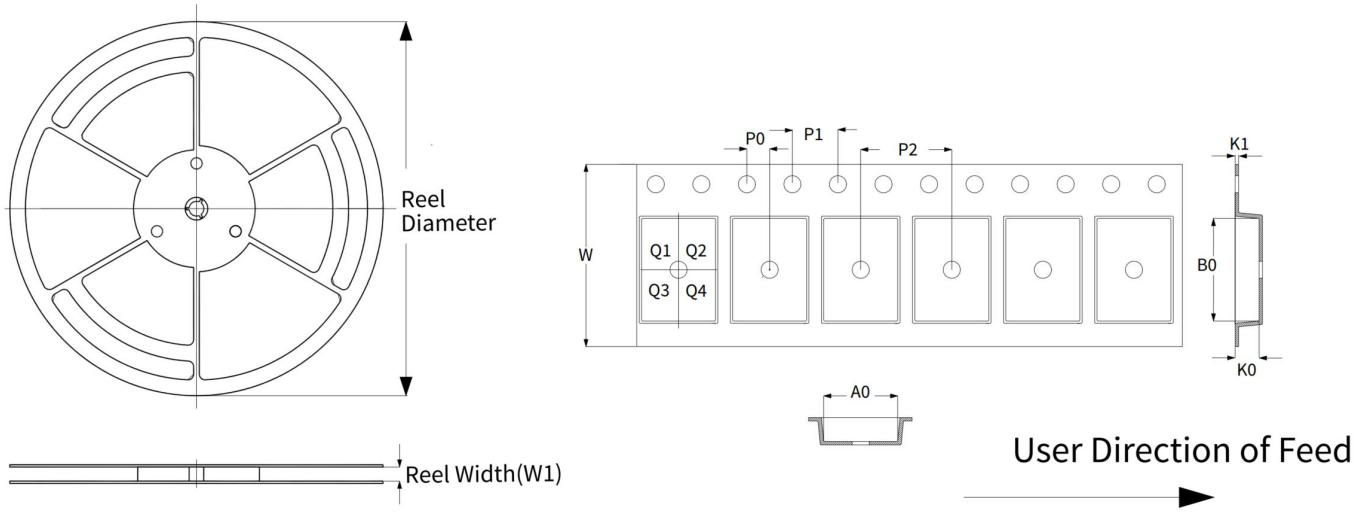
14. Tape and Reel Information



Device	Reel Diameter	Reel Width(W1)	W	A0	B0	P0	P1	P2	K0	K1	PIN1 Quadrant
NSOPA2401-Q1TOAR	330	24.4	24	6.9	10.5	2.0	4.0	4.0	1.4	2.9	Q2
NSOPA2402-Q1HTSKR	330	12.4	12.0	6.85	5.45	2.0	4.0	8.0	1.6	0.3	Q1

Note:

2. All dimensions are nominal.
3. The picture is only for reference. Please make the object as the standard.
4. Unit: mm.

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15. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/7/5
1.1	Add example of solder pads dimensions Add reflow note in order information table	2024/08

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