EV2796-0000/0002-FP-00A

7-Cell to 16-Cell, High-Accuracy I²C/SPI Battery Monitor and Protection System Evaluation Board

DESCRIPTION

The EV2796-0000-FP-00A and EV2796-0002-FP-00A evaluation boards are designed to demonstrate the capabilities of the MP2796, a complete analog front-end (AFE) monitoring and protection IC. The MP2796 supports 7-cell to 16-cell series battery packs with outstanding current and voltage measurement accuracy and a complete set of protection features.

The MP2796 measures each cell's voltage and includes high-side MOSFETs (HS-FETSs) for charge and discharge control. It measures the die temperature and cell temperature via 4 negative temperature coefficient (NTC) thermistor inputs. The MP2796 contains internal passive-balancing MOSFETs capable of driving up to 58mA, and can also drive external balancing transistors for higher currents.

The discharge (DSG) MOSFET includes a configurable soft start (SS) that provides a controlled start-up, eliminating the need for an external pre-charge circuit. The MOSFETs also incorporate over-current protection (OCP), short-circuit protection (SCP), battery under-voltage protection (UVP), battery over-voltage protection (OVP), and high/low-temperature protection. All of these protections have configurable thresholds.

These evaluation boards combine the MP2796 with power MOSFETs and a current-sense resistor to support up to 70A of charge/discharge current. If needed, the EV2796-0000/0002-FP-00A includes placeholders to add external MOSFETs for a higher balancing current.

PERFORMANCE SUMMARY

Specifications are at T_A = -40°C to +85°C, unless otherwise noted.

Parameters	Conditions	Value
Battery pack voltage range		18V to 75.2V
Cell voltage range		0V to 5V
Continuous charge current		0A to 70A
Continuous discharge current		0A to 70A
Internal balancing current	V_{BATT} = 4V, T_A = 25°C	58mA
External balancing current	With external balancing transistors/MOSFETS installed	>58mA
Supported series cells		7 to 16

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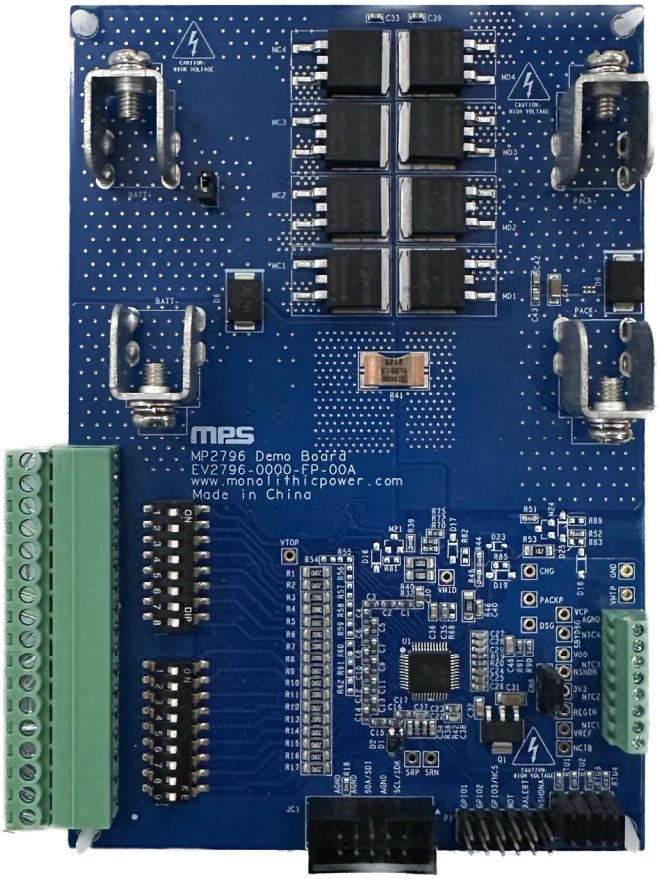
EVALUATION BOARDS



LxWxH (14cmx9.6cmx1.5cm)

Board Number	MPS IC Number	Description
EV2796-0000-FP-00A	MP2796DFP-0000	Supports I²C communication interface.

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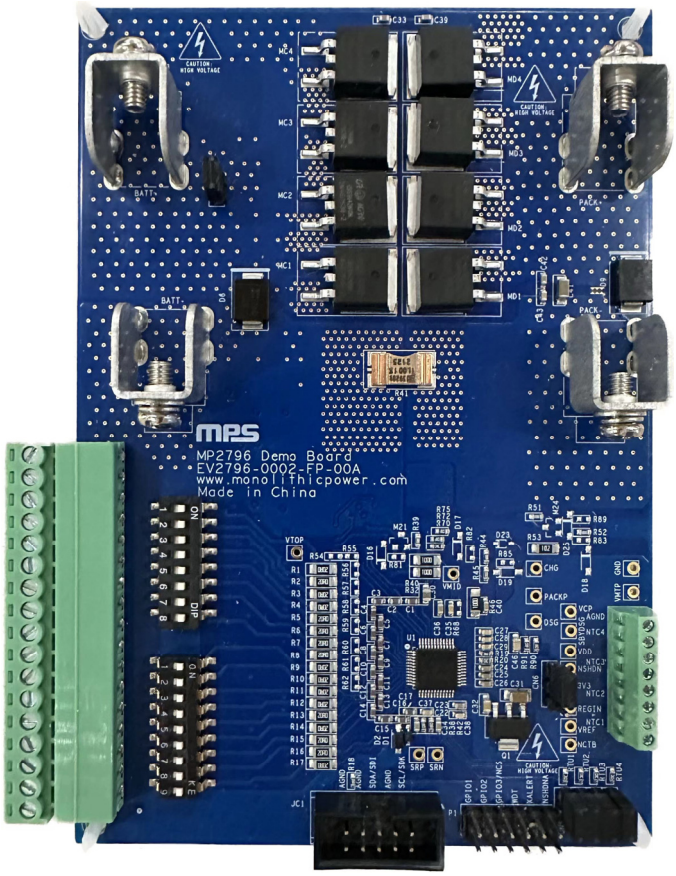
EVALUATION BOARDS *(continued)*



LxWxH (14cmx9.6cmx1.5cm)

Board Number	MPS IC Number	Description
EV2796-0002-FP-00A	MP2796DFP-0002	Supports SPI communication interface.

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QUICK START GUIDE

The EV2796-0000/0002-FP-00A is designed to evaluate the MP2796, which can be configured to support 7-cell to 16-cell series connections. This board incorporates the MP2796, power MOSFETs, a current-sense resistor, and additional components. These evaluation boards include placeholders to add external MOSFETs and balancing resistors to support >58mA of balancing current. The EV2796-0000/0002-FP-00A includes protection capabilities with configurable thresholds for the following conditions: over-current (OC), short-circuit (SC), under-voltage (UV), over-voltage (OV), misbalanced cell(s), and high/low temperature.

Evaluation Platform Preparation

To use the evaluation platform, the following is required: a computer with at least one USB port, a USB cable, and a communication kit. The MP2796 evaluation software must also be properly installed.

1. Use the USB-to-I²C communication kit (EVKT-USBI2C-02) if using the EV2796-0000-FP-00A (see Figure 1).

Figure 1: USB-to-I²C Communication Kit

2. Use the USB-to-SPI communication kit (EVKT-USBSPI-00) if using the EV2796-0002-FP-00A (see Figure 2).

Figure 2: USB-to-SPI Communication Kit

3. To check the software, double-click on the MP2796 evaluation kit .exe file, then open the software. Note that the software is supported by Windows XP, 7, and later versions.
4. Use the cell simulator shunt (short CN7, turn the SW1 and SW2 channels on) to set up the board quickly without a real battery pack.
5. Apply DC power supply between BATT+ and BATT-, then adjust the DC power supply to be about 60V/1A.
6. Connect the communication kit to JC1, and consider the positions of SCL and SDA.

   Figure 3 on page 4 shows the original test set-up for the MP2796DFP-0000.

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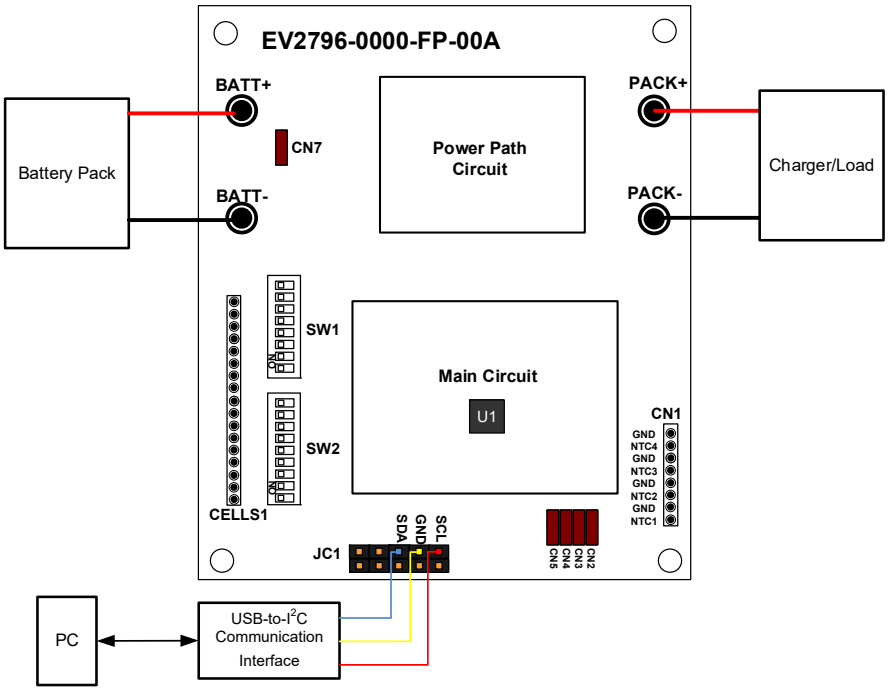

Figure 3: Test Set-Up for the MP2796DFP-0000

Figure 4 on page 5 shows the original test set-up for the MP2796DFP-0002.

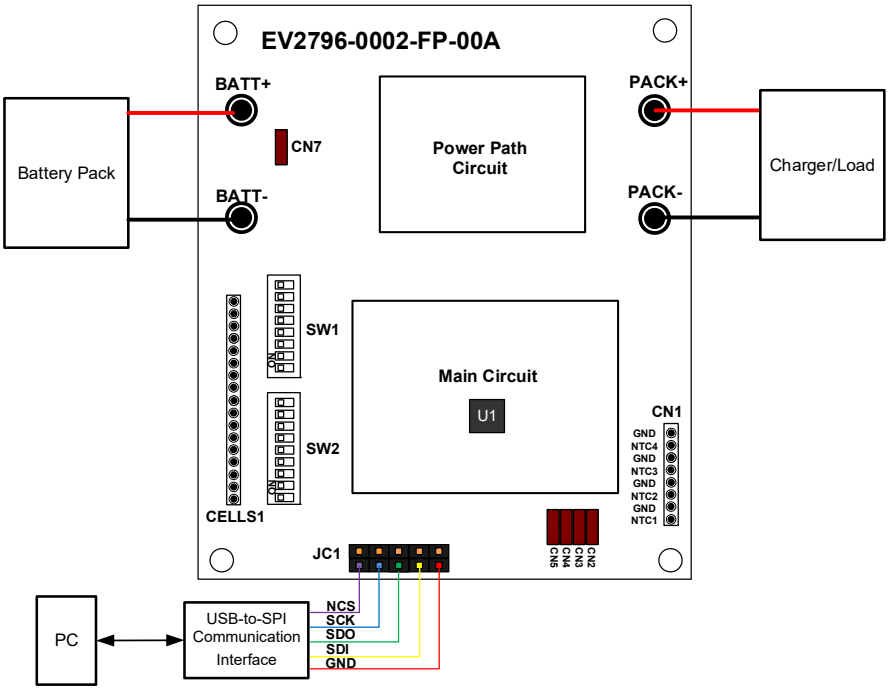

Figure 4: Test Set-Up for the MP2796DFP-0002

7. By default, this board has 16 cells in series. To use the cell simulator shunt and evaluate the device at a lower series number, short circuit the corresponding channels.

   Figure 5 on page 6 shows a 10-cell series connection with the cell simulator shunt. Note that the DC power supply voltage between BATT+ and BATT- should be decreased, depending on the number of cells in series.

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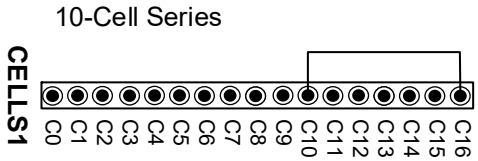

Figure 5: 10-Cell Series Connection

8. Use a real battery pack to test the open-wire and cell balance functions, as these functions cannot be tested using the cell simulator shunt.

   Figure 6 shows the MP2796DFP-0000 test set-up with a battery pack.

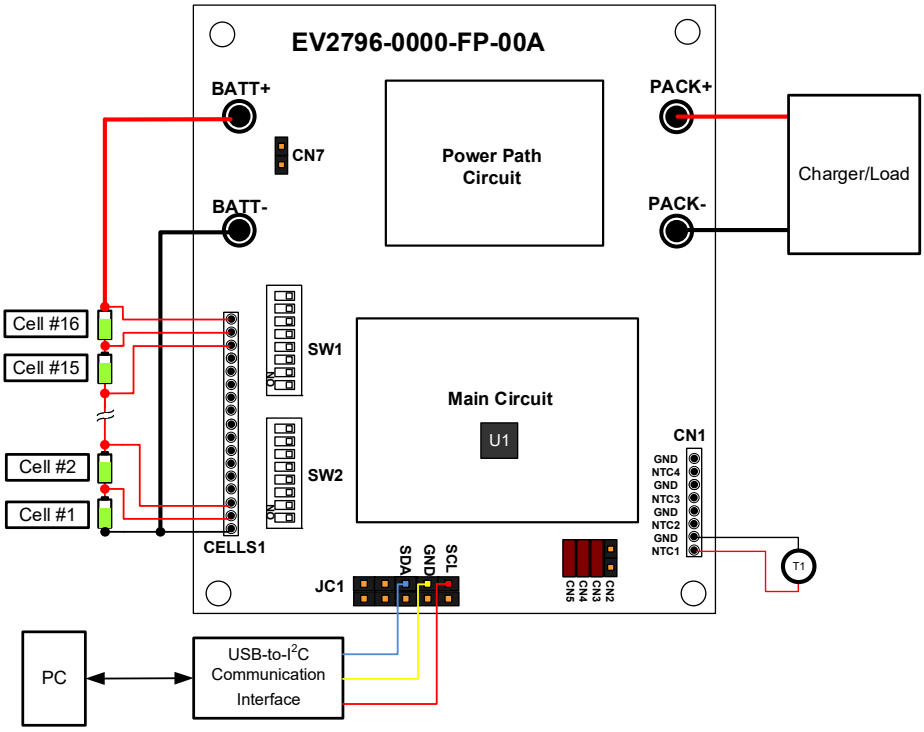

Figure 6: Test Set-Up for the MP2796DFP-0000 with a Battery Pack

Figure 7 on page 7 shows the MP2796DFP-0002 test set-up with a battery pack.

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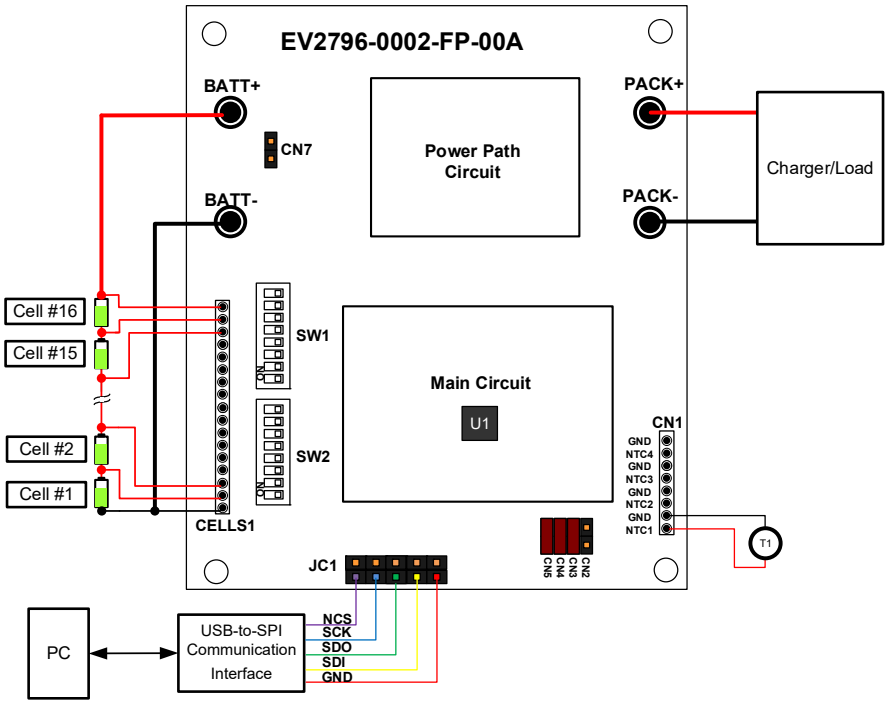

Figure 7: Test Set-Up for the MP2796DFP-0002 with a Battery Pack

9. Remove the CN7 jumper and turn the SW1 and SW2 channels off.
10. Use a 0Ω resistor to short the Cx pins (C1 through C16), depending on the number of cells in the battery pack. If the application has 16 cells in series, skip this step.

    Using a 10-cell series pack as an example, add a 0Ω resistor to R54, R55, R56, R57, R58, and R59.
11. Connect the cell terminals (CELLS1) to each cell-sensing point. If the number of cells in the battery pack is below 16, float the connectors' higher channels.
12. Connect the battery terminals to:
    a. Positive (+): BATT+
    b. Negative (-): BATT-
13. The EV2796-0000/0002-FP-00A has a bypass P-channel MOSFET (P-FET). In safe mode, turn on the P-FET using GPIO2. The P-FET can then power PACK with low power consumption. When $V_{PACK} < V_{TOP} - 2V$, the P-FET current capacity is about 25mA. When $V_{PACK} > V_{TOP} - 2V$, the P-FET can bypass a current of about 1A. If this function is not used, set the GPIO2 output to Hi-Z.
14. Remove CN2, CN3, CN4, and CN5.
15. Connect and locate the temperature sensors to support up to 4 NTCs.
16. Connect the charger (or the load) terminals to:
    a. Positive (+): PACK+
    b. Negative (-): PACK-
17. Connect SDA, SCL, and GND to the USB-to-I²C communication interface (or NCS, SCK, SDO, and SDI for the USB-to-SPI communication interface). Carefully consider where SCL and SDA are positioned.

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18. Connect the communication interface to the PC, turn on the computer, and launch the MP2796 evaluation software. Figure 8 shows the software's main window.

    If the previous steps are correct, "MP2796 Demo board: Connected" should be listed in the lower left corner. Otherwise, the graphic user interface (GUI) should read, "MP2796 Demo board: Disconnected!"

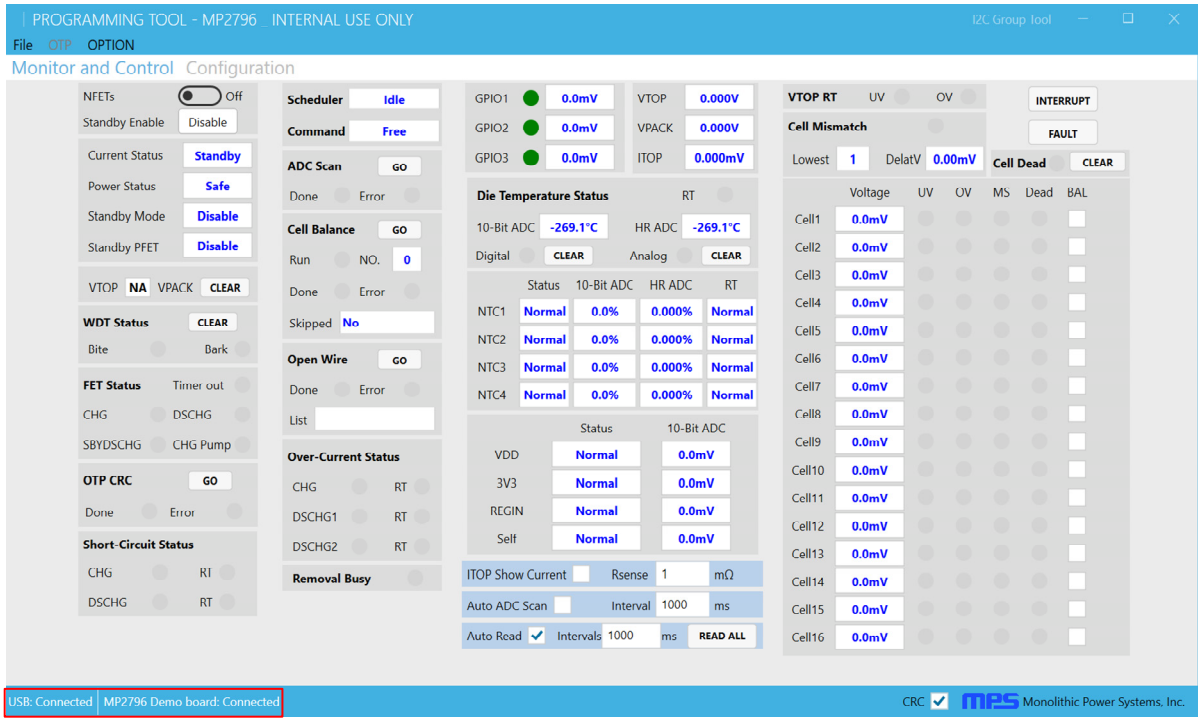

Figure 8: MP2796 Evaluation Software (Monitor and Control)

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PROCEDURE

Ensure that all the connections (e.g. between the USB-to-I²C/SPI communication kit and the EV2796-0000/0002-FP-00A) are successful.

Configuration

1. Click on the Configuration tab to view the configurations (see Figure 9). The software should automatically read all the configurations. Note that items with a lock symbol can be configured as read-only.

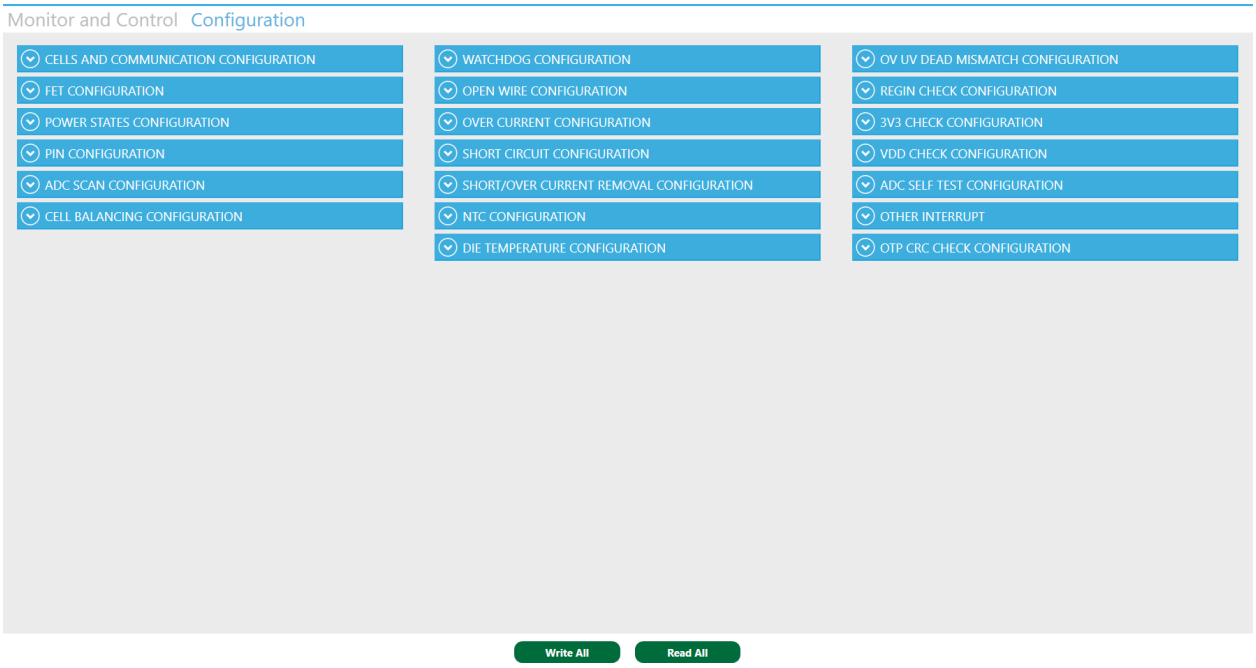

Figure 9: Configuration View

2. Configure the protection thresholds, enable all relevant functions, and set the corresponding faults.
3. Click on the “Write All” button to write configurations to the register, then click the Monitor and Control tab to switch the view.
4. Turn on the N-channel MOSFETs (N-FETs) (see Figure 8 on page 8), then click the “Read All” button. The N-FET status should be displayed in green for CHG, DSG, and CHG Pump, while the power status should be set to active (see Figure 10).

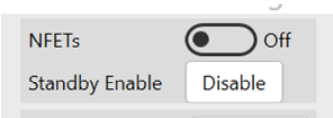

Figure 10: N-FET Status

5. Click the “Read All” button. The updated values should be displayed in the GUI. (After the Auto Read checkbox in checked, it is not required to click the “Read All” button.)
6. Configure the cells and their communication (see Figure 11 on page 10).

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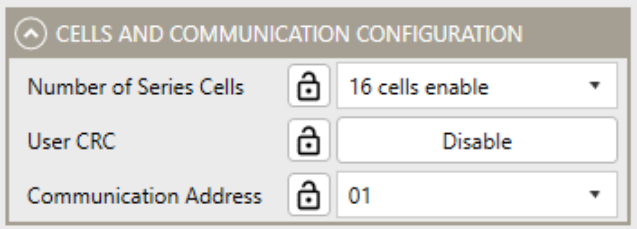

Figure 11: Cell and Communication Configurations

a. Number of Series Cells: Can be between 7 and 16.

b. User CRC: If enabled, check the CRC checkbox at the bottom right of the GUI. Otherwise, the value cannot be written to the register.

c. Communication Address: The default slave address is 01h, and the configurable communication address ranges between 00h and 7Fh. After changing this value, the new address should be used for the next communication. For devices with different “xxxx” suffixes, the default address may be different. The GUI automatically scans the address, though this function can be disabled by unchecking “Monitor chip connection” in the option tab.

7. Configure the FET (see Figure 12).

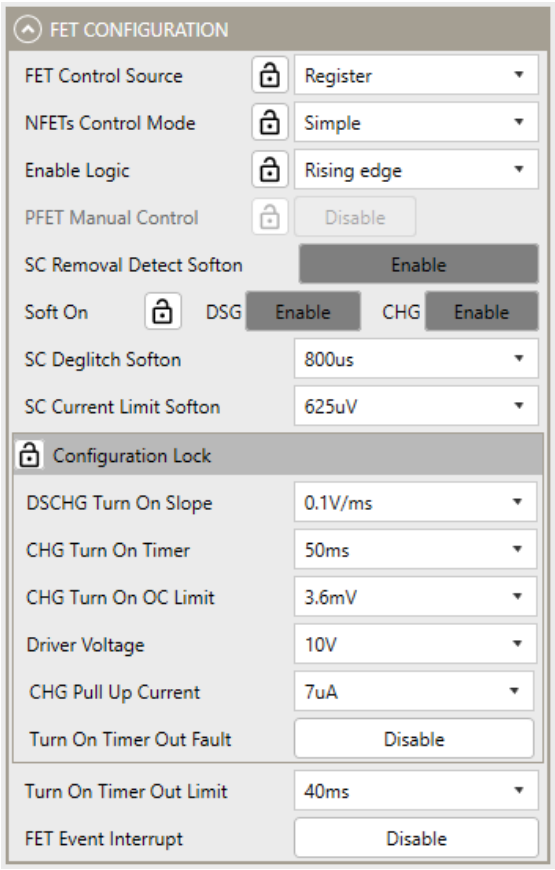

Figure 12: FET Configurations

a. FET Control Source: Can be set to GPIO control or register control.

b. NFETs Control Mode: Can be configured as simple or direct. In direct mode with GPIO control, GPIO1 controls the DSG MOSFET, while GPIO2 controls the CHG MOSFET.

c. Enable Logic: Can be configured to be rising edge active or level active.

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d. SC Removal Detect Soft Start: When enabled, the user can enable or disable the short-circuit detection sequence prior to the MOSFET turning on.

e. SC Deglitch Soft Start and SC Current Limit Soft Start: When enabled, the user protects the DSG FET from the inrush current when charging a large capacitive load. These two settings protect the DSG FET while it ramps up during a soft turn-on sequence.

f. DSCHG Turn-On Slope: Can be set between 0.1V/ms and 1.6V/ms.

g. CHG Turn-On OC Limit: Selects the over-current (OC) threshold that is applied when the charge soft start. The threshold can be set to 3.6mV or 4.8mV.

h. Driver Voltage: Defines the gate-to-source voltage (V_{GS}) for both the CHG MOSFET and DSCHG MOSFET. V_{GS} can be between 7V and 12V.

i. CHG Pull-Up Current: Sets the CHG pin's output current during the CHG soft start period to control the rising slope of the CHG MOSFET's driver voltage. Can be between 3µA and 10µA.

8. Configure the power status (see Figure 13).

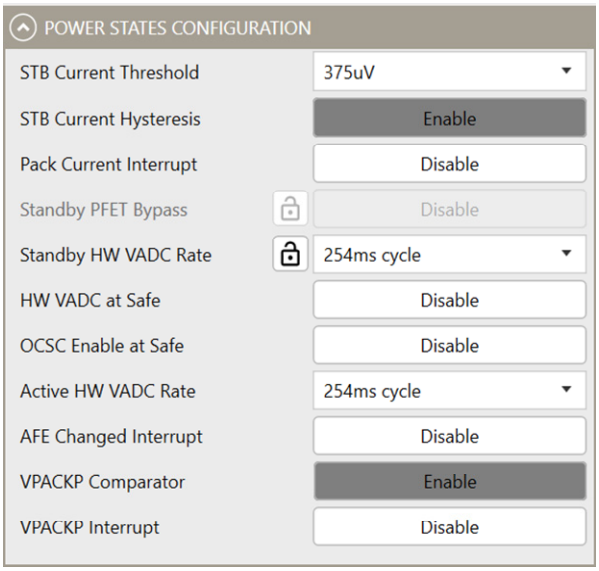

Figure 13: Power Status Configurations

a. HW VADC at Safe: If the protection is required in safe mode, enable this function to ensure that the voltage can be monitored for protections.

b. Standby HW VADC Rate: Can be used with voltage protection monitoring to refresh the analog-to-digital converter (ADC) result while in a safe or standby state. Can be configured to refresh the voltage protection reading every 254ms, 492ms, or 968ms.

c. Active HW VADC Rate: Can be used with voltage protection monitoring to refresh the ADC result while in an active state. Can be configured to refresh the voltage protection reading every 254ms or 135ms.

d. VPACKP Comparator: Enables the PACK vs. V_{TOP} comparator.

9. Configure the GPIO pins (see Figure 14 on page 11).

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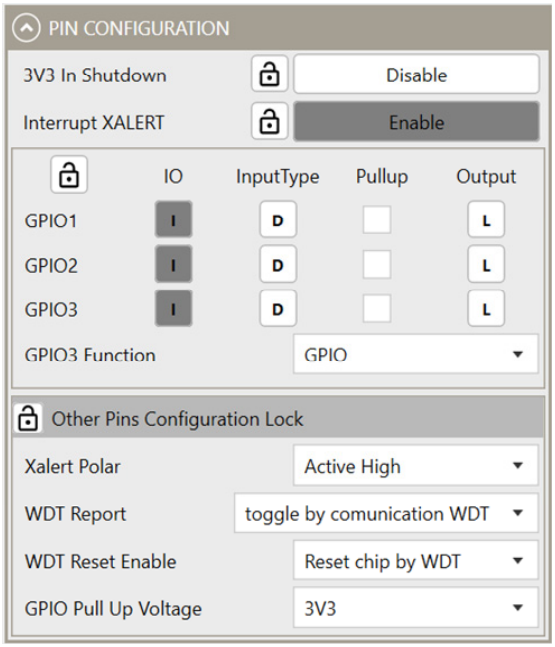

Figure 14: GPIO Pin Configurations

a. IO: The IO setting determines whether GPIO1~GPIO3 are set as inputs or outputs. If they are set to inputs, they cannot be left floating and must be connected to a high or low level; otherwise, GPIO1~GPIO3 can consume excess power.

b. Input Type: Determines whether the input type for GPIO1~GPIO3 is a digital input or a buffered ADC input.

c. Pull-Up: Enables GPIO1~GPIO3 pull-up capability. When enabled, a 20kΩ pull-up resistance is applied.

d. Output: Sets the target output level for GPIO1~GPIO3 to be high or low. This configuration bit is effective only when the corresponding GPIO is used as a digital output.

e. GPIO3 Function: Can be configured as GPIO or a fault indicator. Valid when GPIO3 is set as an output.

f. GPIO Pull-Up Voltage: Sets whether GPIO pulls up to 3V3 or REGIN.

10. Configure the ADC scan parameters (see Figure 15 on page 13).

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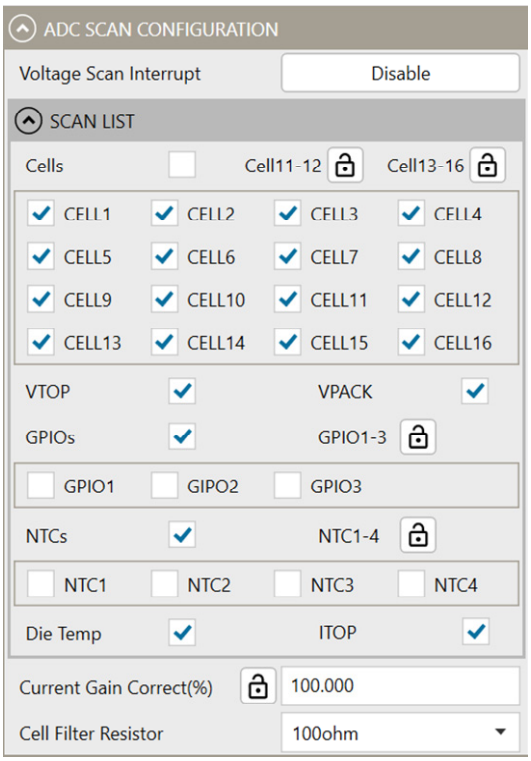

Figure 15: ADC Scan Configurations

a. Tick a checkbox to enable the related parameter. If a parameter is enabled, that parameter is read and updated during the high-resolution VADC scan. If disabled, the parameter is excluded from the high-resolution VADC scan.

b. Current Gain Correct (%): Compensates for the sense resistor and SMT variation. The correction is applied to current ADC readings. The correction is not applied to short-circuit and over-current detection. The configuration range is between 87.5% and 112.476%.

c. Cell Filter Resistor: The default value is 100Ω, and the ADC cell readings are not compensated. This configuration should set to 1kΩ when a 1kΩ filtering resistor is used (e.g. for external balancing), which compensates for the ADC cell readings. It removes the drop caused by the input current during the ADC conversion.

11. Configure the watchdog (see Figure 16).

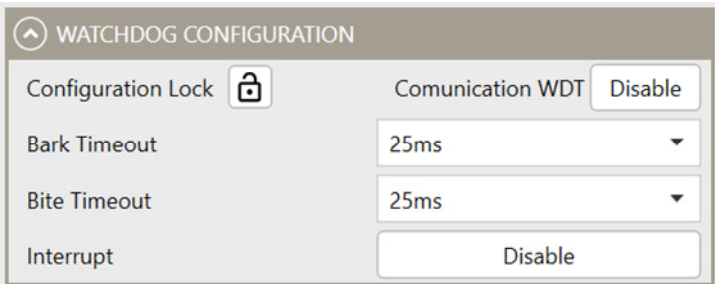

Figure 16: Watchdog Configurations

a. Bark Timeout: Defines the delay from the last watchdog reset to the bark. Ranges between 25ms and 3200ms.

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b. Bite Timeout: Defines the delay from the bark to the bite. Ranges between 25ms and 3200ms.

12. Configure the open-wire parameters (see Figure 17).

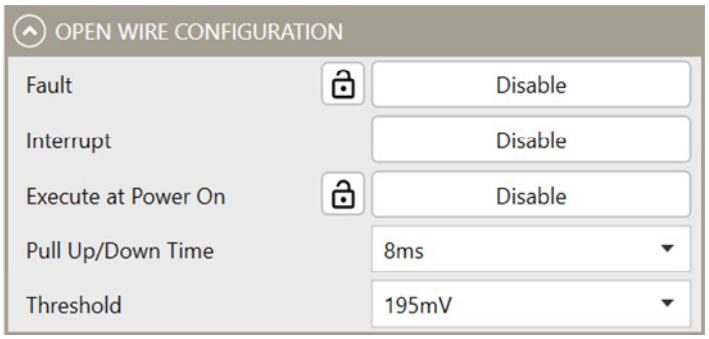

Figure 17: Open-Wire Configurations

a. Execute at Power On: Enables open-wire detection during the power-on sequence (while leaving the shutdown state).

b. Pull-Up/Down Time: Sets the length of each pull-up and pull-down phase, which ranges between 1ms and 16ms.

c. Threshold: Sets the open-wire threshold used in the detection sequence, which ranges between 39mV and 625mV.

13. Configure the OC parameters (see Figure 18).

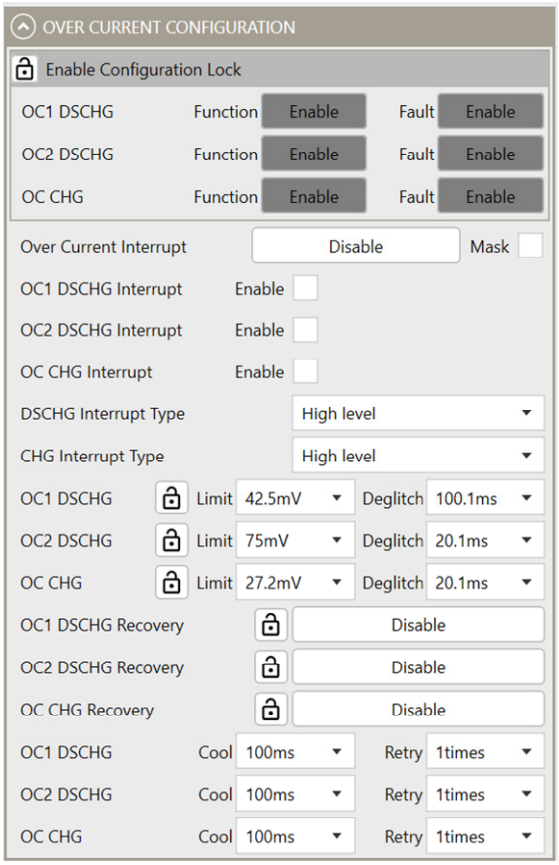

Figure 18: Over-Current Configurations

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a. Click the Over Current Interrupt Mask checkbox to enable this function. When enabled, the OC interrupt flag is cleared, and the interrupt pin goes low unless other interrupts are pending; when disabled, the OC condition can trigger the interrupt flag.

b. OC1 and OC2 DSCHG Limit: The 1x range is between 2.5mV and 80mV, while the 3x range is between 7.5mV and 240mV.

c. OC1 and OC2 DSCHG Deglitch: This time ranges between 0.1ms and 2520.1ms. The response time is about 100µs after the OC condition is detected.

d. OC CHG Limit: The 1x range is between 1.6mV and 51.2mV, while the 3x range is between 4.8mV and 153.6mV.

e. OC CHG Deglitch: Ranges between 0.1ms and 2520.1ms. The response time is about 100µs after the OC condition is detected.

f. Recovery: The OC conditions can be enabled for automatic recovery, or disabled for manual recovery.

g. Cool: The cool down times can be set to 100ms, 200ms, 500ms, or 1s.

h. Retry: The retry attempts can be set to 1 time, 2 times, 3 times, or to keep trying.

14. Configure the SC parameters (see Figure 19).

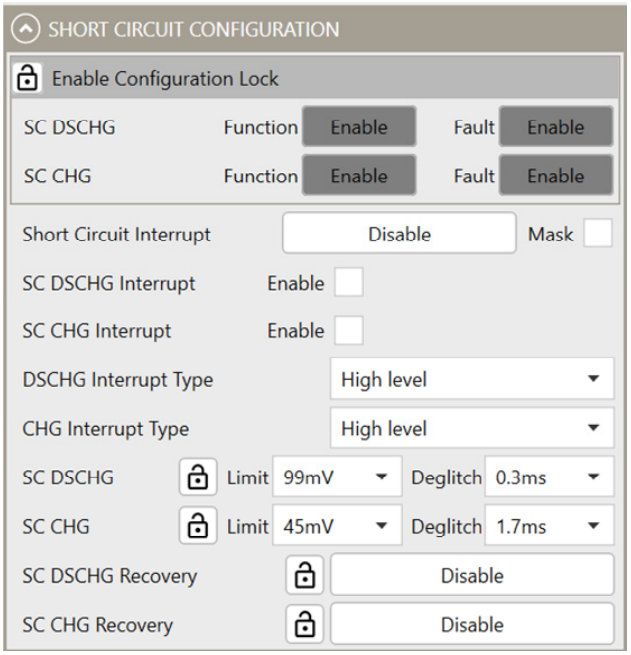

Figure 18: Short-Circuit Configurations

a. Click the Short Circuit Interrupt Mask checkbox to mask an interruption. If an interruption is masked, an SC condition does not affect the interrupt pin. Instead, the interrupt pin goes low unless a different condition occurs. When unchecked, an SC condition can set an interrupt flag.

b. SC DSCHG Limit: The 1x range is between 5.5mV and 176mV, while the 3x range is between 16.5mV and 528mV.

c. SC DSCHG Deglitch: Ranges between 0.1ms and 25.5ms. The response time is about 100µs after the SC condition is detected.

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d. SC CHG Limit: The 1x range is between 2.5mV and 80mV, while the 3x range is between 7.5mV and 240mV.

e. SC CHG Deglitch: Ranges between 0.1ms to 25.5ms. The response time is about 100µs after the SC condition is detected.

15. Configure short-circuit/over-current removal (see Figure 20).

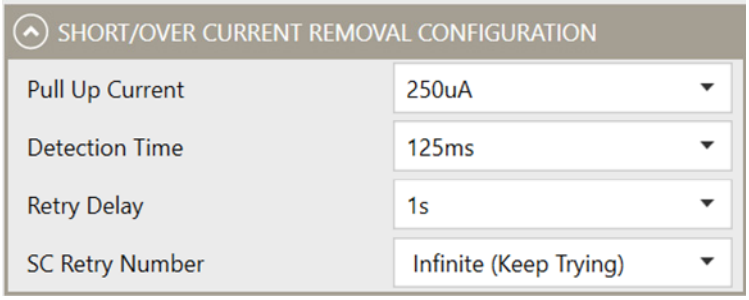

Figure 20: Short-Circuit/Over-Current Removal Configuration

a. Pull-Up Current: The pull-up current during SC removal detection can be set to 250µA, 500µA, or 750µA.

b. Detection Time: The detection time can be set to 125ms, 250ms, 500ms, or 1s.

c. Retry Delay: Sets the delay between SC removal detections to be between 1s and 25s.

d. SC Retry Number: Can be set to 1, 2, 4, or to keep trying.

16. Configure the NTCs (see Figure 21).

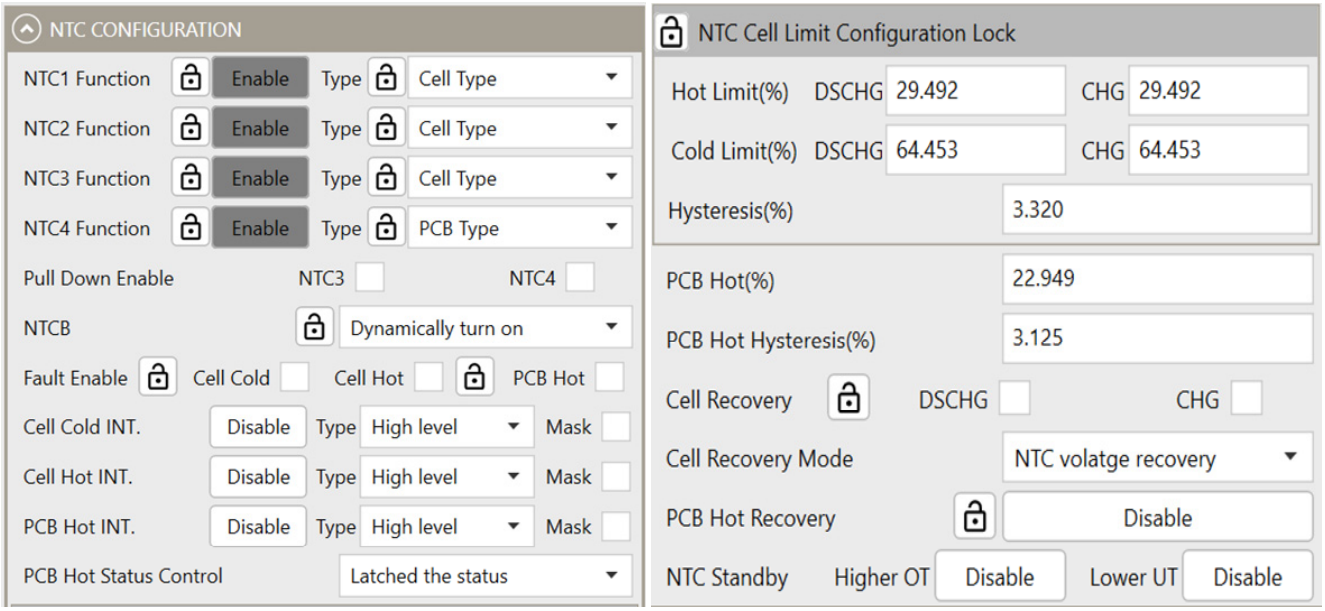

Figure 20: NTC Configurations

a. NTC Type: Can be set to cell monitor or PCB monitor.

b. Pull-Down Enable: Enables NTC3 and NTC4 to be pulled down.

c. NTCB: NTCB is set to dynamically turn on. NTCB is dynamically biased during ADC conversions of the NTC channels; if NTCB is continuously on, current consumption increases.

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d. PCB Hot Status Control: Can be set to show the latched status (which goes to the interrupt controller) or show the real-time status.

e. NTC Cell Limit: Can be set from 0% to 99.9% of NTCB.

f. Hysteresis (%): The hysteresis threshold can be set to be between 0% and 6.055% of NTCB.

g. Cell Recovery Mode: Defines the recovery logic from the NTC hot/cold conditions in charge mode. This bit is set to 0 for NTC voltage recovery, or it can be set to 1 for NTC voltage recovery (or if the charger is removed).

h. Higher OT: Defines the selection criteria for the NTC hot threshold when the battery pack current is within the standby current range. If disabled, select the hotter threshold; if enabled, select the colder threshold.

i. Lower UT: Defines the selection criteria for the NTC cold threshold when the battery pack current is within the standby current threshold. If disabled, select the colder threshold; if enabled, select the hotter threshold.

17. Configure the die temperature parameters (see Figure 22).

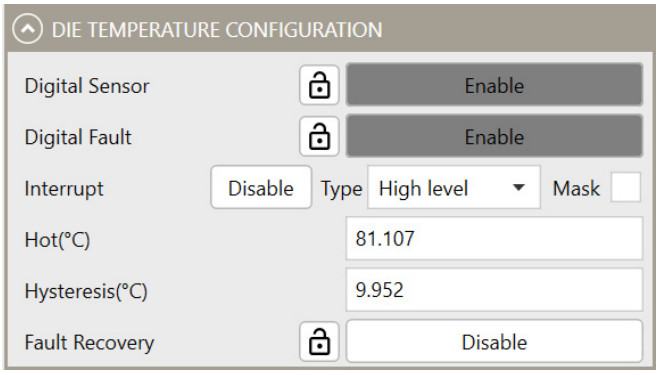

Figure 22: Die Temperature Configurations

a. Hot (°C): The resolution is 0.474°C.

b. Hysteresis (°C): Can be set between 0°C and 14.692°C.

18. Configure the cell-balancing parameters (see Figure 23).

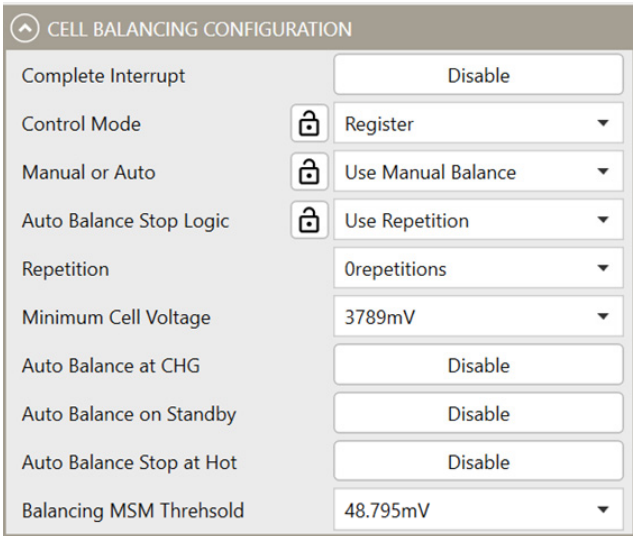

Figure 23: Cell-Balancing Configurations

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a. Control Mode: Can be set to register control or GPIO3 control when using automatic balance.

b. Manual or Auto: Controls the balancing mode, which can be configured for manual balance or automatic balance.

c. Auto-Balance Stop Logic: Only used when automatic balance is enabled. If set to "Use Repetition," balancing uses repetition to control the number of balance iterations. When set to "Use List," balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, disable this bit.

d. Repetition: Sets the number of repetitions for each execution of the balancing list, ranging between 0 and 31 repetitions. If 31 repetitions are selected, 32 balancing cycles are executed.

e. Minimum Cell Voltage: Sets the qualifying minimum cell voltage to run automatic balance, ranging between 2500mV and 4961mV. When a cell is lower than this level, it is excluded from the balancing list. All other qualifying cells are balanced if they meet the criteria.

f. Balancing MSM Threshold: This value is used by the automatic balancing algorithm, and ranges between 19.5mV and 87.85mV.

19. Set the cell over-voltage (OV) parameters (see Figure 24).

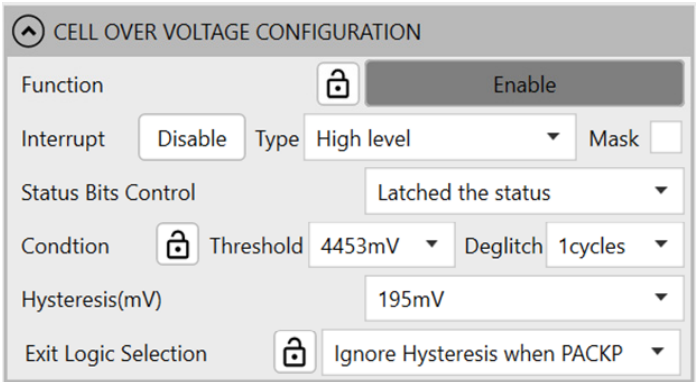

Figure 24: Cell OV Configurations

a. Threshold: The cell OV threshold ranges between 0mV to 4980.15mV.

b. Hysteresis (mV): The OV hysteresis ranges between 0mV to 292.5mV.

c. Exit Logic Selection: Can be set to "Lower than Cell OV - Hysteresis", or "Ignore Hysteresis when PACKP < V_{TOP}".

20. Set the cell under-voltage (UV) parameters (see Figure 25).

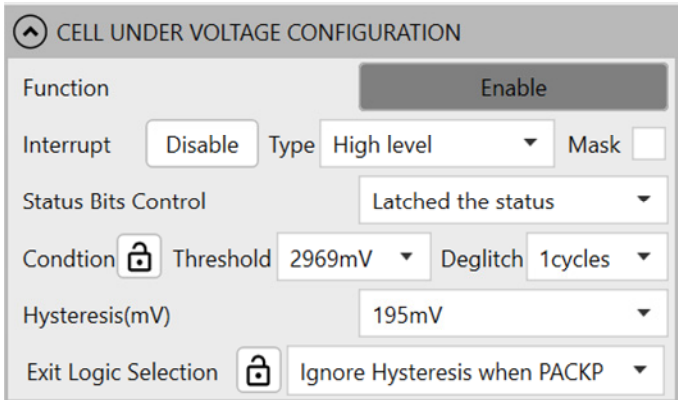

Figure 25: Cell UV Configurations

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a. Threshold: The cell UV threshold ranges between 0mV and 4980.15mV.

b. Hysteresis (mV): The UV hysteresis ranges between 0mV and 292.5mV.

c. Exit Logic Selection: Can be set to “Higher than Cell UV + Hysteresis” or “Ignore Hysteresis when PACKP > V_{TOP}”.

21. Configure the mismatched cell parameters (see Figure 26).

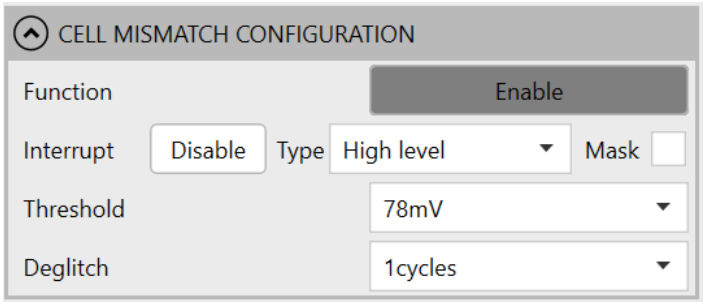

Figure 26: Mismatched Cell Configurations

Threshold: The mismatched cell threshold ranges between 0mV to 1211mV.

22. Set the dead cell parameters (see Figure 27).

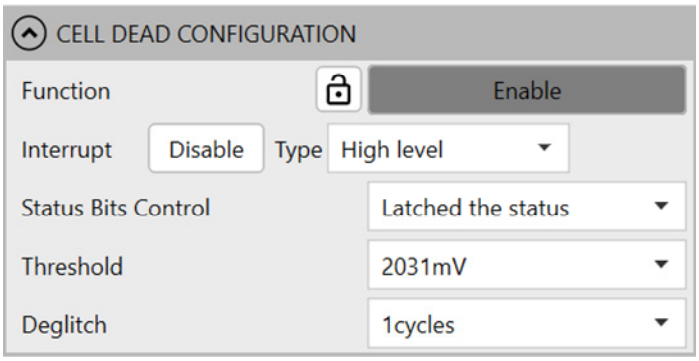

Figure 27: Cell Dead Configurations

Threshold: The dead cell threshold ranges between 0mV to 2480mV.

23. Configure the V_{TOP} UV parameters (see Figure 28).

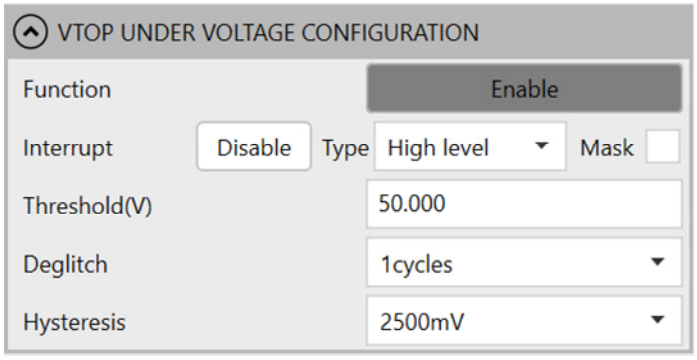

Figure 28: V_{TOP} Under-Voltage Configurations

a. Threshold (V): The V_{TOP} UV threshold ranges between 0V to 79.98V.

b. Hysteresis: Ranges between 0mV and 4922mV.

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24. Configure the V_{TOP} OV parameters (see Figure 29).

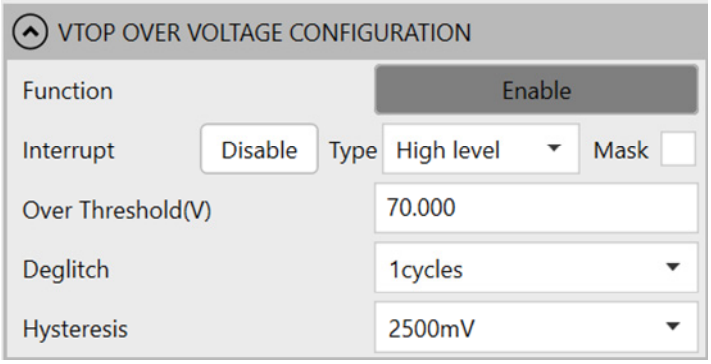

Figure 29: V_{TOP} Over-Voltage Configurations

a. Over-Voltage Threshold (V): The V_{TOP} OV threshold ranges between 0V and 79.98V.

b. Hysteresis: Ranges between 0mV and 4922mV.

25. Configure the REGIN, 3V3, VDD, and ADC self-test checks (see Figure 30).

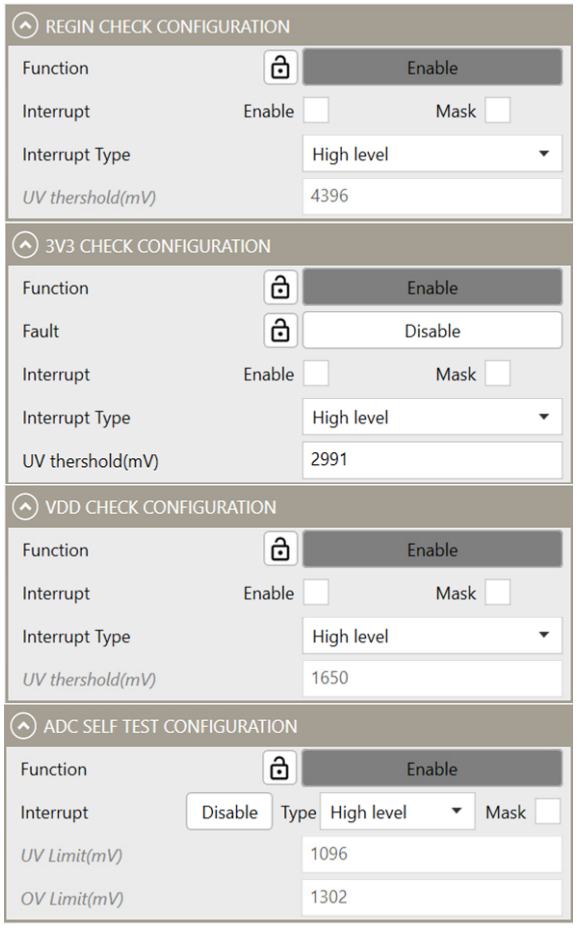

Figure 30: REGIN, 3V3, VDD, ADC Self-Test Check Configuration

26. Configure the one-time programmable (OTP) memory cyclic redundancy check (CRC) (see Figure 31 on page 21).

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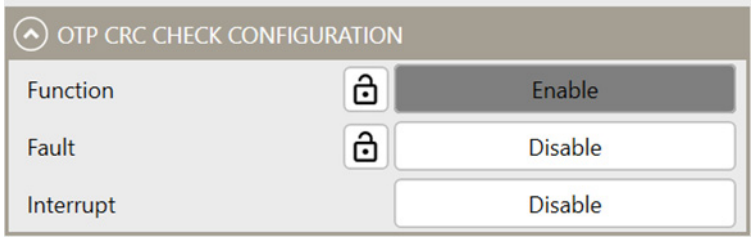

Figure 31: OTP CRC Configuration

Monitor and Control

Click on the Monitor and Control tab to view the device's statuses and faults (see Figure 8 on page 8). The software can automatically update the status, fault, and ADC measurement results by selecting "Auto ADC scan" and "Auto Read".

1. Configure simple mode N-FET control.

Figure 32: Simple Mode N-FFET Control

2. Configure direct mode MOSFET control.

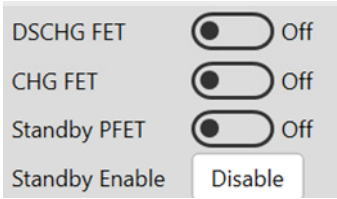

Figure 33: Direct Mode MOSFET Control

3. Check the status monitor (see Figure 34).

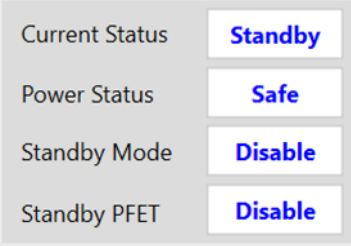

Figure 34: Status Monitor

4. Monitor the watchdog status (see Figure 35).

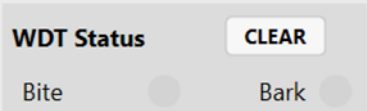

Figure 35: Watchdog Status Monitor

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5. Monitor the MOSFET statuses (see Figure 36).

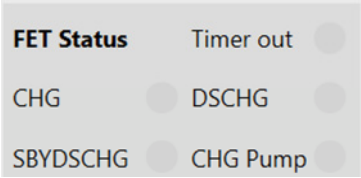

Figure 36: MOSFET Status Monitor

6. Configure the ADC, cell balance, and open-wire control parameters (see Figure 37).

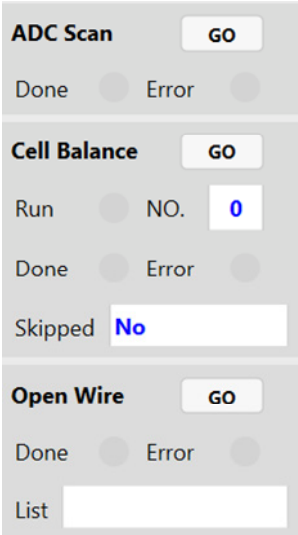

Figure 37: ADC, Cell Balance, Open-Wire Control and Monitor

7. Monitor for OC statuses (see Figure 38).

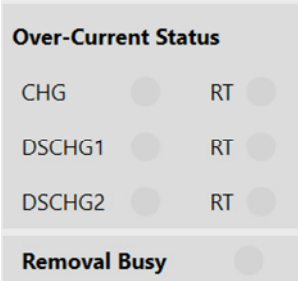

Figure 38: Over-Current Status Monitor

8. Monitor the GPIO and V_{TOP} statuses (see Figure 39).

Figure 39: GPIO and V_{TOP} Status Monitor

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9. Monitor the die temperature (see Figure 40).

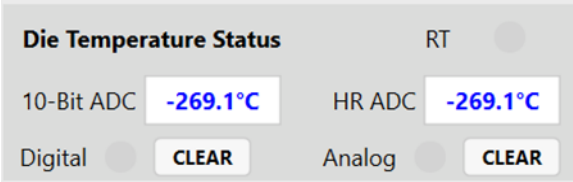


Figure 40: Die Temperature Monitor

10. Monitor the OTP CRC statues (see Figure 41).

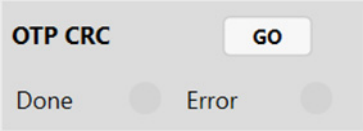
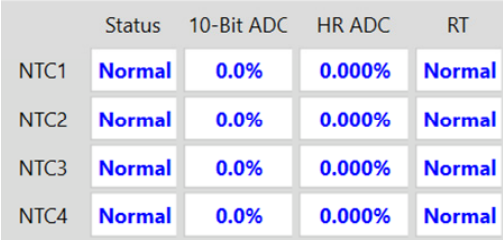


Figure 41: OTP CRC Monitor

11. Monitor the NTC statuses (see Figure 42).



	Status	10-Bit ADC	HR ADC	RT
NTC1	Normal	0.0%	0.000%	Normal
NTC2	Normal	0.0%	0.000%	Normal
NTC3	Normal	0.0%	0.000%	Normal
NTC4	Normal	0.0%	0.000%	Normal

Figure 42: NTC Monitor

Figure 43 shows the NTC functional block.

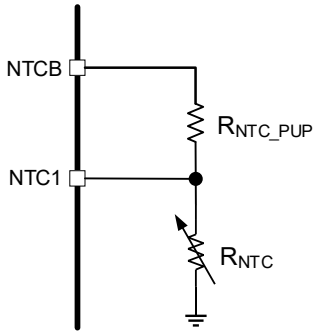


Figure 43: NTC Functional Block

R_{NTC} can be estimated with Equation (1):

$$R_{NTC}=\frac{A \times R_{NTC_PUP}}{32768 - A} \quad (1)$$

Where A is the NTC ADC reading, R_{NTC_PUP} is NTC pull-up resistor value (10kΩ is recommended). The ambient temperature (T, in K) can be calculated with Equation (2)

$$T=\frac{1}{\frac{1}{T_0}+\frac{1}{B}\ln\frac{R_{NTC}}{R_0}} \quad (2)$$

Where R_0 is NTC resistor value when the ambient temperature is T_0 (in K), and B is the

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thermistor constant (in K).

For example, if the NTC ADC reading (A) is 9830 (0x2666) for the thermistor NCP18XH103, R_0 is 10kΩ at 25°C (298.15K), and B is 3380K, then R_{NTC} = 4.285kΩ, and T = 322K. This means that if the NTC ADC reading is 9830, the ambient temperature is about 49°C.

12. Monitor the low-dropout (LDO) regulator (see Figure 44).

	Status	10-Bit ADC
VDD	Normal	0.0mV
3V3	Normal	0.0mV
REGIN	Normal	0.0mV
Self	Normal	0.0mV

Figure 44: LDO Monitor

13. Monitor the cells' ADC statuses (see Figure 45). To do so, click on the ADC scan "Go" button on Configuration sheet (see Figure 9 on page 9). The ADC result should be updated to the corresponding register.

	Voltage	UV	OV	MS	Dead	BAL
Cell1	0.0mV					
Cell2	0.0mV					
Cell3	0.0mV					
Cell4	0.0mV					
Cell5	0.0mV					
Cell6	0.0mV					
Cell7	0.0mV					
Cell8	0.0mV					
Cell9	0.0mV					
Cell10	0.0mV					
Cell11	0.0mV					
Cell12	0.0mV					
Cell13	0.0mV					
Cell14	0.0mV					
Cell15	0.0mV					
Cell16	0.0mV					

Figure 45: Cell ADC Monitor

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EVALUATION BOARD SCHEMATICS

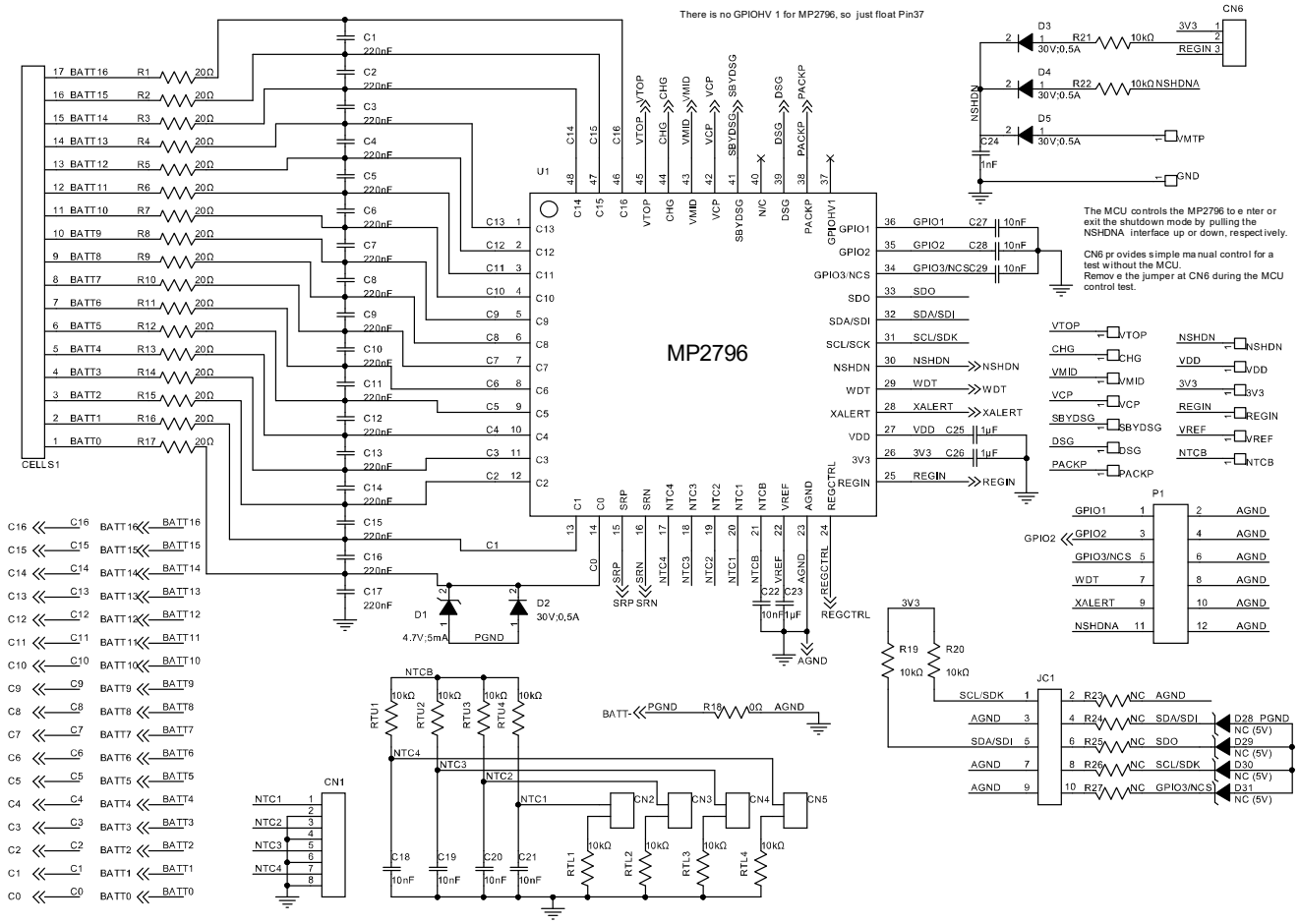

Figure 46: Evaluation Board Schematic (Chip)

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EVALUATION BOARD SCHEMATICS *(continued)*

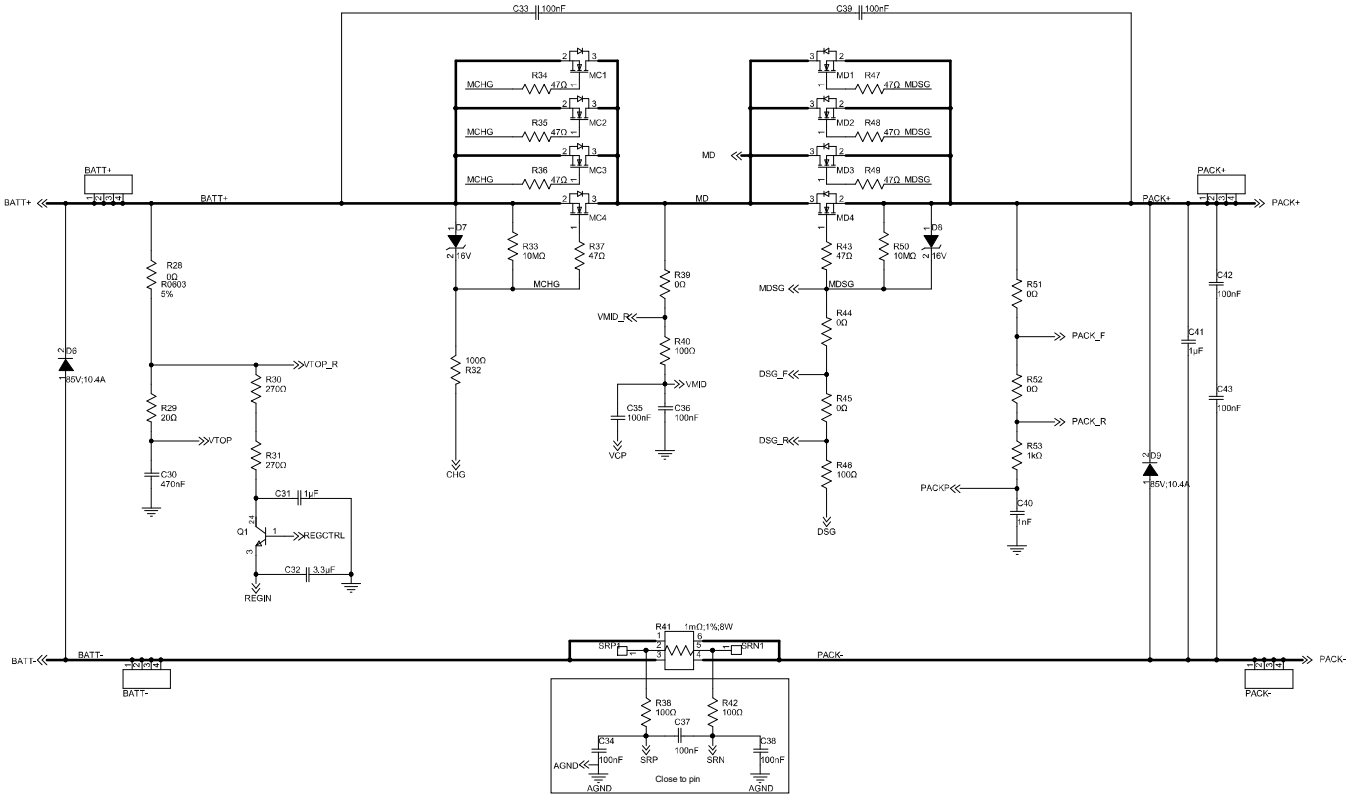

Figure 47: Evaluation Board Schematic (Power Path)

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EVALUATION BOARD SCHEMATICS *(continued)*

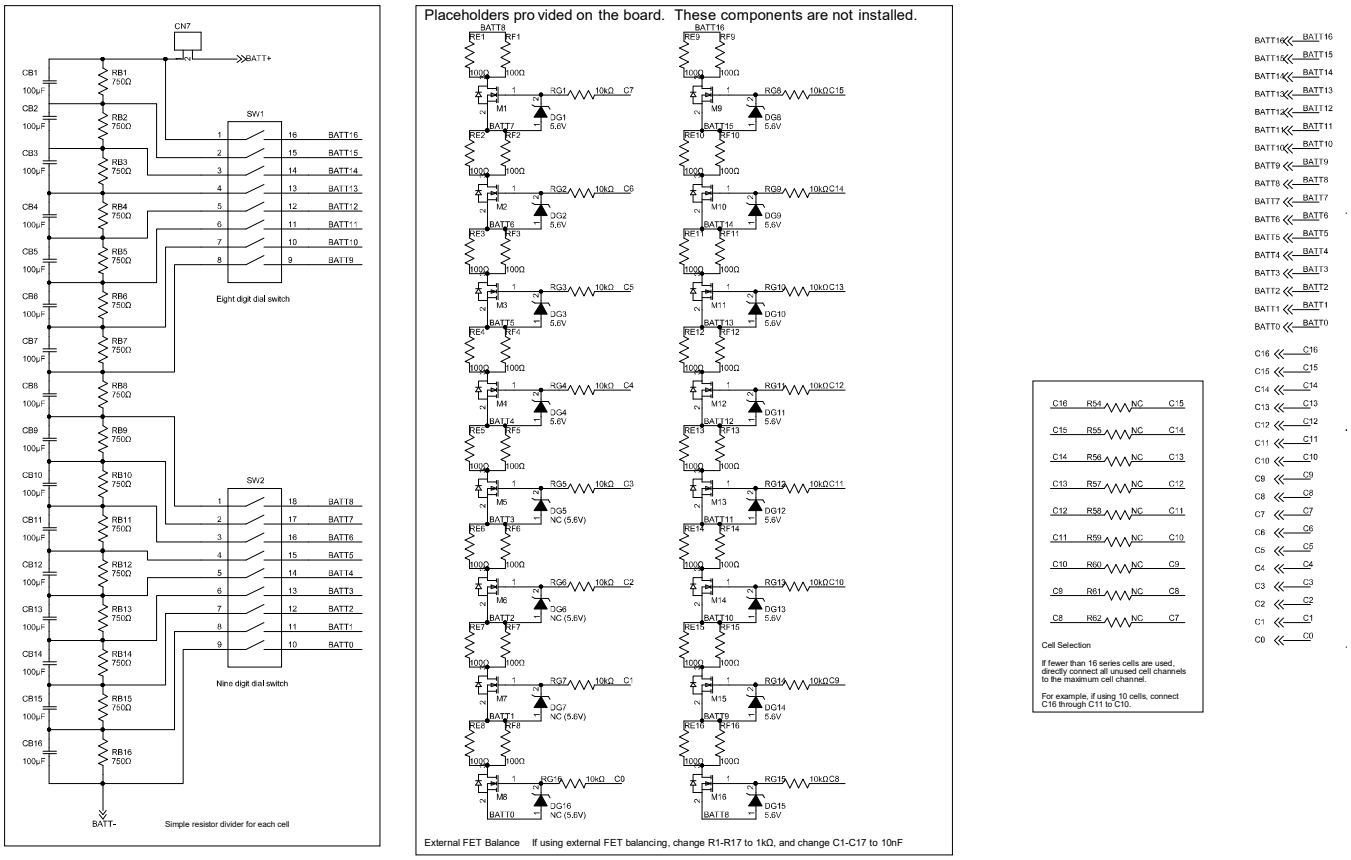

Figure 48: Evaluation Board Schematic (Battery Connection)

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EVALUATION BOARD SCHEMATIC *(continued)*

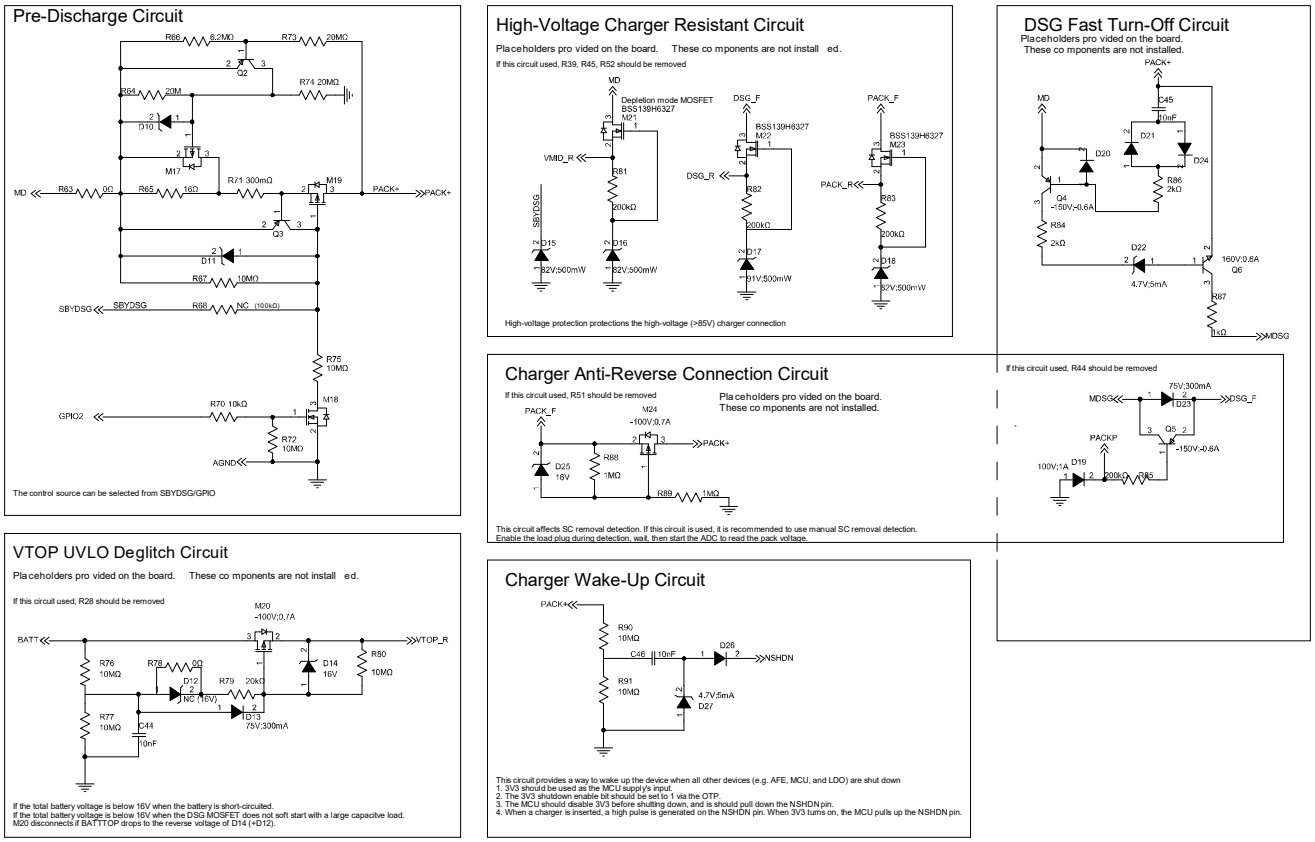

Figure 49: Evaluation Board Schematic (Additional Circuit)

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EV2796-0000-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK, PACK+, BATT-, BATT+	12x 18mm	Connector	DIP	Zhengyou	ZY_50
16	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2, CN3, CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Wurth	60900213421
1	CN6	2.54mm	3-pin connector	DIP	Wurth	60900213421
1	CELLS1	3.5mm	17-pin connector	DIP	KEFA	KF2EDGR-3.5-17P
17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	85V	TVS diode, 10.4A	DO-214AB	Diodes, Inc.	SMCJ85A-13-F
4	D7, D8, D10, D11	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D26	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	JC1	2.54mm	2 x 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2 x 6-pin connector	DIP	HCTL	PZ254-2-06-Z-8.5
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel, 3.6mΩ, 90nC, 120A	TO-263	Crmicro	CRSS042N10N

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EV2796-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
16	RB1, RB2, RB3, RB4, RB5, RB6, RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32,R40,R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
13	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R70	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	M17	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
1	M18	100V	N-channel MOSFET, 6Ω, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	M19	-200V	P-channel MOSFET, 950mΩ, 6A,15nC	TO-252	Analog Power	AM10P20-690D
1	Q1	100V	Transistor, NPN, 6A, 3W	SOT-223	Zetex	FZT853TA
2	Q2,Q3	-20V	Transistor, PNP, -1.5A	SOT-23	JCET	SS8550LT1
17	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
8	R18, R28, R39, R44, R45, R51, R52, R63	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
7	R33, R50, R67, R72, R75, R90, R91	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	1mΩ shunt	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
3	R64 ,R73, R74	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML
1	R65	16Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0716RL
1	R66	6.2MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076M2L
1	R71	300mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R3L
1	SW1	8-pin switch	Button	SMD	KE	DSIC08TSGER

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EV2796-0000-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	SW2	9-pin switch	Button	SMD	KE	DSIC09LSGER
1	U1	MP2796	Battery monitor and protection IC	TQFP-48	MPS	MP2796DFP-0000

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EV2796-0002-FP-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	PACK, PACK+, BATT-, BATT+	12mmx 18mm	Connector	DIP	Zhengyou	ZY_50
16	CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14, CB15, CB16	100µF	Capacitor, 6.3V, X6T	1206	Murata	GRM31CD80J107ME39L
1	CN1	2.54mm	8-pin connector	DIP	Wurth	691210910008
5	CN2, CN3, CN4, CN5, CN7	2.54mm	2-pin connector	DIP	Wurth	60900213421
1	CN6	2.54mm	3-pin connector	DIP	Wurth	60900213421
1	CELLS1	3.5mm	17-pin connector	DIP	KEFA	KF2EDGR-3.5-17P
17	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	220nF	Capacitor, 50V, X7R	0603	Murata	GRM188R71H224KAC4D
8	C18, C19, C20, C21, C22, C27, C28, C29	10nF	Capacitor, 25V, X7R	0603	Wurth	885012206065
3	C23, C25, C26	1µF	Capacitor, 16V, X7R	0603	Wurth	885012206052
2	C24, C40	1nF	Capacitor, 100V, X7R	0603	Murata	GRM188R72A102KA01D
1	C30	470nF	Capacitor, 100V, X7R	0805	Murata	GRM21BR72A474KA73L
2	C31, C41	1µF	Capacitor, 100V, X7R	1206	Murata	GRM31CR72A105KA01L
1	C32	3.3µF	Capacitor, 16V, X5R	0805	Murata	GRM21BR61C335KA88
9	C33, C34, C35, C36, C37, C38, C39, C42, C43	100nF	Capacitor, 100V, X7R	0603	Wurth	885012206120
1	C46	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
2	D1, D27	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D2, D3, D4, D5	30V	Schottky diode, 0.5A	SOD-123	JCET	B0530W
2	D6, D9	85V	TVS diode, 10.4A	DO-214AB	Diodes, Inc.	SMCJ85A-13-F
4	D7, D8, D10, D11	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D26	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	JC1	2.54mm	2 x 5-pin connector	DIP	Wurth	61201021621
1	P1	2.54mm	2 x 6-pin connector	DIP	HCTL	PZ254-2-06-Z-8.5
8	MD1, MC1, MD2, MC2, MD3, MC3, MD4, MC4	100V	N-channel MOSFET, 3.6mΩ, 90nC, 120A	TO-263	Crmicro	CRSS042N10N

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EV2796-0002-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
16	RB1, RB2, RB3, RB4, RB5, RB6, RB7, RB8, RB9, RB10, RB11, RB12, RB13, RB14, RB15, RB16	750Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07750RL
3	R32,R40,R46	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
13	RTU1, RTL1, RTU2, RTL2, RTU3, RTL3, RTU4, RTL4, R19, R20, R21, R22, R70	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	M17	-30V	P-channel MOSFET, 172mΩ, 2.5A	SOT-23	Analog Power	AM2329P-T1-PF
1	M18	100V	N-Channel MOSFET, 6Ω, 170mA	SOT-23	Analog Power	LBSS123LT1G
1	M19	-200V	P-channel MOSFET, 950mΩ, 6A, 15nC	TO-252	Analog Power	AM10P20-690D
1	Q1	100V	Transistor, NPN, 6A, 3W	SOT-223	Zetex	FZT853TA
2	Q2,Q3	-20V	Transistor, PNP, -1.5A	SOT-23	JCET	SS8550LT1
17	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	20Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0720RL
13	R18, R23, R24, R25, R26, R27, R28, R39, R44, R45, R51, R52, R63	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R29	20Ω	Film resistor, 5%	1206	Yageo	RC1206JR-0720RL
2	R30, R31	270Ω	Film resistor, 5%	2512	Yageo	RC2512JK-07270RL
7	R33, R50, R67, R72, R75, R90, R91	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
8	R34, R35, R36, R37, R43, R47, R48, R49	47Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0747RL
2	R38, R42	100Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100RL
1	R41	1mΩ	1mΩ shunt	3920	Bourns	CSS2H-3920R-1L00F
1	R53	1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-071KL
3	R64, R73, R74	20MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720ML
1	R65	16Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0716RL
1	R66	6.2MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076M2L

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EV2796-0002-FP-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R71	300mΩ	Film resistor, 1%	2512	Yageo	RL2512FK-070R3L
1	SW1	8-pin switch	Button	SMD	KE	DSIC08TSGER
1	SW2	9-pin switch	Button	SMD	KE	DSIC09LSGER
1	U1	MP2796	Battery monitor and protection IC	TQFP-48	MPS	MP2796DFP-0002

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EV2796-0000/0002-FP-00A BILL OF MATERIALS

These are the recommended components for the external MOSFET balance circuit (components not installed on standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
16	M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16	50V	N-channel MOSFET, 3.5mΩ, 0.2A	SOT-23	LRC	LBSS138LT1G
32	RF1, RE1, RF2, RE2, RF3, RE3, RF4, RE4, RF5, RE5, RF6, RE6,RF7, RE7, RF8, RE8, RF9, RE9, RF10, RE10, RF11, RE11, RF12, RE12, RF13, RE13, RF14, RE14, RF15, RE15, RF16, RE16	100Ω	Film resistor, 1%	1206	Yageo	RC1206FR-07100RL
15	RG1, RG2, RG3, RG4, RG5, RG6, RG7, RG8, RG9, RG10, RG11, RG12, RG13, RG14, RG15	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
15	DG1, DG2, DG3, DG4, DG5, DG6, DG7, DG8, DG9, DG10, DG11, DG12, DG13, DG14, DG15	5.6V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C5V6S-7-F

These are the recommended components for the V_{TOP} under-voltage lockout (UVLO) deglitch circuit (components not installed on the standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	M20	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
1	D14	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D12	15V	Zener diode, 5mA	SOD-123	Changdian	BZT52C15WJ
1	D13	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
3	R76, R77, R80	10MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710ML
1	R78	0Ω	Film resistor, 5%	0603	Royalohm	0603WAJ0000T5E
1	R79	20kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720KL
1	C44	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03

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EV2796-0000/0002-FP-00A BILL OF MATERIALS *(continued)*

These are the recommended components for the DSG fast turn-off and anti-reverse connection circuit (components not installed on the standard board)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C45	10nF	Capacitor, 250V, X7R	0805	Murata	GRM21BR72E103KW03
4	D20, D21, D23, D24	75V	Diode, 300mA	SOD-323	Diodes, Inc.	1N4148WS
1	D25	16V	Zener diode, 5mA/500mW	SOD-123	Diodes, Inc.	BZT52C16-7-F
1	D19	100V	Schottky diode, 1A	SOD-123-2	ST	BAT41ZFILM
1	D22	4.7V	Zener diode, 5mA	SOD-323	Diodes, Inc.	BZT52C4V7S
4	D28, D29, D30, D31	5V	ESD diode, 5V	SOD-323	NXP	PESD5V0V1BA
1	M24	-100V	P-channel MOSFET, 1.2Ω, 1A	SOT-23	Analog Power	AM2371P
2	Q4, Q5	-80V	Transistor, 0.5A, PNP	SOT-23	Diodes, Inc.	MMBTA56LT1G
1	Q6	80V	Transistor, 0.5A, NPN	SOT-23	onsemi	MMBTA06
1	R85	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
1	R87	47Ω	Film resistor, 1%	1206	Yageo	RC1206FR-0747RL
2	R84, R86	2kΩ	Film resistor, 1%	0805	Yageo	RC0805FR-072KL
2	R88, R89	1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML

These are the recommended components for the high-voltage charger circuit (components not installed on the standard board).

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	D15, D16, D18	82V	Zener diode, 1.5mA	SOD-123-2	onsemi	MMSZ5268BT1G
1	D17	91V	Zener diode, 1.4mA	SOD-123-2	onsemi	MMSZ5270BT1G
3	R81, R82, R83	200kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07200KL
3	M21, M22, M23	250V	N-channel MOSFET, 7.8mΩ, 2.3nC, 30mA	SOT-23	Infineon	BSS139H6327

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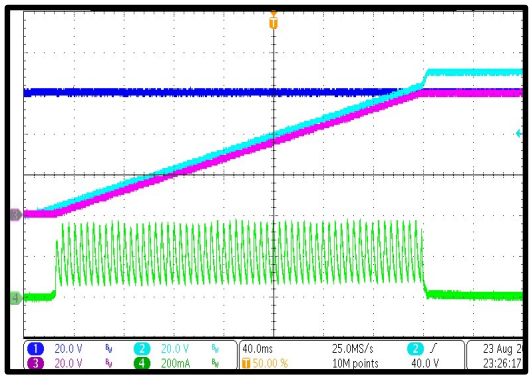
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

DSG Soft Start

PACK+ is connected to a 1mF capacitor, the DSG slope is 0.2V/ms

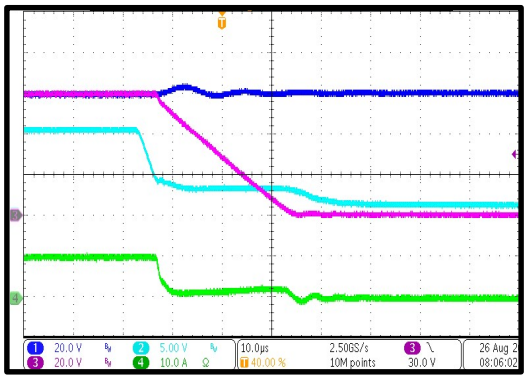
CH1: V_{MID}
CH2: V_{DSG}
CH3: V_{PACK+}
CH4: I_{DSG}



DSG Off

CR load = 6Ω

CH1: V_{MID}
CH2: V_{GS_DSG}
CH3: V_{PACK+}
CH4: I_{DSG}



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PCB LAYOUT (MP2796-0000-FP-00A)

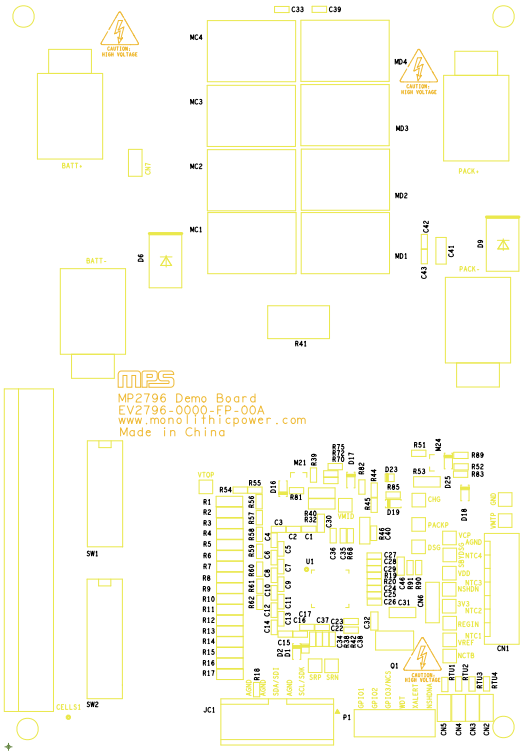

Figure 50: Top Silk

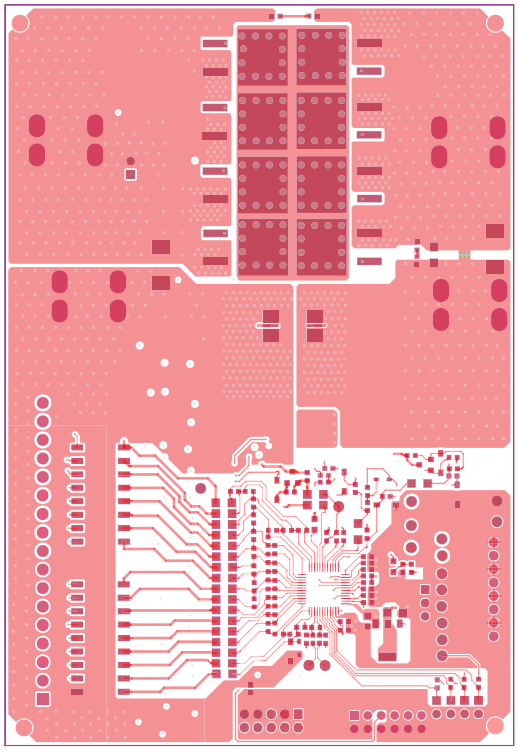

Figure 51: Top Layer

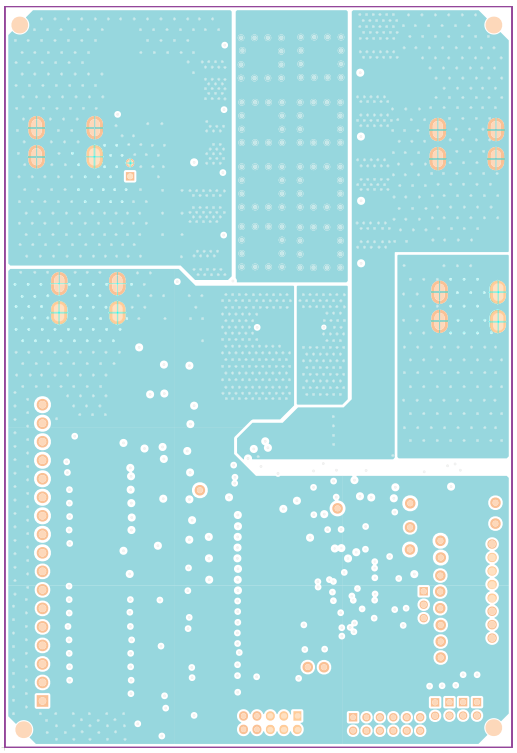

Figure 52: Mid-Layer 1

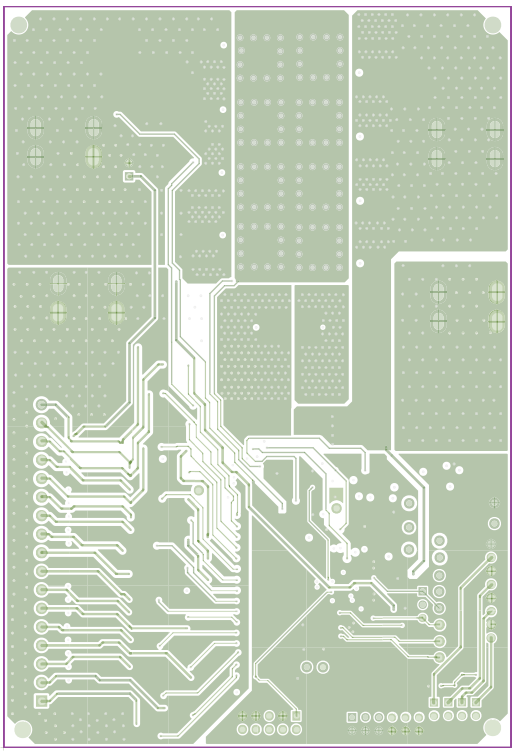

Figure 53: Mid-Layer 2

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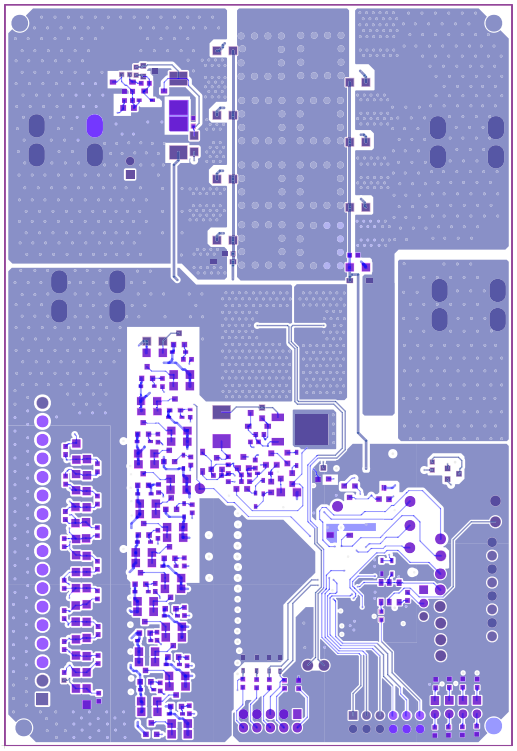

Figure 54: Bottom Layer

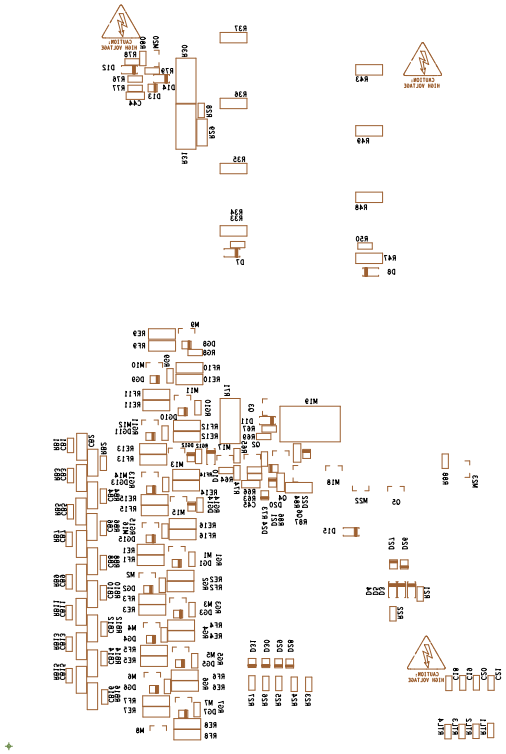

Figure 55: Bottom Silk

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PCB LAYOUT (MP2796-0002-FP-00A)

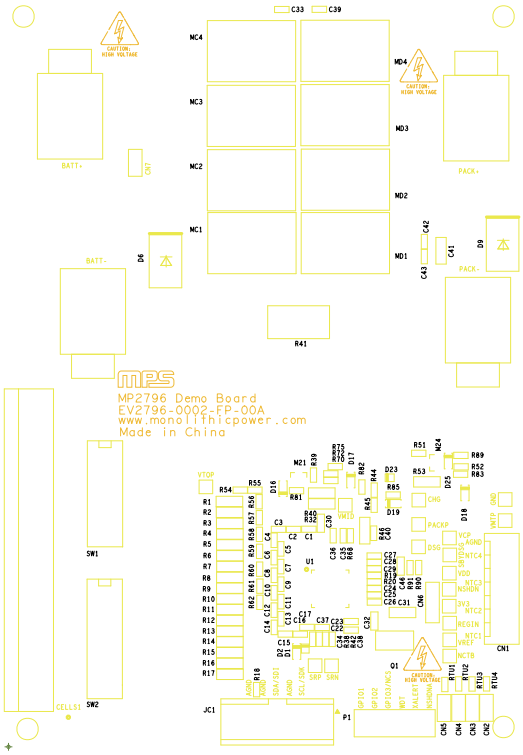

Figure 56: Top Silk

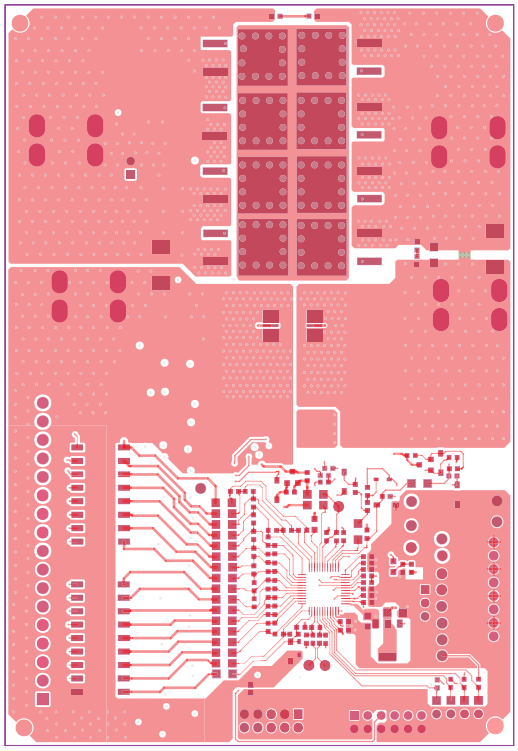

Figure 57: Top Layer

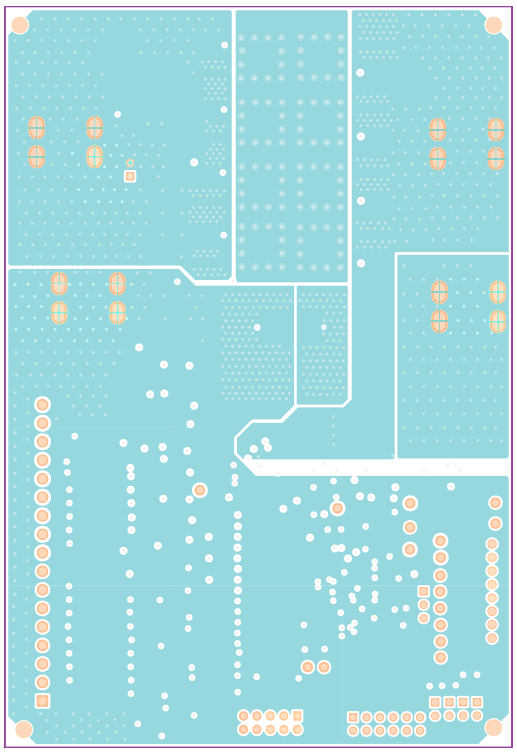

Figure 58: Mid-Layer 1

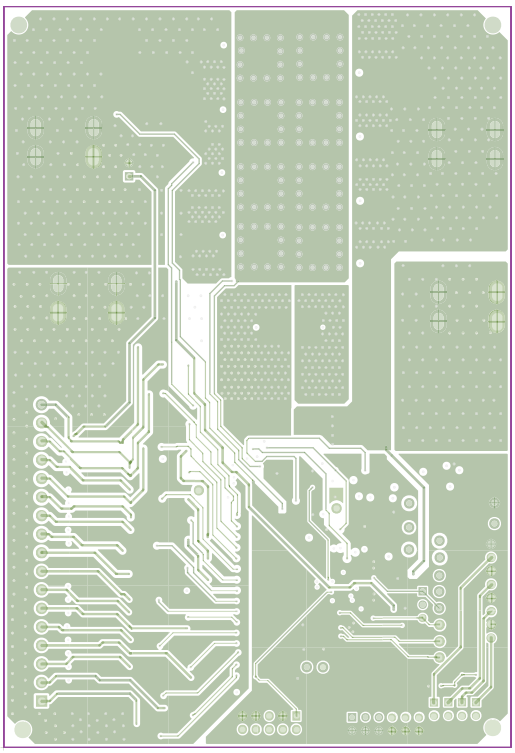

Figure 59: Mid-Layer 2

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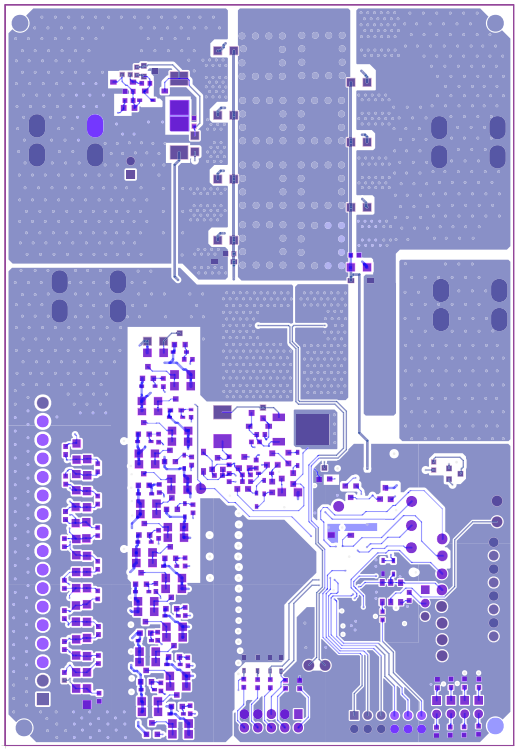

Figure 60: Bottom Layer

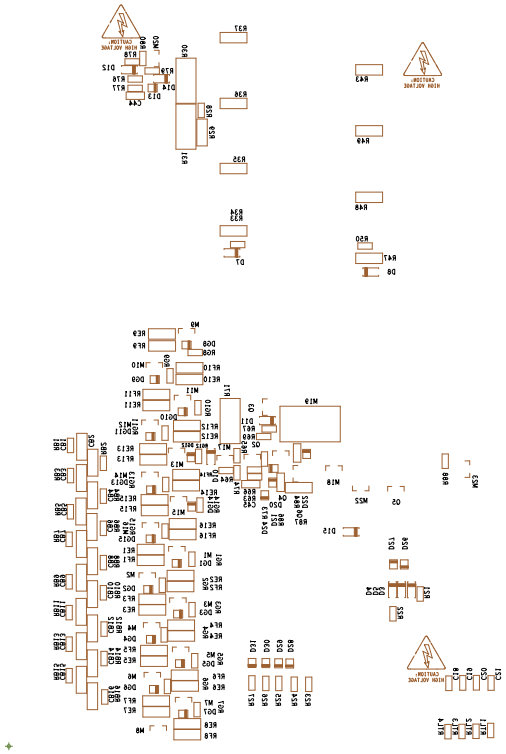

Figure 61: Bottom Silk

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/16/2023	Initial Release	-

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